TESTING AND FAULT TOLERANCE

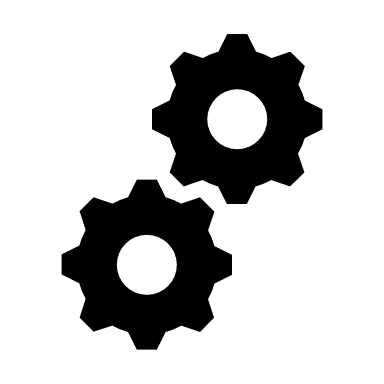
Laboratory Session 6: “Functional Test”

|  |  |  |
| --- | --- | --- |
| **Student Name** | **Student Surname** | **Student ID** |
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A cartoon of a castle

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# **[A] Fault Simulation of External Patterns**

In the provided testbenches, functional patterns for the fault simulation are generated by a Linear Feedback Shift Register (LFSR). You need to run a logic simulation of the testbench using QuestaSim to generate the test responses, which can be stored (dumped) into an External Value Change Dump (eVCD) file. This file can then be read by TestMAX before the fault simulation.

Inspect the provided scripts and HDL files (testbench, LFSR) to comprehend the flow of events. If needed, you can modify the LFSR or the testbench (e.g., change the polynomial, the size, the initial value etc.) to optimize the test.

***Logic Simulation Fault Simulation***

Testbench -------> eVCD -------> Reports

**[A.1] Tasks:**

1. Evaluate the effectiveness of random patterns and fill the following tables

Circuit: b06

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Patterns | 5 | 10 | 20 | 100 | 200 | 500 | 1,000 | 10,000 | 100,000 |
| Stuck-at FC% | 64.58 | 86.57 | 88.19 | 89.35 | 89.35 | 89.35 | 89.35 | 89.35 | 89.35 |
| Transition FC% | 35.57 | 69.59 | 71.65 | 75.00 | 75.00 | 75.00 | 75.00 | 75.00 | 75.00 |

Circuit: b10

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Patterns | 5 | 10 | 20 | 100 | 200 | 500 | 1,000 | 10,000 | 100,000 |
| Stuck-at FC% | 6.79 | 9.30 | 54.31 | 77.78 | 78.43 | 79.40 | 79.40 | 79.40 | 79.40 |
| Transition FC% | 0.00 | 1.34 | 28.63 | 57.54 | 61.74 | 63.26 | 64.03 | 64.03 | 64.03 |

* You can change the simulation time (i.e., the generated patterns) and the fault model by editing the respective .tcl files

Once you collect the results, run the following command **after** the longest fault simulation:

* TEST-T> report\_faults -profile

**[A.2] Tasks:**

1. According to the results how many patterns are needed to reach the maximum fault coverage?

Regarding the b06 circuit, the number of patterns needed to reach the maximum fault coverage for stuck-at faults is 43 while for transition delay faults it is 68.

Instead for b10 circuit, for stuck-at it needs 472 patterns while for transition delay it needs 518 patterns.

**[A.3] Tasks:**

1. Write a testbench for circuit b12 and repeat the flow.
2. Are the results comparable with the previous circuits?
3. If the fault coverage is too low, how can you improve it?
4. Complete the following table (similar to b06 and b10)

2) no, they aren’t. The maximum coverage is almost 1/3 compared to the b10 circuit.

3) it’s possible to try different combination of the lfsr’s outputs as b12’s inputs or it’s possible to change the lfsr’s seed

Circuit: b12

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Patterns | 5 | 10 | 20 | 100 | 200 | 500 | 1,000 | 10,000 | 100,000 |
| Stuck-at FC% | 3.12 | 4.66 | 4.77 | 18.19 | 18.60 | 19.31 | 19.31 | 21.63 | 21.63 |
| Transition FC% | 0.00 | 2.98 | 3.33 | 6.91 | 7.82 | 9.92 | 11.05 | 11.79 | 11.79 |

* The source code of the benchmark circuits is available on [GitHub](https://github.com/squillero/itc99-poli)
* For a list of LFSR polynomials see [Appendix B](#_Appendix_B:_Table)

# **Appendix A: Files of LAB6**

* **All files listed here are included in your remote /home directory under lab6 folder.**

|  |  |
| --- | --- |
| **Filename** | **Description** |
| lfsr.vhd | Linear Feedback Shift Register module |
| b06\_scan.v | ITC’99 b06 scan netlist |
| b06\_testbench.vhd | Testbench for LFSR & b06 |
| b10.v | ITC’99 b10 netlist |
| b10\_testbench.vhd | Testbench for LFSR & b10 |
| b12.v | ITC’99 b12 netlist |
| pdt2002\_sim.vhd | Technology library models for QuestaSim |
| pdt2002\_tmax.v | Technology library models for TestMAX |
| b06\_simulation.sh | Build & run the b06 testbench circuit logic simulation |
| b10\_simulation.sh | Build & run the b10 testbench circuit logic simulation |
| b06\_simulation\_script.tcl | QuestaSim script with commands for the logic simulation of b06 |
| b06\_fsim\_script.tcl | TestMAX script for the fault simulation of b06 |
| b10\_simulation\_script.tcl | QuestaSim script with commands for the logic simulation of b10 |
| b10\_fsim\_script.tcl | TestMAX script for the fault simulation b10 |

# **Appendix B: Table of LFSRs**

Table

Description automatically generated