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Article

Simulations of Monolayer and Multilayer MoS_2 FET

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Version July 2, 2020 submitted to Electronics

Abstract: Two dimensional materials are object of researches due to their ease to fabricate complex structures with them and the high performance that they show. A single layer of MoS_2 can be substituted to a transistor channel. We have implemented some MOSFET models in COMSOL Multiphysics. The results obtained are then compared with the experimental ones found in [1] and [2]. We noticed that the plots are similar to the ones on the papers used for this work, so the simulations are close to the experimental results.

Keywords: Transistor, Molybdenum disulfide, 2-D materials, Ferroelectric

1. Introduction

In the following report different kinds of models of transistors based on the monolayer material have been studied. In section 2.1 is shown a transistor with a monolayer and a four layer MoS_2 channel. This study is based on [1] and results are compared with the simulated ones that are in this paper. This kind on transistor has a single silicon bottom gate. In section 2.2 another transistor shown in [2] is studied. This has a bottom and a top gate made of Cr/Au isolated by a layer of hafnium dioxide. This oxide is used to demonstrate a room-temperature single-layer MoS_2 mobility of at least 200 $cm^2\,V^{-1}\,s^{-1}$, similar to that of graphene nanoribbons. The last model refers to [4] and uses a ferroelectric material, a layer of $Hf_0.3Zr_0.7O_2$ with 6nm of thickness, instead of the silicon oxide. The ferroeletric material polarization can be reversed by an applied electric field, the polarization is dependent not only on the current electric field but also on its history, giving a hysteresis loop.

2. Results

2.1. MoS_2 transistor

In [1] is investigated the band-offsets at monolayer and multilayer MoS_2 junctions by scanning photocurrent microscopy. The thickness dependent band structure of MoS_2 implies that discontinuities in energy bands exist at the interface of monolayer (1L) and multilayer (ML) thin films. The characteristics of such heterojunctions are analyzed using finite element simulations of charge carrier transport. We used that simulations to compare their results to our COMSOL model.

Transition metal dichalcogenides (TMDCs) such as MoS_2 consist of discrete two-dimensional (2D) layers bound together by van der Waals forces, with important consequences for both physical and electronic structure of these ultrathin semiconducting crystals. MoS_2 flakes exhibit distinctive thickness dependent variations in physical properties and the band structure varies with multilayer thickness.

MoS_2 flakes were exfoliated from commercially available crystals of molybdenite onto n^+ Si substrates coated with 300 nm of SiO_2. The devices were formed by electron beam lithography and lift-off of Au ohmic contacts with 75 nm thickness. Fig. 1 shows the device geometry.

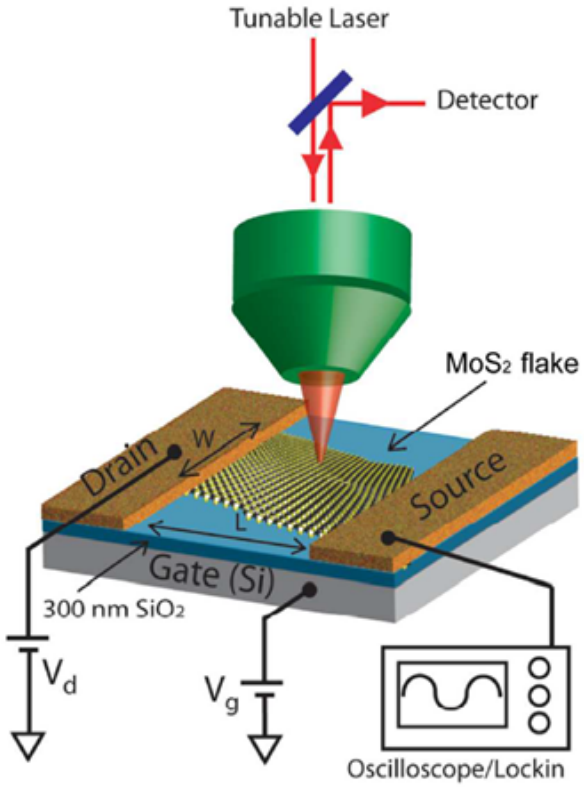

Figure 1. Monolayer model [3]

Figure 2. COMSOL monolayer model

The parameters used in COMSOL are shown in Tab. 1.

Parameter	Value
Thickness of MoS_2	0.7 nm/layer
Band gap 1L MoS_2	2.76 eV
Band gap 4L MoS_2	1.6 eV
Electron affinity 1L Mo_2	4.7 eV
Electron affinity 4L MoS_2	4 eV
Relative permittivity 1L	4.2
Relative permittivity 4L	11
Mobility 1L	6 $cm^2\,V^{-1}\,s^{-1}$
Mobility 4L	25 $cm^2\,V^{-1}\,s^{-1}$
Drain contact type	Ideal ohmic
Source contact type	Ideal ohmic
SRH lifetimes 1L	1.5 ns
SRH lifetimes 4L	0.3 ns
Workfunction of gate	4.05 V
SiO_2 Relative Permittivity	3.9
Electron effective mass	0.5 m_0
Hole effective mass	0.5 m_0
Thickness gold contact	75 nm
Length MoS_2	3.5 µm
Silicon thickness	2 µm
SiO_2 thickness	300 nm
Width	6.8 µm

Table 1. Parameters

The figures shown below are the simulated and experimental (see legend) output characteristics when $V_G = 0.1$ V (5) and transfer characteristics when $V_D = 0.01$ V (6)for a 4L thick FET. Simulated and experimental output characteristics when $V_G = 10$ V (3) and transfer characteristics when $V_D = 0.05$ V (4) for a 1L thick FET. Experimental data are reproduced from [3]. Ideal transistor transfer curves show zero current below the threshold voltage and a linear gate bias dependence above the threshold voltage. Deviations of experimental transfer curves from ideal simulations have been attributed to scattering from unscreened charged impurities and a carrier density dependent mobility. Mobility limited by Coulomb scattering leads to approximately parabolic instead of linear experimental transfer curves above the threshold voltage and reduces current magnitudes. An additional series contact resistance may further limit the current magnitudes in the experimental devices.

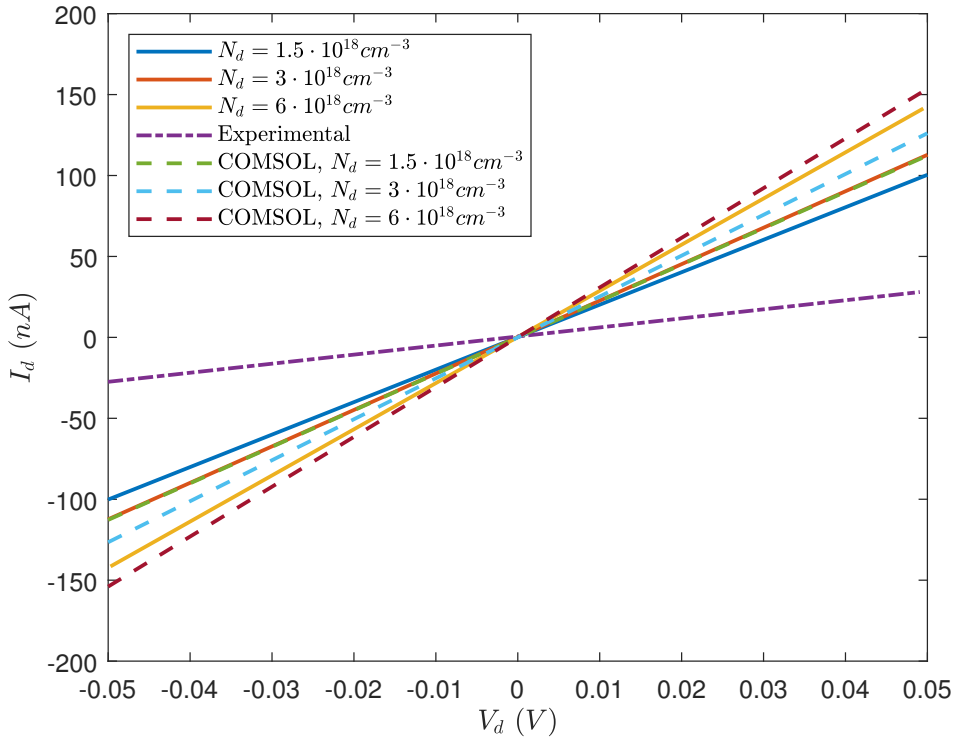

Figure 3. Monolayer $I_d(V_d)$

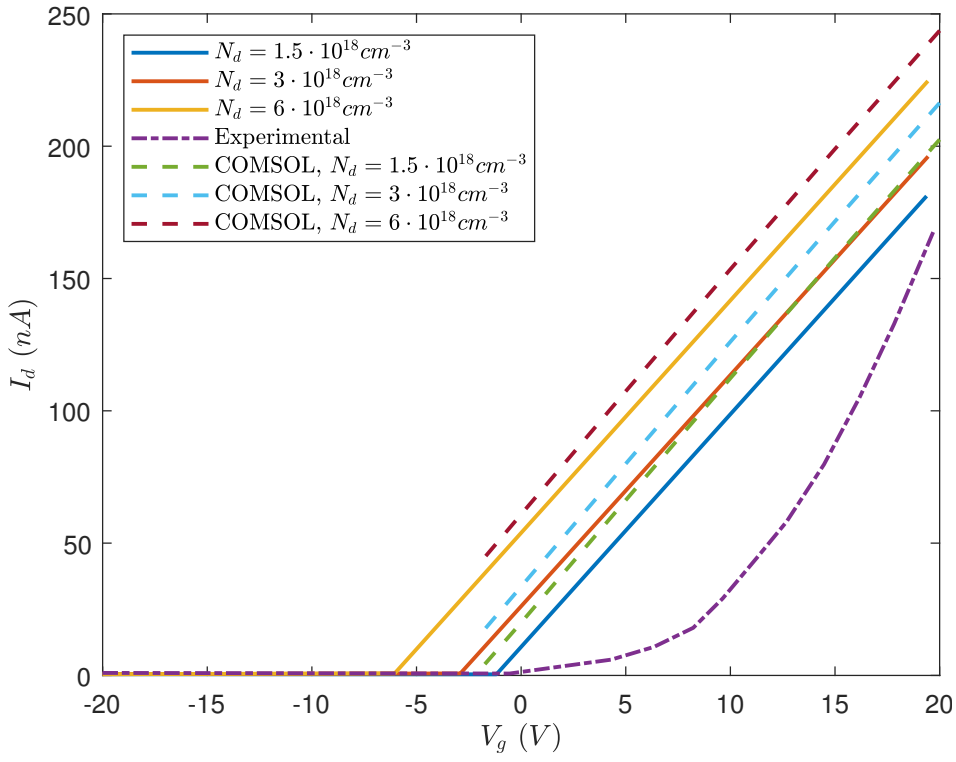

Figure 4. Monolayer $I_d(V_g)$

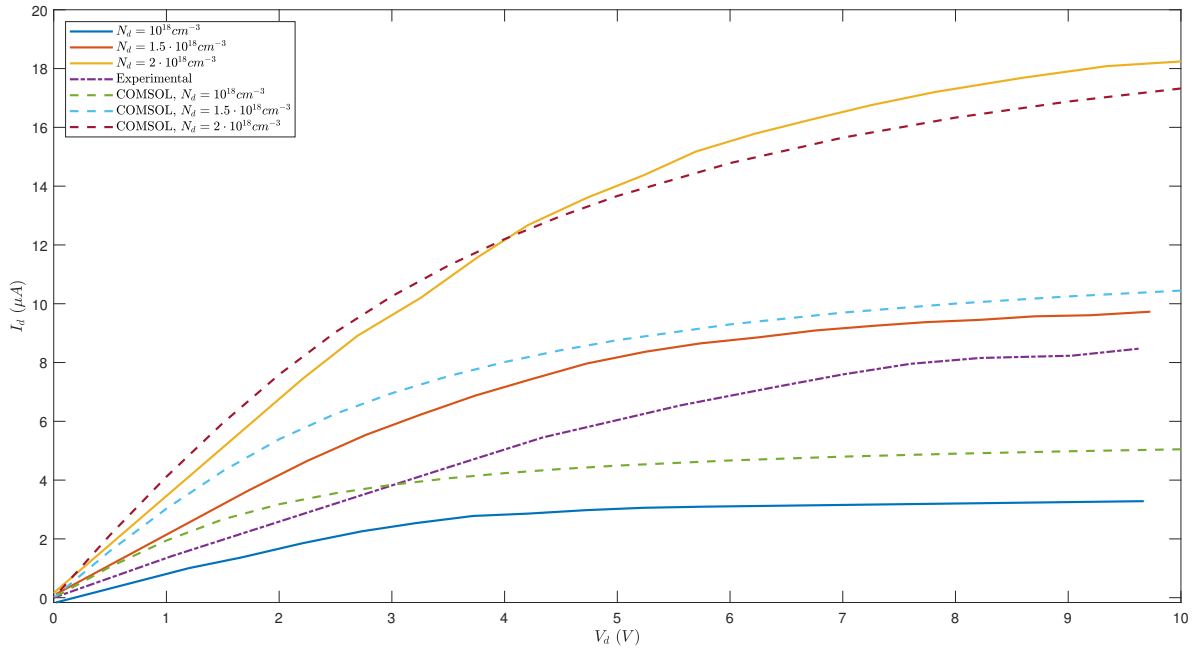

Figure 5. 4 layer $I_d(V_d)$

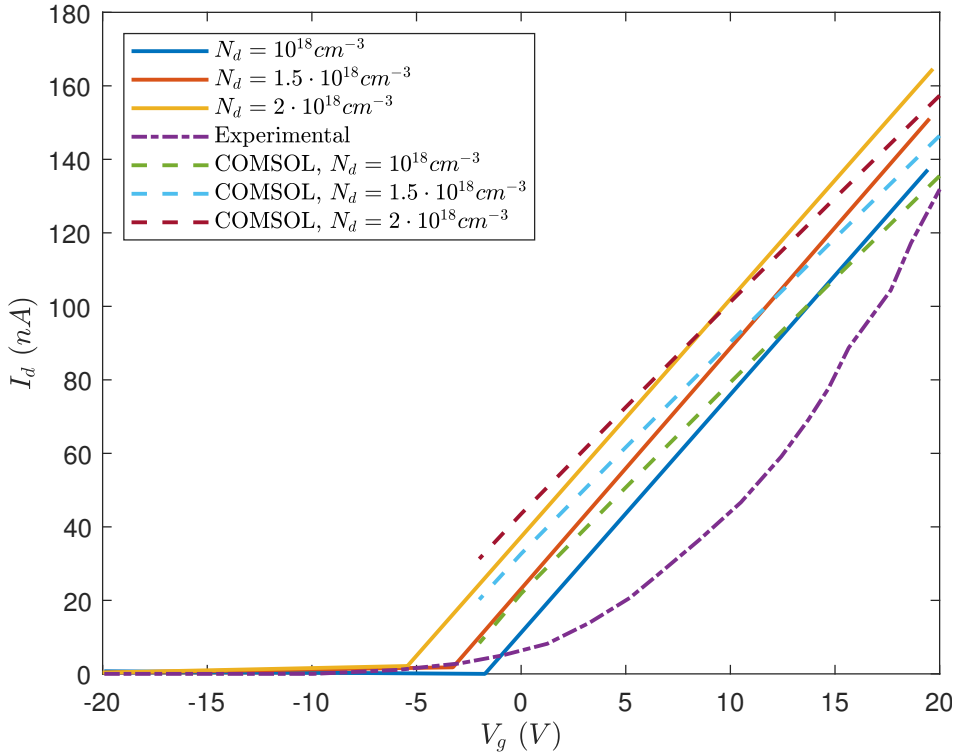

Figure 6. 4 layer $I_d(V_g)$

2.2. MoS_2 transistor with HfO_2

A FET with a 30 nm HfO_2 top gate insulator is studied in [2]. Using recent theoretical studies of mobility improvement by dielectric screening and its successful application to graphene, an atomic layer deposition (ALD) of 30 nm HfO_2 is used as a high-k gate dielectric for the local top gate and mobility booster to realize the full potential of the single-layer MoS_2. HfO_2 is used because of its high dielectric constant of 25, bandgap of 5.7 eV and the fact that it is commonly used as a gate dielectric both by the research community and major microprocessor manufacturers. A schematic depiction of

the device is shown in Fig. 7. The width of the top gate of this device is 4 µm and the top gate length, source–gate and gate–drain spacing were 500 nm.

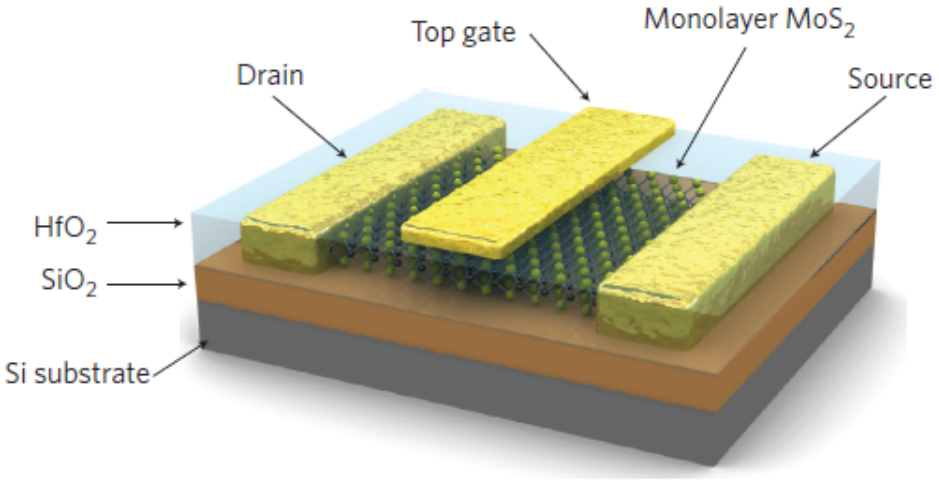

Figure 7. Three-dimensional schematic view of the transistor. [2]

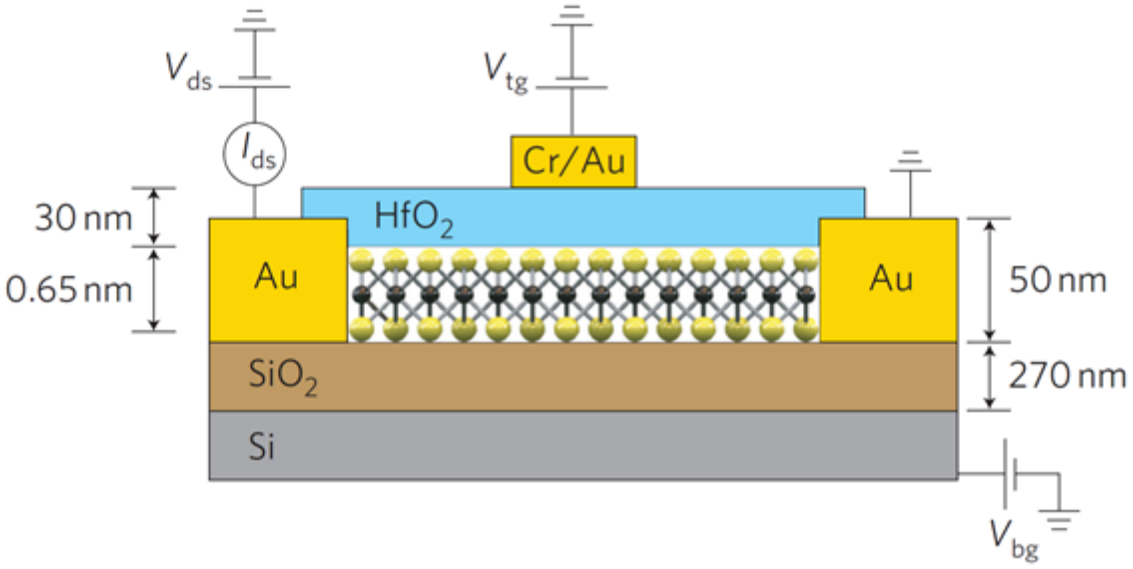

Figure 8. Cross sectional view of the structure of a monolayer MoS_2 FET together with electrical connections used to characterize the device. A single layer of MoS_2 (thickness, 6.5 Å) is deposited on a degenerately doped silicon substrate with 270 nm thick SiO_2. The substrate acts a back gate. One of the gold electrodes acts as drain and the other source electrode is grounded. The monolayer is separated from the top gate by 30 nm of ALD-grown HfO_2. The top gate width is 4 µm and the top gate length, source–gate and gate–drain spacing are each 500 nm. [2]

We created the COMSOL model as described in the previous chapter. We changed some parameters as shown in Tab. 2 and we add the HfO_2 thin gate oxide and and the top gate contact. We also used the charge conservation model in the top gate contact.

In order to find the electron affinity of MoS_2 we did a parametric study. Simulating the $I_d(V_d)$ and $I_d(V_{bg})$ curves, we varied the electron affinity parameter. We saw that an electron affinity of 5 eV the plots are very similar to the curves in [2].

Figure 9. COMSOL HfO_2 model

The parameters used in COMSOL are shown in Tab. 2.

Parameter	Value
Thickness of MoS_2	0.65 nm
Band gap MoS_2	1.8 eV
Electron affinity MoS_2	5 eV
Relative permittivity MoS_2	4.2 eV
Relative permittivity HfO_2	25
Mobility	217 $cm^2\,V^{-1}\,s^{-1}$
SRH lifetimes	1.5 ns
Metal workfunction of top gate	4.5 V
Workfunction of bottom gate	4.05 V
Metal work function source	5.1 V
Metal work function drain	5.1 V
SiO_2 Relative Permittivity	3.9
Electron effective mass	0.5 m_0
Hole effective mass	0.5 m_0
Gold contact length	500 nm
Source-gate spacing	500 nm
Gate-drain spacing	500 nm
Thickness gold contact	50 nm
SiO_2 thickness	270 nm
HfO_2 thickness	30 nm
Width	4 µm

Table 2. Parameters

The source current versus source bias characteristics (Fig. 10) is linear in the ± 50 mV range of voltages. The gating characteristics of the transistor is shown in Fig. 11 and this is typical of FET devices with an n-type channel.

From the data presented in Fig. 11 we can extract the low-field field-effect mobility of $\sim$ 217 $cm^2\,V^{-1}\,s^{-1}$ using the expression $\mu = [dI_{ds}/dV_{bg}] \cdot [L/(WC_iV_{ds})]$, where $L = 1.5\,\mu m$ is the channel length, $W = 4\,\mu m$ is the channel width and $C_i = 1.3 \times 10^{-4}\,F\,m^{-2}$ is the capacitance between the channel and the back gate per unit area ($C_i = \varepsilon_0\varepsilon_r/d$, $\varepsilon_r = 3.9$, $d = 270$ nm).

The improvement in mobility with the deposition of a high-k dielectric could be due to suppression of Coulomb scattering due to the high-k dielectric environment and modification of phonon dispersion in MoS_2 monolayers.

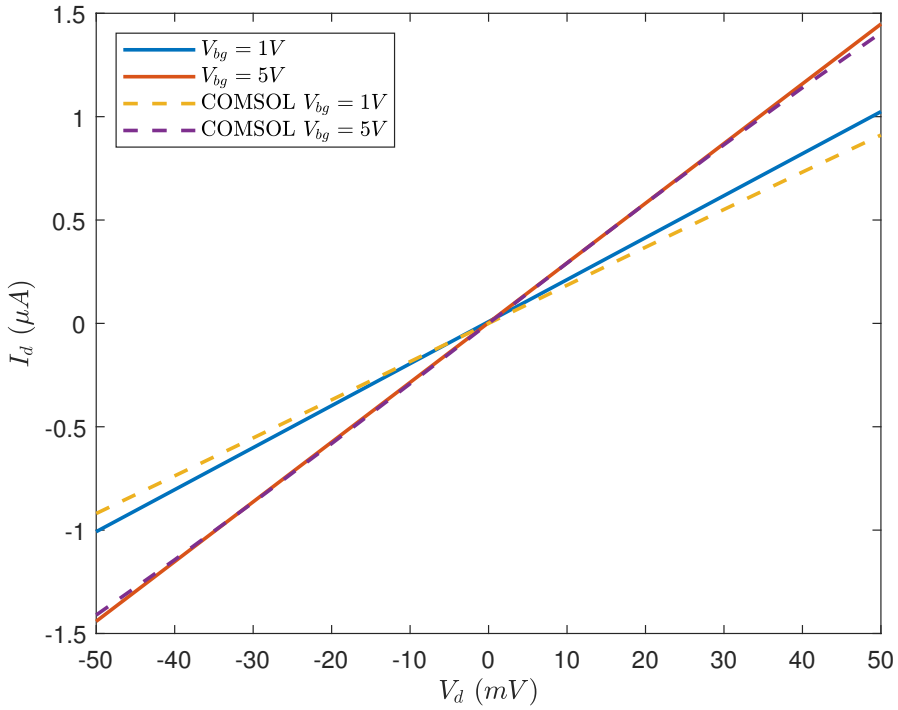

Figure 10. $I_d(V_d)$ curve acquired for V_{bg} values of 0 V, 1 V and 5 V.

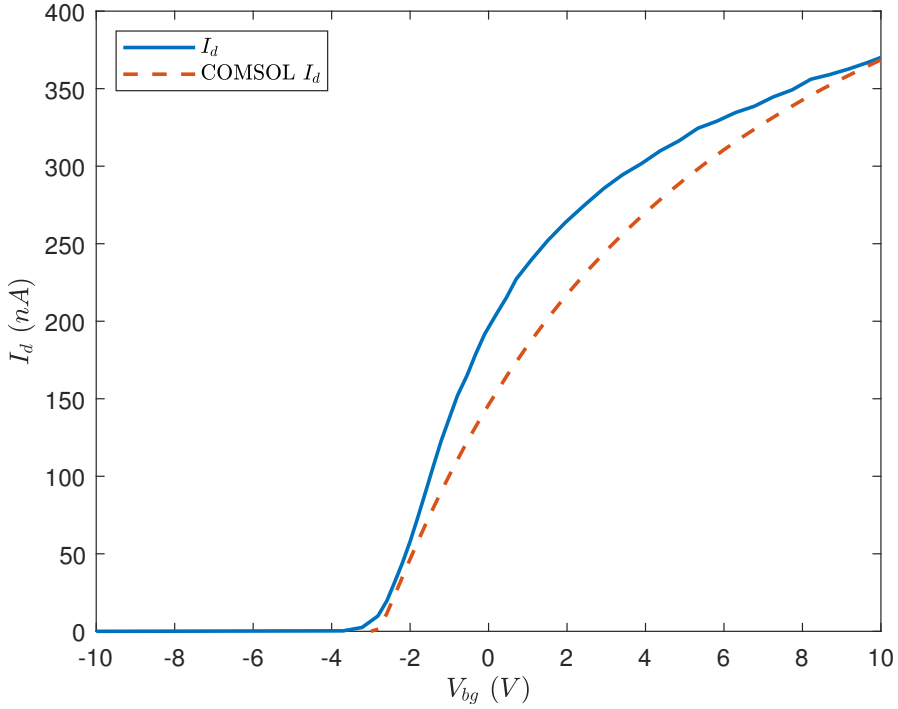

Figure 11. Transfer characteristic $I_d(V_{bg})$ for the FET with 10 mV applied bias voltage V_{ds}. Backgate voltage V_{bg} is applied to the substrate and the top gate is disconnected.

One of the crucial requirements for building integrated circuits based on single layers of MoS_2 is the ability to control charge density in a local manner, independently of a global back gate. We can do this by applying a voltage V_{tg} to the top gate, separated from the monolayer MoS_2 by 30 nm of HfO_2 (Fig. 8), while keeping the substrate grounded.

The corresponding transfer characteristic is shown in Fig. 12. For a bias of 10 mV we observe an on-current of 150 nA (37 nA μm^{-1}), current on/off ratio $I_{on}/I_{off} > 1 \cdot 10^6$ for the ± 4 V range of V_{tg} ,

an off-state current that is smaller than 100 fA (25 fA µm^{-1}) and gate leakage lower than 2 pA µm^{-1}. The observed current variation for different values of V_{tg} indicates that the field-effect behaviour of our transistor is dominated by the MoS_2 channel and not the contacts.

At the bias voltage $V_{ds} = 500$ mV, the maximal measured on-current in [2] is 10 µA (2.5 µA µm^{-1}), with $I_{on}/I_{off} > 1 \cdot 10^8$ for the ±4 V range of V_{tg}. In our simulation for $V_{ds} = 500$ mV the on-current is 3 µA but for $V_{ds} = 100$ mV and $V_{ds} = 10$ mV the on-current is the same as reported in the paper.

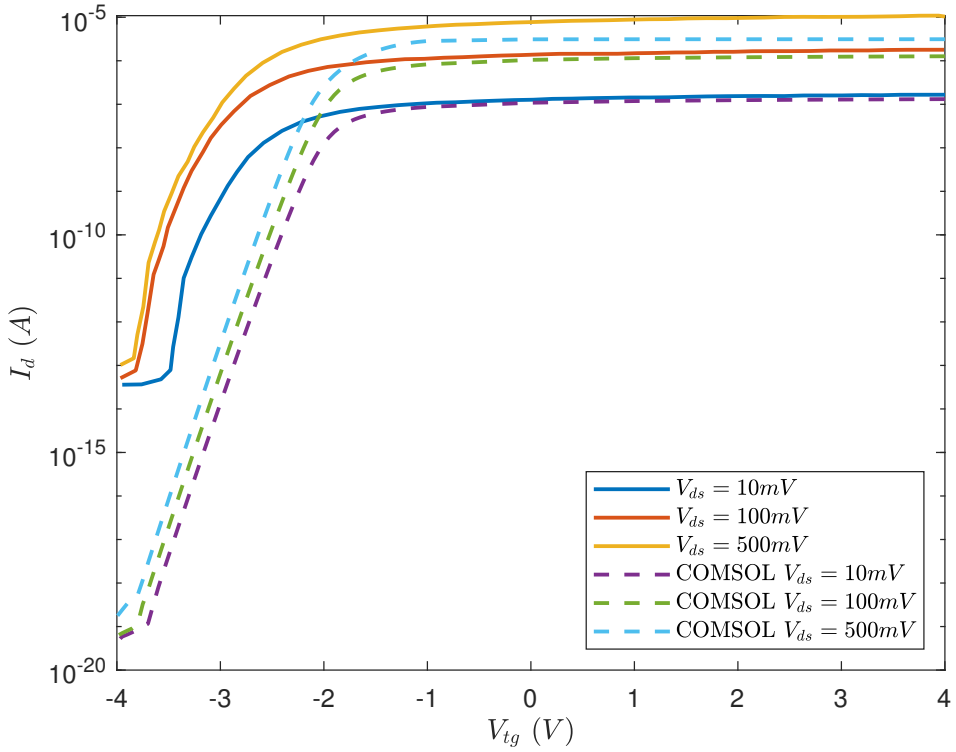

Figure 12. I_{ds}-V_{tg} curve recorded for a bias voltage ranging from 10 mV to 500 mV. Measurements are performed with the back gate grounded. The device can be completely turned off by changing the top gate bias from −2 V to −4 V. In [2] for $V_{ds} = 10$ mV, the I_{on}/I_{off} ratio is 10^6. For $V_{ds} = 500$ mV, the I_{on}/I_{off} ratio is 10^8. We obtain a major value of I_{on}/I_{off} ratio but we can still turn off the transistor with top gate bias from −2 V to −4 V.

Fig. 13 shows the I_{ds}-V_{tg} curve for $V_{bg} = 0$ V and $V_{ds} = 10$ mV.

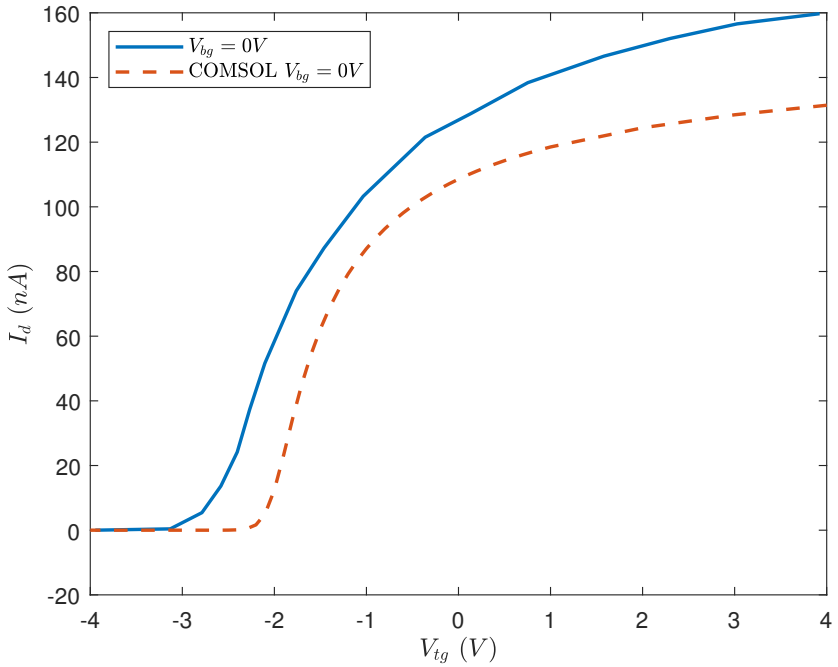

Figure 13. I_{ds}-V_{tg} for $V_{bg} = 0\,\mathrm{V}$.

The large degree of current control in our device is also clearly illustrated in Fig. 14, where we plot the drain–source current versus drain–source bias for $V_{bg} = 0\,\mathrm{V}$.

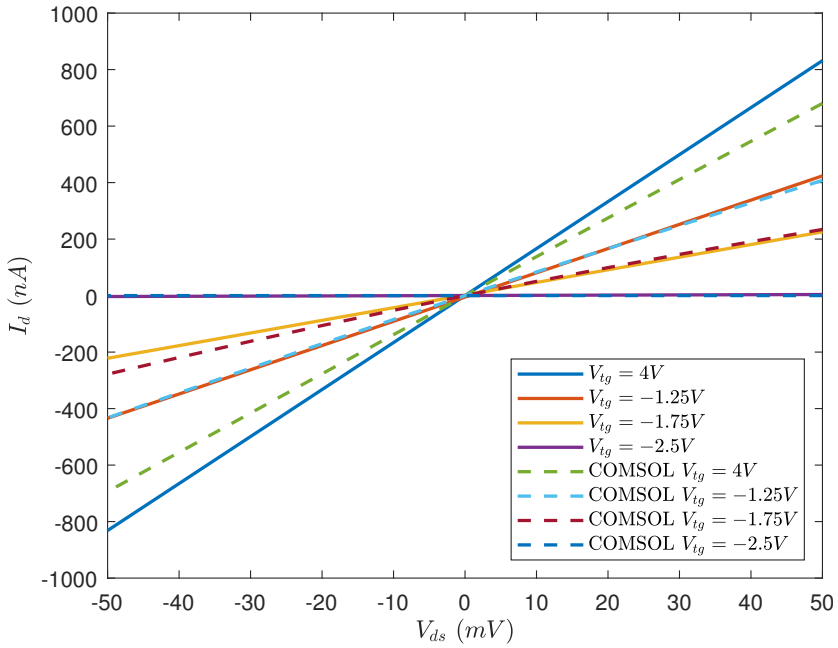

Figure 14. $I_d(V_{ds})$ curves recorded for different values of V_{tg}.

2.3. MoS_2 transistor with $Hf_{0.3}Zr_{0.7}O_2$

We tried to simulate a transitor with a thin layer of ferroelectric material. We used a layer of $Hf_{0.3}Zr_{0.7}O_2$ with 6 nm of thickness. We started from the previous COMSOL model, we changed the HfO_2 thickness from 30 nm to 20 nm.

We used the COMSOL interpolation model to implement the relation between the relative permittivity and the applied voltage described in [4] and shown in 15. We used 10 points from the curve, a linear interpolation and a nearest function extrapolation. The result is shown in Fig. 16.

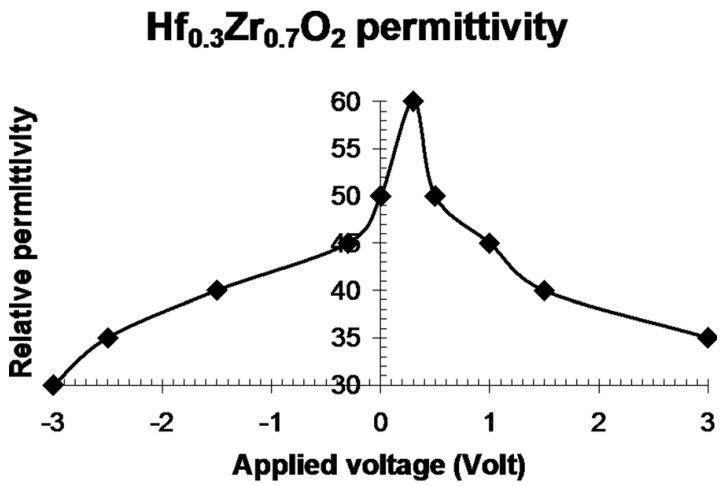

Figure 15. $Hf_{0.3}Zr_{0.7}O_2$ permittivity [4]

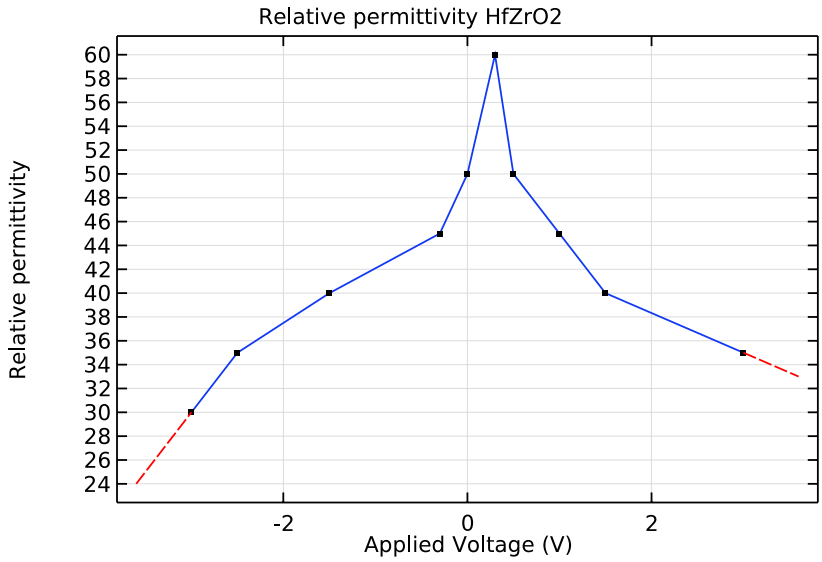

Figure 16. COMSOL $Hf_{0.3}Zr_{0.7}O_2$ permittivity

We simulated the curves in COMSOL to see the FET behaviour. The Fig. 17 shows the I_d-V_{ds} curve and is obtained with the top gate disconnected and for $V_{bg} = 0\,V$ and $V_{bg} = 5\,V$. We can see a resistive behaviour until $\sim 1\,V$ for $V_{bg} = 0\,V$ and $5\,V$.

The Fig. 18 shows the I_d-V_{ds} curve with $V_{bg} = 0\,V$ for $V_{tg} = -2\,V$, $0\,V$ and $5\,V$. In this case the maximum drain current is about $25\,\mu A$ obtained for $V_{tg} = 5\,V$. In the resistive region the slope is greater that the previous study but the maximum current is lower.

Fig. 19, 20, 21, 22 and 23 show the same studies of the previous model. A comparison with Fig. 10, 11 and 13 proves more available current when the device is in the on state compared to the previous case.

Fig. 21 shows a worse I_{on}/I_{off} ratio than Fig. 12. With a ferroelectric material we have an I_{on}/I_{off} ratio of 10^5 for $V_{ds} = 500\,mV$ and about 10^3 for $V_{ds} = 10\,mV$ while in [2] for $V_{ds} = 500\,mV$, the I_{on}/I_{off} ratio is 10^8 and for $V_{ds} = 10\,mV$, the I_{on}/I_{off} ratio is 10^6.

In Fig. 22 is shown the I_d-V_{tg} curve with $V_{bg} = 0\,V$ and $V_{ds} = 10\,mV$. Fig. 23 indicates that for $V_{tg} = -2.5\,V$ the device in still on, while in the same conditions the device is completely turned off in Fig. 14.

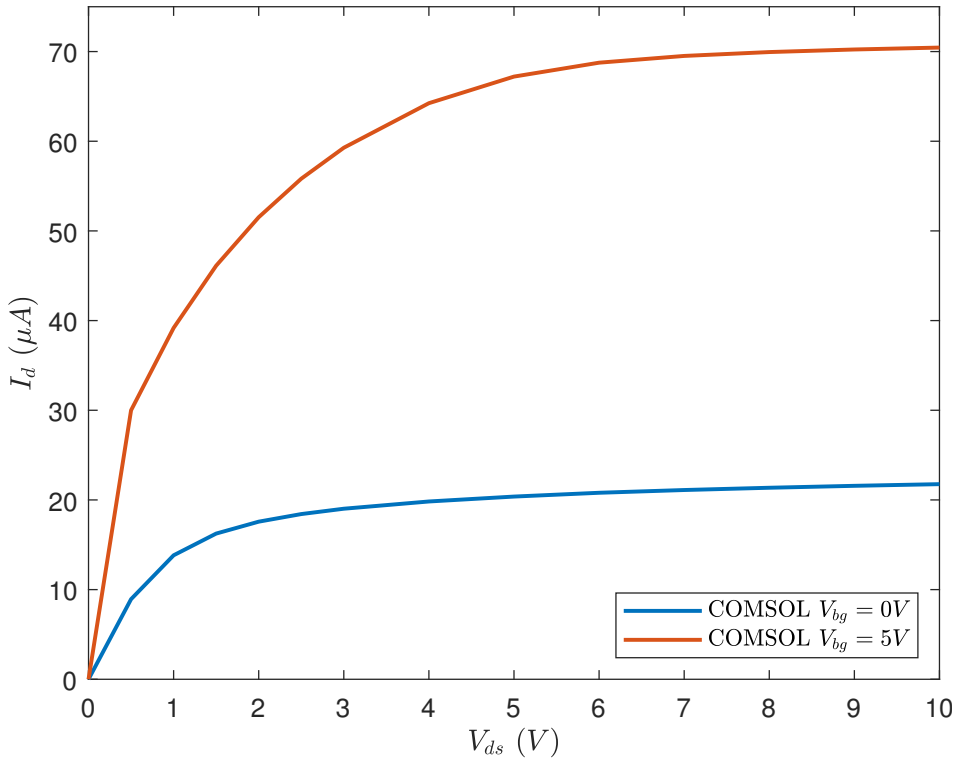

Figure 17. $I_d(V_{ds})$ varying V_{bg}

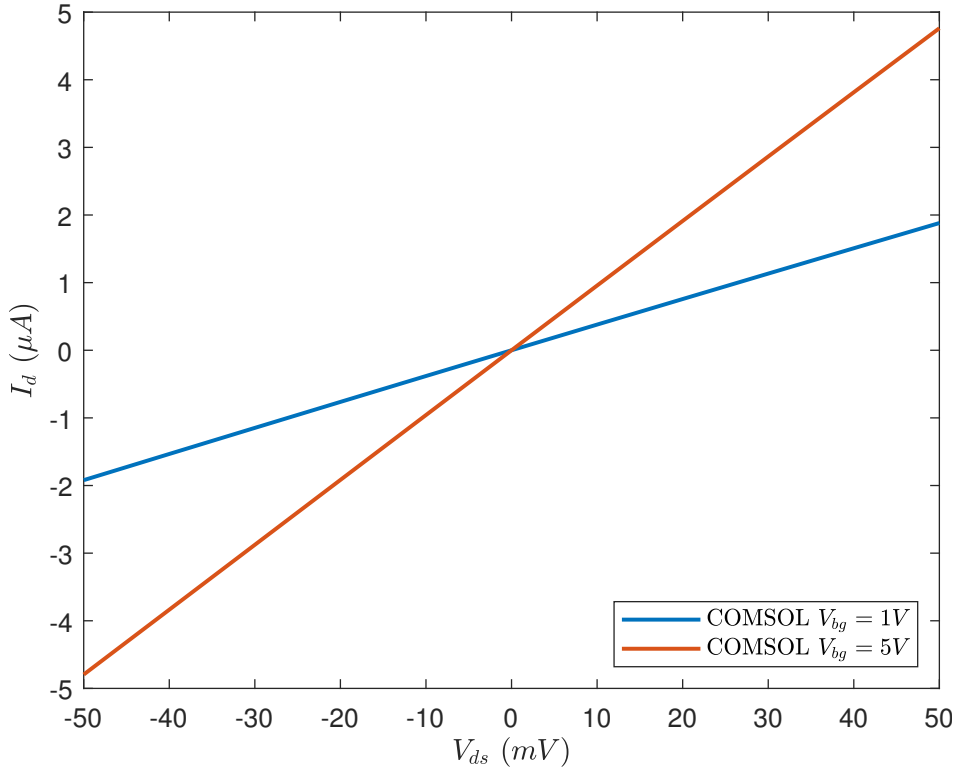

Figure 19. $I_d(V_d)$

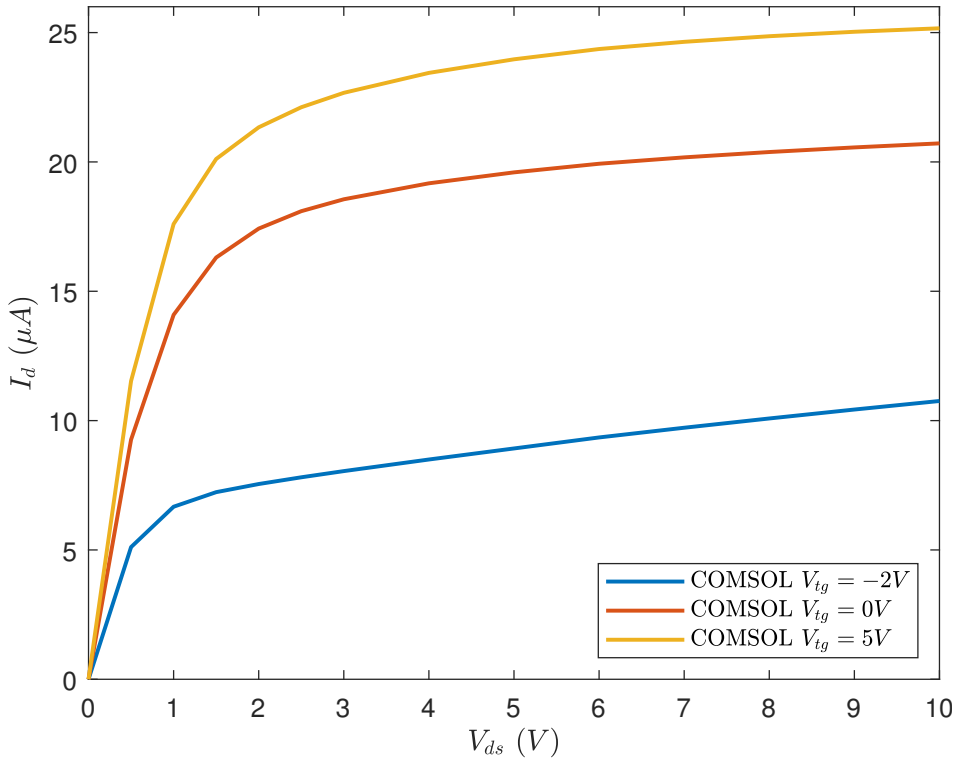

Figure 18. $I_d(V_{ds})$ varying V_{tg}

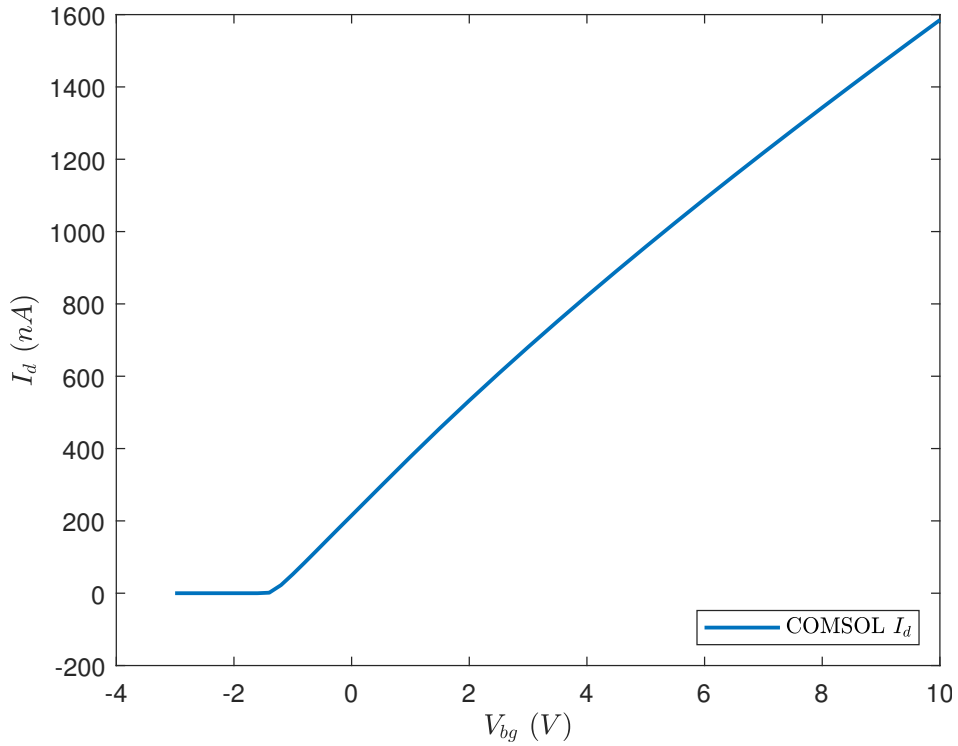

Figure 20. $I_d(V_{bg})$

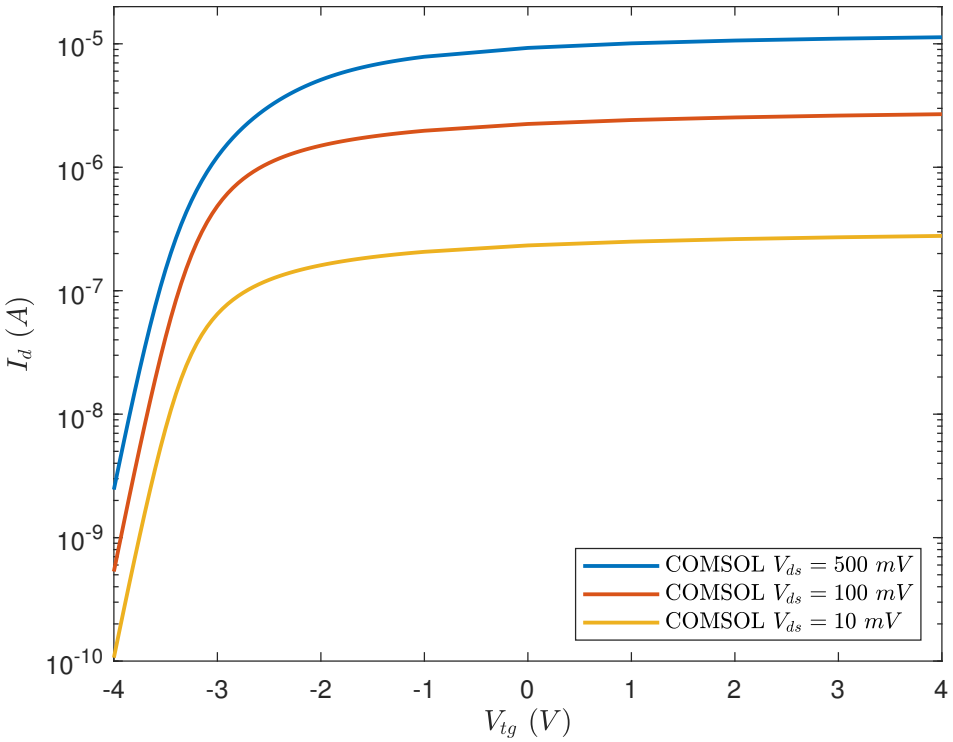

Figure 21. $I_d(V_{tg})$ varying V_{ds}

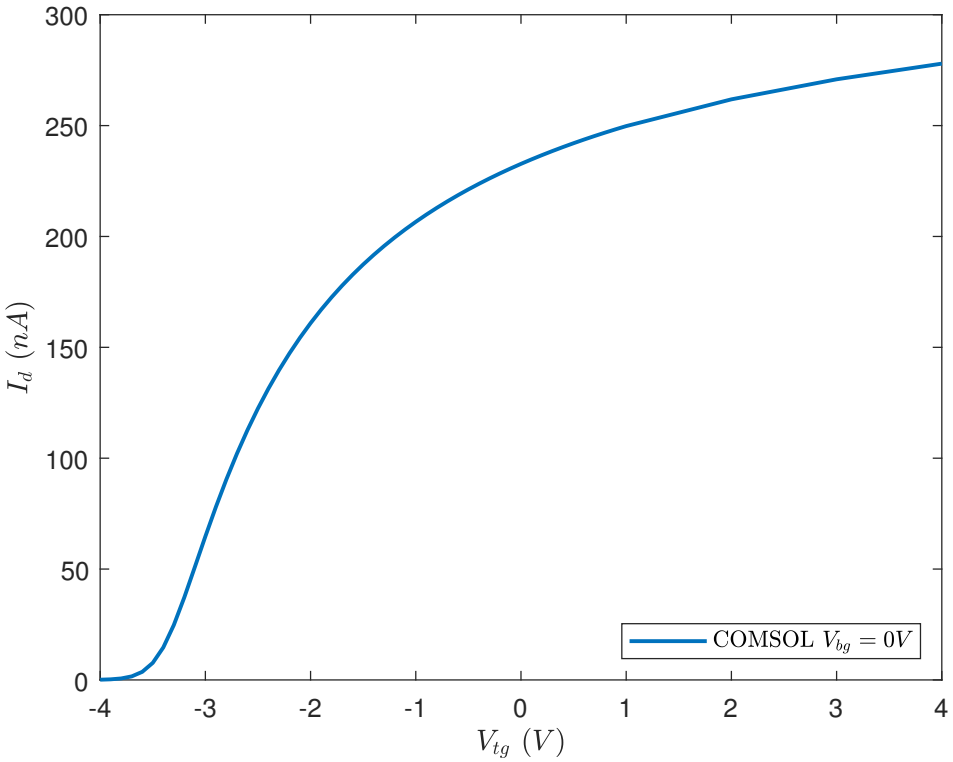

Figure 22. $I_d(V_{tg})$

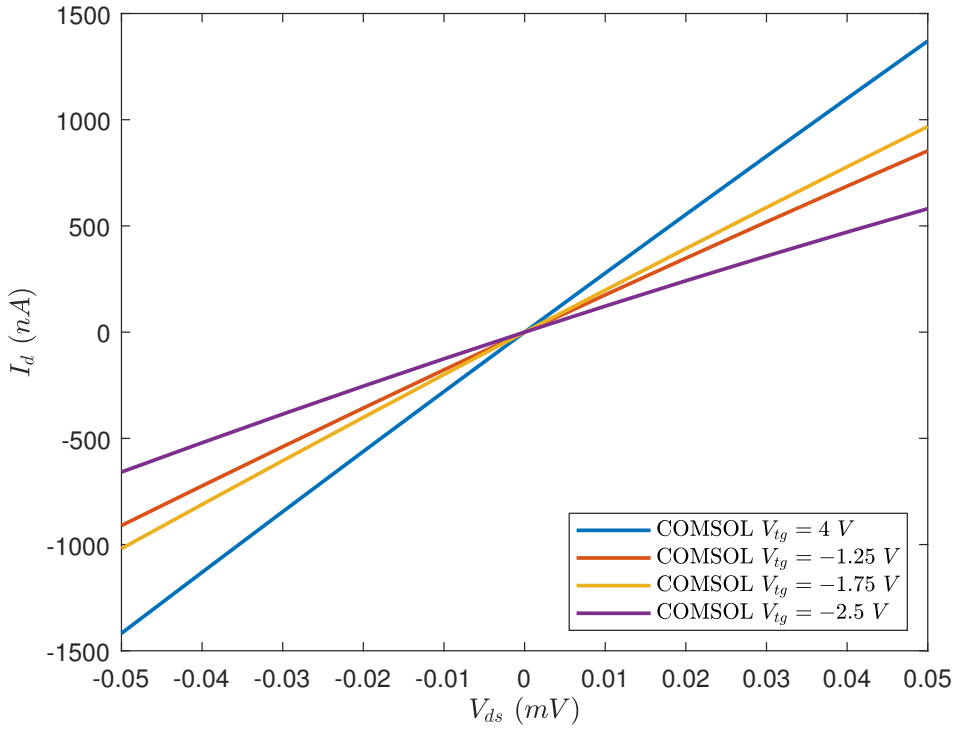

Figure 23. $I_d(V_{ds})$ varying V_{tg}

3. Materials and Methods

The first step through implementing the model in COMSOL Multiphysics was defining the geometry: setting all the sizes and the distances between the materials. Later we specified which materials to associate with the different spatial regions and, for each one of them, we assigned all the physical variables necessary for the equations. We used a table of parameters for the materials defined in [1].

The next step was defining the physics. We used the semiconductor physic that implement the Poisson equation $\nabla \cdot (-\varepsilon_0 \varepsilon_r \nabla V) = \rho$. This physic allows us to specify the MoS_2 characteristics and to define the contacts of source, drain and gates. We defined the charge conservation and its equation $\vec{D} = \varepsilon_0 \varepsilon_r \vec{E}$ in the whole model except for the 2D material. The MoS_2 is treated like a semiconductor material model so we needed to specify the relative permittivity, the band gand, the electron affinity, the effective density of states in valence and conduction band and the electron and hole mobility in the material properties. Using analytic doping model we could set the donor concentration in the MoS_2 layer. The donor concentration is a parameter and it's varied in our studies according to the plot shown in [1]. We used a trap assisted recombination to set the electron and hole lifetime according to Tab. 1.

The mesh generated automatically was acceptable and precise enough. At last we created the studies that generated the plots in this report, trying to imitate the simulated ones found in [1].

The parameters used in COMSOL are shown in Tab. 1.

4. Conclusions

Our models seems to simulate quite correctly the technology, in facts the plots obtained are very similar with the ones found in literature. We can therefore say that they can be used for further experiments and expect that the results will be similar to the real ones.

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