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How Good Can Monolayer MoS_2 Transistors Be?

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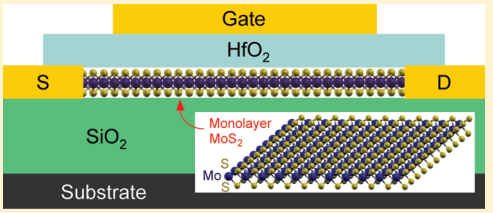
ABSTRACT: Monolayer molybdenum disulfide (MoS_2), unlike its bulk form, is a direct band gap semiconductor with a band gap of 1.8 eV. Recently, field-effect transistors have been demonstrated experimentally using a mechanically exfoliated MoS_2 monolayer, showing promising potential for next generation electronics. Here we project the ultimate performance limit of MoS_2 transistors by using nonequilibrium Green's function based quantum transport simulations. Our simulation results show that the strength of MoS_2 transistors lies in large ON−OFF current ratio (>10^{10}), immunity to short channel effects (drain-induced barrier lowering ~10 mV/V), and abrupt switching (subthreshold swing as low as 60 mV/decade). Our comparison of monolayer MoS_2 transistors to the state-of-the-art III−V materials based transistors, reveals that while MoS_2 transistors may not be ideal for high-performance applications due to heavier electron effective mass ($m^* = 0.45m_0$) and a lower mobility, they can be an attractive alternative for low power applications thanks to the large band gap and the excellent electrostatic integrity inherent in a two-dimensional system.



KEYWORDS: Molybdenum disulfide (MoS_2), layered materials, field-effect transistor, quantum transport, NEGF, device physics

Molybdenum disulfide (MoS_2), a layered transition metal dichalcogenide, has several interesting electrical, mechanical, and optical properties.[1] Apart from being widely used as a dry lubricant for automobiles due to its low friction properties, MoS_2 has been explored for applications in photovoltaics[2] and photocatalysis[3,4] for energy conversion. Structurally, MoS_2 is a stack of planes where covalently bonded S−Mo−S atoms are closely packed in a hexagonal arrangement, and the adjacent planes are held together by van der Waals interactions.[5] These weak interlayer interactions, in contrast to strong intralayer bonding, make synthesis of monolayers of MoS_2 possible by micromechanical exfoliation from bulk crystalline MoS_2[5−7] — identical to the fabrication of graphene from graphite.[8] Recent experimental studies on few layers of MoS_2 using optical absorption and photoluminescence show that, while bulk MoS_2 is an indirect band gap semiconductor with a band gap (E_g) of 1.29 eV,[9] at monolayer thickness (0.65 nm),[10] MoS_2 transitions to a direct band gap semiconductor with E_g = 1.8 eV,[5,6] thereby corroborating earlier ab initio based calculations that predicted a similar band gap.[11] High thermal stability of MoS_2 and the absence of dangling bonds,[7] coupled with the presence of significant band gap in a 2-D material render monolayer MoS_2 as an attractive candidate for switching applications, unlike graphene wherein the absence of band gap inhibits its use despite large reported mobilities (200000 $cm^2/(V\,s)$).[12]

While monolayer MoS_2 has previously exhibited poor mobility (<10 $cm^2/(V\,s)$)[8] limiting its potential for majority of the electronic applications, it has been recently reported that in the presence of a high-κ environment, the mobility of monolayer MoS_2 can increase by several times (~200 $cm^2/(V\,s)$),[7] which is similar to earlier reports of such phenomenon in the case of graphene.[13] This mobility enhancement, one of the reasons of which could be dielectric screening as predicted by theoretical calculations,[14] opens up the possibility of monolayer MoS_2 field-effect transistors for low standby and low operating power electronics. Recently, long channel monolayer MoS_2 transistors with very good ON−OFF current ratio (>10^7) and subthreshold swing (74 mV/decade) have been demonstrated experimentally.[7] While rapid progress in fabrication of short-channel MoS_2 transistors can be expected, it is of significant technological relevance to estimate the ultimate performance limit that can be achieved in such devices before an aggressive pursuit of miniaturization begins. In this Letter, we attempt to answer this question by using rigorous quantum transport simulations and view their performance in light of some of the competing non-silicon technologies to assess the viability of monolayer MoS_2 transistors for future electronic applications.

The schematic of the atomistic configuration of a monolayer MoS_2 and that of the simulated device are shown in Figure 1. To describe electronic transport through MoS_2, we perform self-consistent ballistic quantum transport simulations within the nonequilibrium Green's function (NEGF) formalism using an effective mass Hamiltonian. Transport equations are solved iteratively together with Poisson's equation until a self-consistency between charge density (calculated by analytical summation of transverse momentum modes within the first Brillouin zone) and electrostatic potential is achieved. Subsequently current is calculated as

$$I_D = \frac{e}{\hbar^2}\sqrt{\frac{m_y^* k_B T}{2\pi^3}} \int dE_{k_x} \left\{ F_{-1/2}\left(\frac{\mu_1 - E_{k_x}}{k_B T}\right) - F_{-1/2}\left(\frac{\mu_2 - E_{k_x}}{k_B T}\right) \right\} T_{SD}(E_{k_x}) \quad (1)$$

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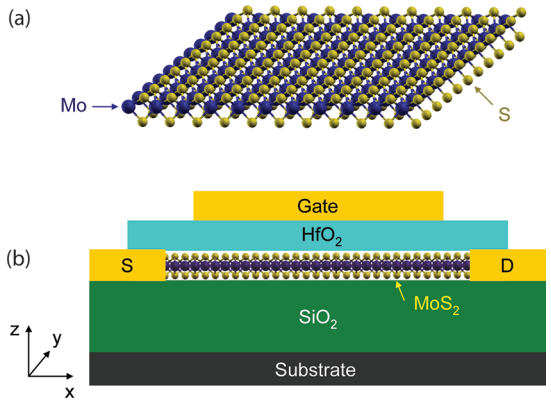

Figure 1. Device structure of a monolayer MoS_2 transistor. (a) Atomistic configuration of two-dimensional MoS_2 monolayer, which is a 6.5 Å thick large band gap semiconductor (E_g = 1.8 eV). (b) Schematic cross section of a monolayer MoS_2 transistor. The channel is an MoS_2 monolayer, and the source and drain contacts can be of a metal like gold (Au), which is believed to make a good contact with small Schottky barrier at the junction (ref 7). The nominal device has the following parameters: Gate length L_G = 15 nm, HfO_2 (κ = 25) gate oxide thickness t_{ox} = 2.8 nm, gate underlap of 2 nm at each side, Schottky barrier height of Φ_B = 0.1 eV, power supply voltage of 0.5 V.

where $F_{-1/2}(.)$ denotes the Fermi−Dirac integral of order −1/2, $T_{SD}(.)$ is the transmission coefficient from source to drain, μ_1 and μ_2 are source and drain electrochemical potentials, $\hbar$, m_y^*, e, k_B, T, and E_{k_x} are reduced Planck's constant, transverse effective mass, elementary charge, Boltzmann constant, temperature, and longitudinal energy, respectively. Gate leakage current is ignored. The conduction band effective mass along the transport direction (x) is calculated to be $0.45m_0$ (K → Γ), m_0 being the free electron mass, from the dispersion relations of monolayer MoS_2.[11] A calculation of effective mass along K → M yields a similar value to the first order. Hence we assume the transverse effective mass to be identical to that along the transport direction. The Hamiltonian of the metallic regions at source and drain is modeled using an effective mass close to m_0 ($1.01m_0$),[15] and Dirichlet boundary conditions are imposed at the contacts. We use a dielectric constant of 3.3 for MoS_2.[16,17] Detailed device parameters used in this work are provided in the caption of Figure 1b. For the simulated device, source and drain work functions are assumed to be the same as that of the gate. A grid spacing as small as 0.1 nm along the x direction ensures the presence of states in both contact and channel regions in the entire energy range of interest within a single band description of effective mass Hamiltonian.

A very good Ohmic contact with low contact resistance is essential in optimizing the device performance. However, one of the issues in the fabrication of an Ohmic contact is the difficulty in finding metals with desired work function. Tunneling contacts using narrow Schottky junctions, which is a more practical way to realize Ohmic contacts, may suffer from Fermi-level pinning due to defects and interface states resulting in a significant tunneling barrier and hence an increased contact resistance.[18] We analyze the experimental I_D-V_{BG} (drain current−back-gate voltage) characteristics at source-to-drain voltage V_D = 10 mV reported in ref 7 in order to estimate the Schottky barrier height for the Au−MoS_2 junction, which we use for simulating our nominal device. The total resistance of the device at any gate voltage $R_{TOT}(V_{BG})$, expressed as V_D/I_D, is composed of three different

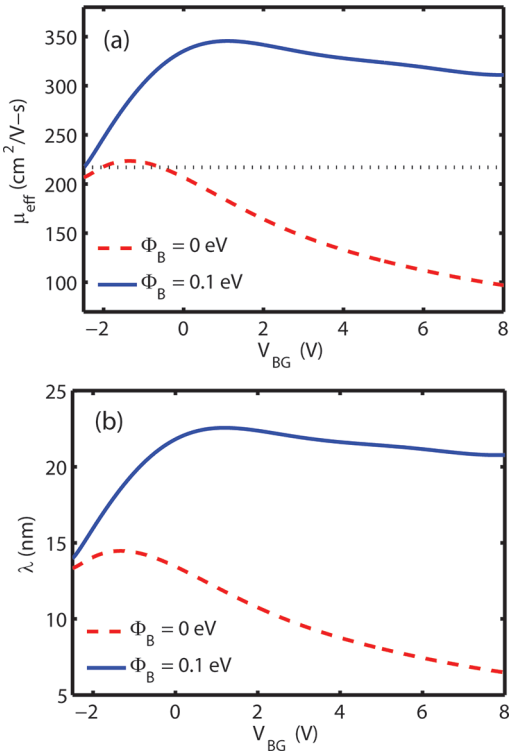

Figure 2. Analysis of experimental back-gated characteristics. (a) Variation of effective mobility μ_{eff} with back-gate voltage V_{BG} obtained from the analysis of experimental back-gated current−voltage characteristics at V_D = 10 mV reported in ref 7. Contact resistances are accounted for by using barrier height Φ_B at the metal−MoS_2 junction as a parameter. For a given I_D, a larger Schottky barrier height decreases the channel resistance resulting in a higher mobility and vice versa. A mobility of 217 $cm^2/(V\ s)$ calculated in ref 7 without accounting for contact resistance is also plotted with a black dotted line. (b) Variation of mean free path λ with V_{BG} for Φ_B = 0 and 0.1 eV.

resistance components: the intrinsic channel resistance $R_{ch}(V_{BG})$ stemming from momentum breaking in the transport direction; the ballistic resistance $R_{Bal}(V_{BG})$ arising due to finite electron group velocity; the specific contact resistivity R_c.[19] The resistance R_c (per unit thickness), for a given Schottky barrier height of Φ_B, assuming only thermionic current for the sake of simplicity, can be written as[18]

$$R_c = \frac{h^3}{4\pi e^2 m^* t k_B T} \exp\left(\frac{e\Phi_B}{k_B T}\right) \quad (2)$$

where h, m^*, and t are Planck's constant, effective mass, and thickness of MoS_2 monolayer, respectively. In order to ensure that $2R_c$ (factor of 2 to account for resistances on both source and drain sides) is less than R_{TOT} for all values of V_{BG}, Φ_B has to be less than or equal to 0.1 eV. Thus, we use a barrier height of 0.1 eV for our nominal device. However, it must be noted that this value of Φ_B represents an upper bound on the actual Schottky barrier height, as all other parasitic, gate-voltage-independent resistances have been lumped into metal−semiconductor (M−S) junction resistance.

We further analyze the I_D-V_{BG} characteristics, following the approach outlined in ref 19 to extract information about mobility (μ_{eff}) and mean free path (λ). Figure 2 shows the variation of μ_{eff} and λ with V_{BG} for two different values of Schottky barrier

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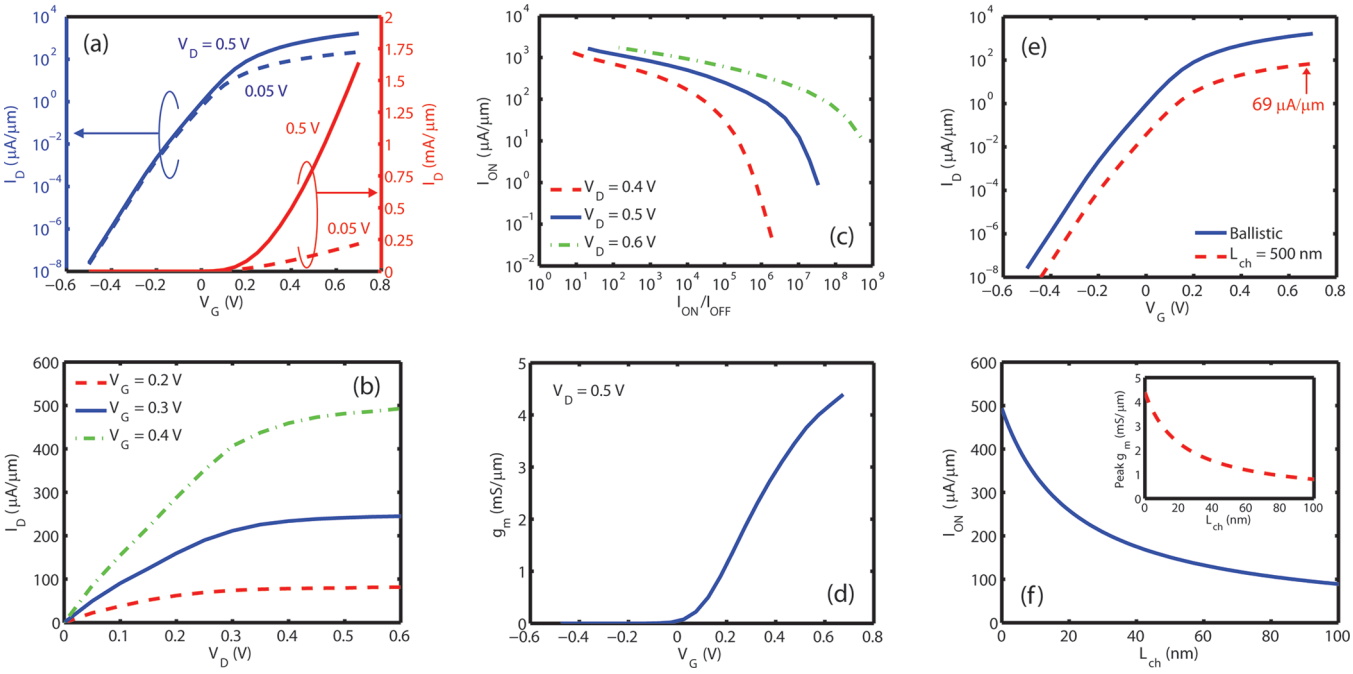

Figure 3. Device characteristics of monolayer MoS_2 transistors. (a) I_D-V_G characteristics at V_D = 0.05 and 0.5 V on logarithmic (left axis) and linear scales (right axis). For the nominal device simulated, a maximum ON current as high as 1.6 mA/μm and a subthreshold swing (SS = $\partial V_G/\partial \log_{10}(I_D)$) close to 60 mV/decade are achieved. Drain-induced barrier lowering (DIBL) is as small as 10 mV/V even with very short channel length. (b) I_D-V_D characteristics at V_G = 0.2, 0.3, and 0.4 V. Beyond V_D = 0.4 V, MoS_2 transistors show a clear saturation behavior with an output conductance ($g_d = \partial I_D/\partial V_D$) of 21, 51, and 133 μS/μm at V_G = 0.2, 0.3, and 0.4 V, respectively. (c) I_{ON} versus I_{ON}/I_{OFF} for V_D = 0.4, 0.5, and 0.6 V. With V_D = 0.5 V, I_{ON} is as high as 500 μA/μm with 4 orders of magnitude in ON−OFF current ratio. For the same ON current, $I_{ON}/I_{OFF} > 10^5$ can be achieved with 0.6 V of drain voltage. (d) Transconductance ($g_m = \partial I_D/\partial V_G$) vs V_G at V_D = 0.5 V. The g_m is as large as 4.4 mS/μm for the nominal device within the voltage range considered in this study. (e) I_D-V_G characteristics for a long channel device with L_{ch} = 500 nm is projected (dashed line) by $I_{proj} = I_{bal} \times \lambda_{max}/(L_{ch} + \lambda_{max})$, where I_{bal} is the ballistic current adopted from our simulation results (solid line), I_{proj} is the projected current for larger size of devices taking scattering into account, λ_{max} is peak mean free path, and L_{ch} is channel length. (f) Variation of I_{ON} (defined at V_{ON} = 0.4 V) with channel length. As L_{ch} increases, current is decreased since carriers are exposed to greater number of scattering events. When L_{ch} = 100 nm, projected current is one-fifth of the ballistic current. The inset shows a similar plot for peak g_m.

heights of Φ_B = 0 and 0.1 eV. The extracted peak mobility is about 220 and 350 $cm^2/(V\,s)$ for Φ_B = 0 and 0.1 eV, respectively. The corresponding mean free paths are 15 and 22 nm. We choose the gate length to be 15 nm so that the device operates away from the diffusive limit where the transport is predominantly limited by scattering, thereby making our performance projections realistic. An underlap of 2 nm each on the source and the drain sides is introduced to reduce the fringe capacitances without significantly increasing the series resistance.

The key device characteristics of MoS_2 transistors are shown in Figure 3. The transfer characteristics reveal that the maximum current (I_{max}) is ~1.6 mA/μm. However, we note that in the case of reflectionless contacts, I_{max} can be even larger due to the nonparabolicity present in the conduction band of monolayer MoS_2 wherein a satellite valley along K → Γ, which is only about $3k_BT$ above the conduction band minima, contributes to enhanced density-of-states than what is predicted from our parabolic band approximation. The maximum−minimum current ratio (I_{max}/I_{min}) can be more than 10 orders of magnitude ignoring the gate leakage (Figure 3a). Gate-induced drain leakage (GIDL), one of the main leakage mechanisms that limits I_{min} in a conventional metal−oxide−semiconductor (MOS) geometry, is significantly less in the case of an MoS_2 transistor than in its Si counterpart due to the larger band gap, and hence a smaller gate voltage can, in principle, further reduce I_{min}. It must be noted, however, that a more rigorous analysis to predict the maximum achievable I_{max}/I_{min} requires a multiband Hamiltonian description (including valence band) to properly account for the effects of GIDL, which is beyond the scope of this study. In practical applications, what is more important than I_{max}/I_{min} is the ON−OFF current ratio (I_{ON}/I_{OFF}), where the voltage window between V_{ON} and V_{OFF} is the same as power supply voltage (i.e., $V_{ON} - V_{OFF} = V_D$). Therefore, I_{ON}/I_{OFF} can be increased with a larger supply voltage for the same ON state current. For the simulated device structure (L_G = 15 nm), drain-induced barrier lowering (DIBL) is negligibly small (10 mV/V, Figure 3a) due to excellent electrostatics of the 2-D geometry, and hence a larger V_D can significantly increase the I_{ON}/I_{OFF} ratio for a given I_{ON} (Figure 3c). In Figure 3b, we can also see that the output characteristics for a given V_G show saturation beyond V_D = 0.4 V with reasonably small output conductance (g_d = 21, 51, and 133 μS/μm at V_G = 0.2, 0.3, and 0.4 V, respectively). We have also plotted the intrinsic device transconductance ($g_m = \partial I_D/\partial V_G$) from the I_D-V_G data at V_D = 0.5 V (Figure 3d). The maximum g_m is 4.4 mS/μm, which is still less in comparison to the peak g_m that can be achieved, as g_m is monotonically increasing over the entire range of V_G considered. This implies that at the largest gate voltage applied (V_G = 0.7 V), additional gate voltage could still significantly enhance current and the consequent voltage drop would mainly be across the semiconductor and not across the gate oxide. Therefore, for the simulated EOT, the operation of a monolayer MoS_2 transistor is mainly

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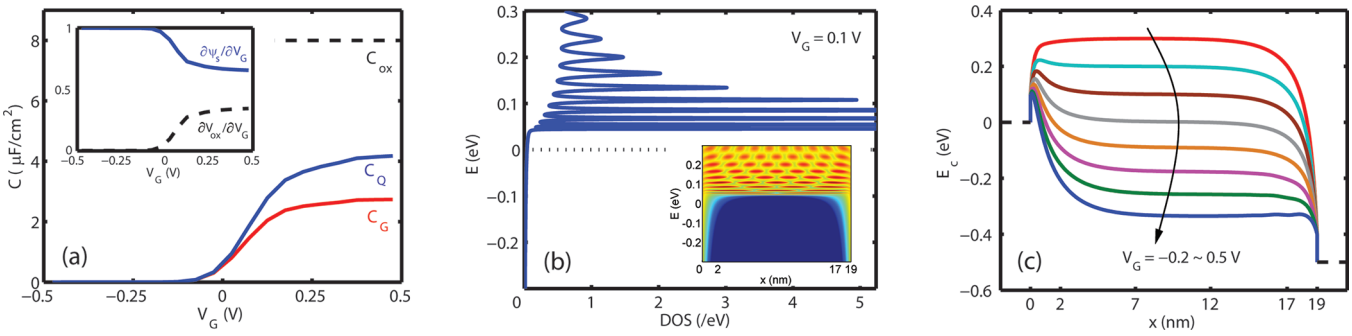

Figure 4. Capacitance−voltage (C−V) characteristics of monolayer MoS_2 transistors with V_D = 0 V. (a) Gate capacitance ($C_G = \partial Q/\partial V_G$) and quantum capacitance ($C_Q = \partial Q/\partial \psi_s$) vs V_G. Oxide capacitance ($C_{ox} = \kappa\varepsilon_0/t_{ox}$) is shown by the dashed line. $\partial\psi_s/\partial V_G$ and $\partial V_{ox}/\partial V_G$ are shown for the same V_G range in the inset. (b) Density-of-states (DOS) vs energy (main panel) and surface plot of logarithmic local density-of-states (LDOS) (inset) at V_G = 0.1 V. The C_Q plot, shown in Figure 4a, can be understood herein by examining the average of DOS near the Fermi level (dotted line) at a given V_G. For gate voltages up to about ~0.1 V, the gate controls the channel potential efficiently, as shown by a large $\partial\psi_s/\partial V_G$ in the inset of Figure 4a; subsequently C_Q increases leading to a reduction in gate control. Due to the short channel length, the DOS is reminiscent of a 1-D material system, wherein the Van Hove peak at each sub-band energy is broadened to a different extent by the contact, rather than that of a 2-D system with constant DOS. (c) Conduction band (E_c) profile along the channel at V_D = 0.5 V and V_G = −0.2 to 0.5 V in steps of 0.1 V. When a considerable V_D is applied, gate control over the channel potential can still be efficient even at high gate voltages, indicating the operation close to quantum capacitance regime at the ON state.

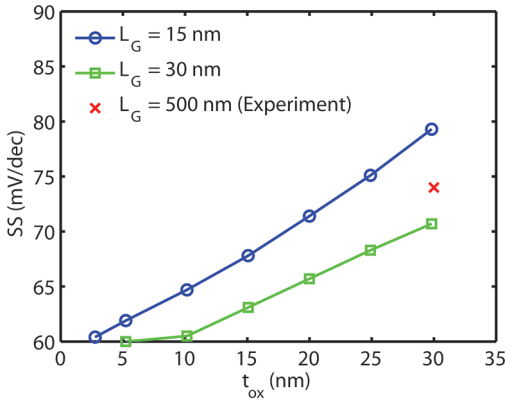

Figure 5. Variation of subthreshold swing with oxide thickness. Subthreshold swing (SS) vs oxide thickness (t_{ox}) with gate length of L_G = 15 and 30 nm. Subthreshold swing increases linearly with oxide thickness due to the decrease in C_{ox}. For the same t_{ox}, the subthreshold swing of a device with longer gate length is significantly smaller due to immunity to short channel effects. The cross shows the experimental data from ref 7, implying that the gate efficiency, in practice, could be significantly improved by optimization.

dictated by its quantum capacitance and not by the oxide capacitance, the details of which will be discussed later.

The experimental characteristics in ref 7 show a maximum drive current of 2.5 μA/μm for a device with a 500 nm long gate. Therefore, it is important to estimate the transfer characteristics for an optimized device with a similar gate length. Using the mean free path extracted from the experimental characteristics (Figure 2b), we calculate the corresponding I_D−V_G characteristics by multiplying the ballistic current from our simulations with $\lambda_{max}/(L_{ch} + \lambda_{max})$ (where λ_{max} and L_{ch} are the peak mean free path and channel length, respectively) as shown in Figure 3e. The maximum current obtained in this case is 69 μA/μm. The difference between this value and the experimentally observed 2.5 μA/μm is then likely due to the underlap series resistances, and a significant performance boost may be expected by reducing them.

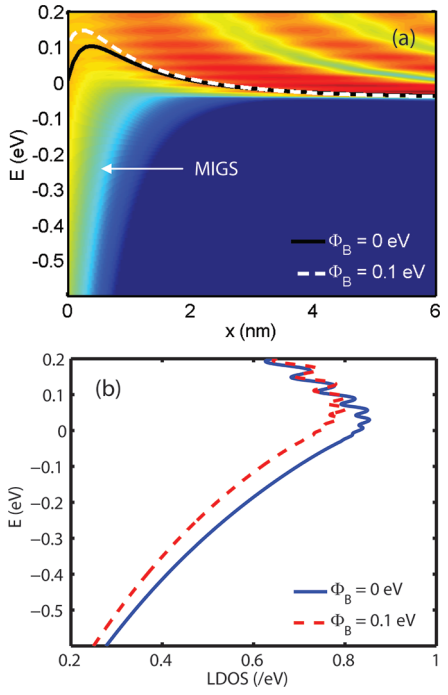

Figure 6. (a) Logarithmic LDOS for Φ_B = 0 at V_G = 0.15 V and V_D = 0.5 V near the source. Conduction band profile is shown as a solid line. The channel electrostatic potential increases near the metal−semiconductor interface, resulting in an effective barrier of ~0.1 eV, due to metal-induced gap states (MIGS). The E_c in the case of Φ_B = 0.1 eV is also plotted for comparison (dashed line). (b) DOS from the source−channel interface (x = 1 Å) for Φ_B = 0 and 0.1 eV. At a given energy, the DOS is larger in the case of a smaller barrier height since carriers in metallic contact effectively see a smaller tunneling barrier.

The scaling behavior is similarly investigated by calculating I_{ON} (defined at V_{ON} = 0.4 V) and the peak g_m as a function of L_{ch} up to 100 nm, as shown in Figure 3f.

Capacitance−gate voltage (C−V_G) characteristics are explored by performing equilibrium simulations, i.e., with source

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Table 1. Comparison of Key Device Performance Parameters of $In_{0.7}Ga_{0.3}As$ Quantum-Well FET (ref 22) and Monolayer MoS_2 FET of Identical EOT and Channel Length

	L_{ch} (nm)	EOT (Å)	I_{max} (mA/μm)	peak g_m (mS/μm)	max I_{ON}/I_{OFF}	min SS (mV/decade)
$In_{0.7}Ga_{0.3}As$ quantum-well FET (ref 22)	75	22	0.49	1.75	312	85
monolayer MoS_2 FET	75	22	0.19	0.3	1.4×10^7	60

and drain terminals grounded. The total gate capacitance C_G ($=\partial Q/\partial V_G$) and the quantum capacitance C_Q ($=\partial Q/\partial \psi_s$) are numerically calculated from self-consistent charge Q and surface potential ψ_s obtained at each gate voltage (Figure 4a). Our numerical simulation results are in accordance with the analytical capacitance model (i.e., $1/C_G = 1/C_Q + 1/C_{ox}$) and the principle of voltage division.[20] At low values of V_G, the total gate capacitance is very small due to negligible charge density in the device. However as V_G increases, C_Q, which is a measure of the average density-of-states (DOS) at equilibrium Fermi level,[20] increases due to lowering of electrostatic potential in the channel (Figure 4b). The saturation in C_Q to a value smaller than the theoretically expected quantum capacitance in 2-D systems ($C_Q^{2\text{-}D} = e^2m^*/\pi\hbar^2$) is a result of reduced DOS in the channel due to wave function reflections at the contacts. With increasing gate voltage, the gate efficiency ($\partial\psi_s/\partial V_G$) decreases (inset of Figure 4a) due to charge accumulation and screening effect. It must, however, be noted that under nonequilibrium conditions (with finite V_D), the gate control over channel electrostatics is good even at large gate voltages ($\partial(E_c/e)/\partial V_G = 0.78$ at $V_G = 0.5$ V as shown in Figure 4c) due to lack of charge accumulation - an indication of the fact that the device operates closer to the quantum capacitance regime than to the oxide capacitance regime.

It has been reported that high-κ dielectric plays an important role in improving the monolayer MoS_2 mobility and hence the device performance.[7] The gate oxide can also significantly affect the switching abruptness, and therefore we examine the effect of oxide thickness on subthreshold swing (SS). As shown in Figure 5, SS increases linearly with oxide thickness, which is also predicted by the analytical subthreshold swing model in a conventional MOSFET.[21] At $t_{ox} = 30$ nm, our nominal device shows larger SS (79 mV/decade with $L_G = 15$ nm) than the experimentally reported value for same oxide thickness (74 mV/decade with $L_G = 500$ nm),[7] owing to short channel behavior. However, with $L_G = 30$ nm, SS improves considerably due to the suppression of short channel effects (71 mV/decade for $t_{ox} = 30$ nm). Our simulations predict that the reported value of SS = 74 mV/decade could be achieved at $L_G = 23$ nm with $t_{ox} = 30$ nm. We also analyzed the electrostatics of the exact geometry reported in ref 7 at OFF state by solving the Laplace equation and confirmed $\partial(E_c/e)/\partial V_G$ to be equal to 1, implying that SS is expected to be 60 mV/decade. Hence we believe that there exists considerable room for optimization of gate dielectrics in MoS_2 transistors.

In fabricating monolayer MoS_2 transistors, gold (Au) has been used to create an Ohmic contact−Schottky contact with negligible barrier height.[7] Our simulations show that the Schottky barrier height can effectively increase (by up to 0.1 eV in the case of $\Phi_B = 0$ for intermediate values of gate voltage) as can be seen from the solid line in Figure 6a. This is due to enhanced polarization in the channel near the M−S junction owing to localized states induced by the metallic contact (known as metal-induced gap states (MIGS), which are clearly shown in the local density-of-states (LDOS) plot in Figure 6a). We note that this increase in barrier height, at identical gate voltage, is smaller for contacts with larger Schottky barriers (dashed line in Figure 6a). This is due to the fact that a larger barrier reduces the tunneling probability for carriers, resulting in a smaller penetration of contact states into the channel, which is confirmed by the density-of-states plot at the source end for $\Phi_B = 0$ and 0.1 eV shown in Figure 6b. However, this increase in effective barrier height vanishes as V_G increases further.

With the above analysis of monolayer MoS_2 transistors, it is instructive to compare some of their key device performance parameters to those of some other nonconventional devices recently explored. Table 1 shows such a comparison with $In_{0.7}Ga_{0.3}As$ quantum-well FETs reported in ref 22. It is evident that the strength of MoS_2 transistors lies in their large band gap, which results in a significant I_{ON}/I_{OFF} and the excellent electrostatic integrity due to the 2-D nature of the system. However, with mobility lower than most of the III−V materials, MoS_2 transistors are more suited for low standby and operating power applications than for high performance where the experimental results from the former outperform the best theoretical predictions for the latter. The other most widely investigated 2-D system − a graphene transistor − has a very poor ON−OFF ratio despite a high ON current,[23] due to lack of band gap, making it very difficult to use them for digital applications. Fabrication of very narrow graphene nanoribbons with a finite band gap still remains a challenge and is prone to edge roughness resulting in a variation in energy gap. While there have been several reports of high-quality graphene nanoribbon transistors with large ON current, poor subthreshold swing and small ON−OFF ratio continue to remain problems.[24,25] Hence monolayer MoS_2 transistors, owing to their unique combination of exquisite electrostatic integrity and large band gap, can prove to be a better alternative for low power applications than several of the non-Si devices already explored.

To summarize, we have projected the ultimate scaling limit of monolayer MoS_2 transistors by performing self-consistent quantum transport simulations. The key features of MoS_2 transistors are (i) large g_m (4.4 mS/μm) due to low DOS, (ii) significant I_{max}/I_{min} ($>10^{10}$) owing to a large band gap, and (iii) excellent short channel behavior (DIBL ~10 mV/V and SS ~60 mV/decade) resulting from enhanced gate control. Along with these very good electrical characteristics, planarity of MoS_2 monolayer makes MoS_2 transistors one of the most viable candidates for future low power applications. Further, the properties of monolayer MoS_2 like high thermal stability, chemical inertness, transparency, flexibility, and relative inexpensiveness give MoS_2 transistors a unique advantage for several low cost electronic applications.

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