Towards mm-wave nanoelectronics and RF switches using MoS_2 2D Semiconductor

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***Abstract*—In this paper, we report state-of-the-art large area CVD monolayer MoS_2-based RF transistors and RF switches. An embedded gate structure was used to fabricate short channel CVD MoS_2 RF FETs with an intrinsic f_T of 20 GHz, intrinsic f_{max} of 11.4 GHz, and the high-field saturation velocity v_{sat} of 1.88 × 10^6 cm/s. The gate-first process allows for enhancement mode operation, I_{ON}/I_{OFF} ratio of 10^8, and a transconductance (g_m) of 70 µS/µm. Also, we use a vertical MIM structure for a RF switch based on CVD MoS_2. The device was programmed with a voltage as low as 1 V, and achieves an ON-state resistance of ~5 Ω and an OFF-state capacitance of ~6 fF. We measured and simulated the RF performance of the device up to 50 GHz and report 0.5 dB insertion loss, 15 dB isolation (both at 50 GHz), and 5 THz cutoff frequency.**

***Index Terms*—Two-dimensional material, TMD, CVD MoS_2, RF applications, transistors, RF switches, GHz regime**

I. Introduction

Research interest in the field of RF nanoelectronics using atomically thin two-dimensional transition metal dichalcogenides (TMDs) has gained significant momentum. MoS_2 is a TMD with higher mobility (~50 cm^2/Vs) than organic semiconductors, large bandgap (~1.8 eV), high I_{ON}/I_{OFF} ratio (>10^6), strong current saturation, and GHz RF performance [1-3]. Recent studies have improved the cutoff frequencies of MoS2 RF FETs [4]. The common mechanical cleavage process of obtaining TMDs is not scalable for industrial purposes and, thus far, there have been few studies on chemical vapor deposited (CVD) MoS_2 RF applications. Here, we report state-of-the-art large area monolayer CVD MoS_2-based RF transistors [5,6] and switches. We employ an embedded gate structure to improve the RF characteristics of MoS_2 FETs. The experimental devices exhibit enhancement mode operation, I_{ON}/I_{OFF} ratio of 10^8, and the highest CVD MoS_2 transconductance of 70 µS/µm. Furthermore, we introduce a new application using a single atomic sheet of MoS_2 as a non-volatile RF switch. The switching performance and retention time was measured with a DC voltage bias. The RF performance of the device was measured up to 50 GHz and simulated with a lumped-element circuit model. Our results suggest that MoS_2 atomic sheets are promising for the design of low power RF applications.

II. CVD MoS_2 RF FETs

Fig. 1(a) is a schematic of the embedded gate MoS_2 RF FETs. Two embedded gate fingers were patterned on intrinsic Si/SiO_2. Then, electron beam lithography (EBL) and e-beam evaporation were used to define and deposit the embedded gate metal consisting of 2/23 nm Ti/Au. Various horizontal gate lengths were defined down to a minimum length of 100 nm.

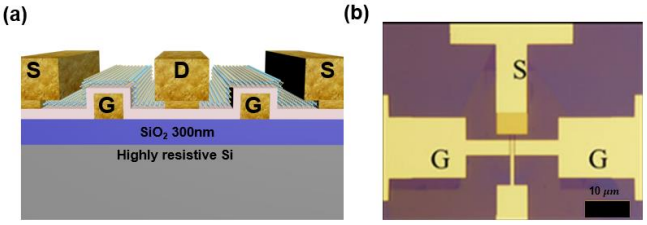

Figure 1. (a) Schematic of an embedded gate MoS_2 FET. (b) Optical image of a CVD MoS_2 device with ground-signal-ground (GSG) gate finger layout.

Atomic layer deposition (ALD) at 200°C was used to deposit 10 nm of Al_2O_3 as the gate dielectric. Large area monolayer CVD MoS_2 was transferred by poly(methyl methacrylate)-assisted wet transfer. Phosphoric acid was used to etch a via to connect the embedded gate fingers with the gate pad. The active MoS_2 channel was defined by Cl_2/O_2 plasma etching. A final EBL step patterned source and drain (S/D) contacts consisting of 2/70 nm Cr/Au. Fig. 1(b) shows the top-view image of the gate fingers.

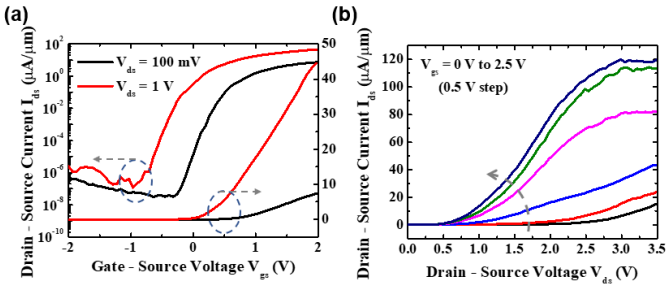

Figure. 2 (a) CVD-grown MoS_2 FET DC transfer curves, I_{ds}–V_{gs}, for a 150nm gate length device with an I_{ON}/I_{OFF} ratio of 10^8 at 100mV of drain bias. (b) Output curves, I_{ds}–V_{ds}, for the same device with current density of 120 µA/µm at a V_{ds} of 3.5 V. The device shows good current saturation beyond a V_{ds} of 3V.

A. MoS_2 FET DC characterization

Fig. 2(a) shows the I_{ds}–V_{gs} characteristics of an embedded gate MoS_2 FET with a gate length of 150 nm. The embedded gate structure was employed due to its superior gate modulation and cleaner MoS_2-dielectric interface with less fixed-charge and organic impurities. Subsequently, the threshold voltage, V_{th}, is positive and close to 0 V, in contrast to many top-gated

structures. The maximum field-effect mobility, μ_{FE}, is 21.2 cm^2/Vs. After transfer, the MoS_2 wraps conformally to the topology of the gate fingers. The electrostatic control is improved over top-gated devices because the electric field flux reaching the MoS_2 channel is increased at an equivalent gate voltage. We obtain a peak transconductance, gm, of 70 µS/µm at a V_{ds} = 2.5 V and an I_{ON}/I_{OFF} ratio of 10^8. Fig. 2(b) shows the I_{ds}–V_{ds} characteristics for the same device with a maximum current density of 120 µA/µm. There is good current saturation beyond a V_{ds} of 3 V, resulting in a drain conductance, g_{ds}, within 5 µS/µm in the current saturation region (3 to 3.5 V of V_{ds}).

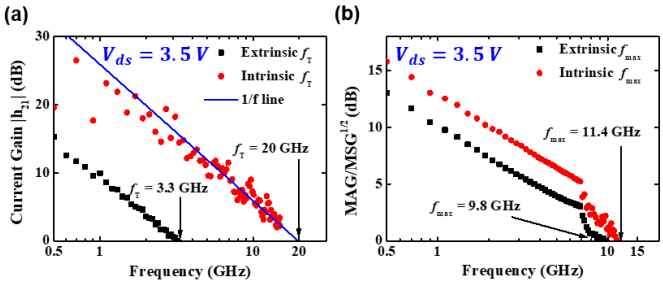

Figure. 3 (a) Short circuit current gain, $|h_{21}|$, versus frequency shows an extrinsic f_T of 3.3 GHz and an intrinsic f_T of 20 GHz at a V_{ds} of 3.5 V with a 150 nm gate length. (b) Maximum available power gain, $MAG/MSG^{1/2}$, versus frequency shows an extrinsic f_{max} of 9.8 GHz and an intrinsic f_{max} of 11.4 GHz.

B. MoS_2 FET RF characterization

The RF performance of CVD MoS_2 FETs were characterized from 0.1–15 GHz using a Keysight two-port vector network analyzer (PNA-E8361C). We employed the standard de-embedding method using OPEN and SHORT measurements on the same device to subtract the parasitic capacitances and resistances in the GSG layout. RF performance is determined by cutoff frequency (f_T), which is defined as the frequency at which current gain (h_{21}) becomes unity, while the maximum oscillating frequency f_{max} is defined as the frequency at which maximum available gain of the transistor drops to unity. Fig. 3(a) shows the short circuit current gain $|h_{21}|$ vs. frequency. Operating at V_{ds} = 3.5 V with L_g = 150 nm, we achieve an extrinsic f_T of 3.3 GHz and, after de-embedding, an intrinsic f_T of 20 GHz. Saturation velocity can be extracted from the f_T measurement in the high-field limit. The extracted V_{sat} for our device is 1.88×10^6 cm/s, the highest extracted v_{sat} for room temperature MoS_2 RF FETs, either exfoliated or CVD (Table I). Fig. 3(b) shows the maximum available power gain vs. frequency. Operating at the same DC bias, we measure an extrinsic f_{max} of 9.8 GHz and an intrinsic f_{max} of 11.4 GHz. We attribute the high f_{max} to good current saturation, leading to a small g_{ds} and a large output resistance, r_o. The different de-embedding result for f_T and f_{max} might be mostly due to different dominating factors. The dominating factors for the cut-off frequency are contact resistance and parasitic capacitance between gate and source/drain, and the dominating factor for the power gain is gate resistance. Note that the standard de-embedding process utilized in this work is to exclude effects of parasitic capacitance and inductance of the pad interconnect. The trend that f_T improves more than f_{max} has been reported in previous 2D material based RF transistor works [4].

TABLE I
COMPARISON OF MoS_2 RF TRANSISTOR PERFORMANCE

Feature\Device	[7]	[8]	[4]	[9]	This work
Configuration (active/substrate /structure)	Exf 3L/Si/ top gate	Exf 2-7nm/Si/ transferred gate	CVD 1L/Flex/ top gate	CVD 1L/Si/ top gate	CVD 1L/Si/ embedded gate
f_T ext/int (GHz)	6/25	-/42	2.7/5.6	2.8/6.7	3.3/20
f_{max} ext/int (GHz)	-/16	-/50	2.1/3.3	3.6/5.3	9.8/11.4
A_v ext/int(GHz)	-/45	-/-	-/-	3/11	4.6/19.5
L_g (nm)	70	68	500	300	150
V_d (V)	2.5	5	2	3.5	3.5
V_{sat} (x10^6 cm/s)	1.1	1.79	1.76	1.26	1.88

III. CVD MoS_2 RF SWITCH

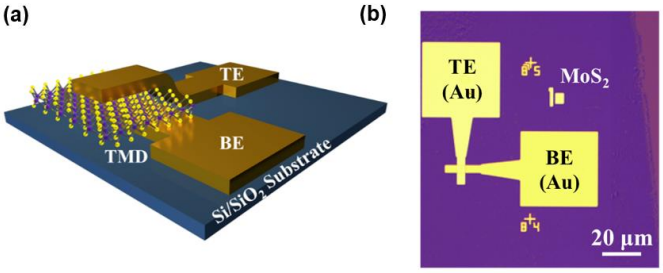

Figure 4. (a) Schematic illustration of vertical MIM structure of a MoS_2 switch. (b) Top-view optical image of a fabricated MoS_2 switch with Au electrodes.

Fig. 4(a) shows the schematic and image of a monolayer CVD MoS_2 atomic sheet switch. The device was fabricated on intrinsic Si/SiO_2 using EBL and e-beam metal evaporation. The switch stack consists 60 nm top and bottom gold (Au) electrodes, with 2 nm chromium (Cr) adhesion layers connecting the electrodes to the MoS_2 layer. Large area CVD and metal-organic CVD MoS_2 atomic sheets are transferred on to the bottom electrode patterned substrate using polydimenthylsiloxane-assisted pick-and-place transfer. The required DC bias for non-volatile resistive switching effect is applied through the same electrodes as the RF signals.

A. MoS_2 switch DC characterization

DC electrical measurements were performed on a MoS_2 RF switch with a DC voltage sweep. At a positive bias, the device was programmed to a low-resistance state (LRS) and a negative bias turns the device to a high-resistance state (HRS). Both the HRS and LRS (OFF/ON) were non-volatile. To protect the device from being damaged, we used a compliance current for a transition (SET) from HRS to LRS. Fig. 5(a) shows typical non-volatile resistive switching DC curves of a monolayer

MoS_2 device. This MoS_2 switch is non-volatile and consumes zero static power. Fig. 5(b) shows stable data retention over 4 hours under ambient conditions. The HRS and LRS retention current was measured at a small bias of 100 mV and showed 10^3 ON/OFF ratios.

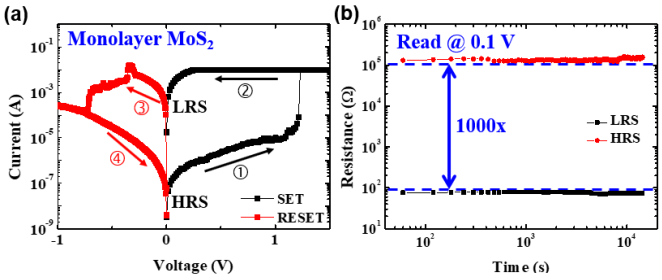

Figure 5. (a) Typical switching performance of the bipolar resistance switching behavior in a monolayer MoS2 RF switch with a lateral area of 0.5 × 1 μm2. (b) Retention time measurement of ON and OFF states at room temperature.

B. MoS_2 switch RF characterization

RF performance of our MoS_2 RF switch was measured up to 50 GHz using a Keysight two-port vector network analyzer (PNA-E8361C). Scattering parameters (S-parameters) were measured using -20 dBm input RF power. Fig. 6(a) shows our CVD MoS_2 atomic sheet RF switch with an acceptable insertion loss of ~0.5 dB and isolation of ~15 dB up to 50 GHz. We characterized the small-signal performance of the RF switch using a simple lumped-element equivalent circuit model. The switch cutoff frequencies ($f_c=1/2\,\pi\,R_{ON}C_{OFF}$) were calculated using ON-state resistance and OFF-state capacitance from the equivalent circuit model. The measured and simulated RF responses are in good agreement. The extracted ON-state resistance is ~5 Ω, the OFF-state capacitance is ~6.23 fF, and the cutoff frequency is ~5.1 THz. These parameters demonstrate comparable performance to that of solid-state, MEMS, and PC material based switches [10-12], with the added advantage of smaller size and frequency scalability by reducing area to achieve even higher frequencies without compromising insertion loss.

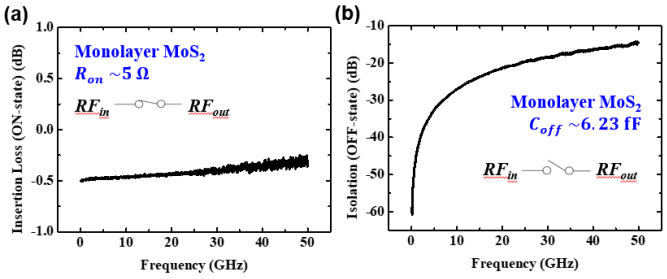

Figure 6. Measured RF response of a monolayer MoS_2 RF switch. (a) Representative insertion loss and isolation of RF switches based on 0.5 × 1 μm^2 monolayer MoS_2.

IV. Conclusion

In conclusion, we have successfully demonstrated CVD MoS_2 based RF FETs and RF switches. Our embedded gate MoS_2 RF transistors have shown relatively high f_T and f_{max}. We also demonstrate a RF switch using MoS_2 atomic sheets. These results suggest promising applications towards the design of future low power RF nanoelectronics systems using two-dimensional materials.

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