Comparative Simulation Study on MoS_2 FET and CMOS Transistor

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***Abstract*—MoS_2 FET and SOI/FinFET are simulated and compared to experimental results and the impact of gate scaling-down on the transistor performance is studied. Though MoS2 FET shows better suppression of the short channel effect, its on-current is still lower than that of sSOI/FinFET down to 10nm physical channel length due to the low saturation velocity of MoS_2. In addition, the improvement of mobility over 60cm^2/Vs has little benefit for the on-current.**

Keywords—MoS_2 FET; SOI; FinFET; On-current

I. Introduction

In recent technology nodes, much effort has been made to reach a higher on-current. Bulk structure is replaced by FinFET structure to maintain a high I_{ON}/I_{OFF} ratio, and thus a high I_{ON} per pitch[1][2]. High I_{ON} is achieved by such a structure at the price of an increased gate capacitance that suppresses the short channel effects, but lowers the cutoff frequency. A variety of the structural optimization is also adopted in SOI structures to achieve a better short channel performance, such as thinning-down of SOI body and buried oxide thickness[3][4]. These optimizations that lower the subthreshold swing(SS), and thus the threshold voltage, will in return improve the on-current.

Novel two-dimensional (2D) channel material, such as MoS_2, has attracted extensive interest due to its built-in advantages in suppressing the short channel effect[5][6]. In this paper, MoS_2 FET is studied using drift-diffusion simulation. Though 2D material with bandgap like MoS_2 demonstrates a better short channel behavior, it has been found that the on-current I_{ON} limited by its saturation velocity shows no improvement over sSOI(strained-SOI)/FinFET devices down to physical channel length of 10nm. In addition, increasing the mobility in such material has little improvement on the on-current, due to low saturation velocity [6].

II. Methods

A. 2D simulation for MoS2 FET

Fig. 1(a) shows the FET structure using MoS_2 as channel. Highly doped regions are assumed on both sides of the channel to ensure a low contact resistance. To avoid confusion, the physical gate length is defined as the distance between the edges of high-doped regions. The I_D-V_G curves based on the 2D drift-diffusion simulation and experiments[5] are shown and compared in Fig.1(b). The high S/D resistances caused by the underlapped gate in experiments are estimated by the current under the high gate voltage[5]. The equivalent oxide thickness(EOT) of SiO_2 for top gate is adopted to mimic the effect of the high-k material.

B. sSOI/FinFET simulation

Simulation using Synopsys Sentaurus is fitted to the current performance of sSOI/FinFET devices[1][2][3][9] and it is also adopted to estimate the performance under scaling-down. Fig.2 shows the comparison between the simulated and experimental I_D-V_G curve in 14/22nm nodes with physical gate length of 20/26nm for FinFET and 20/25nm for sSOI.

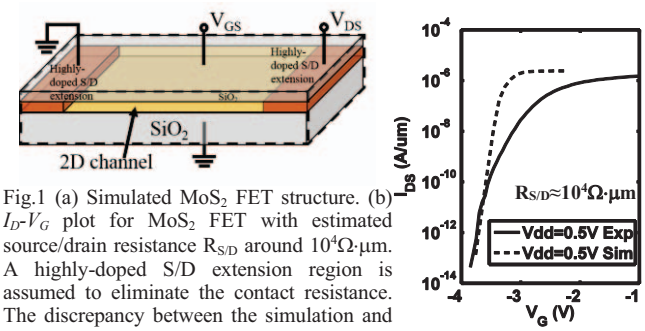

Fig.1 (a) Simulated MoS_2 FET structure. (b) I_D-V_G plot for MoS_2 FET with estimated source/drain resistance $R_{S/D}$ around 10^4Ω·μm. A highly-doped S/D extension region is assumed to eliminate the contact resistance. The discrepancy between the simulation and experiment data[5]due to the degradation of the subthreshold slope may result from the interface/surface defects between the high-*k* material and MoS_2.

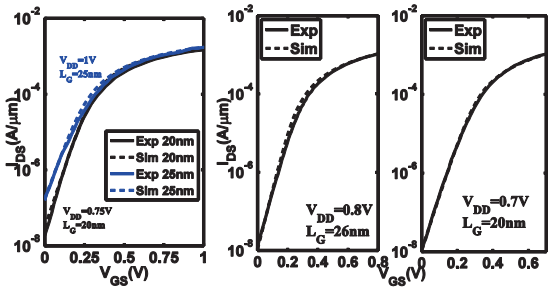

Fig.2 sSOI/FinFET simulation vs experiment. [1][2][3][9] The left figure shows the

By shrinking down the Si body thickness and physical channel length while maintaining all the other parameters, a "brutal-force" scaling down is assumed to predict the degradation limit of sSOI/FinFET performance when the physical channel length scales to 10nm.

TABLE I. Simulation Parameters

MoS_2	*Low-field mobility* μ_n	*Relative permittivity* ε_r	*Saturation velocity* v_{sat}
	60cm^2/V·s[7][a]	4.0[8]	0.28x10^{7}cm/s[6]
MoS_2 FET	*Top gate EOT* T_{ox}	*Back gate EOT* T_{box}	*S/D extension*
	1nm	15nm	10nm
10nm *Lg* FinFET	*Silicon body thickness* T_{Si}	All other parameters remain the same as 14nm FinFET node	
	5nm		
10nm *Lg* sSOI	*Silicon body thickness* T_{Si}	All other parameters remain the same as 14nm sSOI node	
	3.4nm[13]		

[a.] Except for the case when mobility is a variable

III. Results

The simulations of MoS_2 FET and FinFET structures are compared in the terms of their on-current, short channel behavior. The band diagram and electron concentration is plotted along the MoS_2 channel in Fig.3. Table 1 shows the parameters that are used in the simulation for MoS_2 FET and short channel sSOI/FinFET structure.

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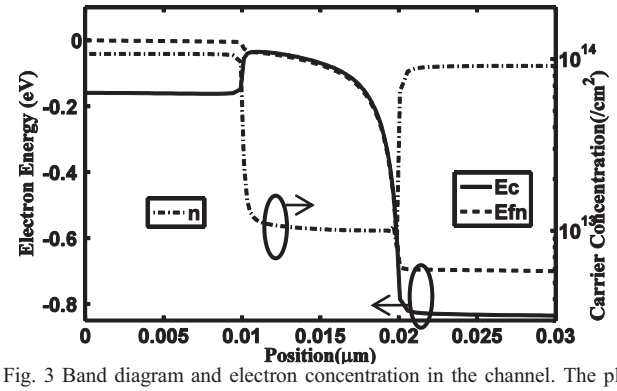

Fig. 3 Band diagram and electron concentration in the channel. The plot shows the band diagram and electron concentration in the MoS_2 channel under a bias of V_D=0.7V and V_G=0.5V,where the flat band voltage is assumed as V_{FB}=-E_g/2q.

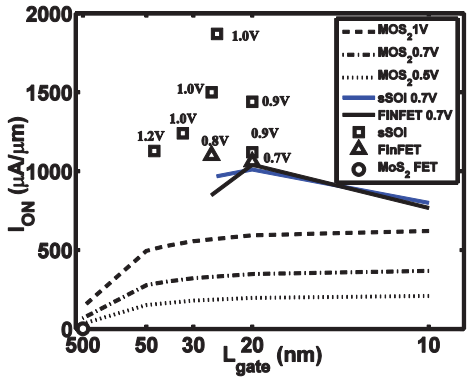

Fig. 4 On-current vs. gate length scaling. All the markers with V_{DD} on the side note the on-current for experiments, while all the lines show the simulated results. The dashed/dash-dotted/dotted line plot the on-current of MoS_2 FET using different supplied voltage V_{DD}=1/0.7/0.5V (I_{OFF}=10^{-7}A/μm). The black/blue solid line illustrates the on-currents I_{ON} for FinFET/sSOI with physical gate length L_G=26nm/20nm/10nm and L_G=25nm/20nm/10nm under V_{DD}=0.7V (I_{OFF}=10^{-8} A/μm for FinFET and 10^{-7}A/μm for sSOI). For L_G=10nm, the "brutal-force" scale down is assumed (as in Table 1). [1][2][3][4][5][9][10][11][12]

A. On-Current Comparison

By defining the off-current same as CMOS for high performance application in ITRS[13] (100nA/μm), the on-current I_{ON} can be found under different supply voltage V_{DD}. Fig. 4 demonstrates the trend for the on-current of MoS_2 FET while scaling down the channel length, compared with those of sSOI and FinFET. It can be easily observed in Fig.4 that the on-currents for MoS_2 FET are more than 50% lower than the one for sSOI/FinFET at V_{DD}=0.7V. The on-current for MoS_2 FET does not scale up as the channel length shrinks when L_G is less than 50nm since the low saturation velocity of MoS_2 limits the increase of the on-current.

B. Short Channel Effects

The drain-induced barrier lowering (DIBL) and subthreshold swing (SS) for L_G less than 50nm are shown in Fig.5 based on MoS_2 FET and sSOI/FinFET simulation, as well as the ones for industry sSOI and FinFET results. Compared with sSOI/FinFET simulation, MoS_2 FET demonstrates better short channel behavior as physical gate length scales down.

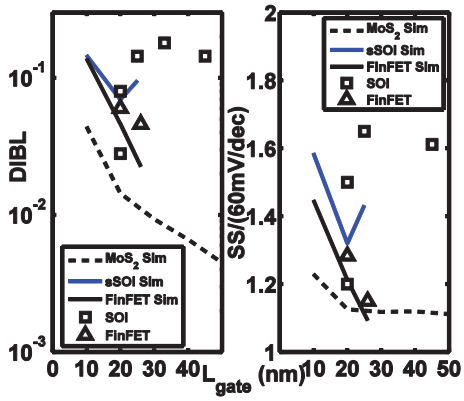

Fig. 5 DIBL/SS vs. gate length scaling. All the markers shows the experiment results for sSOI/FinFET, while blue/black solid line shows the SS and DIBL for simulated sSOI/FinFET and dashed line plots the ones for simulated MoS_2 device.

C. Mobility Improvement

The quality of the film has been a great concern for most 2D materials because the mobility may be compromised by the growth condition or defects. However, increasing mobility over 60cm^2/Vs in MoS_2 has little improvement on the on-current as shown in Fig.6.

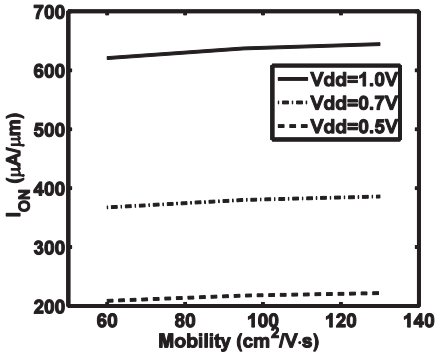

Fig. 6 On-current vs. mobility under different supply voltages V_{DD}. Less than 10% of the current increase is observed when the mobility varies from 60cm^2/Vs to 130 cm^2/Vs.

IV. Conclusion

MoS_2 FET, sSOI and FinFET are simulated and compared with experimental results and the impact of gate scaling-down on the transistor performance is studied. Though MoS_2 FET suppresses the short channel effect, its on-current is still lower than that of sSOI/FinFET down to 10nm physical channel length due to the low saturation velocity of MoS_2. In addition, the improvement of mobility over 60cm^2/Vs has little benefit for the on-current for MoS_2 FET.

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