bit_de_controle

	Instruction	do_jmp_abs	write_reg	do_sub	res_imm	arg2_imm
000 00	nop	0	0	0	0	0
000 01	ldi	0	0	0	1	0
001 00	not	0	1	0	0	0
001 01	lsr	0	1	0	0	0
001 10	or	0	1	0	0	0
001 11	and	0	1	0	0	0
010 00	addi	0	1	0	0	1
010 10	subi	0	1	1	0	1
010 01	add	0	1	0	0	0
010 11	sub	0	1	1	0	0
011 00	muli	0	1	0	0	0
011 01	mul	0	1	0	0	0
100 00	st	0	0	0	0	0
100 01	ld	0	1	0	0	0
100 10	out	0	0	0	0	0
100 11	in	0	1	0	0	0
101 00	jr	0	0	0	0	0
110 00	jeq	0	0	1	0	0
110 01	jle	0	0	1	0	0
110 10	jlt	0	0	1	0	0
110 11	jne	0	0	1	0	0
111 XX	jmp	1	0	0	0	0

	Instruction	src2_is_rd	in	out	and	or
000 00	nop	0	0	0	0	0
000 01	ldi	0	0	0	0	0
001 00	not	0	0	0	0	0
001 01	lsr	0	0	0	0	0
001 10	or	0	0	0	0	1
001 11	and	0	0	0	1	0
010 00	addi	0	0	0	0	0
010 10	subi	0	0	0	0	0
010 01	add	0	0	0	0	0
010 11	sub	0	0	0	0	0
011 00	muli	0	0	0	0	0
011 01	mul	0	0	0	0	0
100 00	st	1	0	0	0	0
100 01	ld	0	0	0	0	0
100 10	out	1	0	1	0	0
100 11	in	0	1	0	0	0
101 00	jr	1	0	0	0	0
110 00	jeq	1	0	0	0	0
110 01	jle	1	0	0	0	0
110 10	jlt	1	0	0	0	0
110 11	jne	1	0	0	0	0
111 XX	jmp	0	0	0	0	0

bit_de_controle

	Instruction	mem_to_reg	write_mem	do_jcc
000 00	nop	0	0	0
000 01	ldi	0	0	0
001 00	not	0	0	0
001 01	lsr	0	0	0
001 10	or	0	0	0
001 11	and	0	0	0
010 00	addi	0	0	0
010 10	subi	0	0	0
010 01	add	0	0	0
010 11	sub	0	0	0
011 00	muli	0	0	0
011 01	mul	0	0	0
100 00	st	0	1	0
100 01	ld	1	0	0
100 10	out	0	0	0
100 11	in	0	0	0
101 00	jr	0	0	0
110 00	jeq	0	0	zero
110 01	jle	0	0	sign=overflow
110 10	jlt	0	0	(sign=overflow) AND (NOT(zero))
110 11	jne	0	0	NOT(zero)
111 XX	jmp	0	0	0

	Instruction	not
000 00	nop	0
000 01	ldi	0
001 00	not	1
001 01	lsr	0
001 10	or	0
001 11	and	0
010 00	addi	0
010 10	subi	0
010 01	add	0
010 11	sub	0
011 00	muli	0
011 01	mul	0
100 00	st	0
100 01	ld	0
100 10	out	0
100 11	in	0
101 00	jr	0
110 00	jeq	0
110 01	jle	0
110 10	jlt	0
110 11	jne	0
111 XX	jmp	0