Unfortunately, students were required to sign a no disclosure that prevents us from using github for ECE 337 ASIC design. For this course we used SystemVerilog, however a small description of knowledge gained in this course can be found on the course webpage.

<https://engineering.purdue.edu/ECE/Academics/Undergraduates/UGO/CourseInfo/courseInfo?courseid=389.0&show=true&type=undergrad>