Department of Electrical and Computer Engineering
The University of Texas at Austin

EE 460N, Spring 2012
Mattan Erez, Instructor
Exam 1, February 27, 2012

Your signature is your promise that you have not cheated and will not cheat on this exam, nor will you help others to cheat on this exam.

Signature : SOLUTION

Printed Name : _____

Question:	1	2	Total
Points:	55	45	100
Score:			

Note: Please be sure that your answers to all questions **(and all supporting work that is required)** are contained **in the space (boxes) provided**. Anything outside the boxes will be ignored in grading. Use the back of each page as scratch paper, if needed.

Note: "I DON'T KNOW" is a valid answer that automatically gives you 10% of the maximum possible grade for that problem. Be sure to either erase, or cross-out everything else and write I DON'T KNOW in large, capital letters. Anything else will result in us grading what you have. **A blank answer does not get you the 10%.**

Note: Please put your name at the top of each page of the exam and remember that anything outside a box will be ignored!

Note: For all questions, unless otherwise stated, find the most efficient (time, resources) solution.

GOOD LUCK!

Name: _____

1. Memory and buses.

This question had a couple of issues that made it less than ideal. If you are looking at this as a practice exam, please note that there are more ranks than I had intended and that the address pattern was meant to be sequential (0, 2, 4, 6, ...).

You have an LC3b processor with the memory configuration shown below. The program you care about most, accesses memory with `LDW` instructions and the access pattern is to sequential memory addresses (e.g. (in bytes): 0, 2, 4, 8, ...).

Memory capacity:	64KB	Row activate:	5 bus cycles
Channel width:	16b	Row precharge:	4 bus cycles
Bus frequency:	1GHz	Column command:	1 bus cycle
Burst length:	1 bus beat	Number of ranks per DIMM:	4
Chip interface width:	8	Number of DIMMs per channel:	2
Number of channels:	2	Columns per row:	32
Number of banks per chip:	4		

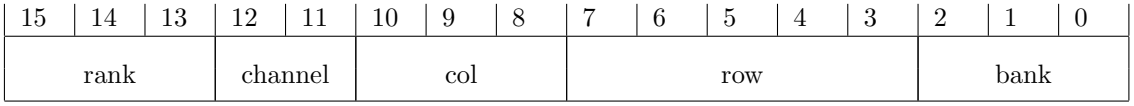
(a) (5 points) Should the bus use pending or split transactions? Why?

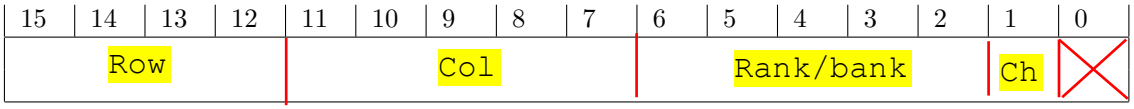
Split -- allows row commands to be sent while waiting for previous column commands to complete.

(b) (10 points) Fill in the table below describing more memory characteristics.

Ranks per channel	8
Total DRAM chips	32
Capacity per bank	512B
Rows per bank	16

(c) (13 points) How would you interleave the different components of the DRAM organization to maximize throughput? Show your answer by associating bits of the address with organization components. The example below is *incorrect and incomplete*, but shows what we mean by associating bits with components.





If interpreted as 0,2,4,8 then only 0 bit mattered + channel not in bit 1-9

Name: _____

(d) (7 points) What would be the throughput (in GB/s) assuming the described access pattern, your interleaving, and a memory controller that issues memory operations in order and does not overlap row and column commands. Assume that the processor is not the bottleneck and can generate requests as fast as memory can handle them – memory or the memory channels will bound the throughput. State any additional assumptions you make.

Just under 2GB/s for sequential
.24GB/s for 0,2,4,8

(e) (13 points) You are now told that you must use a new type of DRAM chip. In this DRAM chip every column command is automatically precharges the bank (removes the row from the row buffer and writes it back to the array). How would you now interleave the different components of the DRAM organization to maximize throughput?

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Unintentionally, same as Part C															

(f) (7 points) What would be the throughput (in GB/s) be now with your new interleaving?

2GB/s for sequential
.24GB/s for 0,2,4,8

Name: _____

2. ISA, Microcode, and Microarchitecture

(a) (3 points) What is the key advantage of the architecture–microarchitecture separation (20 words or fewer)? We accepted anything reasonable. Examples below.

Enables software and hardware to evolve independently.

(b) (3 points) What is an alternative to a microcoded microarchitecture (20 words or fewer)?

One alternative is dedicated hardware resources for each ISA instruction.

(c) (2 points) What is a major advantage of choosing a microcoded microarchitecture (20 words or fewer)?

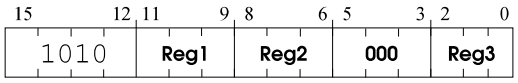
One major advantage is that it is very efficient in terms of number of gates needed for implementation.

(d) (2 points) What is a major disadvantage of choosing a microcoded microarchitecture (20 words or fewer)?

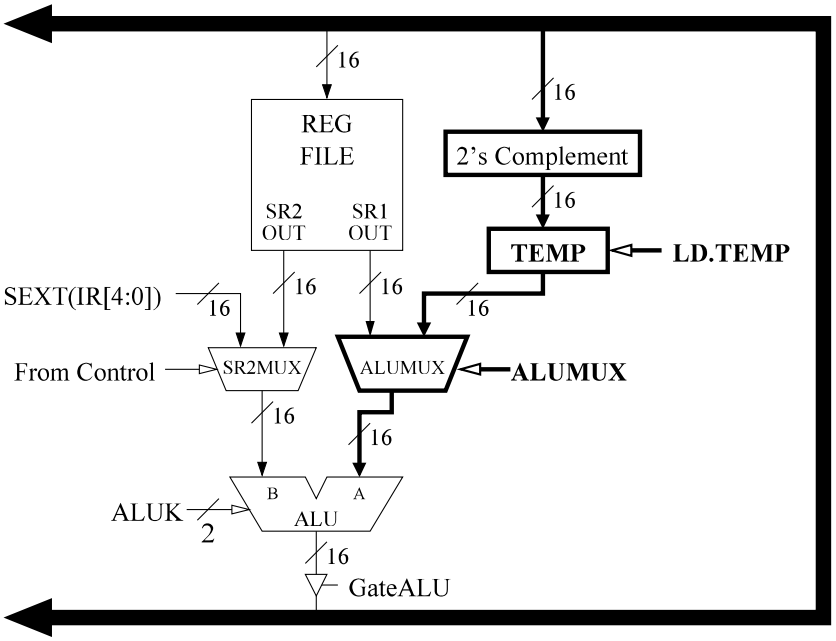
One disadvantage is potentially slower operation (many micro-ops per ISA instruction.

Name: _____

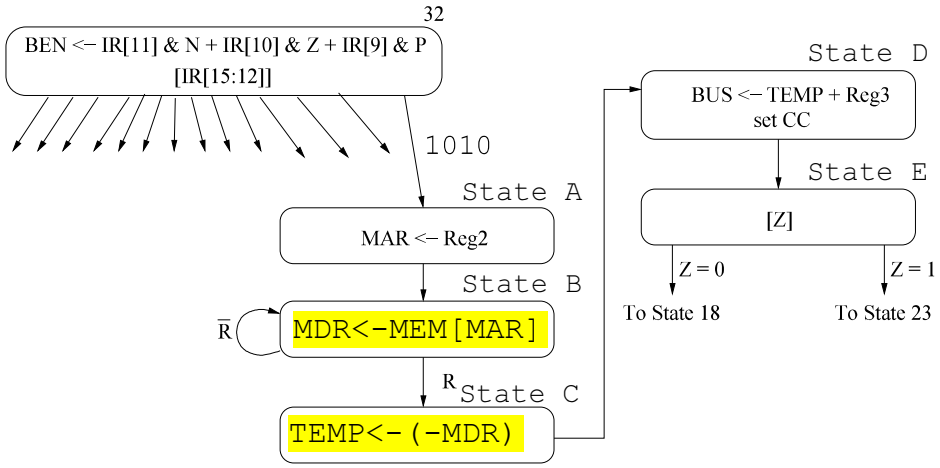
Now, consider adding the following new instruction to the LC3b. Your goal is to use the clues provided to determine the functionality of the instruction, as well as complete its implementation.



To accomplish this, we will need a small addition to the data path, shown below in boldface:



(e) (23 points) Some of the new microcode states, changes to existing microcode states are shown below and the control signal table is shown on the next page. Note that these are incomplete, but you have enough information to complete them. Please do so (on both pages, don't leave any empty boxes in either the table or state diagram).



State 23 is described in bottom right of the LC3b state machine included on Page 7. Also, remember that putting data on the bus is fine provided there is only one writer.

Name: _____

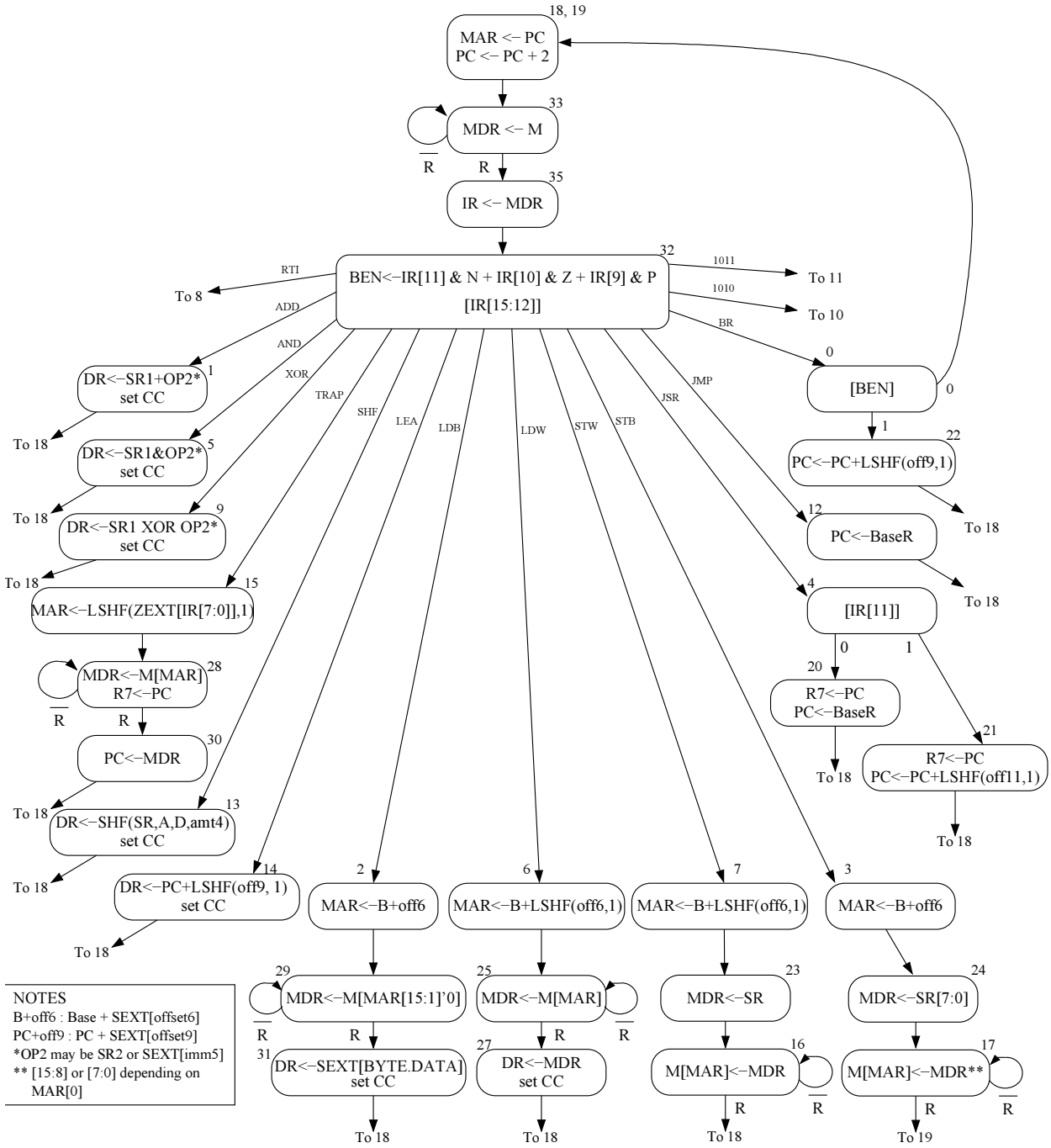
	LD.PC	LD.MAR	LD.MDR	LD.CC	LD.TEMP	GatePC	GateMDR	GateALU	SR1MUX[1]	SR1MUX[0]	ALUMUX	ALUK[1]	ALUK[0]	MIO.EN	R.W
State A	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**1**	**1**	**0**	**X**
State B	0	0	1	0	0	0	0	0	X	X	X	X	X	1	0
State C	0	0	0	0	1	0	1	0	X	X	X	X	X	0	X
State A	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**1**	**X**	**X**	**0**	**0**	**0**	**0**	**X**
State E	0	0	0	0	0	0	0	0	X	X	X	X	X	0	X

```
LD.MDR      0: load not enabled
            1: load enabled

LD.CC       0: load not enabled
            1: load enabled

LD.TEMP     0: load not enabled
            1: load enabled

GatePC      0: do not pass signal
            1: pass signal

GateMDR     0: do not pass signal
            1: pass signal

GateALU     0: do not pass signal
            1: pass signal

ALUK        00: ADD
            01: AND
            10: NOT
            11: Pass input A

MIO.EN      0: MIO not enabled
            1: MIO enabled

R.W         0: Read
            1: Write

ALUMUX      0: TEMP
            1: SR1OUT
```

(f) (12 points) What does this new instruction do (20 words or fewer)?

If MEM[Reg2] equals content of Reg3 then CC set to Z and content of Reg1 is stored to MEM[Reg2]. Otherwise, CC set to N or P and memory remains unchanged.

Name: _____


18, 19
MAR <– PC
PC <– PC + 2
33
MDR <– M
R
R
35
IR <– MDR
32
BEN<–IR[11] & N + IR[10] & Z + IR[9] & P
[IR[15:12]]
RTI
To 8
ADD
AND
XOR
TRAP
SHF
LEA
LDB
LDW
STW
STB
JSR
JMP
1011
To 11
1010
To 10
BR
0
[BEN]
0
1
22
PC<–PC+LSHF(off9,1)
To 18
12
PC<–BaseR
To 18
4
[IR[11]]
0
1
20
R7<–PC
PC<–BaseR
To 18
21
R7<–PC
PC<–PC+LSHF(off11,1)
To 18
1
DR<–SR1+OP2*
set CC
To 18
5
DR<–SR1&OP2*
set CC
To 18
9
DR<–SR1 XOR OP2*
set CC
To 18
15
MAR<–LSHF(ZEXT[IR[7:0]],1)
28
MDR<–M[MAR]
R7<–PC
R
R
30
PC<–MDR
To 18
13
DR<–SHF(SR,A,D,amt4)
set CC
To 18
14
DR<–PC+LSHF(off9, 1)
set CC
To 18
2
MAR<–B+off6
6
MAR<–B+LSHF(off6,1)
7
MAR<–B+LSHF(off6,1)
3
MAR<–B+off6
29
MDR<–M[MAR[15:1]'0]
R
R
31
DR<–SEXT[BYTE.DATA]
set CC
To 18
25
MDR<–M[MAR]
R
R
R
27
DR<–MDR
set CC
To 18
23
MDR<–SR
16
M[MAR]<–MDR
R
R
To 18
24
MDR<–SR[7:0]
17
M[MAR]<–MDR**
R
R
To 19
NOTES
B+off6 : Base + SEXT[offset6]
PC+off9 : PC + SEXT[offset9]
*OP2 may be SR2 or SEXT[imm5]
** [15:8] or [7:0] depending on
MAR[0]

Name: _____

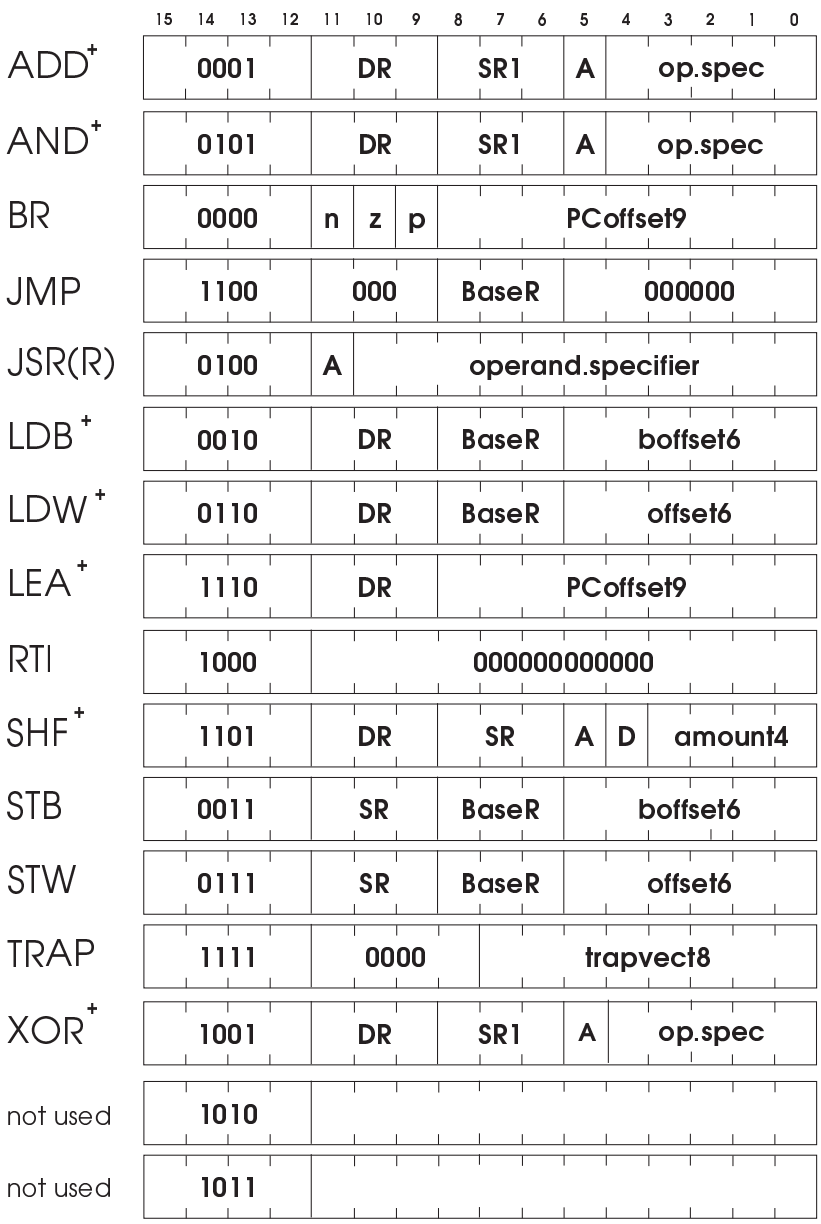


Figure A.2: Format of the instructions for the 16 LC-3b opcodes. NOTE: + indicates instructions that modify condition codes.