Matthew Randall

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Work Experience

R&D Hardware Engineering Intern June 2024 – September 2024
Keysight Technologies *Santa Clara, CA*

- Evaluated and compared the performance, efficiency, cost, and thermal impact of two 12V to 50V step-up circuits for prototype
- Characterized the stability and step response of two 12-50V step-up regulators by developing a switching load circuit
- Characterized the load requirements of a photo diode to help create a sufficient power supply rail
- Designed and tested a SPI module in verilog to facilitate communication between an ADC and CPU
- Developed a clock timing test setup for PCBs using differential probes, preserving the integrity of testing signals
- Wrote a Python script to read oscilloscope data, calculate clock signal delays, and generate plots for analysis

Supplemental Instructor December 2022 – Present
Learning Support Services, UC Santa Cruz

- Led interactive group sessions for 15-20 students improving student problem-solving skills and understanding of complex problems.
- Mentored over 100 students, building collaborative learning environments that contributed to significant improvements in academic performance while demonstrating strong organizational and leadership skills.

Relevant Projects

Cyclical RNA Rehydration Device | *Lead Electrical Engineer*

- Designed and implemented the power distribution system for an automated RNA rehydration device supporting professor David Deamer's origin of life research
- Designed and laid out a PCB to support power regulation and microcontroller interfaces within a sealed electronics enclosure
- Defined system load requirements and created a power budget that informed power supply architecture
- Selected and implemented appropriate voltage regulation techniques to ensure stable and sufficient power delivery to each electrical subsystem

Leaky Integrate & Fire Neural Network on Chip | *Verilog*

- Designed a hardware-based LIF neural network with three input neurons and one output neuron, implementing brain inspired neural network.
- Developed weighted spike summation at the output neuron, enabling correct aggregation of input neuron activity to determine final spiking behavior.

Full-Duplex UART Device Driver for Microchip PIC32 | *C Programming*

- Developed a device driver that enabled full-duplex UART communication by implementing circular buffers and interrupts, enhancing data transmission reliability.
- Designed an application layer to assemble received characters into packets for command execution, which improved system responsiveness and user interaction.
- Engineered response packet generation within the application layer for efficient feedback over UART, facilitating seamless device-to-user communication.

Education

University of California Santa Cruz September 2021 – June 2025
Bachelor of Science in Electrical Engineering

- GPA: 3.96 / 4.0
- Relevant Coursework: Power Electronics, DSP, High-Speed Low Power IC design, High Speed Digital Design, Digital Logic Design, Electromagnetic Fields and Waves, Communication Systems, Feedback Control Systems

Relevant Skills

Technical Skills:Proficient in economic dispatch for power industry, Oscilloscopes for various precision measurements, Spectrum analyzer, Altuim Designer for PCB layout, Embedded System Design, Soldering
Computer Languages: C, Python MATLAB, Verilog, PSpice, VS code, Microsoft apps
Soft Skills: CRLA certified, Leadership experience, Problem-solving abilities, Strong communicator, Attention to detail

Additional Experience & Interests

- 5 years in customer service
- UCSC Dean's List
- Tau Beta Pi: Engineering Honors Society
- Interested in business side of engineering companies
- San Diego Food Bank Volunteer (2020-2023)
- Cabrillo Hospice Volunteer (2017-2023)
- Hobbies: Soccer, Surfing, Snowboarding, Basketball