A Stable 2-Port SRAM Cell Design Against Simultaneously Read/Write-Disturbed Accesses

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***Abstract*—A 2-port SRAM cell has to guarantee stability against simultaneously read and write (R/W)-disturbed accesses while keeping cell current (Icell). We verified that it was difficult to provide the stability without any decrease in Icell and any increase in the cell-area penalty only by using the previously proposed techniques for a 1-port cell, and have proposed a new cell biasing technique that controlled the level of the cell VSS (VSSM) with a dual-Vdd and a reduced write-bit-line (WBL) precharge scheme for an 8-transistor (8T) 2-port cell to address the above issue.**

In this paper, a further consideration was newly demonstrated about the stability for a 2-port SRAM under the random fluctuation of the threshold-voltage (Vth) in 65-nm CMOS technology. The stability with the proposed biasing was compared with that of the conventional cell-Vdd (VDDM) control for write assist [5], [6]. The results under 4-σ random-Vth fluctuation verified that the minimum Icell at a simultaneously R/W-disturbed cell increased by 2.4 times at Vdd $= 0.9$ V while improving the write margin (WRTM). The cell size based on the same Icell was reduced by 20%. The minimum static noise margin (SNM) was also improved by 44%. Each stability also had the tolerance against 6-σ random-Vth fluctuation. Furthermore, we have challenged to apply the proposed cell biasing to a 7-transistor (7T) 2-port cell design for area saving with a unique write-assist scheme. The cell size was reduced by 26% with the 7T cell compared with that of the conventional 8T cell.

This proposed cell biasing satisfied all the requirements of 2-port SRAM operation while improving stability and saving cell size.

***Index Terms*—Cell-current, embedded SRAM, memory cell, stability, 2-port.**

I. Introduction

MANY discussions have been held about the stability for an SRAM cell in recent years [3]–[8] against the reduction in the cell-operating margin due to the device fluctuation with scaling after 65-nm technology node. The useful assist techniques were reported so far to improve the cell-operating margins, such as the new cell topology [3], [4] and the cell-bias control [5]–[8]. However, those discussions were mainly based on the assist technique for a 1-port SRAM cell which is independently read or write accessed at a time.

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As for a 2-port SRAM which is widely used for an interface between the macro-blocks in SoC, a simultaneous R/W access has to be guaranteed with keeping enough Icell even though it is accessed in a same column. This guarantee obligation makes it much more difficult for a 2-port cell design compared with that of a 1-port cell to realize a simultaneous static noise margin (SNM), WRTM and Icell.

We verified that the conventional operating-margin assist techniques proposed so far for 1-port SRAM have not satisfied a 2-port SRAM operation simultaneously as shown in Table I [1], [2]. And we have proposed a new cell-biasing scheme which controlled VSSM for the write assist with a dual Vdd and a reduced write-bit line (WBL) precharge scheme to enhance SNM. This proposed biasing scheme met all the requirements for a 2-port SRAM operation without any decrease in Icell.

In this paper, a further consideration was newly demonstrated about the stability for a 2-port SRAM under the random fluctuation of Vth in 65-nm CMOS technology. The cell-operating margins under 4-σ random-Vth fluctuation that corresponds to a 32-Kbit memory capacitance were verified. And their tolerance against 6-σ random-Vth fluctuation was also estimated. Moreover, we have challenged to apply the proposed biasing to a 7T 2-port cell design for area saving with a unique write-assist scheme. The proposed biasing scheme was implemented in a 32-Kbit 2-port SRAM with a 65-nm LSTP CMOS, and it demonstrated that: 1) the minimum Icell at a simultaneously R/W-disturbed cell was increased by 2.4 times while improving WRTM, and thereby the cell size based on the same Icell was reduced by 20%, 2) the minimum SNM at a half-selected cell was improved by 44%, and 3) the proposed 7T 2-port cell saved the cell size by 26% without any decrease in cell current, each compared with the conventional VDDM control technique [5], [6] under 4-σ random-Vth fluctuation at Vdd $= 0.9$ V. Each operating margin also had the tolerance against the 6-σ random-Vth fluctuation.

This paper is organized as follows. Following the discussions on the requirements for the 2-port operation, the proposed cell-terminal biasing scheme for 8T 2-port cell and the simulated results are described in Section II. Another area-saving 7T 2-port cell design was demonstrated in Section III. After showing the implementation results of a 32-Kbit SRAM in Section IV, the conclusions were given in Section V.

II. Cell-Biasing Scheme for 2-Port SRAM

A. Issues in Conventional Cell-Stability Assist

The several memory-cell topologies [3], [4] and the cell-terminal bias controls [5]–[8] for a 1-port SRAM have been

TABLE I
REQUIREMENTS FOR A 2-PORT OPERATION AND THE TECHNIQUES FOR CELL-MARGIN IMPROVEMENT

		Requirements for 2-port operation				
		WRTM	SNM	Cell current	Area penalty	Bit-write mask
Previous techniques	**Conv. 2-port [9]**	NG	NG	OK	OK	-
	Read-port isolated 8T cell [3]	OK	NG	OK	-	-
	Divided word-line [10]	OK	OK	OK	NG	NG
	VDDM control for write-assist [5,6]	OK	NG	NG	-	-
	Suppressed WL [7,8]	NG	OK	NG	-	-
	This Work [1,2]	OK	OK	OK	OK	OK

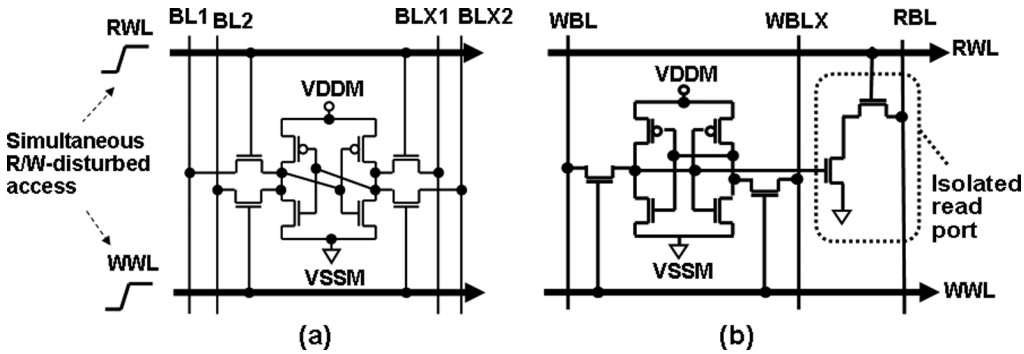


Fig. 1. (a) Conventional 2-port cell [9]. (b) 8T cell with isolated read port [3].

proposed so far to improve the cell-stability. However, these techniques improve the stability only within the limited conditions and cannot meet all the requirements for 2-port operation simultaneously as shown in Table I.

The conventional 2-port cell [9] can be designed to keep either one of SNM or WRTM by refining the beta ratio (access/drive-Tr drivability ratio) in the same way as a 1-port cell [Fig. 1(a)]. However, the 2-port SRAM cell is simultaneously disturbed by a read-word line (RWL) and a write-word line (WWL) even though it has the same stability issue in it as a 1-port cell by including a cross-coupled latch and the access transistors. Therefore, the simultaneous maintenance of SNM and WRTM become hard for the conventional 2-port cell with scaling.

An 8T cell with an isolated read-port [3] has been widely studied as a candidate of the next 1-port cell because it can avoid the RWL-disturbance to the cross-coupled latch and keeps SNM in a read operation [Fig. 1(b)]. However, it unfortunately can not eliminate the undesirable decrease in SNM in a half-selected cell (a WWL-disturbed cell in an unselected column) during a write operation.

A divided-WL configuration may solve this issue [10] by eliminating the any disturbed accesses in the unselected column. However, it causes intolerable area penalty for SRAMs in SoC. And even if using the divided WL access, it still does not work well at a bit-write mask operation because the same issue of the half-selected cell before dividing WL still remains in the write-masked column (Fig. 2).

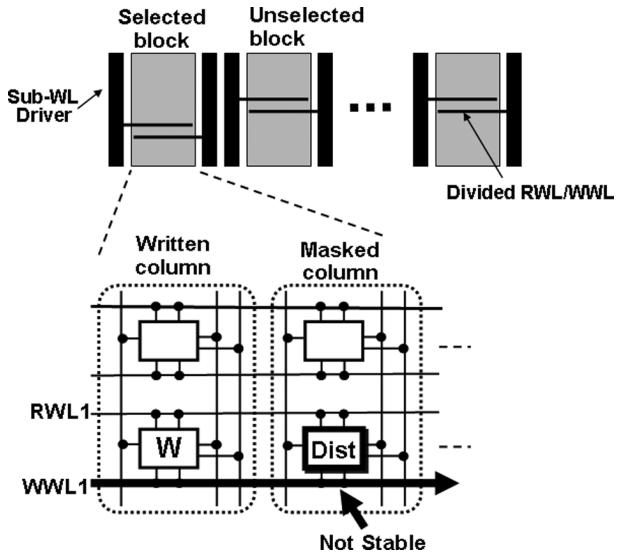


Fig. 2. Unstable cell in the bit-write-masked column disturbed by divided WL [10].

A suppressed-WL level below VDDM level can improve SNM in the half-selected cell [7], [8], while it includes the conflicted problem of decreasing WRTM and Icell.

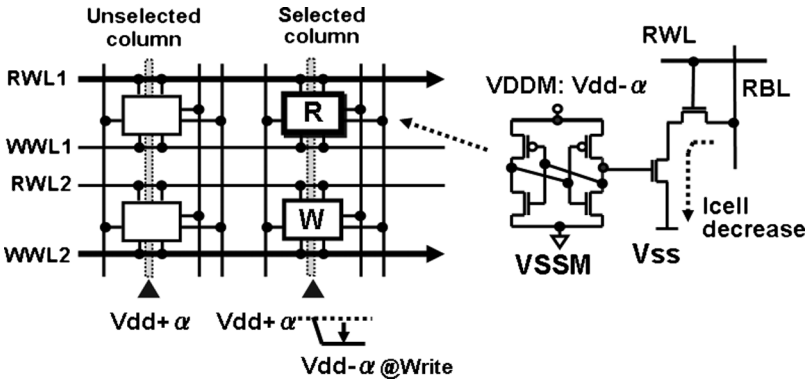


Fig. 3. Cell-current reduction issue of conventional column-based Vdd-control [5], [6] for 2-port SRAM at simultaneous R/W disturbed access in the same column.

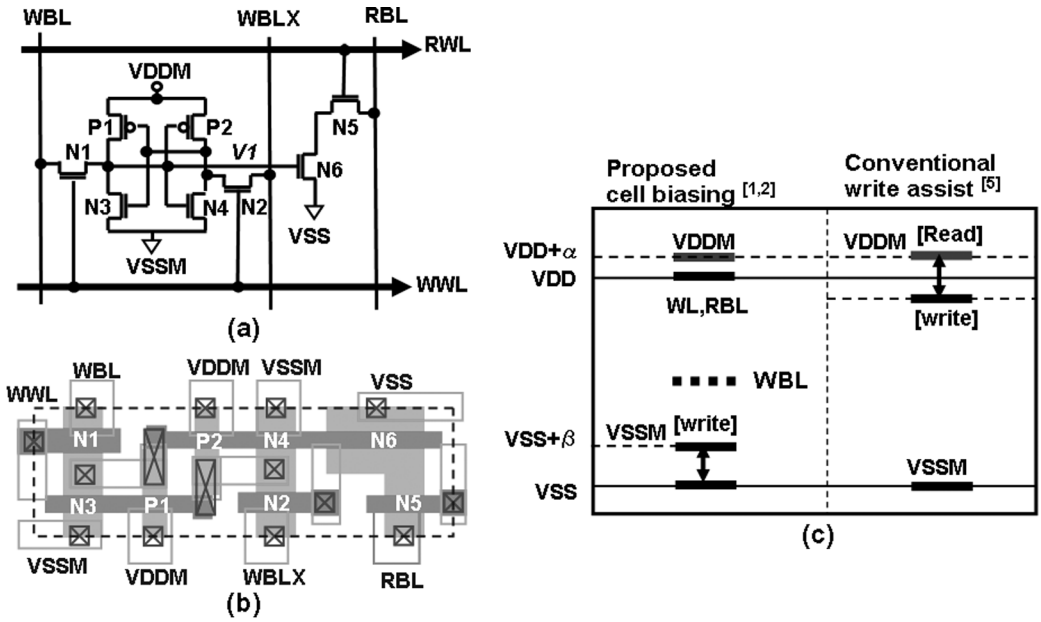


Fig. 4. Proposed 2-port cell biasing: (a) cell schematic diagram, (b) layout, and (c) its biasing.

As mentioned above, the row-direction WWL-disturb causes the unstable half-selected cells in the unselected column. On the other hand, the column-based VDDM control for WRTM-assist was also reported so far [5], [6]. This technique is useful for a 1-port cell which is independently read or write accessed. However, we found that it causes the cell-current degradation at a read cell in the simultaneously write accessed column by the reduced level of VDDM (VDDM $=$ Vdd $+ \alpha$ to Vdd $- \alpha$) in the 2-port SRAM as shown in Fig. 3.

B. Cell-Biasing Scheme With 8T Cell

To meet all the requirements for a 2-port SRAM cell even in a simultaneous read and write access, a new cell-biasing scheme has been proposed [1], [2]. The proposed biasing was applied to an 8T cell with an isolated read-port [3]. This 8T cell can operates as a 2-port (1-read and 1-write: 1R/1W) cell, and is widely used for an interface between macro-blocks in a cost-oriented SoC such as the consumer use. This is because the 1R/1W cell [Fig. 1(b)] can save the peripheral-circuit area of SRAM module compared with the 2R/2W cell [Fig. 1(a)] while keeping a simultaneous read and write access.

Figs. 4(a)–(c) show the cell schematic diagram, layout, and the proposed biasing condition, respectively. The source of NMOS N3 and N4 (VSSM) are separated from that of NMOS N6 (VSS). VSSM is routed along the bit lines in each column and is driven by the divided-resistance driver in each column as shown in Fig. 5(a). This divided-resistance driver consists of an NMOS-NMOS driver and a PMOS-NMOS driver. The former mitigates the VSSM-level variation caused by the device variation, and the latter suppresses the Vdd-dependence of VSSM level.

This proposed biasing scheme improved the operating margins as follows: 1) VSSM is boosted from Vss to Vss $+ \beta$ dynamically at a write-selected column to raise the switching level of a storage node. The level of β was set so as to write at low voltage (Vdd $= 0.9$ V), and not to cause a RBL misread at high voltage (Vdd $= 1.32$ V). 2) The stable level of VDDM (Vdd$+\alpha$) which is slightly higher than WWL-level (Vdd) in the whole cell array. 3) WBL-precharge level is lower than Vdd to suppress the current flow from WBL to the "low" storage node

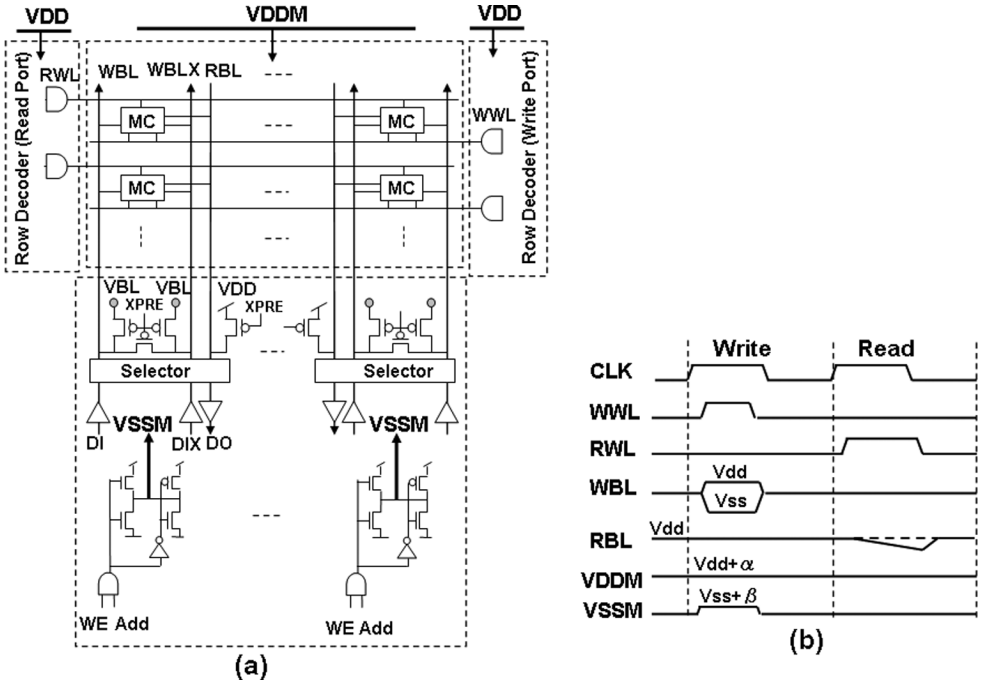


Fig. 5. (a) Schematic diagram of the peripheral circuit and (b) its timing diagram.

in the cell. 4) Read-BL (RBL) is precharged to Vdd to keep the cell current. 5) The divided-WL configuration was not used to avoid the area penalty even for the bit-write-mask operation.

The biasing 1) and 4) improved WRTM without reducing Icell even in a simultaneous R/W-disturbed access in a same column because a write operation is not executed without suppressing VDDM like the conventional write-assist technique, so the gate-level of read drive Tr (N6) is not reduced. On the contrary, the cell current can be increased by the boosted level of VDDM [the biasing 2)]. The gate-source voltage (Vgs) of the data-latch PMOS and NMOS at a write selected column is $(\mathrm{Vdd}+\alpha)-(\mathrm{Vss}+\beta)=(\mathrm{Vdd\text{-}Vss})-(\beta-\alpha)$ with the proposed biasing while that of the conventional SRAM is (Vdd-Vss). So the writability at a write selected column of the proposed SRAM increased with decreasing the drivability of the data-latch transistor by $(\beta-\alpha)$ compared with that of the conventional one. The biasing 2) and 3) enhanced SNM at the half-selected cell. Then the area penalty caused by the sub-WL driver for divided-WL can be avoided with the configuration 5).

C. Cell Margins at Simultaneous R/W Access

To make clear the effectiveness of the proposed biasing scheme, the cell stability was simulated compared with the conventional column-based VDDM control, with 65-nm LSTP CMOS technology assuming to apply to a 32-Kbit module. Each cell stability shown below was simulated under 4-σ random-Vt fluctuation (corresponds to 32-Kbit memory capacitance) at the worst corner of 3-σ global-Vth fluctuation.

Fig. 6 shows the comparison of the 4-σ random distribution of WRTM defined as WBL level at a cell-storage-data flip between the proposed biasing and the conventional one at $\mathrm{Vdd}=0.9\,\mathrm{V}$, $-40\,^{\circ}\mathrm{C}$ and NMOS-slow/PMOS-fast global device condition (the worst condition for write operation). As the aim of this

	μ	μ-4σ.
Proposed	0.193	0.068
Conv.	0.113	-0.022

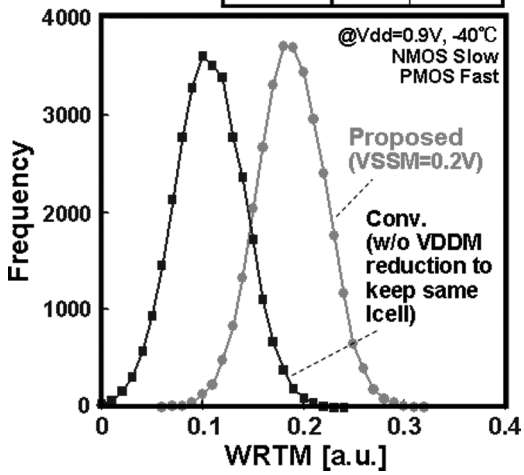


Fig. 6. Distribution of WBL level at storage-data flip (WRTM) for the same cell current.

work is improving WRTM with keeping the Icell at a simultaneous R/W access in a same column, WRTM was compared under the same VDDM bias condition $(\mathrm{VDDM}=\mathrm{Vdd}+0.1\,\mathrm{V})$ for the same Icell. The minimum WRTM of the proposed VSSM control was improved by 0.9 points compared with that of the conventional one, and it had the 6.2-σ margin from mean to the point of WRTM $=0$. Thus, the proposed biasing can increase WRTM by raising the switching level of the memory cell without reducing Icell.

The main concern of this work is keeping Icell at a read cell even in a simultaneously write-access operation in a same

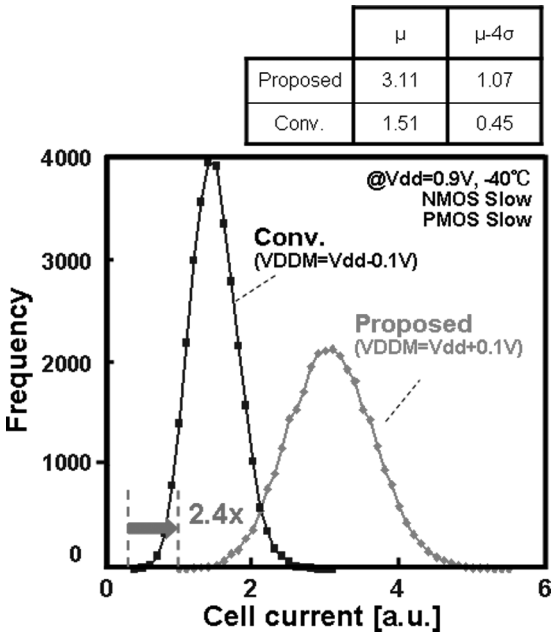


Fig. 7. Distribution of cell current at read cell in simultaneously write accessed column.

column. Icell at a simultaneously R/W-accessed column was compared with the conventional VDDM control in Fig. 7 at Vdd $= 0.9$ V, -40 °C, and NMOS-slow/PMOS-slow global device condition. Icell was not degraded like conventional control, and the minimum Icell was improved by 2.4 times with the higher level of VDDM that was applied to the gate of the read-drive Tr [N6 in Fig. 4(a)]. And it had 6.1-σ margin from mean to the point of Icell $= 0$. This demonstrated that the proposed VSSM control was the effective way to improve WRTM and Icell simultaneously for 2-port operation.

Although Icell for "high"-data storage was increased, the undesirable increase in the cell current for "low"-data storage (the storage node V1 in Fig. 4(a) is "low") caused by the boosted VSSM should be considered not to cause a misread. The distribution of correlation between Icell of the proposed biasing and Vth of NMOS N6 at high Vdd $= 1.32$ V (10% higher than typical Vdd), 125 °C and NMOS-fast/PMOS-fast global device condition is shown in Fig. 8. The distribution is compared between V1 = VDDM and VSSM (the cell storage node is "high" and "low"). Icell for "low" increases as Vth of NMOS N6 reduces. However, the minimum Icell for "high" was still 45 times larger than the maximum Icell for "low".

Then, to make clear the proposed VSSM control does not cause misread, RBL-discharge time was compared. Fig. 9 shows the distribution of the RBL-discharge time from VDD to half-VDD (the sensing level of RBL) under the same condition in Fig. 8. The shortest RBL length in module-compile of 16 row is demonstrated to show the worst case for the selected cells which hold VDDM ("high") and VSSM ("low") at the storage node V1. It can be seen that the clearance of RBL-discharge time between the slowest bit of Icell for "high" and the fastest bit of Icell for "low" is 904 ps, so enough timing margin after Icell for "high" discharge RBL remains to latch the data exactly.

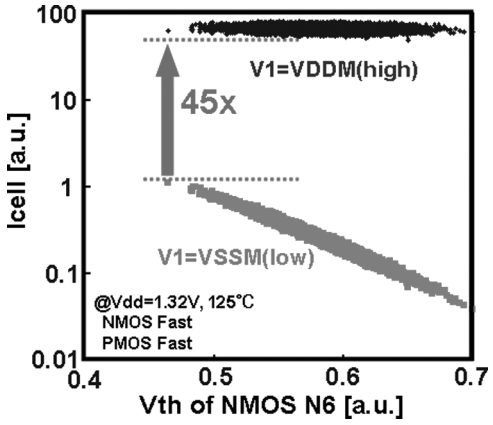


Fig. 8. Distribution of correlation between the cell current of proposed biasing and Vth of read-drive Tr N6.

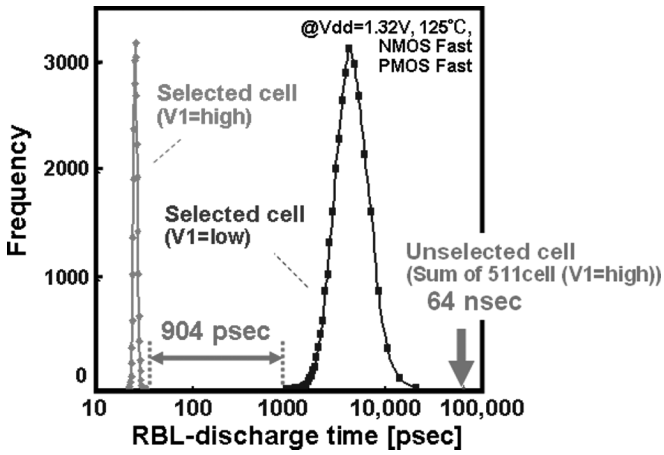


Fig. 9. Comparison of distribution of RBL-discharge time depending on storage data level. (16 cell/RBL for a selected cell, and 511 cell/RBL for unselected cells.)

Furthermore, the RBL-discharge time with the unselected cells is also shown in Fig. 9 because the boosted VDDM level applied to the gate of NMOS N6 increased the off leakage. Since the maximum number of cells per RBL is 512 in our module-compile, the RBL-discharge time with the sum of 511 unselected cells are demonstrated. The total off leakage was calculated assuming that all the unselected cells hold "high" data to show the worst RBL leakage condition, and the random leakage variation was averaged because each leakage offset was cancelled. The discharge time with 511 unselected cells was 64 ns which was enough slower than the Icell for "low" of the selected cell, so the boosted VDDM does not cause RBL misread.

As the proposed biasing can improve Icell compared with the conventional VDDM control biasing, the cell size can be reduced while keeping the same Icell by reducing the width of the read-drive Tr [N6 in the cell layout in Fig. 4(b)]. Assuming that the required minimum Icell $= 4.5$ μA at Vdd $= 0.9$ V under 4-σ random-Vt fluctuation, the cell size based on the same cell current can be reduced by 20% compared with the conventional VDDM control as shown in Fig. 10.

SNM at a half-selected cell was also improved with the proposed reduced WBL-precharge biasing. The minimum SNM

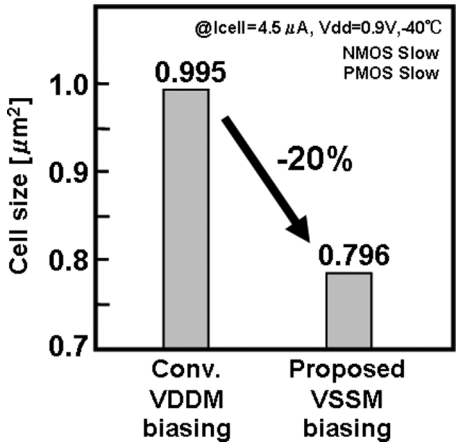


Fig. 10. Estimated reduction in cell size to realize the same cell current.

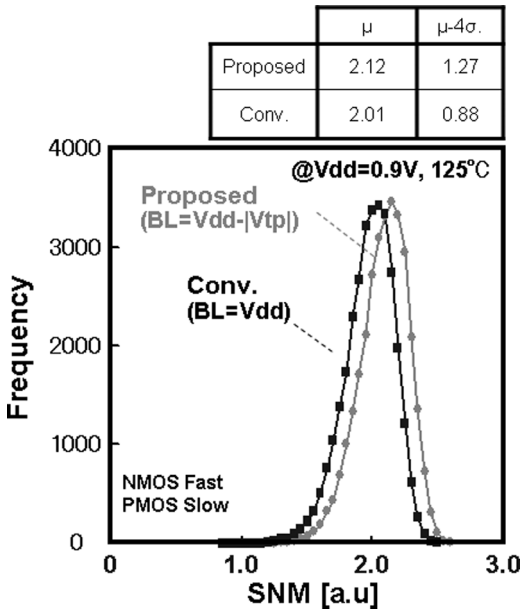


Fig. 11. Distribution of SNM at half-selected (WWL-disturbed) cell.

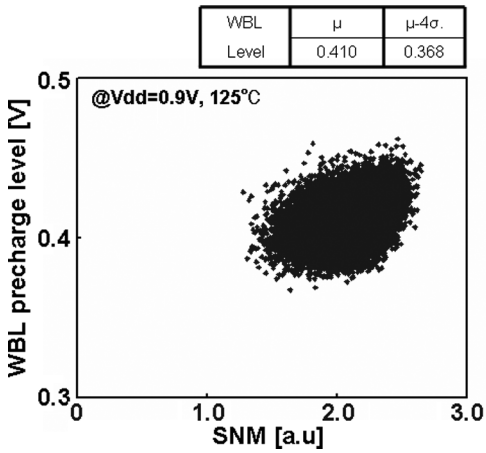


Fig. 12. Distribution of correlation between WBL precharge level versus SNM at half-selected cell.

at a half-selected cell was improved by 44% compared with the conventional biasing under 4-σ random-Vth fluctuation at Vdd = 0.9, 125 °C and NMOS-fast/PMOS-slow global device condition as shown in Fig. 11. It also can be seen that the enough clearance against the 6-σ random-Vth fluctuation was obtained. This is because the current flow from WBL to low-level storage node is suppressed by the lower precharge level of WBL at VDD − |Vthp|, where Vthp is Vth of PMOS, compared with the conventional VDD-level precharge. The distribution of correlation between WBL-precharge level and SNM at a half-selected cell at the same condition is shown in Fig. 12. The minimum WBL-precharge level was 0.368 V. It can be seen that enough SNM was kept with this low WBL-precharge level.

III. Cell Area Saving

A. 7Tansistor Cell

We have also challenged to apply the proposed cell-terminal biasing scheme to a 7T cell as shown in Fig. 13 to save the cell area. To achieve smaller 2-port cell, the write-access Tr N2 in the 8T cell [Fig. 4(b)] was removed and the single WBL is connected with the single write-access Tr N1 in 7T cell. Since the gate separation between the N2 and N5 in 8T cell is not necessary, the width of the read-access Tr N5 can be enlarged. Therefore, the Icell of the 7T cell can be increased while keeping the same cell size, or the lateral cell size can be reduced while keeping the same cell current compared with the 8T cell.

A part of the proposed cell-terminal biasing for 8T cell was also applied to the 7T cell, that is: 1) VDDM for the whole cell array which is higher than Vdd for logic, and 2) the reduced WBL-precharge level which is lower than Vdd to improve SNM.

The main concern for the stable operation of this 7T cell is how to write a high-data into the cell. As WBL is not differential, WWL is required to boost to assist at a high-data write operation. However, this causes the reduction in SNM at a half-selected cell in the unselected column. To address this issue and suppress the WWL-boost level for SNM, the following high-data write-assist techniques were additionally proposed.

B. High-Data Write Assist Scheme

A high-data-write operation for the 7T cell was assisted with the following two techniques: 1) a differential VSSM (Diff-VSSM) biasing, and 2) a temperature-dependent cell biasing.

As for a Diff-VSSM biasing, VSSM is separated to two nodes (VSSM1 and VSSM2) as shown in the schematic diagram in Fig. 14(a). And those VSSM lines are boosted differentially depending on the input data. VSSM1 is boosted at a write access for a high data on WBL, and VSSM2 is inversely boosted for a low-data-write access [Fig. 14(b)]. A low-data on the storage node V1 is assisted to flip because the drivability of the data-latch transistors [a drive-Tr (N3) and a load-Tr (P2)] is reduced by boosting VSSM1 at a high-data-write access.

While WRTM can be increased with Diff-VSSM biasing, this biasing technique causes the undesirable reduction in SNM at an unselected cell in a write-selected column because the offset biasing between VSSM1 and VSSM2 causes the asymmetric SNM characteristics which affects the data retention. To make clear the SNM reduction and how balance the operating margins, Figs. 15(a) and (b) show the position of the disturbed cell

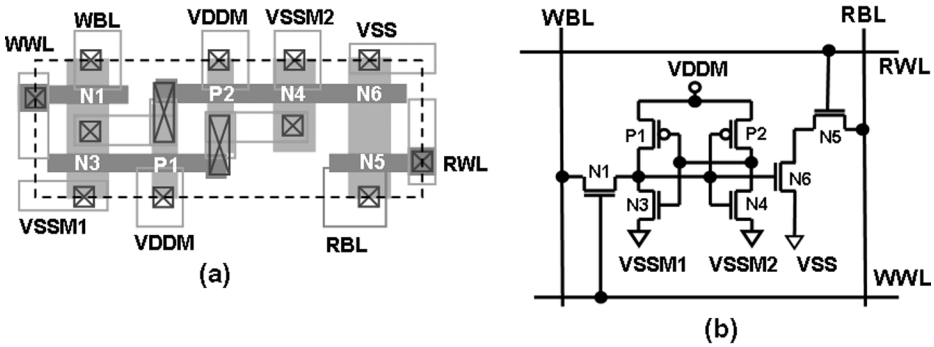


Fig. 13. Proposed area-saving 7T cell. (a) Cell layout and (b) its schematic diagram.

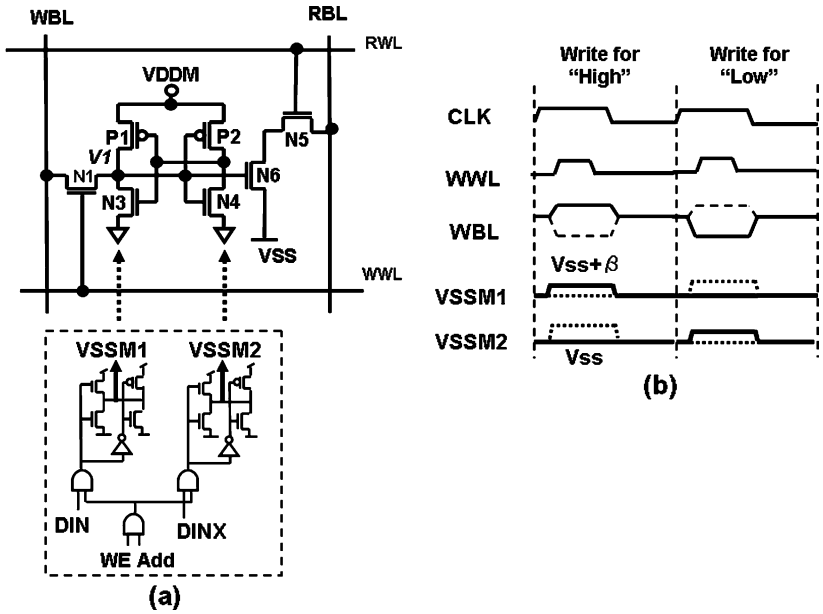


Fig. 14. Concept of differential VSSM control. (a) Schematic diagram of input-data-dependent Diff-VSSM control. (b) Timing diagram.

around the written cell and the comparison of their SNM, respectively. SNM at the Diff-VSSM disturbed cell is decreased by offset VSSM biasing as shown in the butterfly curve of Cell B. On the other hand, the relative SNM at WWL-disturbed cell (Cell C) is 0.39 compared with that of unselected cell (Cell D) at Vdd $= 0.9$ V and 125 °C. We set the target SNM at Cell B to higher than that of Cell C by controlling VSSM biasing level. As shown Fig. 15(b), the relative SNM at Cell B is set 0.47 compared with that of Cell D at Vdd $= 0.9$ V by setting Diff-VSSM level $= 0.2$ V. This SNM is higher than Cell C. SNM can be kept with this way while WRTM increases at Diff-VSSM biasing technique.

Another write-assist technique is a temperature-dependent cell biasing that makes use of the temperature characteristics of the cell operating margin as shown in Fig. 16(a). WRTM decreases as the temperature drops while SNM increases because Vth of the cell Tr increases. Therefore, the level of WWL can be boosted to assist a high-data write while keeping SNM at a half-selected cell in lower temperature (LT). The level of WWL and VDDM is switched, and WWL is driven by the level shifter [Fig. 16(b)] with the off-chip power supply in LT [Fig. 16(c)] with the assist of the on-chip temperature detector [11]. The area and DC current penalty of this detector were 0.3 mm2 and 200 μA. These penalties can be reduced by sharing it with multiple SRAM modules.

With those two high-data-write assist techniques described above, the required WWL-boost level at a written cell and the distribution of SNM at a half-selected cell at VDDM $= 0.9$ V, -40 °C and NMOS-slow/PMOS-fast global device condition (the worst condition for write) are shown in Fig. 17(a) and (b), respectively. Diff-VSSM biasing and the temperature dependent biasing reduced the required WWL-boost level by 0.45 V as shown in Fig. 17(a). As for SNM at a half-selected cell, the data hold failed (all 4-σ SNM < 0) if WWL was boosted for write assist without bias control as shown in Fig. 17(b). Although SNM was improved with Diff-VSSM control [Step 1 in Fig. 17(b)], the minimum SNM was close to zero under 4-σ random-Vth variation. The additional temperature-dependent bias control can keep enough SNM at half-selected cells for 7T write assist [Step 2 in Fig. 17(b)].

C. Cell Size

The cell current of proposed 7T 2-port cell can be increased by enlarging the width of read-access Tr N5 compared with

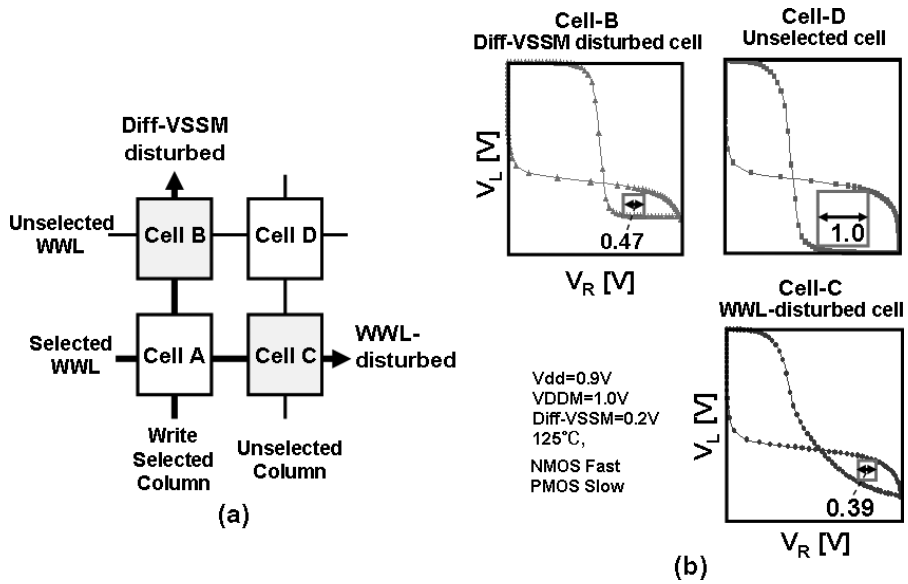


Fig. 15. (a) Position of the disturbed cell around the written cell (Cell A). (b) Butterfly curves and SNM comparison between Diff-VSSM disturbed cell (Cell B), WWL-disturbed cell (Cell C), and unselected cell (Cell D).

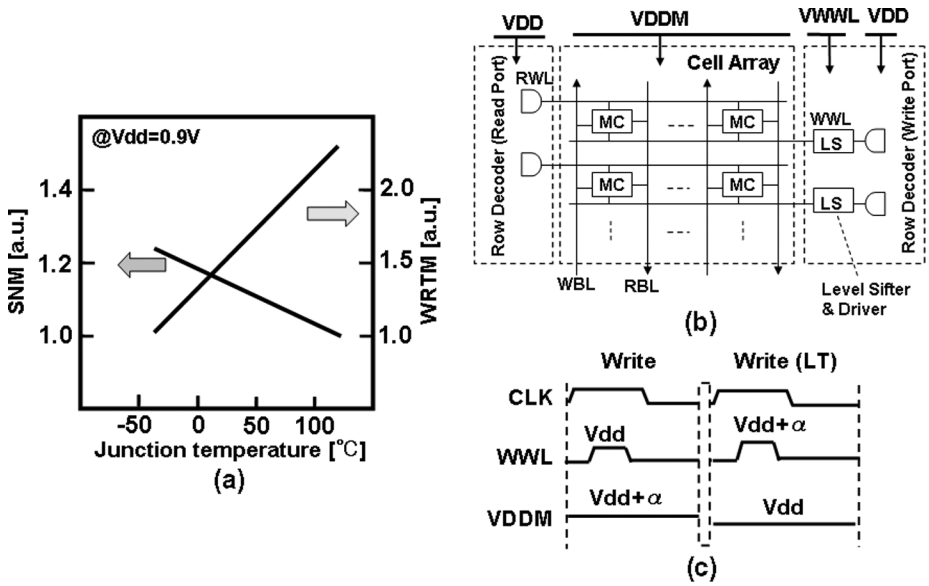


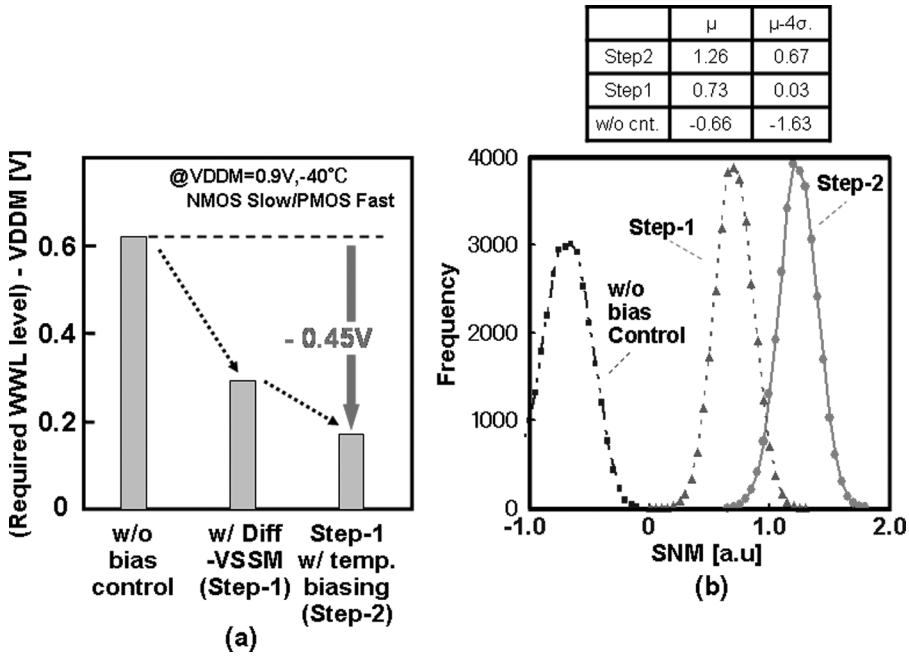
Fig. 16. Concept of temperature dependent cell-bias control. (a) Temperature dependence of cell margins. (b) Biasing for cell array and row decoder. (c) Biasing of WWL and VDDM depends on temperature.

the conventional 8T cell. The minimum Icell was increased by 2.1 times at Vdd $=$ 0.9 V while keeping the same cell size compared with the 8T cell with conventional VDDM control as shown in Fig. 18. Then the lateral cell size can be reduced by 26% while keeping the same Icell (4.5 μA at Vdd $=$ 0.9 V) compared with the 8T cell by reducing the width of read-drive Tr N6.

IV. Implementation

These proposed techniques have been implemented into a 32-Kbit 2-port SRAM module, and fabricated with 65-nm LSTP CMOS technology. The photograph and features of the module with 7T cell are shown in Fig. 19 and Table II, respectively. The organization is 1024-word $\times$ 32-bit. The VSSM drivers were located below the memory core and drove VSSM in each column. The area penalty of VSSM driver and the level shifter for WWL were 7% and less than 1% at this module. VDD and VDDM are supplied from the off-chip generator. The top-down SEM photo of the 7T cell is compared with 8T cell in Fig. 20. As the width of the read-port transistors (N5 and N6) was reduced in the 7T cell, the lateral cell size was reduced compared with the 8T cell.

The simulated wave form at the simultaneously R/W-disturbed access in the same column is shown in Fig. 21. A pulsed VSSM is generated during the write access at a written column to suppress the increase in power dissipation by boosting VSSM. The operating power of 32-Kbit module is compared between the proposed biasing and the conventional VDDM



	μ	μ-4σ.
Step2	1.26	0.67
Step1	0.73	0.03
w/o cnt.	-0.66	-1.63

Fig. 17. (a) Required WWL-boost level depending on write-assist techniques in LT. (b) Distribution of SNM at half-selected cell.

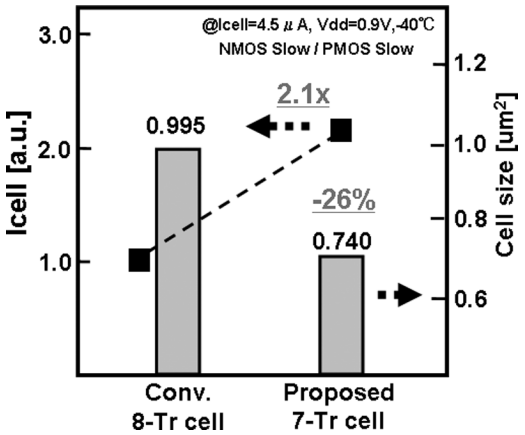


Fig. 18. Comparison of the cell current and cell-size reduction to realize the same cell current between proposed biasing with 7T cell and conventional control.

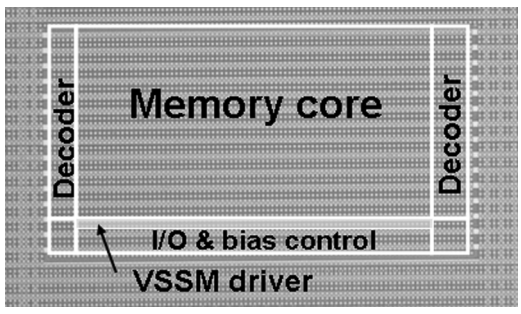


Fig. 19. Photograph of 32-K bit SRAM module.

TABLE II
FEATURES OF 32-Kbit SRAM MODULE

Configuration	1K words x 32bits
Process	65-nm LSTP CMOS
Cell size	1.45 μm x 0.51 μm (7-Tr cell)
Module size	392 μm x 198 μm
Operating Power	6.87mW @ 0.9V, 200MHz

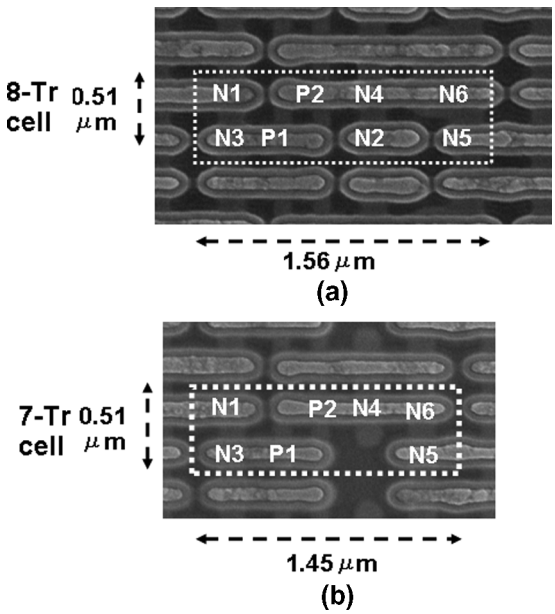


Fig. 20. Top-down SEM photos of the proposed 2-port cells: (a) 8T cell, (b) 7T cell.

control in Fig. 22. The increase in the operating power of the proposed biasing was 13% and 5.0% at 8T and 7T module, respectively. This power overhead was mainly caused by VSSM boost (+12.6% for 8T, and +5.0% for 7T) compared with the conventional VDDM control. The power overhead of 7T SRAM module was lower than the proposed 8T module because of the single VSSM boosting. The remaining power

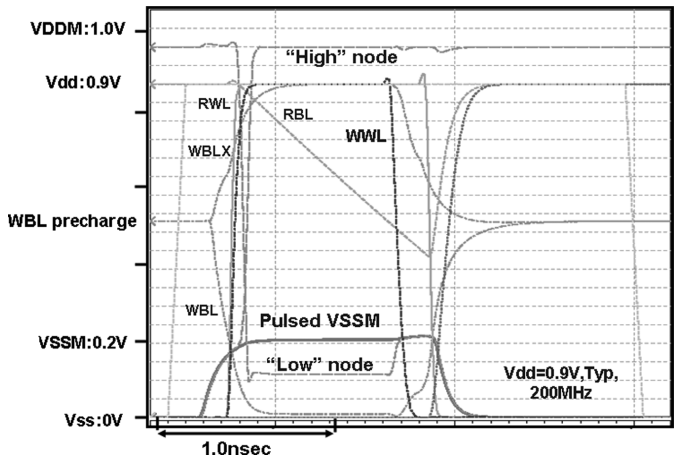


Fig. 21. Simulated wave form at a simultaneous R/W-disturbed access (8T cell).

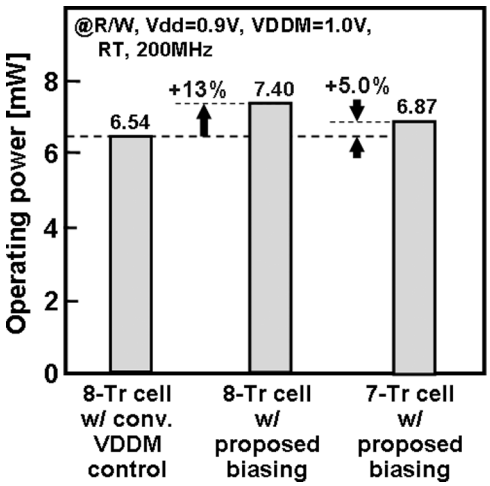


Fig. 22. Comparison of the operating power between proposed biasing and conventional VDDM control.

increase was mainly caused by the current flow from cell NMOS to WBL and RBL off leakage those were much smaller than that of VSSM boosting.

V. Conclusion

We have verified that the previous circuit techniques for improving cell stability have not met all the requirements for stable 2-port SRAM operation simultaneously. A new cell-terminal biasing which controlled the level of VSSM was proposed for an 8T 2-port cell. This biasing realized the stable operation at a simultaneous R/W access in the same column without any decrease in cell-current. The proposed cell biasing was implemented in a 32-Kbit 2-port SRAM module with 65-nm CMOS technology, and compared with the conventional VDDM control for write assist under 4-σ random-Vth fluctuation at Vdd $=$ 0.9 V. It demonstrated that the minimum Icell at a simultaneously R/W-disturbed cell was increased by 2.4 times while improving WRTM. The cell size based on the same Icell could be reduced by 20%. The minimum SNM at a half-selected cell was also improved by 44%. We have also challenged to design a 7T cell with the high-data write-assist techniques to save the cell-size. A 26% area-reduction was realized while keeping the cell current.

The proposed cell design satisfied all the requirements of 2-port SRAM operation while improving stability and saving cell size. This can be an effective solution for a future 2-port SRAM cell design.

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