What is a hierarchy?

1

Define digital.

2

Define analogue.

3

How many values can be represented by a binary number containing n bits?

4

Arrange `AND`, `OR` *and* `NOT` *in order of operator precedence.*

5

What is the symbol for `AND`*?*

6

What is the symbol for `OR`*?*

7

What is the symbol for `NOT`

8

A hierarchy is a group of objects arranged in tiers of descending magnitude, importance or complexity.

1

An entity that can reside in one of two states at any one time.

2

An entity that can reside in an infinite number of possible states.

3

2^n

4

`NOT`, `AND`, `OR`

5

$\cdot$

E.g. $A \cdot B$

6

$+$

E.g. $A + B$

7

$\overline{}$

E.g. $\overline{A}$

8

What is the symbol for `XOR`

9

What is De Morgan's theorem commonly used for when designing digital circuits?

10

What is the symbol for an `AND` *gate?*

11

What is the symbol for an `OR` *gate?*

12

What is the symbol for an `XOR` *gate?*

13

What is the symbol for an `NOT` *gate?*

14

What is the symbol for an `NAND` *gate?*

15

What is the symbol for an `NOR` *gate?*

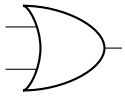
16

Converting gates such as `AND`, `OR`, `XOR` *etc into* `NAND` *and* `NOR` *since they are cheap and fast.*

10

$\oplus$
E.g. $A \oplus B$

9



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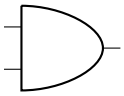

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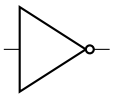

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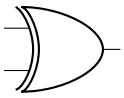

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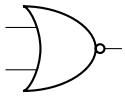

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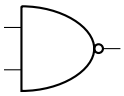


15

What's the symbol for a n:1 multiplexer?

17

What is the truth table for binary addition?

A	B	c_{in}	S	c_{out}
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

18

How do you negate a binary number?

19

Convert binary 6 *to* -6

20

Which bit is the signed bit when using 2's complement?

21

How do you subtract two binary numbers?

22

What is the sum-of-products?

23

What is the product-of-sums?

24

What is the truth table for binary addition?

A	B	c_{in}	S	c_{out}
0	*0*	*0*	*0*	*0*
0	*0*	*1*	*1*	*0*
0	*1*	*0*	*1*	*0*
0	*1*	*1*	*0*	*1*
1	*0*	*0*	*1*	*0*
1	*0*	*1*	*0*	*1*
1	*1*	*0*	*0*	*1*
1	*1*	*1*	*1*	*1*

18

17

1. Start with `0110`
2. Invert the bits - `1001`
3. Add 1 - `1010`

20

1. Invert the bits
2. Add 1

19

1. Invert the number you're subtracting
2. Add 1 to the inverted number
3. Add the number you're subtracting from with the inverted number.
Basically, add the original number to the 2's complement negative of what you're taking away.

22

The left most bit.

21

When a number of `OR` *gates are* `AND`*'ed together.*

24

When a number of `AND` *gates are* `OR`*'ed together.*

23

What is the structure of a half adder (in terms of gates)?

25

What is the truth table for the half adder?

A	B	S	c_{out}
0	*0*		
0	*1*		
1	*0*		
1	*1*		

26

Define propagation delay.

27

Fill in the table:

State	*Symbol*
Low	
High	
Tristate	
Unknown	

28

What does active high and active low mean?

29

What are the advantages of a hierarchy:

30

What is a combinatorial circuit?

31

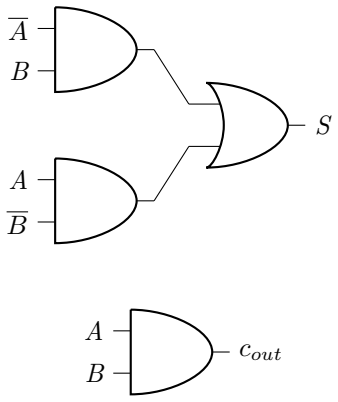
What is a sequential circuit?

32

What is the truth table for the half adder?

A	B	S	c_{out}
0	*0*	*0*	*0*
0	*1*	*1*	*0*
1	*0*	*1*	*0*
1	*1*	*0*	*1*

26



25

Fill in the table:

State	*Symbol*
Low	*0*
High	*1*
Tristate	*Z*
Unknown	*X*

28

Propagation delay is the time taken for the output of a gate to change after it's inputs have changed.

27

1. Encapsulation
2. Reuse of logic
3. Only have to define and test things once

30

If a signal is active high, then it is interpreted as `True` *when the signal is high (e.g. a light is on, or the voltage is positive etc).*
If a signal is active low, then it is interpreted as `True` *when the signal is low (e.g. a light is off, or the voltage is negative etc).*

29

A circuit where the value of the output depends on the values of the input and the past history of it's inputs. A sequential circuit requires a clock and memory.

32

A circuit where the value of the output depends only on the values of the input.

31

What is a synchronous clock?

33

What is a clock edge?

34

Define bistable.

35

What is a flip flop?

36

What is a register made of?

37

What is a finite state machine?

38

What do `S` *and* `R` *stand for on a S-R flip flop?*

39

What is the circuit symbol for a D-type latch?

40

The point on a clock signal where the signal is going from low to high (rising or positive edge) or high to low (falling or negative edge.)

34

A synchronous clock is one that is effective system wide; all components in the system adhere to this clock.

33

A bistable device that latches onto a state.

36

An entity that can be in one of two stable states.

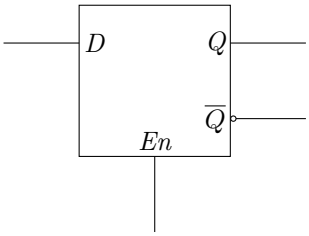
35

A digital system that holds the current state of itself and progresses to a new state based on the value of the current state.

38

A series of flip flops, each containing one bit.

37



40

`S` - *Set*
`R` - *Reset*

39

Is a D-type latch level sensitive or edge sensitive? What does that mean?

41

What is the circuit symbol for a D-type flip flop?

42

What does a D-type flip flop implement to make it synchronous?

43

What are the three delays in the D-type flip flop?

44

In order to ensure that a D-type flip flop will change state successfully, when does the input have to be constant?

45

What is the propagation delay?

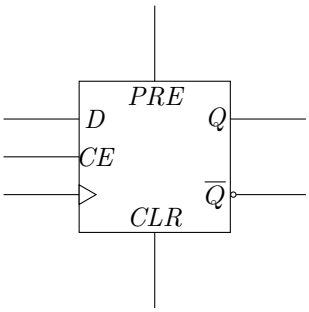
46

What is edge speed?

47

What does RTL mean?

48



42

The D-type latch is level sensitive, meaning that it will change state whenever the input changes, this means it's **asynchronous**.

41

The set-up time (T_{SU}), the hold time (T_H) and the propagation delay (T_{PD}).

44

It has an enable switch that can be linked to the clock so that it will only change state when the device is clocked.

43

The time taken for the flip flop to output a change of state.

46

From the beginning of the set-up time to the end of the hold time.

45

Register Transfer Layer

48

The time taken for a signal to change state.

47

Order the following in terms of their level of abstraction from lowest to highest:
- *Logic Gate Level*
- *Transistor Level*
- *Register Transfer Level*

49

What does the CE pin do on a register?

50

What are registers made up of?

51

Define the datapath.

52

What does the control block do at the Register Transfer Level?

53

1 *Transistor Level*
2 *Logic Gate Level*
3 *Register Transfer Level*

49

CE stands for clock enable, and when it is low, the register will ignore clock cycles.

50

Lots of flip flops.

51

The datapath is the path of registers and logical functions that the data flows through.

52

The control block controls the operation of the datapath. It sends control signals to the datapath so that the data does indeed, take the right path.

53