

# **The Role of Areal Capacity in Determining Short Circuiting of Sulfide-Based Solid-State Batteries**

*John A. Lewis<sup>1</sup>, Chanhee Lee<sup>2,3</sup>, Yuhgene Liu<sup>1</sup>, Sang Yun Han<sup>2</sup>, Dhruv Prakash<sup>1</sup>, Emily J. Klein<sup>1</sup>, Hyun-Wook Lee<sup>3</sup>, Matthew T. McDowell<sup>1,2\*</sup>*

<sup>1</sup>School of Materials Science and Engineering, Georgia Institute of Technology, 771 Ferst Drive, Atlanta, GA, 30332

<sup>2</sup>George W. Woodruff School of Mechanical Engineering, Georgia Institute of Technology, 801 Ferst Drive, Atlanta, GA, 30332

<sup>3</sup>Department of Energy Engineering, School of Energy and Chemical Engineering, Ulsan National Institute of Science & Technology (UNIST), Ulsan 44919, Republic of Korea.

\*Corresponding Author: mattmcowell@gatech.edu

## Abstract

Solid-state batteries (SSBs) with lithium metal anodes offer higher specific energy than conventional lithium-ion batteries, but they must utilize areal capacities  $>3 \text{ mAh cm}^{-2}$  and cycle at current densities  $>3 \text{ mA cm}^{-2}$  to achieve commercial viability. Substantial research effort has focused on increasing rate capabilities of SSBs by mitigating detrimental processes such as lithium filament penetration. Less attention has been paid to understanding how areal capacity impacts plating/stripping behavior, despite the importance of areal capacity for achieving high specific energy. Here, we investigate and quantify the relationships among areal capacity, current density, and plating/stripping stability using both symmetric and full-cell configurations with a sulfide solid-state electrolyte ( $\text{Li}_6\text{PS}_5\text{Cl}$ ). We show that unstable deposition and short circuiting readily occur at rates much lower than the measured critical current density when a sufficient areal capacity is passed. A systematic study of continuous plating under different electrochemical conditions reveals average “threshold capacity” values at different current densities, beyond which short circuiting occurs. Cycling cells below this threshold capacity significantly enhances cell lifetime, enabling stable symmetric cell cycling at  $2.2 \text{ mA cm}^{-2}$  without short circuiting. Finally, we show that full cells also exhibit threshold capacity behavior, but they tend to short circuit at lower current densities and areal capacities. Our results quantify the effects of transferred capacity and demonstrate the importance of using realistic areal capacities in experiments to develop viable solid-state batteries.

## **Introduction**

Solid-state batteries (SSBs) are at the forefront of next-generation energy storage technologies as they offer improved specific energy, energy density, and safety<sup>1–3</sup>. In particular, the use of lithium metal anodes in SSBs has attracted significant attention due to the opportunity to achieve specific energies greater than 350 Wh kg<sup>-1</sup><sup>4,5</sup>. It is believed that the use of a solid-state electrolyte (SSE) can mitigate the effects of dendritic deposition and inactive lithium formation that plague lithium metal anodes in liquid electrolytes<sup>6,7</sup>, thereby safely taking advantage of the extremely high theoretical capacity (3,860 mAh g<sup>-1</sup>) and low reduction potential (-3.05 V vs. SHE) of lithium.

A key challenge in the development of lithium metal-based SSBs is to achieve uniform lithium deposition at Li/SSE interfaces<sup>8–10</sup>. While SSEs were originally theorized to mechanically resist dendrite or filament formation<sup>11</sup>, it has been shown that lithium metal penetrates through a wide variety of SSE materials during deposition, which results in catastrophic short circuits<sup>12–17</sup>. This behavior is more prominent at high current densities, where electrodeposition becomes increasingly non-uniform and filamentary. Although the exact mechanisms behind lithium penetration are not entirely understood and depend on the properties of the SSE, recent work has suggested that lithium penetration is primarily driven by fracture of the SSE and subsequent deposition of lithium into cracks<sup>18–21</sup>. Furthermore, a variety of studies has shown that unstable lithium deposition is affected by surface defects, grain boundaries, microstructural inhomogeneities, electronic conductivity, and other factors<sup>12,16,19–24</sup>.

Recent studies have also demonstrated that stripping at Li/SSE interfaces plays a major role in destabilizing subsequent lithium deposition<sup>25–29</sup>. Stripping current densities that exceed the rate at which lithium can be replenished at the interface via deformation and/or self-diffusion lead to contact loss through the formation of interfacial voids. Contact loss causes higher current densities at the interface, and current constriction at the edges of interfacial voids further increases local current densities<sup>10,25</sup>. When plating occurs after contact loss, these higher local current densities increase the likelihood that lithium will penetrate through the SSE to form a short circuit.

Efforts toward reducing the prevalence of lithium penetration and short circuiting in lithium metal SSBs have primarily emphasized the importance of plating/stripping rates in dictating cell stability. It has been widely reported that sufficiently high plating current densities drive lithium penetration, and that stripping current densities exceeding the lithium replenishment rate destabilize subsequent plating. However, this prevailing focus on current density has overshadowed another

important parameter: the amount of lithium (*i.e.*, areal capacity) that can be stably plated and stripped over many cycles. The general effect of areal capacity on cell stability has been previously observed; for instance, critical current density measurements vary when using different cycle times, suggesting that plating/stripping larger amounts of lithium capacity makes cell failure more likely<sup>30</sup>. Critically, however, the impact of areal capacity on filamentary growth and short circuiting has not been systematically investigated and quantified. Furthermore, many studies that probe plating/stripping behavior use limited areal capacities that are well below the commercial requirements of at least 3 mAh cm<sup>-2</sup> for high-energy cells<sup>4,31,32</sup>. Given the importance of reaching high areal capacities while also operating at high current densities, there is a need to carefully examine the effects of cycling capacity on the stability of the lithium electrode in SSBs.

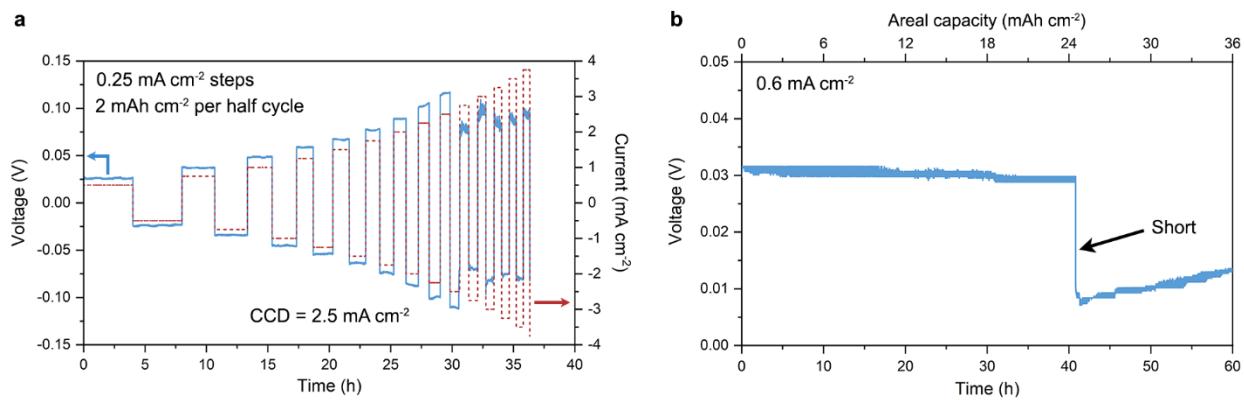
In this work, we investigate the relationships between current density, areal capacity, and plating/stripping stability in lithium metal SSBs with the Li<sub>6</sub>PS<sub>5</sub>Cl electrolyte. We compare conventional “critical current density” (CCD) measurements to results in which lithium is continuously plated in one direction at different current densities. We find that continuous plating eventually causes short circuits even at current densities far below the CCD. For instance, short circuits can form at ~1/4 of the measured CCD of 2.4 mA cm<sup>-2</sup> when plated for long enough. Analysis of many cells allows for identification of “threshold capacities” at various current densities, below which lithium can be reversibly plated and stripped over many cycles. With this understanding, we show excellent symmetric cell cycling stability at room temperature for current densities up to 2.2 mA cm<sup>-2</sup>. However, increasing the amount of lithium plated in each cycle leads to rapid cell failure at the same current densities, proving that capacity plays a key role in maintaining stable plating/stripping. Full cells with NMC-based cathodes show similar relationships between cycle capacity and cell lifetime as in symmetric cells, but are more susceptible to short circuiting than symmetric cells. Mechanistically, these results suggest that lithium filaments form over a wide range of current densities, but they can be reversibly stripped as long as they do not form catastrophic short circuits. Together, these findings reveal the effects of areal capacity on lithium short circuiting, representing an important advance in our understanding of SSB behavior.

## Results and Discussion

We used Li<sub>6</sub>PS<sub>5</sub>Cl (abbreviated LPSC, purchased from NEI Corp.) as the SSE for this study, as it exhibits kinetic interfacial stability against lithium metal via the formation of Li<sub>2</sub>S, Li<sub>3</sub>P, and LiCl<sup>33</sup>. It is also well-documented that lithium metal can penetrate through this SSE during cycling<sup>26,34-37</sup>. LPSC was verified to be single-phase with the expected cubic crystal structure using X-ray

diffraction (Fig. S1). To study lithium plating and stripping, we first investigated symmetric Li/LPSC/Li cells to avoid the rate limitations and degradation that cathodes can impose on cells. Symmetric cells were assembled using a custom housing similar to others that are widely used for testing sulfide SSEs (see methods)<sup>37,38</sup>.

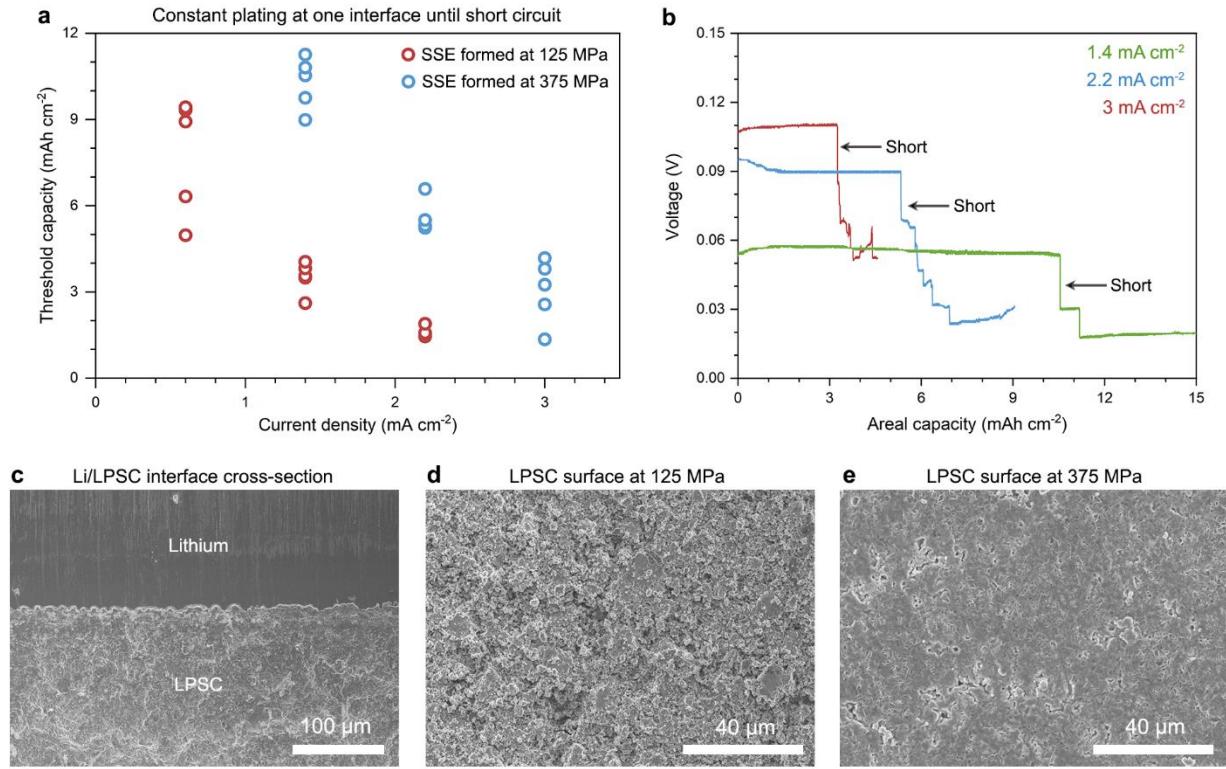
Understanding current density limits is critical for designing commercial SSBs, which must be able to plate at least 3 mAh cm<sup>-2</sup> of lithium at current densities greater than 3 mA cm<sup>-2</sup><sup>4,31,32</sup>. In the SSB literature, lithium metal deposition performance is often reported using a critical current density (CCD) test, which involves ramping the current density in sequential cycles until a short circuit is detected. We ran typical CCD experiments to determine the rate capabilities of optimized symmetric cells that were assembled with an SSE fabrication pressure of 375 MPa and stack pressure of 15 MPa. The current density was ramped in 0.25 mA cm<sup>-2</sup> steps starting at 0.5 mA cm<sup>-2</sup>, and 2 mAh cm<sup>-2</sup> of lithium was plated during each half cycle. A representative cell cycled using this procedure is shown in Fig. 1a, and additional experimental results from other cells are shown in Fig. S2. The CCD of this cell was 2.5 mA cm<sup>-2</sup>, and the average CCD for five cells using the same conditions was 2.4±0.4 mA cm<sup>-2</sup>. In the context of the wider literature, this CCD value is among the highest reported for SSBs at room temperature with unmodified interfacial chemistry and flat interfaces (non-porous electrodes), as shown in Figure S3 and Table S1.



**Figure 1. a)** Critical current density test of a Li/LPSC/Li cell. The initial current density was 0.5 mA cm<sup>-2</sup>, and the current density was increased in 0.25 mA cm<sup>-2</sup> steps after each cycle. The half-cycle capacity was 2 mAh cm<sup>-2</sup>. The CCD for this cell was 2.5 mA cm<sup>-2</sup>. **b)** Continuous plating at one interface in a Li/LPSC/Li cell at 0.6 mA cm<sup>-2</sup>. A short circuit formed after plating over 24 mAh cm<sup>-2</sup> (~120 µm of lithium metal plated). Both cells were assembled using an SSE fabrication pressure of 375 MPa and stack pressure of 15 MPa.

The CCD is often used as a metric to determine whether lithium metal will penetrate through the SSE. However, it is known that measured CCD values depend on the electrochemical conditions of the experiment, such as time per half-cycle and current step size<sup>30</sup>. The sensitivity of the CCD test to these parameters makes it challenging to understand whether there is a current density below which uniform plating occurs. To highlight this fact, we constructed a symmetric cell and continuously plated lithium at one interface using a current density of  $0.6 \text{ mA cm}^{-2}$  (Fig. 1b), which is far below the measured CCD. After plating for over 40 hours (corresponding to  $100+\mu\text{m}$  of lithium), the cell failed due to a short circuit. This experiment reveals that lithium can still grow in a filamentary fashion to penetrate the SSE when given enough time at current densities that are less than  $\frac{1}{4}$  of the measured CCD, and it highlights that CCD tests do not provide complete insight into the rates at which non-uniform deposition occurs.

Building on the experiment presented in Fig. 1b, we used continuous plating until short circuit formation as a screening method to probe the susceptibility of symmetric cells to lithium filament penetration under an array of electrochemical and assembly conditions. The cumulative areal capacity of lithium plated until the point of short circuiting was used as a metric to compare performance between cells, and we denote this value as the “threshold capacity” for that cell. A decrease in the cell impedance accompanied the short-circuiting process (Fig. S4). We probed cells with six different pairs of electrolyte fabrication pressures and current densities, with five cells being tested for each pair (a total of 30 cells). Repeated tests were necessary to evaluate the average effects of current density and cell fabrication conditions on short circuiting. Figure 2a is a plot of the threshold capacity as a function of current density for these 30 cells; the corresponding electrochemical curves are shown in Fig. 2b and Fig. S5, and Table 1 lists the average threshold capacity values measured. Half of the cells were assembled using an electrolyte fabrication pressure of 125 MPa (red circles), while the other half were assembled with a fabrication pressure of 375 MPa (blue circles). The fabrication pressure is applied during cold-pressing of the pellet before cell testing, and it affects the density of the SSE pellet (density results are reported below). The stack pressure applied to all cells during testing was 15 MPa. Figure 2c shows that good interfacial contact was established between the LPSC layer and the lithium electrode under these conditions.



fabrication pressure to 375 MPa resulted in a substantially higher average threshold capacity of  $10.3 \text{ mAh cm}^{-2}$ . SEM images of the surface morphology of LPSC pressed at 125 MPa and 375 MPa (Fig. 2d, e) show that the porosity decreased at higher pressures. This observation is supported by measurements of the pellet geometric density, which yielded 73% relative density at 125 MPa, and an increased relative density of 83% at 375 MPa. SSEs with higher density have fewer void spaces into which lithium can electrochemically grow or be mechanically deformed to fill during application of stack pressure<sup>37,39</sup>.

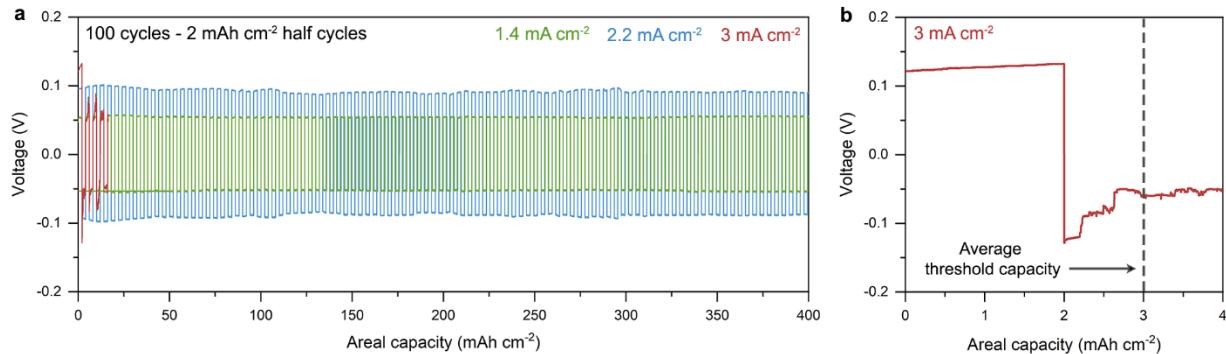
With five cells tested for each fabrication pressure/current density pair, the plot in Fig. 2a also shows that there is variation of the threshold capacity among cells despite using the same assembly procedure. For example, cells fabricated at 125 MPa and plated at  $0.6 \text{ mA cm}^{-2}$  had threshold capacities ranging from  $5.0 \text{ mAh cm}^{-2}$  to  $9.4 \text{ mAh cm}^{-2}$ . This variation could be related to differences in pore distribution and morphology of the interfaces in different cells, which can affect the initial uniformity of the Li/LPSC interface after application of stack pressure. Variation could also be attributed to the nature of crack formation and lithium propagation across the electrolyte<sup>19,20,24</sup>, which will depend partially on the locations of defects that differ even under the same assembly conditions due to their stochastic nature. Regardless of the mechanisms involved, the observed variation in threshold capacity indicates that collecting data from multiple cells is important to correctly assess the behavior of Li/SSE interfaces in both research and industrial settings. Practical lithium-metal SSBs must account for such cell-to-cell variations and operate under conditions that are safe for the full range of conditions required to ensure sufficient quality control over cell lifetime. We note that this may be a distinct challenge for SSBs due to the presence of defects in SSEs like pores, cracks, and grain boundaries that are absent in liquid electrolytes and likely cannot be precisely controlled between cells.

**Table 1.** Summary of average threshold capacities measured for different plating conditions.

Fabrication pressure (MPa)	Current density ( $\text{mA cm}^{-2}$ )	Average threshold capacity ( $\text{mAh cm}^{-2}$ )
125	0.6	$7.8 \pm 2.0$
125	1.4	$3.5 \pm 0.5$
125	2.2	$1.6 \pm 0.2$
375	1.4	$10.3 \pm 0.9$
375	2.2	$5.6 \pm 0.6$
375	3.0	$3.0 \pm 1.1$

We also found that stack pressure plays a major role in resisting filament formation, consistent with other studies<sup>36,37</sup>. An optimal stack pressure for symmetric cells in this work was found to be 15 MPa, which was the value used for all cells in Figs. 1 and 2. A lower stack pressure of 6 MPa resulted in voltage polarization due to voiding at the stripping interface (Fig. S6a), which could be attributed to less lithium deformation. Plating at 30 MPa resulted in less areal capacity transported before short circuiting (Fig. S6b). This behavior is likely caused by the higher pressure driving greater quantities of lithium into the SSE before plating, as demonstrated by Doux *et al.*<sup>37</sup>.

The data presented in Fig. 2 focused on understanding the resistance to lithium metal penetration and short circuiting without the effects of previous stripping. Since stripping is an integral part of a real lithium metal battery, it is important to investigate the following: 1) the effectiveness of stripping toward dissolving existing filaments, 2) how contact loss during stripping impacts subsequent plating, and 3) how the areal capacity used during cycling impacts cell stability. To understand these issues, we conducted cycling experiments using our optimized cell assembly with a fabrication pressure of 375 MPa and stack pressure of 15 MPa. The same current densities (1.4, 2.2, and 3.0 mA cm<sup>-2</sup>) were used to facilitate comparison to the data in Fig. 2a.



**Figure 3. a)** Cycling of symmetric Li/LPSC/Li cells at current densities of 1.4 mA cm<sup>-2</sup> (green), 2.2 mA cm<sup>-2</sup> (blue), and 3.0 mA cm<sup>-2</sup> (red) with half-cycle areal capacities of 2.0 mAh cm<sup>-2</sup>. **b)** Magnified plot from the cell cycled at 3.0 mA cm<sup>-2</sup> in (a). The dashed line represents the average threshold capacity for cells plated at 3.0 mA cm<sup>-2</sup>, as presented in Fig. 2a and Table 1. The SSE fabrication pressure and stack pressure were 375 MPa and 15 MPa for all cells.

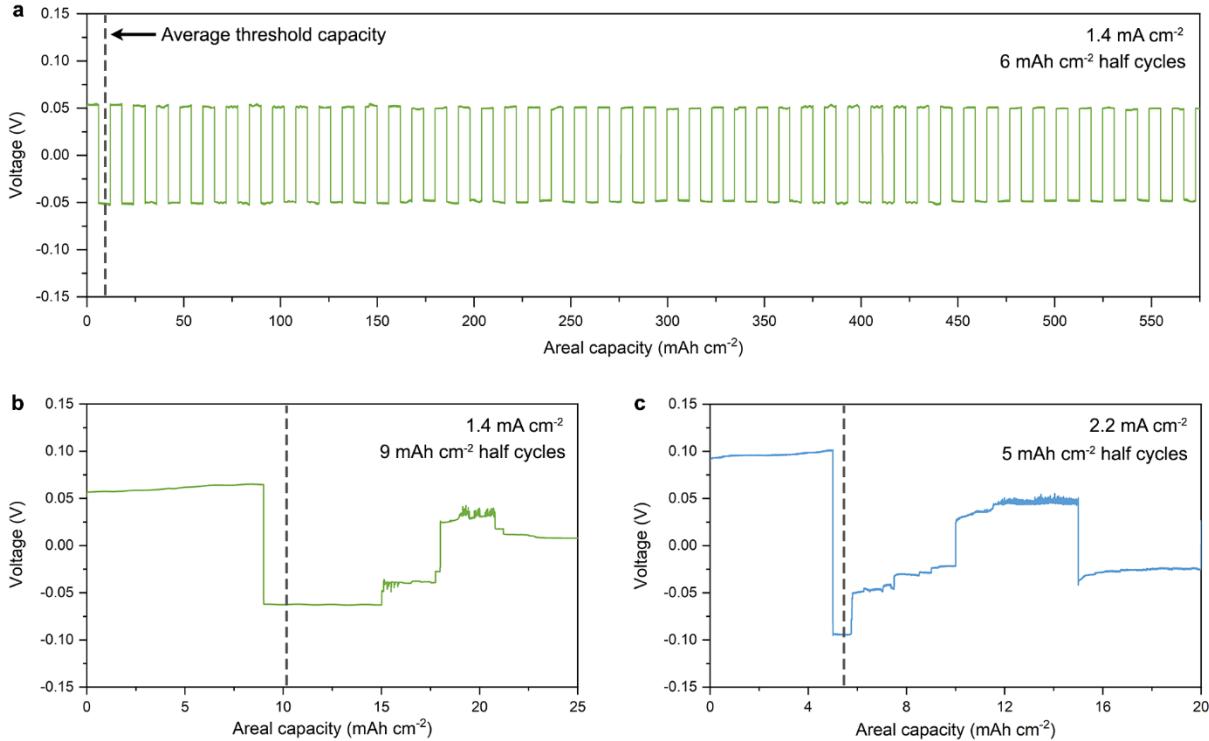
Figure 3 shows symmetric cell cycling using a half-cycle capacity of 2.0 mAh cm<sup>-2</sup>. This areal capacity was chosen because it is less than the threshold capacity in all cases (Fig. 2a and Table 1), ensuring that short circuiting will not occur during the first half cycle. Data from repeated experiments are included in Figs. S7-9 to support the validity of these results. Figure 3a shows

that cells cycled at 1.4 and 2.2 mA cm<sup>-2</sup> exhibited excellent stability for 100 cycles without short circuiting or voltage polarization associated with poor stripping<sup>25-28</sup>. Cycling these cells substantially increases the cumulative amount of lithium that can be plated before failure compared to the continuous plating experiments in Fig. 2a. For example, the average plating threshold capacity at a current density of 2.2 mA cm<sup>-2</sup> was 5.6 mAh cm<sup>-2</sup> (Fig. 2a), whereas cells cycled at 2.2 mA cm<sup>-2</sup> using 2.0 mAh cm<sup>-2</sup> per half cycle were able to cumulatively plate over 200 mAh cm<sup>-2</sup> at one interface without short circuiting (Fig. 3a). Since filaments can be formed at current densities well below the CCD, these experiments strongly indicate that stripping is effective at removing previously-grown lithium filaments even at relatively high current densities and capacities. However, contrasting behavior was observed for cells cycled with the same cycle capacity of 2.0 mAh cm<sup>-2</sup> with the higher current density of 3.0 mA cm<sup>-2</sup>, as shown in Fig. 3a and b. Instead of extended lifetime, these cells rapidly failed in the second half cycle when plating began at the freshly stripped interface. Notably, the half-cycle capacity of 2.0 mAh cm<sup>-2</sup> was 66.7% of the average threshold capacity for plating at 3.0 mA cm<sup>-2</sup>, compared to 19.4% for 1.4 mA cm<sup>-2</sup> and 35.7% for 2.2 mA cm<sup>-2</sup>. This behavior suggests that using a capacity well below the average threshold capacity for short circuiting mitigates the risks of symmetric cell failure, but cycling with capacities near the threshold can lead to rapid short circuiting.

We next investigated how approaching the threshold capacity in a half-cycle affects cycling stability. Symmetric cells were cycled at 1.4 mA cm<sup>-2</sup> with half-cycle capacities of 6.0 mAh cm<sup>-2</sup> (Fig. 4a and Fig. S10); this half cycle capacity is 58.2% of the average threshold capacity found in Fig. 2a. Using these cycling conditions, we found that it was possible to reversibly plate 6.0 mAh cm<sup>-2</sup> of lithium in each half cycle for a total capacity of over 550 mAh cm<sup>-2</sup>, demonstrating similar stability as shown in Fig. 3a. However, Fig. 4b shows that increasing the half-cycle capacity to 9.0 mAh cm<sup>-2</sup> (87.3% of the average threshold capacity) severely reduced the cell lifetime, with a short circuit forming in the first cycle. Similar stability issues were observed in cells cycled at 2.2 mA cm<sup>-2</sup> with 5.0 mAh cm<sup>-2</sup> transported per half cycle (89.3% of the average threshold capacity), as shown in Fig. 4c. Additional cells cycled under these conditions corroborated these conclusions (Figs. S11 and S12).

These extensive results from symmetric cells show that cell stability is linked to the amount of lithium that is plated each cycle, which is critical information that is usually absent from conventional CCD measurements. Understanding the average threshold capacity at a given current density allows for tuning of the cycling capacity to substantially increase the lifetime of symmetric cells. Furthermore, these cells can be reversibly cycled without polarization and

contact loss caused by stripping, indicating that lithium is sufficiently replenished at the interfaces at current densities up to  $2.2 \text{ mA cm}^{-2}$ .

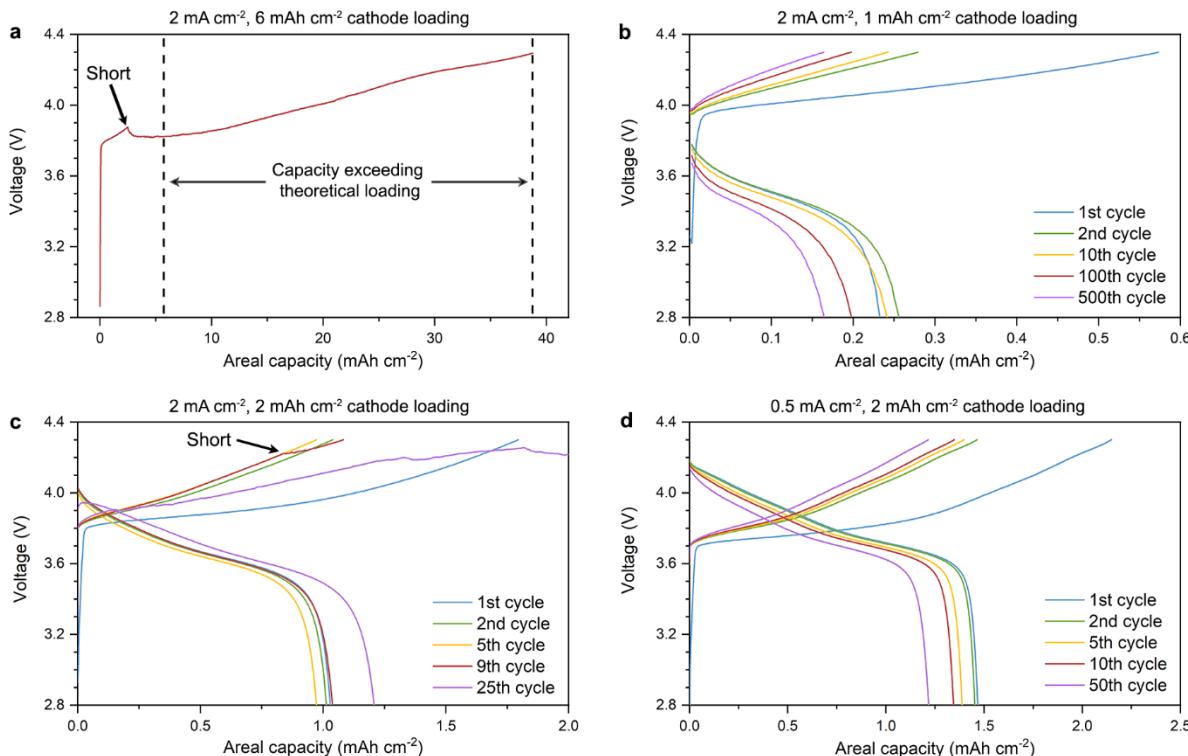


**Figure 4.** **a)** Stable symmetric cell cycling at  $1.4 \text{ mA cm}^{-2}$  using a half-cycle capacity of  $6.0 \text{ mAh cm}^{-2}$ . **b)** Unstable cycling at  $1.4 \text{ mA cm}^{-2}$  when the half cycle capacity is increased to  $9.0 \text{ mAh cm}^{-2}$ . **c)** Unstable cycling at  $2.2 \text{ mA cm}^{-2}$  using a half cycle capacity of  $5.0 \text{ mAh cm}^{-2}$ . The dashed line in each plot represents the average threshold capacity for the corresponding current density as measured in Fig. 2.

The data presented thus far have leveraged symmetric cells to probe Li/SSE interfaces. However, these results must be connected to data from full SSBs that incorporate both a lithium metal anode and a cathode, as there may be fundamental differences in lithium metal penetration when plating/stripping in a full cell compared to symmetric cells. To compare to our symmetric cells, we constructed full cells with a composite cathode consisting of 70 wt%  $\text{LiNbO}_3$ -coated  $\text{LiNi}_{0.8}\text{Mn}_{0.1}\text{Co}_{0.1}\text{O}_2$  (NMC811), 27.5 wt% LPSC, and 2.5 wt% carbon black. Using five full cells, we replicated the continuous plating symmetric cell experiments in Fig. 2 by applying a high current density of  $2.0 \text{ mA cm}^{-2}$  during the first charge. The theoretical areal capacity loading of the cathode was  $6.0 \text{ mAh cm}^{-2}$  in these experiments to ensure that a short circuit would occur before the cathode was depleted of lithium. Figure 5a shows a cell charged under these

conditions, which was able to plate 2.5 mAh cm<sup>-2</sup> before shorting. The average threshold capacity for the five cells was 2.8 mAh cm<sup>-2</sup>; the additional charge curves are shown in Fig. S13.

The charging curve in Fig. 5a shows the typical short-circuiting behavior that we observed in the full cells (also shown in Fig. S13). The short circuits in the full cells are identified as a sudden drop in cell voltage, which is also sometimes followed by a slow decrease in voltage that should not occur if lithium is being extracted from the cathode. The cell voltages eventually continued to increase and reached the voltage limit, but the cells exhibited large charging capacities substantially exceeding the theoretical areal capacity of the cathode. For example, the cell in Fig. 5a showed an excess capacity of 33 mAh cm<sup>-2</sup> beyond the 6.0 mAh cm<sup>-2</sup> theoretical cathode capacity. This behavior indicates that the full-cell failure we observed is a form of “soft shorting.” Similar short-circuit voltage profiles have also been reported by other groups<sup>35,40–42</sup>.



**Figure 5.** Understanding threshold capacity behavior in full cells. **a)** Charging a Li/LPSC/NMC811 full cell at 2.0 mA cm<sup>-2</sup> with a cathode loading of 6.0 mAh cm<sup>-2</sup> to form a short circuit during the first charge. **b)** Cycling a Li/LPSC/NMC811 cell at 2.0 mA cm<sup>-2</sup> using a lower cathode loading of 1.0 mAh cm<sup>-2</sup>. **c)** Cycling a Li/LPSC/NMC811 cell at 2.0 mA cm<sup>-2</sup> using a cathode loading of 2.0 mAh cm<sup>-2</sup>. **d)** Cycling a Li/LPSC/NMC811 cell at 0.5 mA cm<sup>-2</sup> with a loading of 2.0 mAh cm<sup>-2</sup>. The SSE fabrication pressure was 375 MPa and the stack pressure was 16 MPa for all cells.

With an average threshold capacity established for these full cells charged at  $2.0 \text{ mA cm}^{-2}$ , we cycled full cells with lower cathode loadings to intentionally reduce the plated capacity to be below the threshold. If the relationship between capacity and plating/stripping stability for full cells is similar to symmetric cells, then we expect full cells with lower cathode loadings to have greatly enhanced lifetimes. We note that cycling at  $2.0 \text{ mA cm}^{-2}$  with lower cathode loadings will increase the cathode C-rate and result in a lower fraction of the theoretical capacity being accessed, as well as higher overpotentials. Figure 5b shows charge-discharge curves for a cell cycled at  $2.0 \text{ mA cm}^{-2}$  with a cathode loading of  $1.0 \text{ mAh cm}^{-2}$ . Due to the high C-rate of 2C, the first charge only reached 58 % of the theoretical capacity, and the first cycle had a low Coulombic efficiency of 40.6%. These penalties limited the average amount of lithium plated in each charge to be  $0.19 \text{ mAh cm}^{-2}$ , which is far below the average threshold capacity of  $2.8 \text{ mAh cm}^{-2}$ . Similar to the symmetric cells, this full cell was capable of cycling 500 times without the formation of a short circuit. The cumulative lithium plated over these 500 cycles was  $94 \text{ mAh cm}^{-2}$ , which is much larger than the average threshold capacity and demonstrates the cell's reversibility, albeit at low areal capacities.

Increasing the cathode loading to  $2.0 \text{ mAh cm}^{-2}$  enabled a higher fraction of the theoretical cathode loading to be accessed at the same current density of  $2.0 \text{ mA cm}^{-2}$  (Fig. 5c), but the cell still had a low initial CE of 57.3%. As a result, the average capacity plated per charge in the first eight cycles was  $1.09 \text{ mAh cm}^{-2}$ . Despite being cycled at areal capacities well below the average threshold capacity of  $2.8 \text{ mAh cm}^{-2}$ , this cell began to short in the 9<sup>th</sup> cycle, and continued to gain excess charge capacity during subsequent cycles. The shorting behavior could also be identified by a rapid decay in CE associated with the increase in excess charge capacity (Fig. S14). However, the cumulative capacity plated before the short circuit initiated in cycle 9 was  $\sim 9.5 \text{ mAh cm}^{-2}$ , demonstrating a modest improvement over the threshold capacity. Cycling a cell at  $0.5 \text{ mA cm}^{-2}$  with the same cathode loading resulted in over 50 cycles without any short circuiting, as shown in Fig. 5d.

These data reveal important information about plating/stripping behavior in full cells. First, it appears that full cells are prone to short circuiting at lower areal capacities compared to symmetric cells. In our case, plating an average areal capacity of  $2.8 \text{ mAh cm}^{-2}$  at  $2.0 \text{ mA cm}^{-2}$  in full cells led to failure, whereas symmetric cells tested at  $2.2 \text{ mA cm}^{-2}$  could withstand an average areal capacity of  $5.6 \text{ mAh cm}^{-2}$ . Second, the benefits of using a half-cycle capacity below the average threshold capacity may be diminished for full cells. While cycling without a short circuit was possible in full cells when using low half-cycle capacities of  $0.19 \text{ mAh cm}^{-2}$  (6.8% of the average

threshold capacity), increasing the half-cycle capacity to just 38.9% of the average threshold capacity only yielded moderate improvements in cell lifetime and did not prevent short circuiting. The greater susceptibility to lithium metal penetration and lower reversibility during cycling suggests that there could be important differences in plating/stripping mechanisms at Li/SSE interfaces in full cells compared with symmetric cells. Detailed characterization of plating/stripping in full cells using pure lithium metal anodes is thus urgently needed, as the vast majority of the mechanistic understanding of Li/SSE interfaces is based on symmetric configurations.

In this work, we have further developed our understanding of the relationships between current density, capacity, and plating/stripping stability in SSBs. We have found that given enough time, lithium metal penetration through the SSE occurs and causes short circuits even at current densities much lower than the CCD. The average “threshold capacity” was used as a parameter to gauge resistance to short circuiting, and a relatively large dataset revealed that the average threshold capacity is strongly impacted by current density, SSE fabrication pressure, and stack pressure. We observed some variation in the amount of lithium that could be plated even when using the same electrochemical and cell assembly conditions, demonstrating the challenges of achieving consistent performance between cells. When symmetric cells were cycled using a plating capacity much lower than the threshold capacity, they exhibited excellent stability at current densities up to  $2.2 \text{ mA cm}^{-2}$ . However, increasing the plating capacity closer to the threshold capacity resulted in rapid cell failure. These findings demonstrate the importance of controlling areal capacity transported in each cycle to ensure long cell lifetime. Lastly, full cells were fabricated and tested using similar experiments to understand how these concepts apply to practical SSBs. While similar phenomena were observed in the relationship between areal capacity and short circuiting, we also found that full cells were more susceptible to short circuiting at lower areal capacities transferred, motivating the need for future studies to elucidate potential mechanistic differences.

The results herein represent a systematic investigation that sheds light on the role of areal capacity transferred in determining short circuiting behavior of SSBs. Critical current density measurements widely used in the SSB literature are important, but they do not provide a full picture of interfacial stability for a given material and set of conditions. In particular, if CCD measurements are performed with low areal capacity transferred ( $< 1 \text{ mAh cm}^{-2}$ ) per half-cycle, this can artificially inflate the CCD since higher areal capacities are necessary for high-energy-density full-cell SSBs. Thus, it would be ideal if both average CCD values and threshold capacity

measurements (or another similar metric) are reported for new materials and SSB configurations in future studies.

## Methods

### Symmetric cell assembly

$\text{Li}_6\text{PS}_5\text{Cl}$  (LPSC) powder was purchased from NEI Corp. Before cell assembly, the as-received powder was ground by hand using a mortar and pestle (typically ~600 mg of LPSC for 20 min of active grinding). 90 mg of ground LPSC was poured into a polyether ether ketone (PEEK) die with an inner diameter of 10 mm and compressed in a uniaxial press to either 125 MPa or 375 MPa for one minute. The surfaces of the formed pellet were then inspected to verify that no macroscale defects, such as cracking or warping, were present. Lithium metal discs were punched out and pressed onto stainless steel or titanium plungers until the mass of each disc was ~13 mg (roughly 0.3 mm thick). This thickness was chosen to ensure that lithium could be consistently deformed to contact the entire electrolyte surface for every cell. The lithium discs were then cleaned using a toothbrush and the plungers were inserted into each end of the die. The symmetric Li/LPSC/Li stack was placed in the uniaxial press and compressed to ~20 MPa for 5 min. The cell was then sandwiched between two steel plates and four nuts were tightened with a torque wrench until the stack pressure was 15 MPa. Cells were electrochemically tested using either a Landt battery cycler or a Bio-Logic SP200 potentiostat. Electrochemical impedance spectroscopy (EIS) was performed using a voltage amplitude of 10 mV between 7 MHz and 2 Hz with 10 points per decade. All assembly and cycling steps were conducted in an Ar-filled glovebox at temperatures between 27 °C and 29 °C.

### Full cell assembly

The composite cathode was prepared following a procedure similar to that reported by Doerrer *et. al*<sup>43</sup>. A 1.4 g mixture of 70 wt %  $\text{LiNbO}_3$ -coated  $\text{LiNi}_{0.8}\text{Mn}_{0.1}\text{Co}_{0.1}\text{O}_2$  (NMC811, NEI Corp.), 27.5 wt % LPSC, and 2.5 wt % Super P carbon black (MTI) was added to a  $\text{ZrO}_2$  jar with 18  $\text{ZrO}_2$  balls (10 mm diameter) inside an Argon filled glovebox. The jar was then sealed and removed from the glovebox for milling in a planetary ball mill (Fritsch Pulverisette 7). A milling speed of 140 RPM was used with 3 cycles, with each cycle consisting of 10 min of milling and 5 min of resting. The jar was then brought back into the glovebox, unsealed, and the powder was removed by shaking the balls in the jar and lightly scraping excess powder stuck to the jar walls with a steel spatula.

Full cells were assembled by first pouring 90 mg of ground LPSC powder into a 10 mm-diameter PEEK die. Titanium plungers were used to hand press the powder into a soft packed layer. The amount of composite cathode needed for the desired cathode loading was then added to one side of the pellet and was carefully distributed to form a uniform cathode layer. For reference, 5.6 mg of composite mass was equivalent to a loading of 1.0 mAh cm<sup>-2</sup> based on a theoretical capacity of 200 mAh g<sup>-1</sup> of the NMC811. The stack was then pressed at 375 MPa for one minute using a uniaxial press to densify the SSE and cathode layers. The plungers were removed and a lithium disc (~13 mg) was pressed onto the anode plunger. This disc was then cleaned with a toothbrush and the plungers were inserted back into the die. The stack was inserted between two steel plates and tightened with a torque wrench to a pressure of 16 MPa. All assembly and cycling steps were conducted in an Ar-filled glovebox. The full cells were charged/discharged between 2.8 and 4.3 V using either a Landt battery cycler or a Bio-Logic SP200 potentiostat.

### **Characterization**

The X-ray diffraction pattern for pristine LPSC was collected using a Panalytical Empyrean X-ray diffractometer with Cu K- $\alpha$  radiation,  $\lambda=1.5406\text{ \AA}$ , 45 kV, 40 mA, and scan angle step size of 0.0131°.

Scanning electron microscopy images were collected using a Zeiss Ultra 60 SEM with an accelerating voltage of 5 kV. Samples for surface imaging were prepared by pressing 90 mg of LPSC at either 125 or 375 MPa in a PEEK die, extracting the pellets from the die, and mounting them to aluminum SEM stubs with carbon tape. For the Li/LPSC interface cross-section imaging, a symmetric cell was assembled using an SSE fabrication pressure of 375 MPa and stack pressure of 15 MPa. The stack pressure was held for an hour and then released to extract the sample. During assembly, copper discs were placed between the lithium electrodes and plungers to prevent damage due to the sample extraction process. A razor blade was used to cut the cross-section.

For geometric density measurements, 90 mg of powder was pressed at either 125 or 375 MPa and extracted from the die. The freestanding pellets were then massed and a micrometer (accuracy of  $\pm 2.5\text{ }\mu\text{m}$ ) was used to measure their thickness and diameter to calculate the density.

### **Author Contributions**

J. A. Lewis: Conceptualization, Methodology, Validation, Formal Analysis, Investigation, Writing – Original Draft, Writing – Review & Editing, Visualization. C. Lee: Methodology, Validation,

Investigation. Y. Liu – Methodology, Investigation. S. Y. Han – Methodology, Investigation. D. Prakash – Investigation. E. J. Klein – Investigation. H.-W. Lee: Writing – Review & Editing, Supervision, Funding Acquisition, M. T. McDowell: Writing – Review & Editing, Supervision, Project Administration, Funding Acquisition.

## Conflicts of Interest

There are no conflicts to declare.

## Acknowledgments

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## **Supporting Information**

### **The Role of Areal Capacity in Determining Short Circuiting of Sulfide-Based Solid-State Batteries**

*John A. Lewis<sup>1</sup>, Chanhee Lee<sup>2,3</sup>, Yuhgene Liu<sup>1</sup>, Sang Yun Han<sup>2</sup>, Dhruv Prakash<sup>1</sup>, Emily J. Klein<sup>1</sup>, Hyun-Wook Lee<sup>3</sup>, Matthew T. McDowell<sup>1,2\*</sup>*

<sup>1</sup>School of Materials Science and Engineering, Georgia Institute of Technology, 771 Ferst Drive, Atlanta, GA, 30332

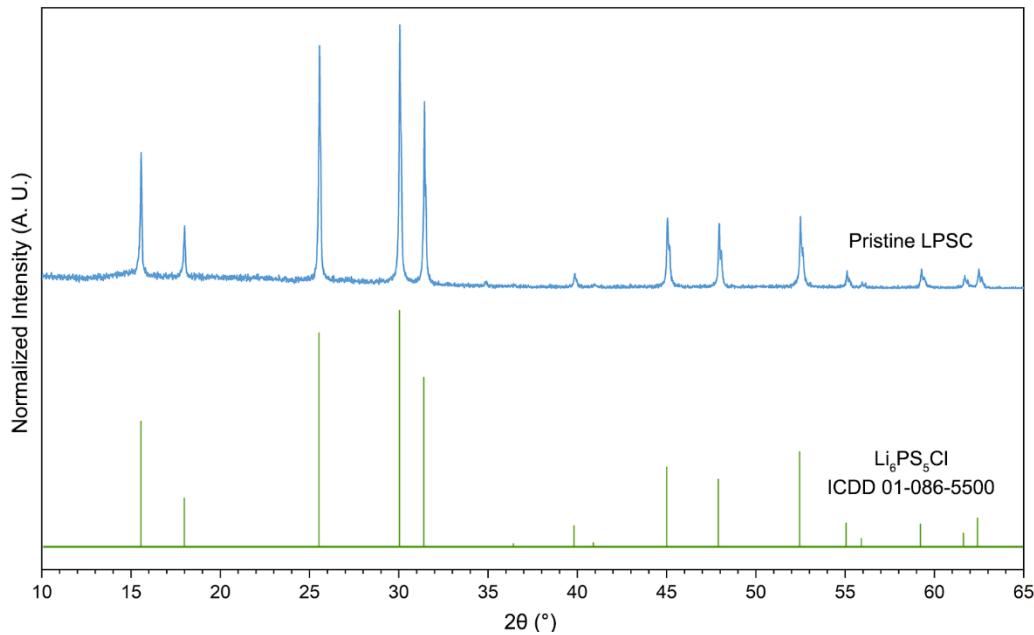
<sup>2</sup>George W. Woodruff School of Mechanical Engineering, Georgia Institute of Technology, 801 Ferst Drive, Atlanta, GA, 30332

<sup>3</sup>Department of Energy Engineering, School of Energy and Chemical Engineering, Ulsan National Institute of Science & Technology (UNIST), Ulsan 44919, Republic of Korea.

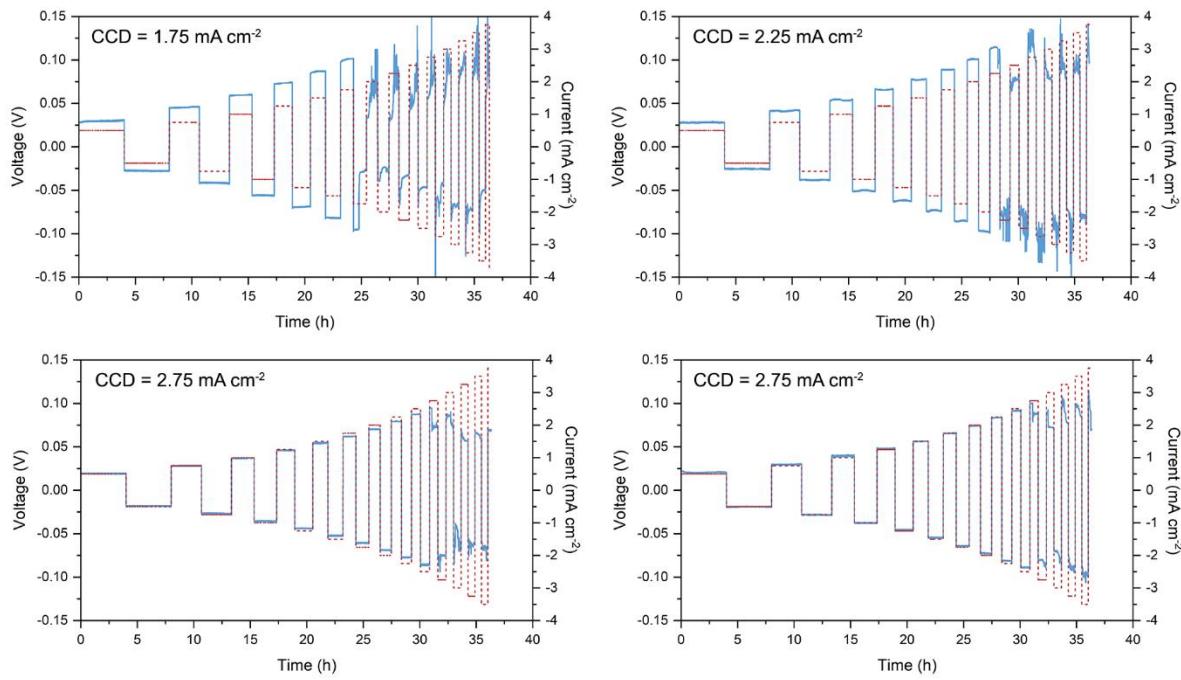
\*Corresponding Author: [mattmcdowell@gatech.edu](mailto:mattmcdowell@gatech.edu)

**Table S1.** Comparison of symmetric cell data presented in this work to other literature reports. A dash means that the value was not reported.

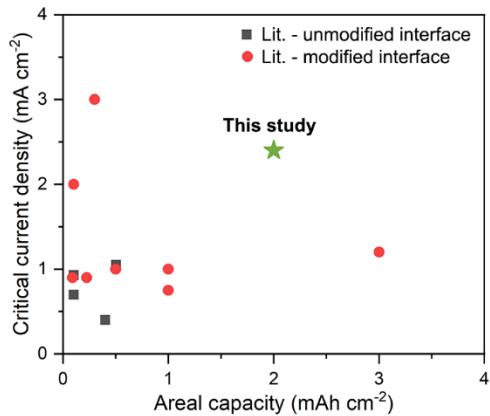
SSE type	CCD (mA cm <sup>-2</sup> )	CCD half-cycle step time / capacity	Cycling current (mA cm <sup>-2</sup> )	Half cycle capacity (mA cm <sup>-2</sup> )	Number of cycles	Stack pressure (MPa)	Temp. (°C)	Modified interface	Ref.
<b>Sulfides</b>									
LPSC	2.4	2 mAh cm <sup>-2</sup>	2.2	2	100+	19	28	No	This work
LPSC	-	-	0.075	0.075	500+	5	25	No	1
LPS	0.4	1 hr	0.3	0.3	9	-	25	No	2
LPS-LiI	1	1 hr	0.3	0.3	100+	-	25	Yes	2
LPS	0.7	0.1 mAh cm <sup>-2</sup>	0.3	0.6	22	-	25	No	3
LiFSI coated LPS	>2	0.1 mAh cm <sup>-2</sup>	0.3	0.6	90+	-	25	Yes	3
LPSC	1.05	0.5 hr	0.5	0.5	1500+	-	25	No	4
Amorph. LPS	0.75	1 hr	-	-	-	29	60	No	5
LPS-LiI	4	1 hr	-	-	-	29	60	Yes	5
LPSC	-	-	1	1	100+	7	25	No	6
Li <sub>3</sub> N-LiF-LPS	>3	0.3 mAh cm <sup>-2</sup>	1	1	110+	-	25	Yes	7
LPSC <sub>0.3</sub> F <sub>0.7</sub>	-	-	6.37	5	98+	-	25	Yes	8
<b>Oxides</b>									
LLZTO	0.9	10 min	0.2	-	3000+ hours	-	25	Yes	9
LLZTO	0.9	0.25 hr	0.5	0.25	200+	0.1	60	Yes	10
LLZO	0.93	0.1 mAh cm <sup>-2</sup>	-	-	-	3.4	25	No	11
LLZTO	1	0.5 hr	0.3	0.15	250+	-	25	Yes	12
LLZTO	1.2	>3 mAh cm <sup>-2</sup>	-	-	-	1.5	25	Yes	13
Trilayer LLZO	-	-	3	2	400+	-	25	Yes	14



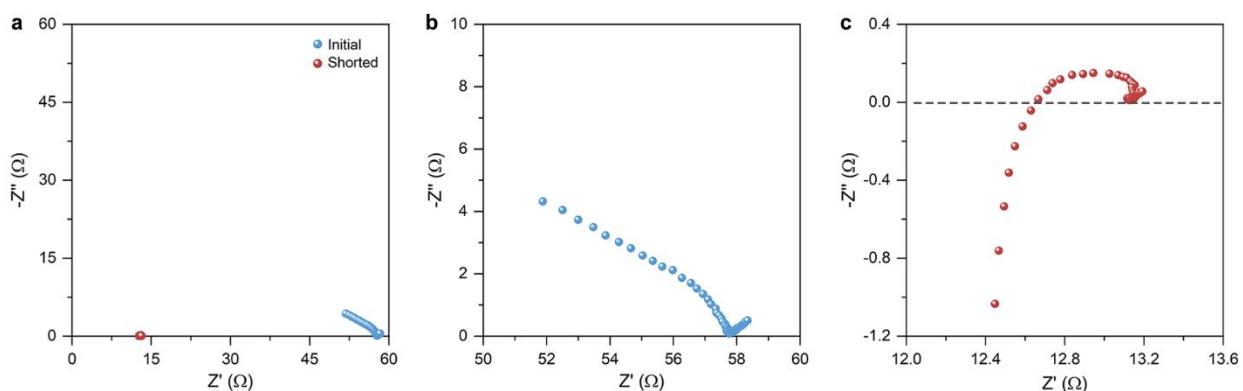
**Figure S1.** X-ray diffraction pattern for pristine  $\text{Li}_6\text{PS}_5\text{Cl}$  powder (blue) and the corresponding ICDD pattern (green).



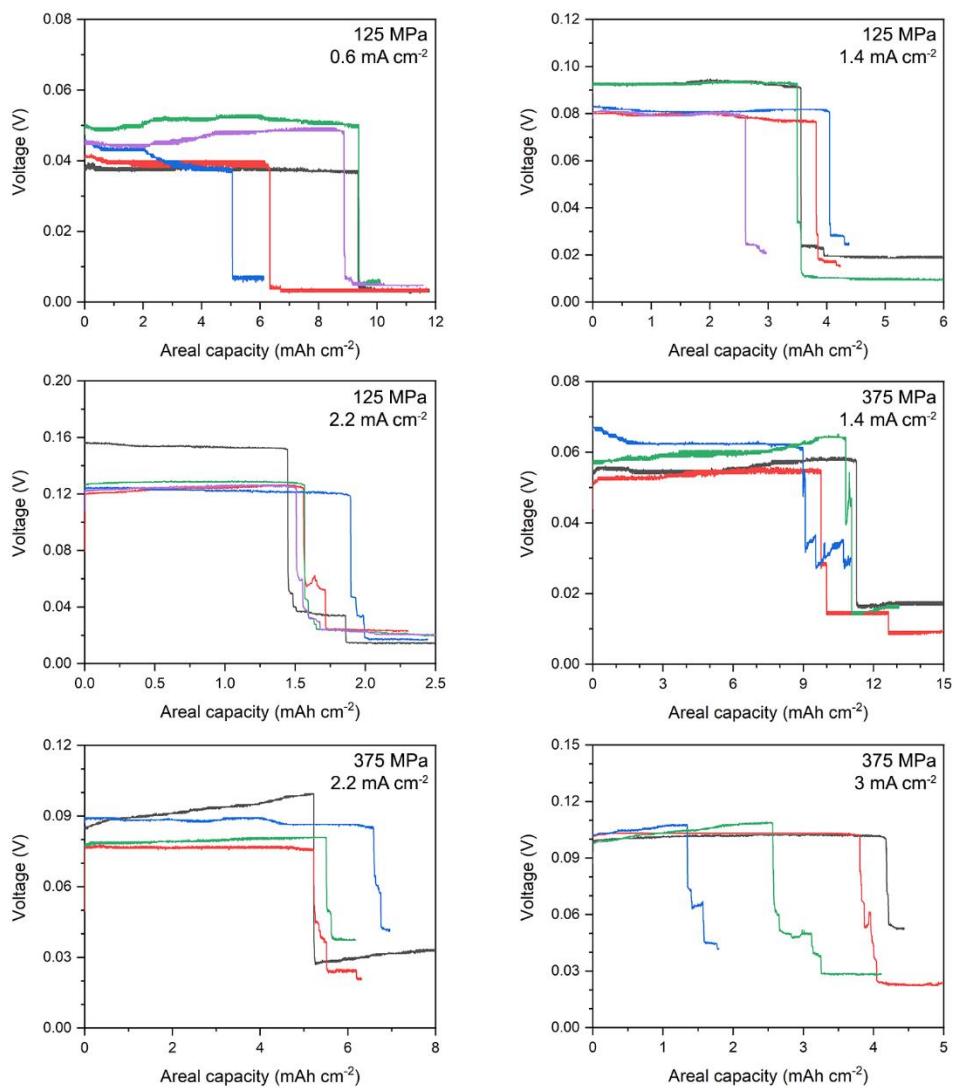
**Figure S2.** Additional critical current density tests of optimized symmetric cells. The testing procedure was the same as for the cell shown in Fig. 1a, and the CCD values for each cell are shown in the plots.



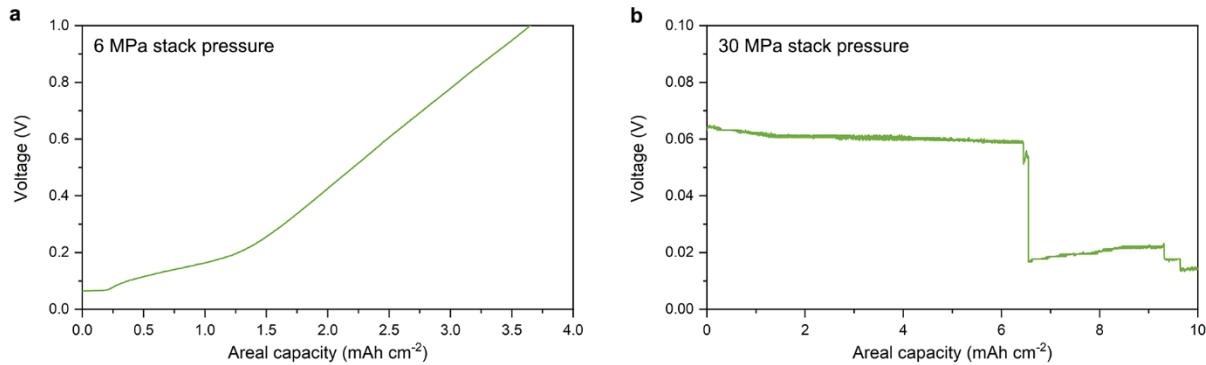
**Figure S3.** Plot of the measured CCD against the areal capacity used for the CCD measurement from the current study (green star) compared to other reports. Red circles represent data points that were collected at elevated temperatures or that featured a modified Li/SSE interface to enhance performance. Black squares represent data for unmodified interfaces at room temperature. For studies where cycle duration was controlled by time (instead of capacity), the areal capacity in this plot was taken from the final cycle where failure occurred. References and more information regarding these data are found in Table S1.



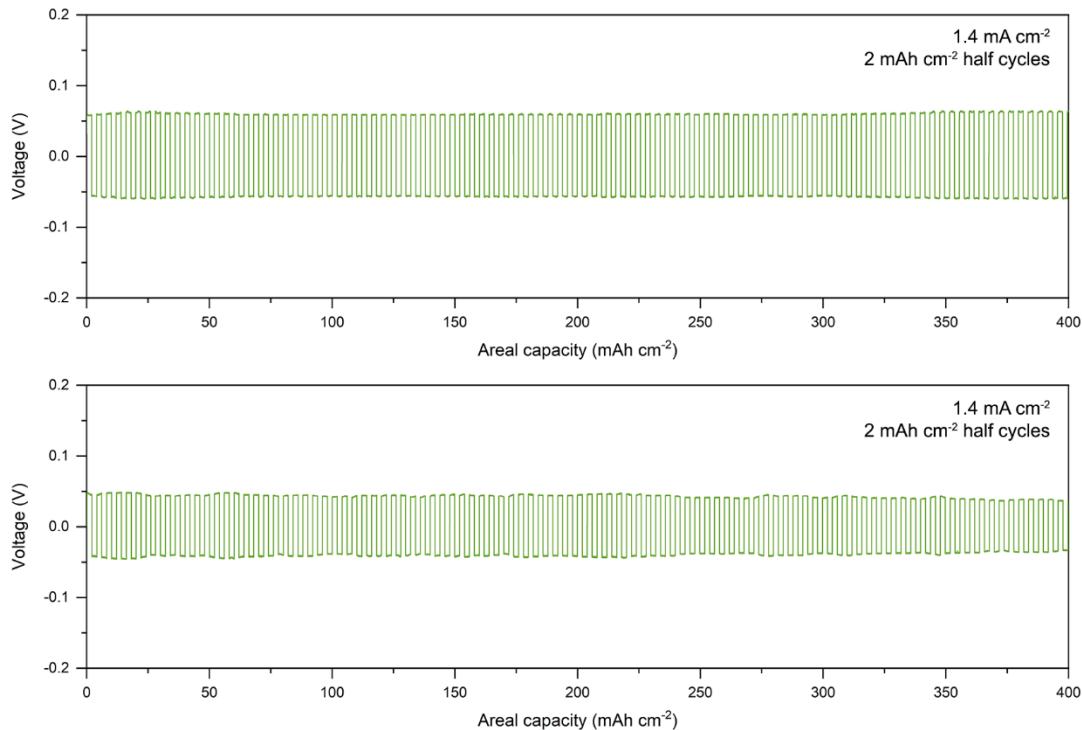
**Figure S4. a)** Electrochemical impedance spectra collected from a symmetric Li/LPSC/Li cell before plating (blue) and after a short circuit formed (red). **b)** Magnified view of the initial impedance spectrum of the cell. **c)** Magnified view of the shorted impedance spectrum.



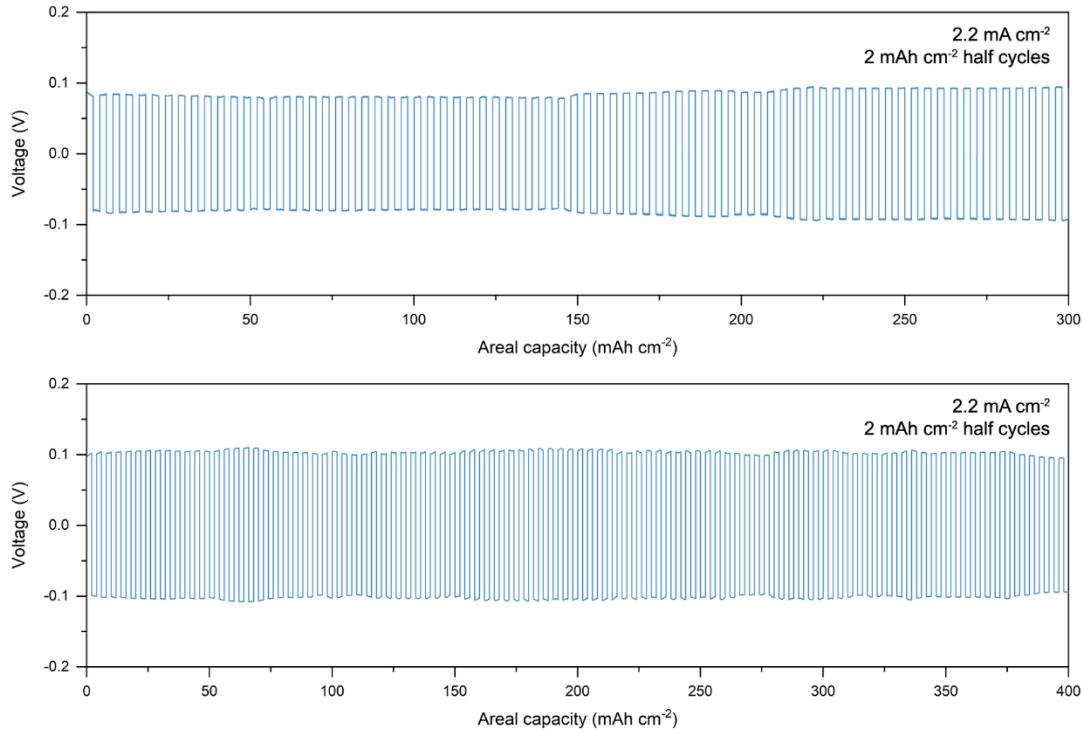
**Figure S5.** Additional data from symmetric Li/LPSC/Li cells plated continuously in one direction until a short circuit occurred. The corresponding electrolyte fabrication pressure and current density are listed in each plot. The stack pressure was 15 MPa for every cell.



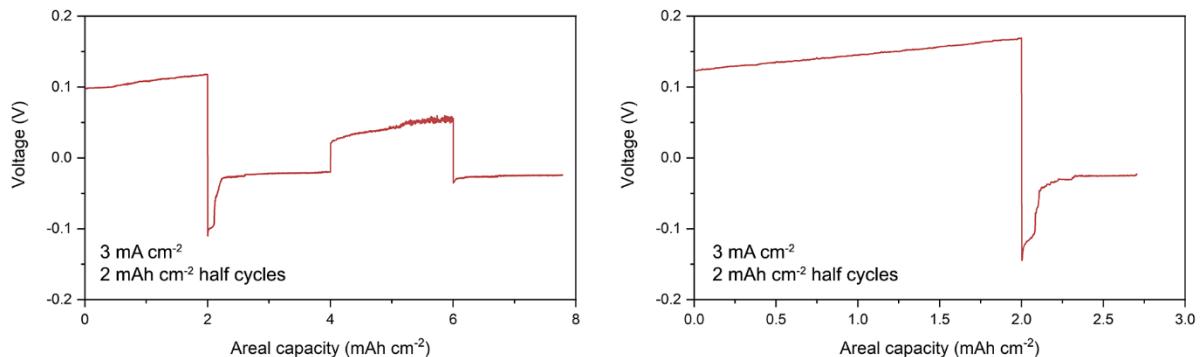
**Figure S6.** Continuous plating at  $1.4 \text{ mA cm}^{-2}$  with an SSE fabrication pressure of 375 MPa and a stack pressure of **a)** 6 MPa and **b)** 30 MPa.



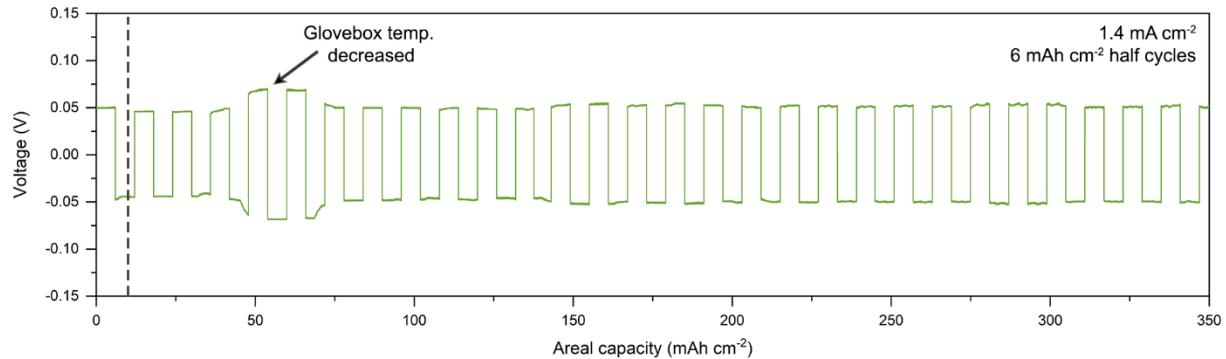
**Figure S7.** Additional symmetric cell data from a cell cycled at  $1.4 \text{ mA cm}^{-2}$  with  $2.0 \text{ mAh cm}^{-2}$  half cycles, as also shown in Fig. 3.



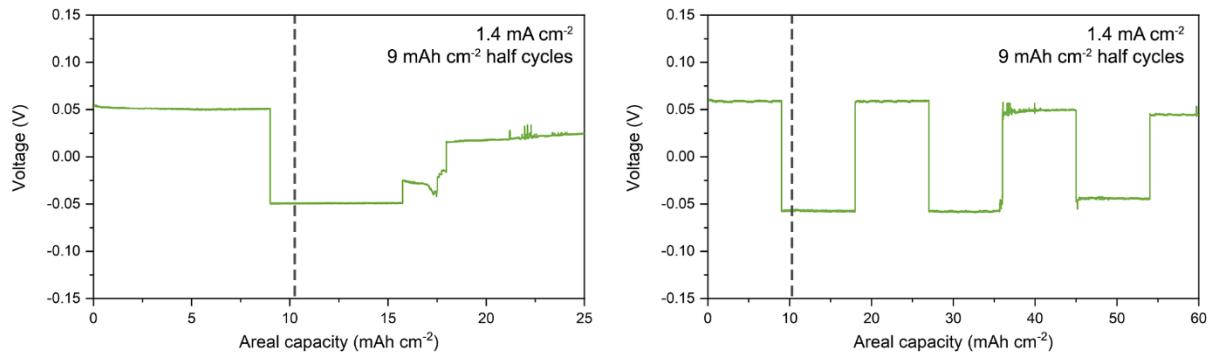
**Figure S8.** Additional symmetric cell data from a cell cycled at  $2.2 \text{ mA cm}^{-2}$  with  $2.0 \text{ mAh cm}^{-2}$  half cycles, as also shown in Fig. 3.



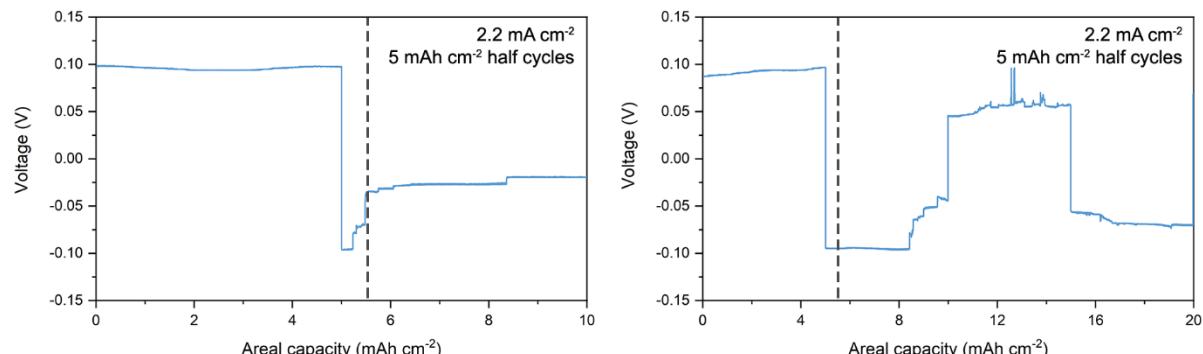
**Figure S9.** Additional symmetric cell data from a cell cycled at  $3.0 \text{ mA cm}^{-2}$  with  $2.0 \text{ mAh cm}^{-2}$  half cycles, as also shown in Fig. 3.



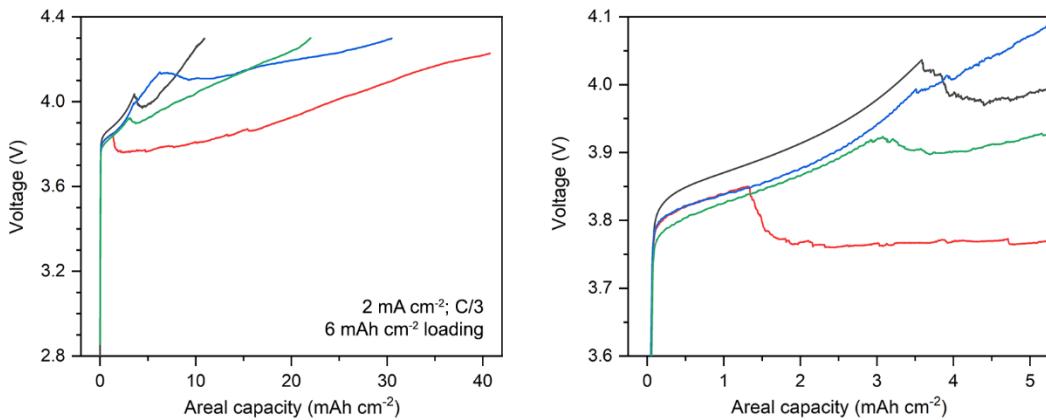
**Figure S10.** Additional symmetric cell data of cycling at  $1.4 \text{ mA cm}^{-2}$  with  $6.0 \text{ mAh cm}^{-2}$  half cycles, as also shown in Fig. 4. The dashed line represents the average threshold capacity measured in Fig. 2. The glove box that housed this cell experienced a temporary decrease in temperature  $\sim 50$  h into the experiment, which corresponds to the brief increase in cell voltage.



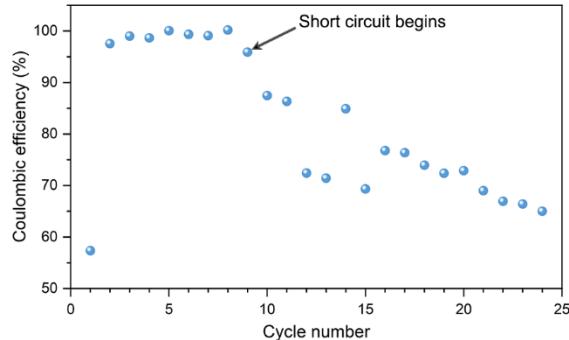
**Figure S11.** Additional symmetric cell data from cells cycled at  $1.4 \text{ mA cm}^{-2}$  with  $9.0 \text{ mAh cm}^{-2}$  half cycles, as also shown in Fig. 4. The dashed lines represent the average threshold capacity measured in Fig. 2.



**Figure S12.** Additional symmetric cell data of cycling at  $2.2 \text{ mA cm}^{-2}$  with  $5.0 \text{ mAh cm}^{-2}$  half cycles, as also shown in Fig. 4. The dashed lines represent the average threshold capacity measured in Fig. 2.



**Figure S13.** Additional full cell data of plating at  $2 \text{ mA cm}^{-2}$  showing the formation of a short circuit during the first charge, as also shown in Fig. 5. A magnified region of the short circuiting behavior is shown in the plot on the right.



**Figure S14.** Coulombic efficiency as a function of cycle number for the full cell with a cathode loading of  $2 \text{ mAh cm}^{-2}$  cycled at  $2 \text{ mA cm}^{-2}$  presented in Fig. 5c.

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