Assignment Embedded Computer Architectures 1

The assignment for the course Embedded Computer Architectures 1 consists of 2 parts. Within both parts, the basic mathematical operation that has to be executed is $(X \cdot Y)+(X+Y)$ where X and Y are matrices and '$\cdot$' and '+' are matrix multiplication and addition respectively. The size of each matrix is 13 x 13 elements where each element is an 8 bit signed number. Multiplications have to be executed completely and overflow has to be dealt with correctly.

Part 1: Performance assessment on an Arduino

Within Part 1, an Arduino is used as a processing platform. For more information and tooling for the Arduino see www.arduino.cc. The goal is to realize the fastest (compared to your fellow student groups) implementation of the mathematical operation on the Arduino processing platform. Measuring time should start after matrix values are loaded in the on-chip memory of the Arduino and must end after results are written back to memory. To assess the performance, repeat the execution of a single operation a large number of times (e.g. 1000 times) and use the Real Time Counter to determine the execution time. Your code will have to run on an Arduino provided by the lecturers (with ATMEGA328P) in order to do a final and fair assessment of the performance. The group which has achieved the best performance will receive a small reward.

The results will have to be presented in week 3. Furthermore, Part 1 has to result in a report which describes the implementation and the way in which the performance is assessed. The report has to be handed in in week 4

Part 2: Performance assessment on an alternative architecture

Within Part 2, two implementations of the mathematical operation have to be realized on an alternative platform. Student groups have to decide themselves what alternative platform to choose and options are an FPGA platform, GPU or multi-core GPP.

In the first implementation, only one hardware element that is executing the multiplications within the matrix-matrix multiplication, is used and the performance of this implementation is assessed for example by measuring the execution time of 1000 matrix-matrix multiplications.

In the second implementation, the available parallelism within the platform should be exploited and the performance of this second implementation should be assessed and compared with the performance of the first implementation.

The results will have to be presented in week 8. Furthermore, Part 2 has to result in a report describing the key specifications of the alternative architecture, the two different implementations and their performance, and an explanation of the performance improvement (if achieved). This report has to be handed in in week 10.

Requirements for the presentations

- 5 minutes presentation only addressing key aspects (note that all other students have become experts in the time being)
- The presentations have to be sent to the lecturers in PDF afterwards.

Requirements for the reports

- The report should be written In English
- It should contain a table of contents
- Pages should be numbered.
- PDF format
- 11 point font
- Part 1: maximum 3 pages
- Part 2: maximum 5 pages

Grading the assignment

The final mark for the assignment will be: 0.3 * grade for part 1 + 0.7 * grade for part 2