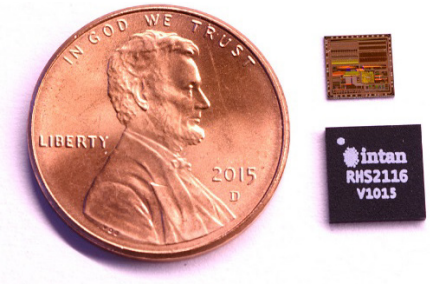
intan TECHNOLOGIES

RHS2116



Digital Electrophysiology Stimulator/Amplifier Chip

20 January 2016; updated 12 December 2018

Features

- Fully integrated electrophysiology interface chip with 16 channels of low-noise amplifiers and constant-current stimulators controlled by industry-standard serial peripheral interface (SPI)
- Stimulators source and sink currents ranging from 10 nA to 2.55 mA over an 18 V range with integrated compliance monitors
- Integrated charge-recovery circuits and fault current detection
- Low input-referred noise: 2.4 μV_{rms} typical
- ADC operation to 714 kSamples per second; supports sampling 16 amplifier channels at 40 kSamples/s each
- Standard four-wire 32-bit SPI interface with CMOS or low-voltage differential signaling (LVDS) I/O pins
- Upper cutoff frequency of all amplifiers set by on-chip registers; adjustable from 100 Hz to 20 kHz
- Lower cutoff frequency of all amplifiers set by on-chip registers; adjustable from 0.1 Hz to 1 kHz
- Fast amplifier artifact recovery for post-stimulus recording
- Integrated multi-frequency *in situ* electrode impedance measurement capability
- Individual amplifier and stimulator power up/down for power minimization

Applications

- Miniaturized multi-channel headstages for neural recording and stimulation
- Low-power wireless headstages or backpacks for electrophysiology experiments
- Multielectrode array (MEA) *in vitro* recording and stimulation systems

Description

The Intan Technologies RHS2116 microchip is a complete bidirectional electrophysiology interface system. This device contains an array of 16 stimulation/amplifier blocks. Each channel includes a low-noise amplifier with programmable bandwidth and a constant-current stimulator with programmable amplitude.

The RHS2116 is suitable for a wide variety of biopotential interfacing applications. Innovative circuit architecture combines stimulators, amplifiers, analog and digital filters, a multiplexed 16-bit analog-to-digital converter (ADC), and a flexible electrode impedance measurement module on a single silicon chip. **In practice, an array of electrodes are connected directly to one side of the chip, and a digital bus on the other side is used to control stimulation and read digitized electrode signals.**

The bandwidths of the amplifiers may be dynamically programmed by means of internal registers on each chip. This flexibility allows the chips to be optimized for different types of signals. Integrated charge-recovery circuits and fast amplifier settling can be employed following stimulation pulses to minimize residual artifacts.

A low-distortion, high-speed analog multiplexer (MUX) allows all the amplifiers to share one on-chip ADC. The ADC can sample each channel up to 44.6 kSamples/s. Additional on-chip circuitry enables *in situ* electrode impedance measurements at user-programmable frequencies. By interfacing electrodes directly with a digital command and data stream, **the RHS2116 replaces all analog instrumentation circuitry** in electrophysiology monitoring and stimulation systems.

RHS2116 chips are packaged in standard 7mm × 7mm QFN surface mount packages, or available in bare die form. The small footprint and low power consumption of the multi-channel chips enable the miniaturization of front end electronics for miniature headstages and other portable biopotential interface systems.

Simplified Chip Diagrams

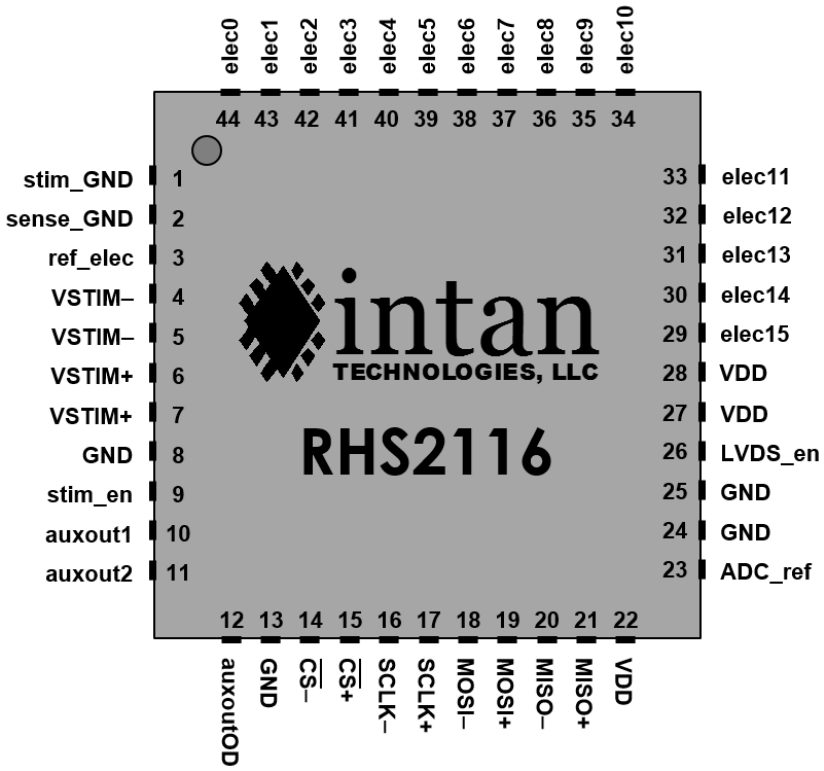
RHS2000-SERIES FAMILY

There is currently one device in the RHS2000-series electrophysiology interface family: the RHS2116, which is described in this datasheet. The following table lists the features of this chip:

DEVICE	AMPLIFIER/STIMULATOR CHANNELS PER CHIP	AMPLIFIER INPUT PINS	PACKAGE SIZE	BARE DIE SIZE
RHS2116	16	16 unipolar amplifier inputs; 1 common reference input	7 mm × 7 mm 44-pin QFN	4.94 mm × 4.74 mm

Package Description

RHS2116: 44-Pin QFN Package

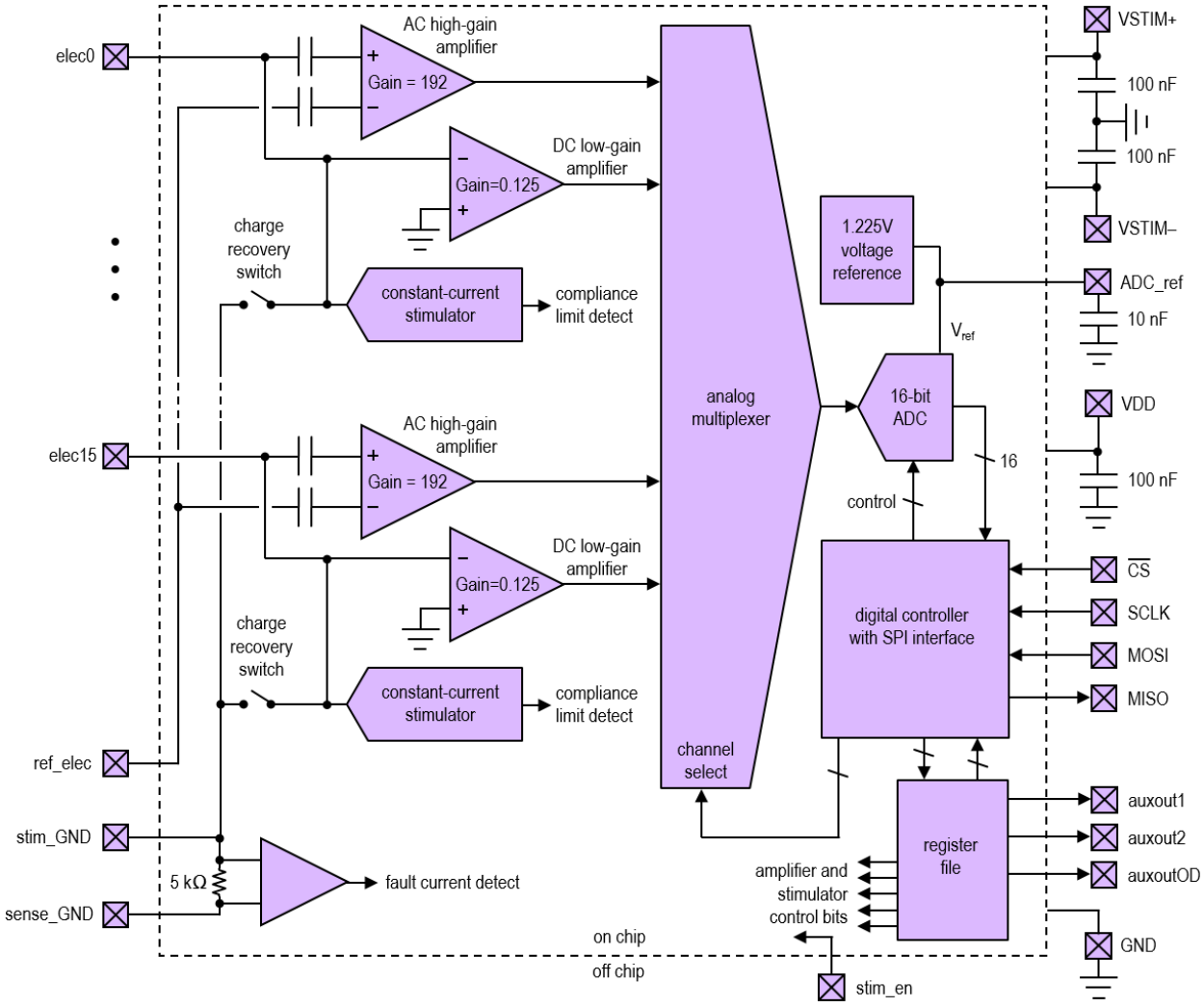


RHS2116 Simplified Diagram

The RHS2116 contains an array of 16 stimulator/amplifier blocks controlled through a digital SPI interface. Each stimulator/amplifier channel includes two amplifiers for sensing electrode voltages: (1) an AC-coupled high-gain amplifier for observing small electrophysiological signals (e.g., extracellular action potentials, local field potentials) in the range of a few microvolts to a few millivolts; and (2) a DC-coupled low-gain amplifier for monitoring electrode potential in response to stimulation, in the range of tens of millivolts to several volts. The high-gain amplifiers are referenced to a common, shared pin (**ref_elec**) that can be connected to a low-impedance reference electrode to reduce common-mode interference (e.g., 50/60 Hz line noise). The low-gain amplifiers are referenced to ground. In many applications, the reference electrode will also be used as the stimulation counter (return) electrode and will be tied to ground.

Each channel has an independent stimulator module that can generate biphasic constant-current pulses with amplitudes varying from 10 nanoamps to 2.55 milliamps. These stimulators are capable of maintaining constant current output over a wide range of electrode voltages, with compliance limits near the stimulation voltage supplies VSTIM+ and VSTIM–. Stimulator modules automatically detect electrode voltages exceeding compliance limits and set corresponding register bits.

Most stimulation protocols use charge-balanced pulses to avoid oxidation-reduction reactions at the electrode-tissue interface. Variations in transistor characteristics across a chip make it impossible to achieve perfect charge balance, so recovery circuits are included to bleed off residual charge after stimulation pulses. A charge recovery switch can be used to briefly connect an electrode to a common **stim_GND** pin, which is typically tied to ground. Other charge recovery circuits in each channel pull the electrodes toward a user-specified potential with small, programmable currents. A global fault current detector is also included on the chip; this circuit can be inserted into a common return current path and used to detect any unintended current.



Pin Descriptions

PIN	TYPE	FUNCTION
VDD, GND	power	3.3V power supply (3.2V – 3.6V). All **VDD** pins must be connected to the same potential. All **GND** pins must be connected to the same ground potential.
VSTIM+, VSTIM–	power	Stimulation power supplies. The total stimulation power supply (**VSTIM+** – **VSTIM–**) may not exceed 18V. **VSTIM+** is limited to the range of +3.3V to +14V with respect to ground. **VSTIM–** is limited to the range of -3.3V to -14V with respect to ground. **Power must be applied to these pins during operation of the chip, otherwise excessive current will be drawn through VDD. Do not leave these unconnected.**
elec0, elec1, …	analog I/O	Electrode I/O pins. Unipolar amplifier inputs and stimulator outputs.
ref_elec	analog input	Amplifier array common reference (negative) input.
stim_GND	analog I/O	Common pin for stimulator charge recovery. Typically tied to **GND**.
sense_GND	analog I/O	Optional pin used for return current sensing and stimulation fault detection.
LVDS_en	digital input	When **LVDS_en** is pulled high, communication with the SPI data bus is conducted using low-voltage differential signaling (LVDS). When **LVDS_en** is pulled low, SPI communication uses traditional CMOS-level signaling.
$\overline{\textbf{CS}}$**+,** $\overline{\textbf{CS}}$**–**	digital LVDS input pair	Active-low chip select input for SPI data bus. The falling edge of this signal is also used to trigger an ADC sample. If **LVDS_en** is pulled low, only $\overline{\textbf{CS}}$**+** is used as a standard CMOS-level input. If **LVDS_en** is pulled high, both pins are used as an LVDS input pair.
SCLK+, SCLK–	digital LVDS input pair	Serial clock input for SPI data bus. The base value of the clock is zero (CPOL = 0). If **LVDS_en** is pulled low, only **SCLK+** is used as a standard CMOS-level input. If **LVDS_en** is pulled high, both pins are used as an LVDS input pair.
MOSI+, MOSI–	digital LVDS input pair	Serial data input ("Master Out, Slave In") for SPI data bus. The RHS2116 chip always acts as slave in an SPI data link. This line is sampled on the rising edge of SCLK. If **LVDS_en** is pulled low, only **MOSI+** is used as a standard CMOS-level input. If **LVDS_en** is pulled high, both pins are used as an LVDS input pair.
MISO+, MISO–	digital LVDS output pair	Serial data output ("Master In, Slave Out") for SPI data bus. The RHS2116 chip always acts as slave in an SPI data link. The value of this line changes in response to a falling edge on SCLK. If **LVDS_en** is pulled low, only **MISO+** is used as a standard CMOS-level output. If **LVDS_en** is pulled high, both pins are used as an LVDS output pair.
auxout1, auxout2	digital outputs	These pins are auxiliary CMOS digital outputs that are controlled or tristated by setting registers on the chip. If not used, these pins should be left unconnected. These pins should never be tied to ground or VDD, as their operation is undefined at power-up.
auxoutOD	open-drain high-voltage digital output	This pin is an auxiliary open-drain digital output that is controlled by setting a register on the chip. When the pin is activated, it pulls current to VSTIM–. This pin can tolerate voltage levels ranging from VSTIM– to VSTIM+.
stim_en	digital input	If this pin is pulled low (to ground), all on-chip stimulators are disabled. To enable stimulation, **stim_en** should be pulled high (to VDD).
ADC_ref	analog output	An external 10 nF ceramic capacitor to ground must be connected to this pin, and placed in close proximity to the chip to stabilize the on-chip voltage reference generator used by the ADC. A voltage of approximately 1.225V will appear on this pin during operation. See the "Analog-to-Digital Converter" section for more information.

Electrical Characteristics

T_A = 25ºC, VDD = 3.3V, VSTIM± = ±9V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNITS	COMMENTS
VDD	Supply Voltage		3.2 – 3.6	V	Recommended nominal supply voltage is 3.3V.
VSTIM+	Positive Stimulator Supply Voltage	Total stimulator supply (VSTIM+ – VSTIM–) cannot exceed 18 V.	+3.3 +14	V V	Minimum Maximum
VSTIM–	Negative Stimulator Supply Voltage	Total stimulator supply (VSTIM+ – VSTIM–) cannot exceed 18 V.	-3.3 -14	V V	Maximum Minimum
$Z_{diginCMOS}$	CMOS Digital Input Impedance	**LVDS_en** = 0	5	pF	
$Z_{diginLVDS}$	LVDS Digital Input Impedance	**LVDS_en** = 1	150	kΩ	LVDS inputs are weakly pulled to VDD if unconnected. User must add 100 Ω termination.
V_{inLO}	CMOS Digital "Low" Input Voltage	For all non-LVDS digital inputs to chip	-0.4 – +0.7	V	Nominal "low" input voltage is GND (0 V).
V_{inHI}	CMOS Digital "High" Input Voltage	For all non-LVDS digital inputs to chip	2.4 – 3.6	V	5V signals should never be applied directly to the chips.
$V_{inLVDS-CM}$	LVDS Input Common-Mode Voltage		1.0 – 1.5	V	Suggested common-mode level is 1.25 V.
$V_{inLVDS-D}$	LVDS Input Differential Voltage		±250 – ±500	mV	Suggested differential voltage is ±350 mV.
$V_{outLVDS-CM}$	LVDS Output Common-Mode Voltage		1.25	V	Typical
$V_{outLVDS-D}$	LVDS Output Differential Voltage	With 100 Ω termination	±350	mV	Typical
A_D	AC High-Gain Amplifier Differential Gain	In midband region between f_L and f_H	192 45.7	V/V dB	This gain yields an ADC step size (V_{LSB}) of 0.195 µV, referred to the electrode.
A_0	AC High-Gain Amplifier DC Differential Gain		0	V/V	Complete DC rejection, unlike amplifiers that have A_0 = 1 V/V.
A_{DC}	DC Low-Gain Amplifier Gain		-0.125 -18.1	V/V dB	Note: DC amplifier gain is negative.
V_{DCamp}	DC Low-Gain Amplifier Input Voltage Range	VSTIM+ = +9V VSTIM– = -9V	-7.8 – +8.4	V	Values beyond this range are subject to nonlinearity/clipping.
V_{LSB}	Voltage Step Size of ADC (Least Significant Bit)	referred to AC high-gain amplifier input (16 bit resolution) referred to DC low-gain amplifier input (10 bit resolution)	0.195 19.23	µV mV	
f_L	AC High-Gain Amplifier Low-Frequency 3-dB Cutoff Frequency (High-Pass Filter)		0.1 – 1000	Hz	1-pole roll-off below f_L. Bandwidth selection registers have range of 0.1 Hz- 1000 Hz.

Electrical Characteristics

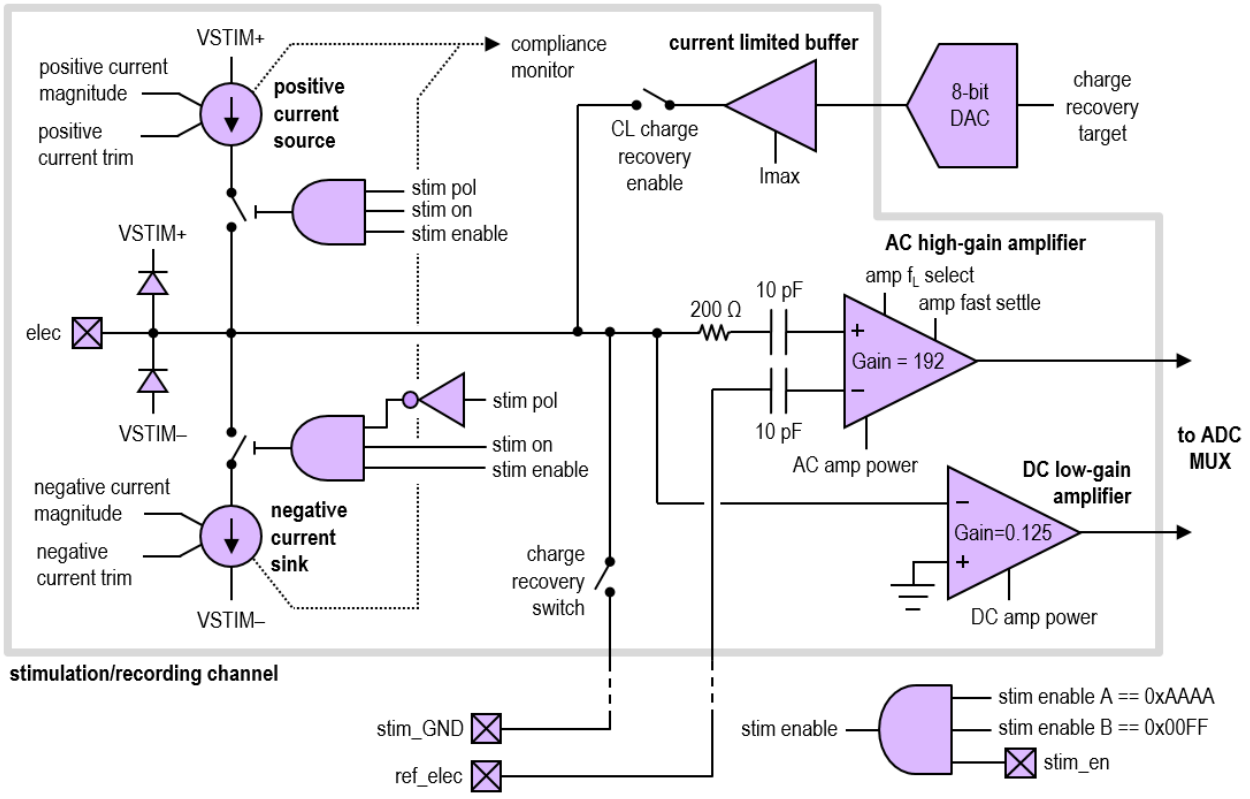
T_A = 25ºC, VDD = 3.3V, VSTIM± = ±9V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNITS	COMMENTS
f_H	AC High-Gain Amplifier High-Frequency 3-dB Cutoff Frequency (Low-Pass Filter)		100 – 20000	Hz	3-pole 3rd-order Butterworth filter roll-off above f_H. Bandwidth selection registers have range of 100 Hz- 20 kHz.
$V_{ACamp-AC}$	AC High-Gain Amplifier AC Input Voltage Range		±5.0	mV	Values beyond this range are subject to nonlinearity/clipping.
$V_{ACamp-DC}$	AC High-Gain Amplifier Input Voltage Allowable DC Offset	Limited by ESD diodes	VSTIM– VSTIM+	V V	Minimum Maximum
V_{OS}	AC High-Gain Amplifier Input-Referred Offset Voltage	DSP offset removal filter disabled	< ±100	µV	Output offset varies by 192x this value (i.e., ±19.2 mV).
CMRR	AC High-Gain Amplifier Common Mode Rejection Ratio	f = 50 or 60 Hz f = 1 kHz	82 82	dB dB	Typical
PSRR	AC High-Gain Amplifier Power Supply Rejection Ratio	f = 50 or 60 Hz f = 1 kHz	75 75	dB dB	Typical
	AC High-Gain Amplifier Crosstalk	f = 0.1 Hz to 10 kHz	–68	dB	Typical; measured between adjacent amplifiers on chip.
I_b	Electrode Pin Bias Current (Stimulator Off)	V_{elec} > VSTIM– V_{elec} < VSTIM+	< 1	nA	Individual **elecX** pin
I_{bREF}	Amplifier Reference Input Bias Current	V_{REF} > VSTIM– V_{REF} < VSTIM+	< 1	nA	Common amplifier reference (**ref_elec** pin)
C_{in}	Electrode Pin Input Capacitance		10	pF	Individual **elecX** pin
C_{inREF}	Amplifier Reference Input Capacitance		91	pF	Common amplifier reference (**ref_elec** pin)
$\|Z_{in}\|$	Electrode Pin Input Impedance	f = 10 Hz f = 1 kHz	1600 16	MΩ MΩ	Individual **elecX** pin
$\|Z_{inREF}\|$	Amplifier Reference Input Impedance	f = 10 Hz f = 1 kHz	170 1.7	MΩ MΩ	Common amplifier reference (**ref_elec** pin)
v_{ni}	AC High-Gain Amplifier Input-Referred Noise		2.4	μV_{rms}	Typical. Varies slightly (< 15%) with amplifier bandwidth.
THD	AC High-Gain Amplifier Total Harmonic Distortion (with f_L = 0.1 Hz, f_H = 10 kHz)	f = 1 kHz V_{IN} = 4 mV_{P-P} V_{IN} = 10 mV_{P-P}	 0.1 < 0.8	 % %	Includes any nonlinearity in MUX. Distortion may increase near f_L and f_H.
f_{MUX}	Maximum ADC MUX Switching Frequency		714	kHz	16 amplifiers can be sampled up to 44.6 kSamples/s each.
I_{STIM}	Stimulation Current	When stimulator is turned on	10 2.55	nA mA	Minimum magnitude Maximum magnitude
$I_{STIM-step}$	Stimulation Current Step Size	LSB of 8-bit current-output DAC	10 10	nA µA	Minimum magnitude Maximum magnitude

Electrical Characteristics

T_A = 25ºC, VDD = 3.3V, VSTIM± = ±9V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNITS	COMMENTS
	Size of Packaged RHS2116		7.0 × 7.0	mm^2	44-pin plastic QFN package (0.80 mm thick)
	Mass of Packaged RHS2116		133	mg	
	Size of RHS2116 Bare Die		4.94 × 4.74	mm^2	Bare silicon die (0.20 mm thick)
	Mass of RHS2116 Bare Die		11	mg	



Stimulator/Amplifier Block

At the core of the RHS2116 chip is an array of 16 stimulator/amplifier blocks containing the circuitry modules illustrated in the diagram above. These modules perform three basic functions: (1) monitoring the AC and DC voltage on each electrode; (2) delivering constant-current stimulation pulses to the same electrode; and (3) recovering residual charge from the electrode following stimulation pulses. The circuits responsible for these tasks are listed here and described in more detail in the following pages.

AC-Coupled High-Gain Amplifier

Each channel has a high-gain amplifier with a band-pass response that senses electrophysiological signals (e.g., extracellular neural action potentials, local field potentials, electrocorticogram signals) within a range of ±5 mV and a typical noise floor of 2.4 µVrms. The upper and lower cutoff frequencies of these amplifiers can be selected by registers. Two different mechanisms are provided for recovering quickly from large voltage artifacts caused by stimulation pulses. Unused amplifiers may be disabled to reduce power consumption. These amplifiers are sampled at 16-bit resolution by the on-chip ADC.

The high-gain amplifiers are referenced to a common, shared pin (**ref_elec**) that can be connected to a low-impedance reference electrode to reduce common-mode interference (e.g., 50/60 Hz line noise).

DC-Coupled Low-Gain Amplifier

A second DC-coupled amplifier with a wide range (from VSTIM– + 1.2V to VSTIM+ – 0.6V) can be used to monitor electrode potentials in response to stimulation pulses (e.g., to ensure that electrodes remain inside the "water window" to prevent chemical reactions from occurring). Unused amplifiers may be disabled to reduce power consumption. These amplifiers are sampled at 10-bit resolution by the on-chip ADC.

Stimulator Current Source and Sink

Constant-current stimulation can be delivered using an integrated current source and current sink. These circuits produce currents with user-specified magnitudes in the range of 10 nA to 2.55 mA. Each current source and sink is controlled by an 8-bit current-output DAC which has an 8-bit "trim" setting that can adjust the current by ±28% to compensate for variations between devices. The step size of the current-output DACs is set globally. Each stimulator has a built-in compliance monitor that sets a register bit if the electrode voltage becomes so high or low (i.e., close to VSTIM+ or VSTIM–) that it becomes impossible to deliver the specified current.

All stimulators are disabled until the **stim_en** pin is pulled to VDD and a specific 32-bit code is programmed into the **stim enable** registers. This prevents random stimulation from occurring when the chip is first powered up.

Charge Recovery Switch

Most stimulation protocols use charge-balanced pulses to avoid oxidation-reduction reactions at the electrode-tissue interface. Variations in transistor characteristics across a chip make it impossible to achieve perfect charge balance, so recovery circuits are included to bleed off residual charge after stimulation pulses. Each stimulator/amplifier block includes a charge recovery switch which can be used to briefly connect an electrode to a common **stim_GND** pin, which is typically tied to ground. This switch has an 'on' resistance on the order of 1 kΩ.

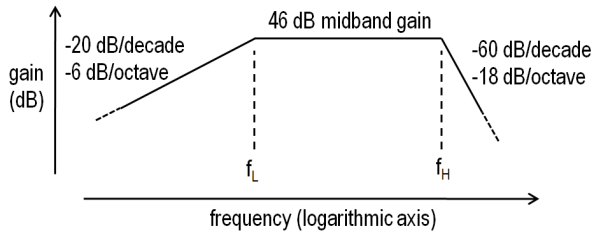
Current-Limited Charge Recovery Circuit

An alternate charge recovery circuit is included in each stimulator/amplifier block. The current-limited (CL) charge recovery circuit pulls the electrode toward a user-specified voltage with a small, programmable current ranging from 1 nA to 1 μA. The target recovery voltage may be set in the range of ±1.22V. Some stimulation protocols initially hold the electrode at a slightly positive potential when using biphasic pulses that begin with a cathodic (negative) current. This issue is discussed in greater depth below.

AC Amplifier Bandwidth

Electrophysiological signals of interest are sensed by an array of AC-coupled low-noise amplifiers with integrated analog filters that can be configured to isolate frequencies of interest and minimize aliasing by attenuating signals above the Nyquist rate (i.e., half the ADC per-channel sampling rate). Each AC high-gain amplifier has a pass band extending from a low-frequency cutoff f_L to a high-frequency cutoff f_H. The upper end of the pass band has a 3rd-order Butterworth low-pass filter at the 3-dB frequency f_H. The lower end of the pass band has a 1st-order high-pass filter characteristic at the 3-dB frequency f_L.

The 3rd-order Butterworth low-pass filter characteristic at f_H has a maximally flat pass band region with -60 dB/decade (-18 dB/octave) of attenuation beyond f_H. The diagram below illustrates the analog frequency response of the AC high-gain amplifiers:



An additional pole of high-pass filtering can be applied using the optional DSP filter module described later in the datasheet.

Setting Amplifier Bandwidth

Registers 4 and 5 are used to set the upper bandwidth of the high-gain amplifiers (f_H) in the range of 100 Hz to 20 kHz. Registers 6 and 7 are used to set the lower bandwidth of the high-gain amplifiers (f_L) in the range of 0.1 Hz to 1 kHz. Register values for common bandwidths are listed in a table on page 11. For bandwidths not listed on this table, contact Intan Technologies for recommended values.

Amplifier Stimulus Artifact Recovery

If an AC-coupled amplifier is subjected to a large voltage pulse (like the artifacts created by stimulation pulses) the amplifier responds with a large step in its output (which may saturate the amplifier) that decays exponentially back to baseline with a time constant equal to $1/(2\pi f_L)$. If the amplifier saturates in response to a stimulation pulse, it is effectively blind until its output decays back into its operating range.

In many situations it is desirable to set f_L quite low to observe low-frequency signals of interest (e.g., local field potentials or electrocorticograms). However, a low value of f_L implies long recovery time from stimulation artifacts: with f_L set to 0.1 Hz, the amplifier recovery time constant is 1.6 seconds! Yet it is often necessary to observe neural activity a few milliseconds following stimulation.

The RHS2116 provides two mechanisms for reducing the time required to recovery from a stimulation artifact: low-frequency cutoff shifting and amplifier fast settle.

Low-Frequency Cutoff Shifting

The RHS2116 provides a means to select two different values of f_L (an "A version" and a "B version") and rapidly switch between them to speed up amplifier recovery following stimulation. Registers 6 and 7 select the two value of f_L (e.g., 5 Hz for normal recording and 500 Hz for post-stimulation recovery) and the **amp fL select** variable in Register 12 selects which value of f_L is used for each amplifier channel.

Amplifier Fast Settle

It may also be useful to reset the amplifiers if a large stimulation artifact causes the output signals to saturate. The "fast settle" function built into each high-gain amplifier allows users to clamp the output of the amplifier at baseline. To settle the amplifiers, the **amp fast settle** bit in Register 10 should be set high momentarily and then returned to zero. The recommended duration of a fast settle pulse is $2.5/f_H$; as the upper bandwidth of the amplifiers is lowered, settling takes more time. Using this guideline, if f_H

is set to 10 kHz then setting **amp fast settle** high for 250 µs, and then low, is sufficient to settle the amplifiers to baseline.

Depending on the nature and severity of the stimulation artifacts encountered, either or both of these artifact recovery techniques may be used to optimize amplifier performance.

Recommended Artifact Recovery Procedure

In benchtop testing at Intan Technologies, we found the following procedure to be effective in recovering from artifacts within 1-2 ms following a stimulation pulse delivered to a simple series RC model of an electrode:

- Set the "A version" of f_L to the desired lower cutoff frequency for recording (e.g., 5 Hz) (Register 6).
- Set the "B version" of f_L to a much higher frequency in the range of 500 to 1000 Hz (Register 7).
- Immediately before the onset of a stimulation pulse on channel X, switch the low-frequency cutoff on channel X from the "A version" of f_L to the "B version" of f_L (Register 12)
- After the stimulation pulse has ended, wait 1 ms before switching back to the "A version" of f_L (Register 12)
- It may be necessary to disable the DSP high-pass filter for offset removal to optimize the recovery speed (Register 1).

The optimum technique for artifact recovery may depend on the particular type of electrode used. Some experimentation may be necessary to find the best parameters for a given situation.

In general, artifact recovery time will shorten with higher values of f_L and higher values of the DSP high-pass filter cutoff frequency. Consider using the highest acceptable lower bandwidth in any particular recording application.

Setting Upper Bandwidth: Register Values

The following settings for variables in Registers 4 and 5 are used to configure the upper bandwidth (f_H) of the amplifiers. These settings are identical to the ones used by the RHD2000 series of amplifier chips from Intan Technologies.

UPPER BANDWIDTH f_H	RH1 sel1	RH1 sel2	RH2 sel1	RH2 sel2
20 kHz	8	0	4	0
15 kHz	11	0	8	0
10 kHz	17	0	16	0
7.5 kHz	22	0	23	0
5.0 kHz	33	0	37	0
3.0 kHz	3	1	13	1
2.5 kHz	13	1	25	1
2.0 kHz	27	1	44	1
1.5 kHz	1	2	23	2
1.0 kHz	46	2	30	3
750 Hz	41	3	36	4
500 Hz	30	5	43	6
300 Hz	6	9	2	11
250 Hz	42	10	5	13
200 Hz	24	13	7	16
150 Hz	44	17	8	21
100 Hz	38	26	5	31

Setting Lower Bandwidth: Register Values

The following settings for variables in Registers 6 and 7 are used to configure the lower bandwidth (f_L) of the amplifiers. These settings are identical to the ones used by the RHD2000 series of amplifier chips from Intan Technologies.

LOWER BANDWIDTH f_L	RL sel1	RL sel2	RL sel3
1.0 kHz	10	0	0
500 Hz	13	0	0
300 Hz	15	0	0
250 Hz	17	0	0
200 Hz	18	0	0
150 Hz	21	0	0
100 Hz	25	0	0
75 Hz	28	0	0
50 Hz	34	0	0
30 Hz	44	0	0
25 Hz	48	0	0
20 Hz	54	0	0
15 Hz	62	0	0
10 Hz	5	1	0
7.5 Hz	18	1	0
5.0 Hz	40	1	0
3.0 Hz	20	2	0
2.5 Hz	42	2	0
2.0 Hz	8	3	0
1.5 Hz	9	4	0
1.0 Hz	44	6	0
0.75 Hz	49	9	0
0.50 Hz	35	17	0
0.30 Hz	1	40	0
0.25 Hz	56	54	0
0.10 Hz	16	60	1

Constant-Current Stimulator

Each stimulator/amplifier block in the RHS2116 includes a constant-current stimulator capable of driving positive or negative currents ranging in magnitude from 10 nA to 2.55 mA. Each stimulator has an 8-bit current-output DAC with an 8-bit trim setting that can adjust the DAC over the range of ±28%. The step size of these DACs is set globally by the **step DAC** variables in Register 34.

The following **step DAC** settings are used to configure the step size of the stimulators. For values not listed on this table, contact Intan Technologies for recommended values.

STIMULATOR STEP SIZE	FULL SCALE RANGE	sel1	sel2	sel3
10 nA	±2.55 µA	64	19	3
20 nA	±5.10 µA	40	40	1
50 nA	±12.75 µA	64	40	0
100 nA	±25.5 µA	30	20	0
200 nA	±51.0 µA	25	10	0
500 nA	±127.5 µA	101	3	0
1 µA	±255 µA	98	1	0
2 µA	±510 µA	94	0	0
5 µA	±1.275 mA	38	0	0
10 µA	±2.55 mA	15	0	0

Note: Stimulation currents exceeding ±2.55 mA are possible if multiple channels are tied together off-chip and stimulation pulses on these channels are coordinated.

Once a stimulator step size has been selected, the **stim Pbias** and **stim Nbias** variables in Register 35 should be set to optimize the compliance range of the current drivers. The following settings should be used.

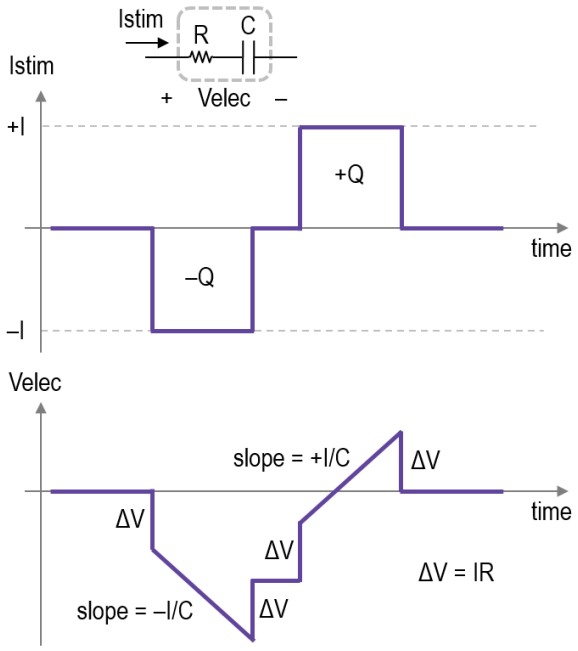
STIMULATOR STEP SIZE	STIMULATOR FULL SCALE RANGE	STIM PBIAS	STIM NBIAS
10 nA	±2.55 µA	6	6
20 nA	±5.10 µA	7	7
50 nA	±12.75 µA	7	7
100 nA	±25.5 µA	7	7
200 nA	±51.0 µA	8	8
500 nA	±127.5 µA	9	9
1 µA	±255 µA	10	10
2 µA	±510 µA	11	11
5 µA	±1.275 mA	14	14
10 µA	±2.55 mA	15	15

Once a global stimulator step size has been configured, the positive and negative stimulation magnitudes can be set in Registers 64-79 and 96-111. Then, stimulation currents are easily turned on and off, and polarities selected, with the 32 bits in Registers 42 and 44.

Note that all of these stimulation controls are in **triggered registers**, which means many of them can be updated using WRITE commands but their new contents are stored in internal buffers. The new values only take effect when an SPI command is issued with the U flag set. At this time, **all** triggered registers on the chip update to their new values simultaneously. This mechanism allows complex stimulation patterns to be choreographed and executed with precision timing.

Note that there are no timers on the RHS2116 to control the duration of stimulation pulses. All timing is controlled explicitly through sequences of SPI commands. To generate a biphasic current pulse a stimulator must first be set to a negative polarity (for example) and turned on, then set to a positive polarity, and then turned off, each with separate SPI commands. The timing of the commands determines the duration of the stimulation pulses, so the host that is dispatching commands must observe a regimented timing structure.

A typical biphasic current pulse is shown in the diagram below, along with a simplified series RC model of an electrode. The positive and negative currents can be of different magnitudes, but in this case the pulse durations are typically adjusted to maintain a constant area under the positive and negative curves, which corresponds to the total charge delivered.



The resulting electrode voltage is shown in the lower half of the figure. The onset of a stimulation pulse causes a quick voltage drop ΔV across the electrode equal to IR. The capacitive component of the electrode then begins charging towards a negative voltage with a constant rate of –I/C. When the current stops, the IR drop goes away. The positive stimulation current pulse produces the same voltage changes in the opposite direction.

If charge balance is maintained (and if the electrode behaves linearly) the electrode voltage should end where it started. The DC low-gain amplifiers on the RHS2116 may be employed to track this voltage following stimulation pulses. If a consistent positive or negative drift is observed, the trim settings in particular stimulation current drivers can be adjusted to compensate for inherent biases and maintain charge balance.

Note that the plot of electrode voltage on the previous page is asymmetric with respect to voltage: because the stimulation started with a negative current pulse in this example, the electrode voltage excursion is primarily in the negative direction. That is, $|V_{elec\text{-}min}| > |V_{elec\text{-}max}|$. In this case, voltage compliance problems or "water window" concerns will be skewed towards the negative voltage supply VSTIM– or the negative end of the water window.

To balance electrode voltages in the middle of the water window or voltage compliance range, the current-limited recovery circuit can be used to bias the resting potential of the electrode to small positive voltages (that stay within the water window) and make the electrode voltage excursions more symmetric with respect to ground. Alternatively, an asymmetric stimulation voltage supply may be used (e.g., VSTIM+ = +6V; VSTIM– = -12V).

Compliance Monitor

Each stimulator has a built-in compliance monitor that sets a bit in Register 40 if the electrode voltage becomes so high or low (i.e., close to VSTIM+ or VSTIM–) that it becomes impossible to deliver the specified current. Register 40 is a read-only register containing compliance monitor bits from all 16 channels, but its value can be reset to zero by issuing an SPI command with the M flag asserted. Typically this register should be cleared prior to stimulation and checked periodically during or after stimulation to detect voltage compliance problems.

If a particular channel consistently exceeds the compliance limit, there are several potential remedies:

(1) Reduce the magnitude of the stimulation currents.

(2) Reduce the duration of stimulation pulses.

(3) Increase the stimulation voltage supplies. Although the total stimulation supply is limited to 18V (e.g., VSTIM+ = +9V, VSTIM– = -9V), it may be better to use asymmetric supplies (e.g., VSTIM+ = +6V, VSTIM– = -12V) to accommodate particular stimulation protocols (e.g., negative currents first).

(4) Use lower-impedance electrodes.

(5) Use the current-limited charge recovery circuits to set a resting potential within the water window but opposite the direction of the electrode voltage excursion during stimulation (see discussion in the previous section).

Charge Recovery Switch

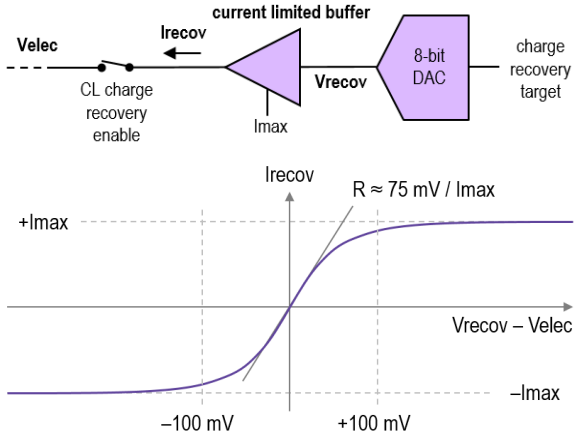
Most stimulation protocols use charge-balanced pulses to avoid oxidation-reduction reactions at the electrode-tissue interface. Variations in transistor characteristics across a chip make it impossible to achieve perfect charge balance, so recovery circuits are included to bleed off residual charge after stimulation pulses. Each stimulator/amplifier block includes a charge recovery switch which can be used to briefly connect an electrode to a common **stim_GND** pin, which is typically tied to ground. Register 46 controls these switches for all 16 channels.

The 'on' resistance of this switch is on the order of 1 kΩ but varies with stimulation supply voltages. The following table lists the typical on resistance of the charge recovery switch as a function of the stimulation supply voltages VSTIM+ and VSTIM–.

VSTIM+	VSTIM–	Ron
+9 V	–9 V	570 Ω
+6 V	–6 V	770 Ω
+3.3 V	–3.3 V	1500 Ω
+12 V	–6 V	450 Ω
+6 V	–12 V	1200 Ω

Current-Limited Charge Recovery Circuit

An alternate charge recovery circuit is included in each stimulator/amplifier block. The current-limited (CL) charge recovery circuit, illustrated in the diagram below, pulls the electrode toward a user-specified voltage with a small, programmable current **Imax** ranging from 1 nA to 1 µA (set in Register 37). The target recovery voltage **Vrecov** may be set in the range of ±1.22V with the **charge recovery DAC** variable in Register 36. The target recovery voltage and current limit are set globally for all channels.



The graph above shows the current driven by the current-limited buffer as the electrode voltage **Velec** differs from the target recovery voltage **Vrecov**. For voltages differences greater than about ±100 mV, the buffer supplies a constant current **Imax** that weakly drives the electrode toward the target recovery voltage.

The table to the right lists settings for variables in Register 37 are used to configure the current limit **Imax** of the buffer.

For voltages differences smaller than ±100 mV, the buffer acts like a resistor with a resistance of approximately 75 mV / Imax.

Some stimulation protocols initially hold the electrode at a slightly positive potential when using biphasic pulses that begin with a cathodic (negative) current. This issue is discussed in greater depth at the end of the "Constant-Current Stimulator" section.

RECOVERY CURRENT LIMIT	EQUIVALENT RESISTANCE FOR SMALL ΔV	sel1	sel2	sel3
1 nA	75 MΩ	0	30	2
2 nA	38 MΩ	0	15	1
5 nA	15 MΩ	0	31	0
10 nA	7.5 MΩ	50	15	0
20 nA	3.8 MΩ	78	7	0
50 nA	1.5 MΩ	22	3	0
100 nA	750 kΩ	56	1	0
200 nA	380 kΩ	71	0	0
500 nA	150 kΩ	26	0	0
1 µA	75 kΩ	9	0	0

Supply Voltage Levels

RHS2116 chips require a regulated voltage supply (VDD) between 3.2V and 3.6V for operation meeting all performance specifications. A nominal supply voltage of 3.3V is recommended for most applications. All **VDD** pins should be kept at identical potentials.

An additional bipolar power supply VSTIM is required for the constant-current stimulators on the chip. The **VSTIM+** pins must be tied to a voltage within the range of +3.3V to +14V. The **VSTIM–** pins must be tied to a voltage within the range of -3.3V to -14V. It is not necessary to use symmetric supplies (i.e., |VSTIM–| does not have to equal VSTIM+), but the total stimulation voltage supply cannot exceed 18V: (VSTIM+ – VSTIM–) ≤ 18V.

All **GND** pins must be kept at the same potential, and the DC level of tissue connected to the amplifier inputs and reference should be kept at this same ground potential.

Power Supply Decoupling Capacitors

A ceramic 100 nF (0.1 µF) power supply bypass capacitor should be connected between **VDD** and **GND** pins, and should be located less than 1 cm from the bottom side of the chip (near pins 13 and 22) on the printed circuit board. This capacitor should have an X5R or X7R dielectric, should be no smaller than a 0402 SMD device, and should be rated for at least 16V. (While the capacitor will only be exposed to 3.3V, small SMD capacitors are known to dramatically decrease in capacitance as the voltage across the device approaches the maximum rated voltage. It is best to use a capacitor with a voltage rating several times higher than the expected voltage.)

If LVDS signaling is used, a single 100 nF capacitor near the bottom edge of the chip is sufficient to smooth the power supply for the RHS2116. If standard CMOS signaling is used, an **additional** 100 nF capacitor should be placed within 1 cm of the right side of the chip (near pins 24-28).

Ceramic 100 nF (0.1 µF) power supply bypass capacitors should be connected between **VSTIM+** and **GND** pins, and between **VSTIM–** and **GND** pins near the left side of the chip (near pins 4-8). These capacitors should have an X5R or X7R dielectric, should be no smaller than a 0402 SMD device, and should be rated for at least 25V.

Analog-to-Digital Converter

The RHS2116 contains a 16-bit successive-approximation ADC with an integrated analog MUX, allowing it to sample voltage signals from the AC high-gain amplifiers and DC low-gain amplifiers connected to each electrode pin. When sampling the DC low-gain amplifiers, the ADC performs a 10-bit conversion. In most applications, the SPI master device will sample all 16 channels in round-robin fashion and then include perhaps four additional commands for sending commands related to stimulation or impedance measurement. In this case, the per-channel sampling rate will be 20 times lower than the total ADC sampling rate. (See the "SPI Command Sequences" section for details.)

ADC results are easily converted into electrode voltages using the following equations (assuming the **twoscomp** bit in Register 1 is set to zero and the ADC result is read as an unsigned integer). For the AC-coupled high-gain amplifiers, the electrode voltage is given by:

$$V_{elec}(AC) = 0.195\ \mu V \times (\text{ADC result} - 32768)$$

For the DC-coupled low-gain amplifiers, the electrode voltage is given by:

$$V_{elec}(DC) = -19.23\ mV \times (\text{ADC result} - 512)$$

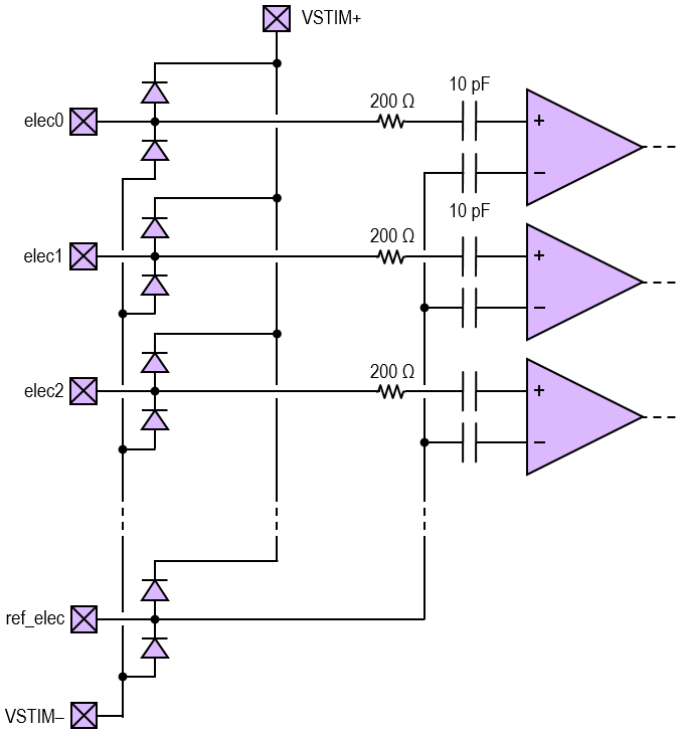
Note the negative sign on the DC amplifier conversion. The least-significant bit (LSB) of the DC amplifier conversion is not reliable, and can be ignored (cleared to zero) for improved linearity.

The ADC may be operated at speeds up to 714 kS/s, which permits 16 channels to be sampled at more than 40 kS/s each. (For typical neural recording applications, per-channel sampling rates of 20 kS/s to 30 kS/s are sufficient since the analog bandwidth of the amplifiers is usually set to 10 kHz or lower.) The variables **ADC buffer bias** and **MUX bias** in Register 0 should be set to the following values based on the total ADC sampling rate:

ADC sampling rate	ADC buffer bias	MUX bias
≤ 120 kS/s	32	40
140 kS/s	16	40
175 kS/s	8	40
220 kS/s	8	32
280 kS/s	8	26
350 kS/s	4	18
440 kS/s	3	16
≥ 440 kS/s	3	5

The ADC contains a temperature- and supply-independent voltage reference that requires an off-chip 10 nF ceramic capacitor to be placed near the chip (within 1 cm of pin 23) and tied from **ADC_ref** to ground. This capacitor should have an X5R, X7R, C0G, or NP0 dielectric and should be rated for at least 16V. (See the "Supply Voltage Levels" section for an explanation of this requirement.) When the chip is powered up, a DC voltage of approximately 1.225 V should appear on this capacitor.

If multiple RHS2116 chips are used, each chip must have its own 10 nF capacitor. The **ADC_ref** pins of different chips should not be connected.



Amplifier Input Protection

All CMOS integrated circuits are susceptible to damage by exposure to electrostatic discharge (ESD) from charged bodies. Electrostatic charges of greater than 1000 V can accumulate on the human body or test equipment and can discharge without detection. All RHS2116 chips incorporate protection circuitry to guard against mild ESD events. However, permanent damage may occur on devices subjected to high energy electrostatic discharges. It is important for users to understand the nature of the ESD protection circuitry used on the chip.

The figure above illustrates the on-chip passive elements (diodes and resistors) used for ESD protection at the input to each amplifier. Diodes are connected to VSTIM+ and VSTIM–, and are used to bleed off charge quickly to prevent the voltage on the series capacitors from exceeding damaging levels. Small 200 Ω series resistors create voltage drops in response to large transient ESD currents, further protecting the amplifiers.

The DC level of all amplifier input pins should never rise above (VSTIM+ + 0.4V) or drop below (VSTIM– – 0.4 V). This prevents the ESD diodes from becoming significantly forward biased and passing current. As long as the electrode pin voltage stays between the stimulation power supplies, the resulting current will be less than 200 pA.

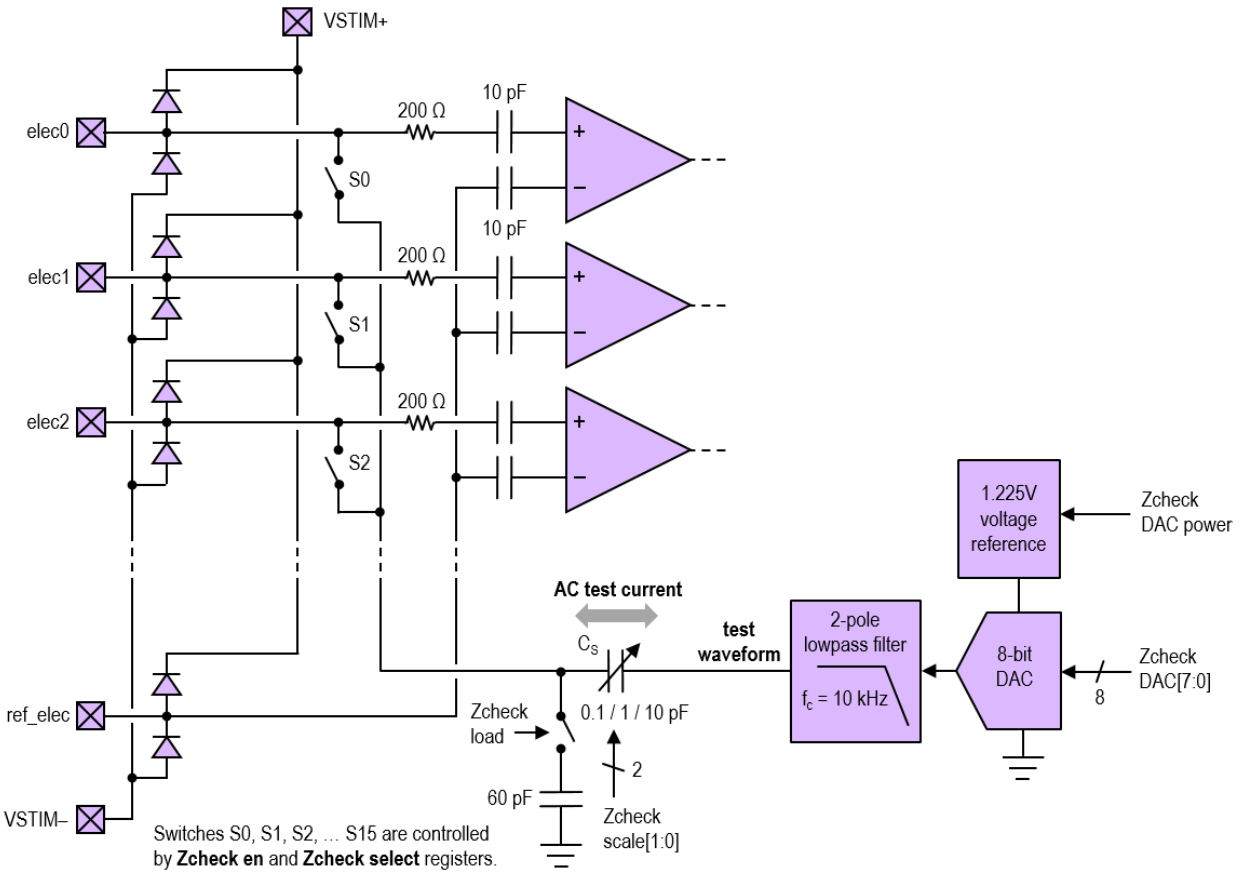
The voltages on VSTIM+ and VSTIM– capacitively couple to amplifier inputs through the capacitance of the reverse-biased ESD diodes, these power supplies should be kept free of AC noise. Otherwise, noise will be injected directly into the amplifier input (and the electrode).

Electrode Impedance Test

All RHS2116 chips have built-in circuitry that provides selectable, direct access to any of the amplifier input pins for the purpose of measuring the impedance of electrodes connected to the chip. Additional on-chip circuitry is provided to generate an AC current waveform needed to measure electrode impedance.

The figure on the next page shows a detailed schematic of the amplifier array input circuitry on the RHS2116. Transistor switches S0 through S15 can be closed to connect one selected amplifier to the on-chip current generator. If the register **Zcheck en** is set to zero, all switches remain open. This is the normal mode of operation for the chip.

If **Zcheck en** is set to one, then the switch corresponding to the amplifier that is selected by the **Zcheck select** register is closed, and that amplifier's input is connected to the on-chip current generator. This mode of operation should be used for measuring the impedance of individual electrodes. If an AC current waveform (with no DC current component) is generated on chip, then the resulting voltage waveform will pass through a high-gain amplifier and may be observed by the ADC. The impedance of the electrode may then be calculated as the ratio of peak voltage to peak current.



Note that this technique requires small currents, as the RHS2116 amplifiers saturate for input voltages larger than ±5.0 mV. For example, a 5 nA peak current will elicit a 5 mV peak voltage with an electrode impedance of 1 MΩ.

Note that any impedance measurement will include the input capacitance of the on-chip amplifiers and parasitic capacitance associated with the ESD protection diodes, stimulator circuitry, bond pad, and QFN package. This 10 pF of capacitance has an impedance magnitude of 16 MΩ at 1 kHz, and should only affect impedance measurements for relatively high-impedance electrodes.

On-Chip AC Current Waveform Generator

RHS2116 chips include circuitry for generating user-specified low-magnitude AC current waveforms that may be directed to any selected electrode for the purposes of electrode impedance testing. The waveform generator consists of an 8-bit digital-to-analog converter (DAC) followed by a two-pole 10 kHz low-pass filter to smooth the "stairstep" edges of the DAC waveform. The DAC is enabled by setting the **Zcheck DAC power** bit to one. The voltage produced by the DAC varies from a minimum of 0 V to a maximum of (255/256) × 1.225 V = 1.220 V, and is set by the register **Zcheck DAC**. Incrementing this register by one increases the DAC output voltage by (1/256) × 1.225 V = 4.785 mV.

The resulting "test waveform" is connected to the selected electrode via a series capacitor C_S that transforms the AC voltage into an AC current. The value of this capacitor is selectable by means of the **Zcheck scale** register and can have a value of 0.1 pF, 1.0 pF, or 10 pF.

If the DAC/filter produces a voltage waveform $v_{DAC}(t)$, the resulting current $i_{DAC}(t)$ injected to the electrode under test is given by

$$i_{DAC}(t) = C_S \frac{dv_{DAC}(t)}{dt}.$$

If the DAC output is unchanging then i_{DAC} = 0, so the SPI master must regularly update the output DAC to create an AC voltage waveform in order to produce an AC current waveform through the series capacitor. For example, the DAC could be used to approximate a sine wave with an amplitude V_A and a DC offset of V_{off} (which is needed since the DAC output cannot go below zero), described as

$$v_{DAC}(t) = V_A \sin(2\pi f t) + V_{off}.$$

The resulting current injected into the electrode under test will be a cosine wave with zero offset and amplitude given by:

$$i_{DAC}(t) = 2\pi f C_S V_A \cos(2\pi f t).$$

For example, if we regularly update the DAC to approximate a 1 kHz sine wave with the maximum possible amplitude of 1.225V / 2 = 0.6125V (and an offset of 0.6125V), then the following table shows the current amplitude produced by all possible series capacitor settings:

C_S	CURRENT AMPLITUDE WITH 1 kHz SINE WAVE (MAX. AMPLITUDE)
0.1 pF	0.38 nA
1 pF	3.8 nA
10 pF	38 nA

If we chose a series capacitor value of 1 pF and connected the 3.8 nA amplitude AC current waveform to a 1 MΩ electrode, the resulting electrode voltage would have an amplitude of 3.8 nA × 1 MΩ = 3.8 mV, which is within the ±5.0 mV range of the amplifiers.

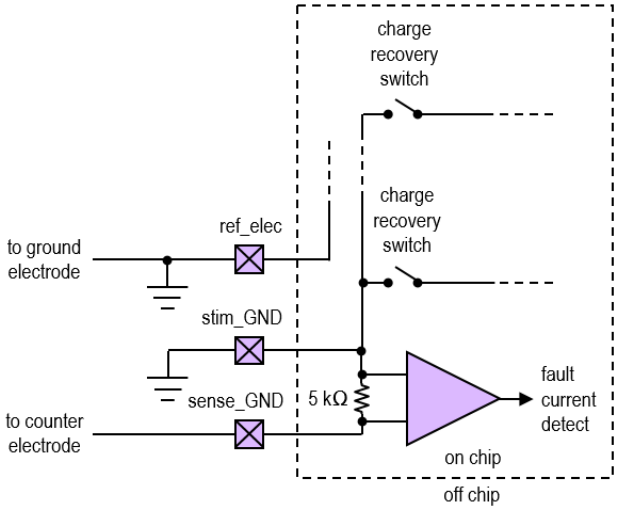
If the frequency of the test waveform were reduced to 100 Hz then the test current would also drop by a factor of ten. However, switching C_S from 1 pF to 10 pF would boost the current back to its original value.

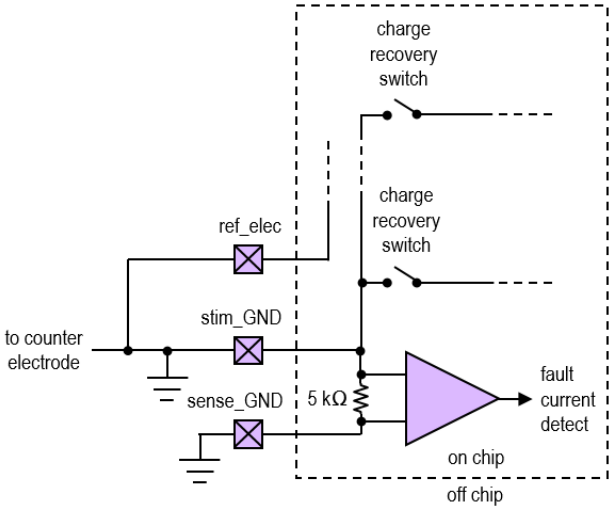
By adjusting the series capacitor value and the amplitude of the waveform produced by the DAC, the AC test current amplitude can be adjusted to measure a wide range of electrode impedances at a number of different frequencies.

Electrode Activation

The stimulation circuitry may also be used to activate electrodes connected to an RHS2116 chip by applying sustained DC currents while electrodes are immersed in electroplating solution that is held at the ground potential with a low-impedance counter electrode.

Some microelectrode electroplating procedures use 10-second current pulses between -30 nA and -60 nA, but this can vary depending on electrode surface area, plating material, and many other factors.





Fault Current Detector

A global fault current detector is also included on the chip, connected between the **stim_GND** pin and the **sense_GND** pin. This circuit can be inserted into a common return current path (e.g., from the counter electrode to ground) and used to detect any unintended current that might result from erroneous SPI commands or partial chip failure.

As shown in the diagrams above, the fault current detector consists of a 5 kΩ sense resistor and an amplifier that looks for significant positive or negative voltages across this resistor. The **fault current detect** bit in Register 50 goes high any time the current through the sense resistor exceeds a typical threshold of 20 µA in either direction, though this detection threshold can vary between 10 µA and 35 µA from chip to chip.

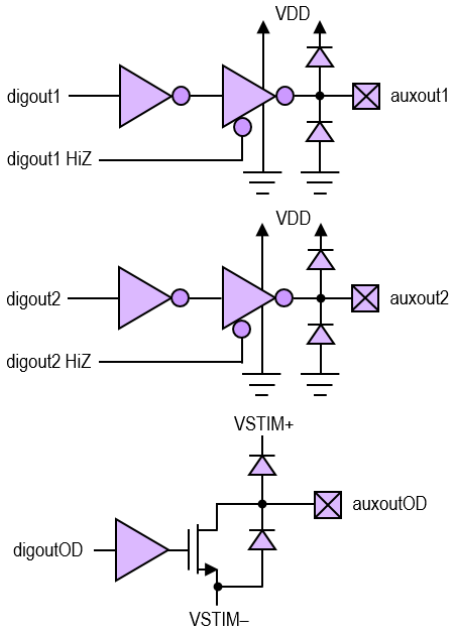
To enable the fault current detector, the return current from a common counter electrode should be routed to ground through the sense resistor as shown in the left figure above. If the fault current detector will not be used, the counter electrode should be configured as shown in the right figure above, with both sides of the sense resistor shorted to the same potential (usually ground).

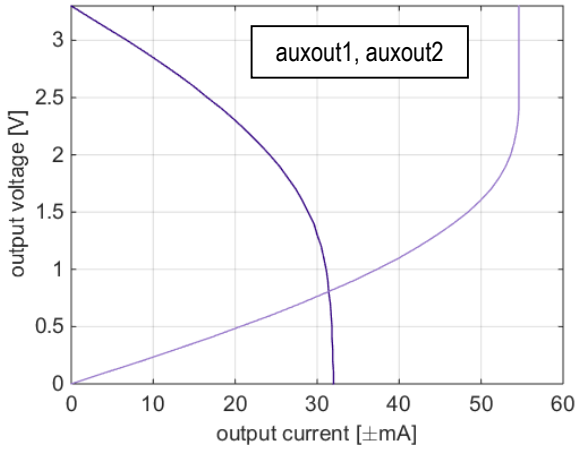
A typical use case of the fault current detector is to occasionally check the fault current detect bit when all stimulators are turned off. If current is detected, then various means can be taken to stop current flow, from reprogramming the SPI registers responsible for stimulation, to cutting power to the RHS2116 chip.

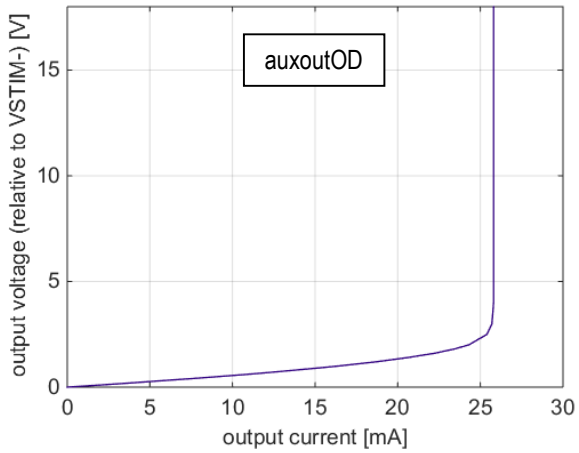
Auxiliary Digital Outputs

All RHS2116 chips have three user-programmable digital output pins (**auxout1**, **auxout2**, and **auxoutOD**) which may be used to control external devices via SPI commands. Register 1 contains control registers that configure the states of these signals. Setting **digout1 HiZ** to zero enables the **auxout1** pin; if **digout1 HiZ** is set to one then the **auxout1** pin assumes a high-impedance state. The **digout1** register controls the value of the **auxout1** pin. If **digout1** is set to zero then **auxout1** is driven to ground; if **digout1** is set to one then **auxout1** is driven to VDD.

Similarly, the **digout2 HiZ** and **digout2** variables control the **auxout2** pin. A plot on the next page shows the maximum currents the **auxout1** and **auxout2** pins can supply while maintaining particular voltage levels. If additional drive current is needed, the user must add external circuitry.







The **digoutOD** variable controls the open-drain **auxoutOD** pin. This pin is connected to the drain of an on-chip MOSFET switch whose source is tied to VSTIM–. Setting **digoutOD** to one pulls the **auxoutOD** pin to the negative stimulation voltage. If **digoutOD** is set to zero, the **auxoutOD** pin assumes a high-impedance state. The voltage on the **auxoutOD** pin can range between VSTIM+ and VSTIM–, so this pin may be used to control devices that require voltages larger than 3.3V (e.g., blue or white LEDs). Any load connected to **auxoutOD** must be tied to a voltage above VSTIM–, like VSTIM+ or GND, that will pull this pin to a higher voltage when it is placed in a high impedance state.

The **auxoutOD** pin can sink a typical maximum output current of 25 mA (see plot above). For pin voltages greater than 3V above VSTIM– this pin behaves as a current source. For pin voltages less than 2V above VSTIM– the on-chip MOSFET behaves like a resistor with a typical 'on' resistance of 55 Ω. If precise current levels are needed, a current-limiting resistor should be added in series with the load connected to this pin.

The auxiliary digital output pins can be used for many applications: to control the gate of an external MOSFET that optionally shorts **ref_elec** to ground or enable an LED or laser diode for optogenetic stimulation. It is important to remember that the values of these registers are indeterminate when the chip is first turned on, so care should be taken to ensure that any device connected to this pin does not cause trouble if an auxiliary digital output pin assumes an unexpected value when the chip is initially powered up.

Absolute Value Mode

If the **absmode** bit in Register 1 is set to one, the output results from all AC high-gain amplifier channels are passed through an absolute value function: all negative results are sign inverted so that the output of each channel is a strictly positive "full wave rectified" waveform. This destroys some information in the waveform (e.g., both –100 and +100 are reported as +100), but this function may be useful if only the amplitude or "energy" of a signal is required for a particular application.

For example, in a system that detects and counts neural spikes using a simple threshold algorithm, enabling absolute value mode allows the controller to check only one threshold instead of checking both a positive and negative threshold. Also, many EMG-based prosthetic limb controllers estimate the energy or envelope of the EMG signal, and computing the absolute value of the raw EMG waveform is often the first step in this estimation. The ability of the RHS2116 to perform this operation automatically can relieve some of the computational burden on the controller in an electrophysiology acquisition system.

It is recommended that absolute value mode be used with the DSP high-pass filter enabled so that the amplifier offsets are removed and the baseline level of each channel will be precisely zero.

ADC results from the DC low-gain amplifiers are not affected by the **absmode** bit.

DSP High-Pass Filter for Offset Removal

RHS2116 chips include a custom digital module that performs digital signal processing (DSP) to implement single-pole high-pass filters on each sampled amplifier channel. This feature can be used to remove the residual DC offset voltages associated with the AC high-gain amplifiers, which can range from ±100 μV (referred to the electrode). (Despite the series capacitors that block DC voltages at the amplifier input, small DC offsets are introduced in the amplifier circuitry after the capacitors.) The DSP module can also be used to add an additional pole of high-pass filtering to the single pole inherent in the amplifier circuits. The chip uses an IIR filter architecture; the

magnitude and phase characteristics of this filter are similar to those of an analog high-pass filter implemented with a capacitor and resistor.

The DSP high-pass filter module is enabled by setting the **DSPen** bit in Register 1 to one. The DSP module affects only affects AC high-gain amplifier channels; DC low-gain amplifiers are not filtered.

The cutoff frequency of the DSP high-pass filter is determined by two factors: the rate at which each amplifier channel is sampled (f_{sample}), and the four-bit **DSP cutoff freq** variable in Register 4. The cutoff frequency f_c is calculated using the following equation:

$$f_c = k_{freq} \cdot f_{sample} = \frac{\ln\left(\frac{2^N}{2^N - 1}\right)}{2\pi} \cdot f_{sample}$$

where N is the value of the **DSP cutoff freq** variable, ranging from 1 to 15. Calculated values of k_{freq} are presented in the table below for convenience:

DSP cutoff freq [3:0]	k_{freq} ($f_c = k_{freq} \cdot f_{sample}$)
0	differentiator; see below
1	0.1103
2	0.04579
3	0.02125
4	0.01027
5	0.005053
6	0.002506
7	0.001248
8	0.0006229
9	0.0003112
10	0.0001555
11	0.00007773
12	0.00003886
13	0.00001943
14	0.000009714
15	0.000004857

Note that f_{sample} is the sampling frequency of each channel; not the overall ADC sampling frequency.

For example, if we sample each amplifier channel at 30 kSamples/s and set the **DSP cutoff freq** variable to 12, the resulting DSP high-pass cutoff frequency will be 0.00003886 × 30 kHz = 1.2 Hz, which is a good value for removing offsets while preserving low frequency biological signals such as cortical local field potentials (LFPs). Alternatively, if we sample at 30 kSamples/s/channel and set the **DSP cutoff freq** variable to 4, the resulting DSP high-pass cutoff frequency will be 308 Hz, which is a good value for removing LFP fluctuations so that neural action potentials can be subjected to amplitude thresholds.

If the **DSP cutoff freq** variable is set to zero, the DSP filter acts like a perfect differentiator; the output of the filter is the current ADC result minus the previous ADC result for a particular channel.

Since the DSP filter has perfect linearity while the analog amplifier circuits have imperfect linearity, it is good practice to set the DSP cutoff frequency f_c higher than the analog amplifier lower cutoff frequency f_L to minimize the distortion of large signals.

If a large signal is applied to an AC high-gain amplifier channel with the DSP filter enabled, the sampled output will "hard limit" at the numerical minimum or maximum permitted by the 16 bit representation; it will not "roll over" due to numerical overflow or underflow.

When using the DSP filter module, it is important to sample amplifiers at a steady and consistent rate. The filter state variables for each channel are updated only when that particular channel is sampled. If each channel is not sampled at exactly the same rate during the time the DSP filter is enabled, the filter output will not be accurate.

The time constant associated with the DSP high-pass filter is given by $1/(2\pi f_c)$. If a step input is applied to the filter, the output will exponentially decay back to zero with this time constant. If a relatively low value of f_c is used (e.g., less than 1 Hz), the time constant can become quite long and result in long recovery times from large transient signals. Each channel's DSP high-pass filter can be instantly reset to zero by setting the H flag of the CONVERT command to one. This operation clears the digital state variable associated with the selected amplifier channel.

Power Dissipation

The total power dissipation of an RHS2116 chip depends on how it is configured and operated. This section provides a breakdown of currents pulled from the three power supplies (VDD, VSTIM+, and VSTIM–) under various modes of operation. Power dissipation can then be calculated as the absolute value of the product of the supply current and the supply voltage.

The most important consideration in reducing power in the RHS2116 is setting the **DC amp power** variable in Register 38 to all ones (hex FFFF). While this register was originally included on the chip to provide a modest power savings in cases where the DC amplifiers were not used, a hardware bug in the chip counterintuitively causes current drawn from VDD to **increase** when these amplifiers are

powered down. For each DC amplifier channel that is powered down, the current from VDD increases by 1.93 mA. **It is therefore strongly recommended that Register 38 be set to all ones as soon as the chip is powered up.**

Once this register is set, currents drawn from the VSTIM supplies are relatively constant if stimulation pulses are not being generated. The table below lists quiescent currents for various supply levels.

VSTIM±	supply current from VSTIM+	supply current from VSTIM–
±3.3V	0.57 mA	0.41 mA
±6.0V	0.61 mA	0.46 mA
±9.0V	0.65 mA	0.51 mA
+3.3V / -14V	0.57 mA	0.52 mA
+14V / -3.3V	0.65 mA	0.41 mA

Currents drawn from the VSTIM supplies may increase significantly during stimulation, as discussed below.

The bulk of non-stimulation current is drawn from the +3.3V power supply (VDD). Following is a list of guidelines for estimating total VDD supply current under various operating conditions.

Baseline current: Each RHS2116 pulls 3.2 mA of quiescent current from VDD to power various voltage references, bias current generators, and ADC circuitry.

AC amplifiers: Each AC amplifier consumes current in proportion to its upper cutoff frequency, approximately 9.2 µA/kHz per amplifier. Powering off an amplifier via Register 8 essentially sets its upper cutoff frequency to zero for power calculation purposes.

ADC and MUX dynamic current: The ADC/MUX assembly consumes additional current in proportion to the total sampling rate, approximately 5.2 µA/(kS/s). Enabling or disabling 10-bit sampling of the DC amplifiers (via the D flag in the CONVERT command) does not significantly affect power consumption.

LVDS I/O: If **LVDS_en** is pulled high to enable on-chip LVDS driver and receivers, the chip pulls an additional 5.7 mA. Current draw with standard CMOS signaling is proportional to SPI data rate and MISO wire capacitance; for low data rates and short wires, it is very small.

Impedance measurement module: With **Zcheck DAC power** in Register 2 set to one, the DAC used for impedance testing consumes 120 µA.

Using these guidelines, we can now estimate whole-chip power dissipation, not including additional current required for stimulation pulses:

Example: Wideband neural recording headstage

VSTIM± = ±9V
f_H = 10 kHz
sample rate = 16 × 30 kS/s/channel = 480 kS/s

Baseline current: 3.2 mA
AC amplifiers: 16 × 9.2 µA/kHz × 10 kHz = 1.47 mA
ADC/MUX: 5.2 µA/(kS/s) × 480 kS/s = 2.50 mA
LVDS I/O: 5.7 mA
Impedance measurement: 0.12 mA

Total supply current from VDD: 12.99 mA
Total supply current from VSTIM+: 0.65 mA
Total supply current from VSTIM–: 0.51 mA

Total power dissipation: (12.99 mA × 3.3 V) + (0.65 mA × 9.0 V) + (0.51 mA × 9.0 V) = 53.3 mW

Example: ECoG recording front-end with CMOS I/O

VSTIM± = ±6V
f_H = 1 kHz
sample rate = 16 x 2 kS/s/channel = 32 kS/s

Baseline current: 3.2 mA
AC amplifiers: 16 × 9.2 µA/kHz × 1 kHz = 0.15 mA
ADC/MUX: 5.2 µA/(kS/s) × 32 kS/s = 0.17 mA
Impedance measurement: 0.12 mA

Total supply current from VDD: 3.64 mA
Total supply current from VSTIM+: 0.61 mA
Total supply current from VSTIM–: 0.46 mA

Total power dissipation: (3.64 mA × 3.3 V) + (0.61 mA × 6.0 V) + (0.46 mA × 6.0 V) = 18.4 mW

Power Due to Stimulation

Generating stimulation pulses draws additional current from all three power supplies. If a positive stimulation current with magnitude I_{STIM} is supplied from one channel, the currents drawn from each power supply increase by the following amounts during stimulation:

VDD: $\Delta I = 0.23 \cdot I_{STIM}$
VSTIM+: $\Delta I = 1.15 \cdot I_{STIM}$
VSTIM–: $\Delta I = 0$

If a negative stimulation current with magnitude I_{STIM} is supplied from one channel, the currents drawn from each power supply increase by the following amounts during stimulation:

VDD: $\Delta I = 0.10 \cdot I_{STIM}$
VSTIM+: $\Delta I = 0.34 \cdot I_{STIM}$
VSTIM–: $\Delta I = 1.31 \cdot I_{STIM}$

Note: If any of the auxiliary digital output pins (**auxout1**, **auxout2**, or **auxoutOD**) are used with low-impedance loads, these may draw additional supply current as well. See the "Auxiliary Digital Outputs" section for more details.

Minimizing Power Consumption

While the criteria listed above are the major factors determining power consumption in the RHS2116, several other chip settings can help to minimize current drawn from the VDD supply:

- Set the stimulation current magnitudes of all unused channels to zero (Registers 64-79 and 96-111).
- If current-limited charge recovery is not used, set the charge recovery current limit to 1 nA (Register 37).
- If stimulation is not used, set the stimulation current step size to 10 nA (Register 34).
- If the second AC amplifier lower cutoff frequency is not used, set it to 0.10 Hz (Register 7).
- Power down unused AC amplifiers (Register 8), but make sure to leave all DC amplifiers powered up (Register 38; see above for explanation).

Excessive Power Consumption Warning

Leaving VSTIM+ and VSTIM– unconnected will cause excessive power dissipation. These power pins should always be connected to voltage supplies during operation of the chip. If stimulation functions will not be used, VSTIM+ can be tied to VDD and VSTIM– can be tied to ground.

SPI Command Sequences

The rate and timing of SPI commands sent to the chip determines the ADC sampling rate; sample times are set by the falling edge of $\overline{CS}$. In most applications, all 16 amplifiers on the chips will be sampled in round-robin fashion. This can be accomplished by repeating the following command sequence:

CONVERT(0)
CONVERT(1)
CONVERT(2)
…
CONVERT(14)
CONVERT(15)

If a per-channel sampling rate of R is desired, then SPI commands are sent at a rate of 16R.

The problem with simply repeating 16 CONVERT commands is that additional commands (e.g., to write to registers to control stimulation) must be substituted for regular CONVERT commands (which results in a missing sample on one channel) or else the sequence must be interrupted by an inserted command, which makes the per-channel sampling rate irregular.

The simplest solution to this problem is to always insert a fixed number (typically 1-4) of extra "auxiliary" commands into the round-robin command sequence:

CONVERT(0)
CONVERT(1)
CONVERT(2)
…
CONVERT(14)
CONVERT(15)
auxiliary command 1
auxiliary command 2
auxiliary command 3
auxiliary command 4

Now having a list of 20 commands, the SPI commands are sent at a rate of 20R to achieve a per-channel sampling rate of R. Extra commands (e.g., to control stimulation, to update the impedance check DAC, etc.) may be inserted into one of the auxiliary command "slots", and these extra commands will not interrupt the steady, constant-rate sampling of the amplifiers on the chip. Dummy commands (e.g., reading a ROM register) can be inserted into these slots as place holders when no auxiliary actions are required.

See the "Example Chip Initialization Procedure" section near the end of this datasheet for an example SPI command sequence to initialize the chip.

Circuit Board Design

Careful printed circuit board (PCB) design is critical for achieving the specified performance of the RHS2116. The chip is designed to work with a single ground and a single VDD, plus positive and negative stimulation voltage supplies. It is not necessary (or recommended) to use separate "analog" and "digital" power lines. Rather, it is important to use a good ground plane and power plane underneath the chip. This requires the use of a four-layer PCB, at minimum. If a four-layer board is used, the top (first) and bottom (fourth) layers should be used for signal routing. The second layer should be a ground plane and the third layer should be a VDD plane.

A 100 nF (0.1 µF) ceramic capacitor between VDD and ground should be placed as close as possible to the bottom of the chip (near pins 13 and 22). Additional 100 nF capacitors should be tied from VSTIM+ to ground and from VSTIM– to ground; these capacitors should be placed close to the left side of the chip (near pins 4-8). See the "Supply Voltage Levels" section for guidance selecting the proper types of capacitors. If standard CMOS signaling will be used, place an **additional** 100 nF decoupling capacitor near pins 24-28 on the right side of the chip.

A 10 nF ceramic capacitor should be tied from **ADC_ref** to ground and placed close to the bottom or right side of the

chip, near the **ADC_ref** pin. See the "Analog-to-Digital Converter" section above for guidance selecting the proper type of capacitor.

If LVDS signaling is used, 100 Ω termination resistors for $\overline{CS}$, SCLK, and MOSI should be placed within 20 cm of the chip. The 100 Ω termination resistor for MISO should be placed near the controller and will likely not reside on the same board as the RHS2116. (Many LVDS receivers and FPGAs have built-in termination resistors, so this device may not be necessary.)

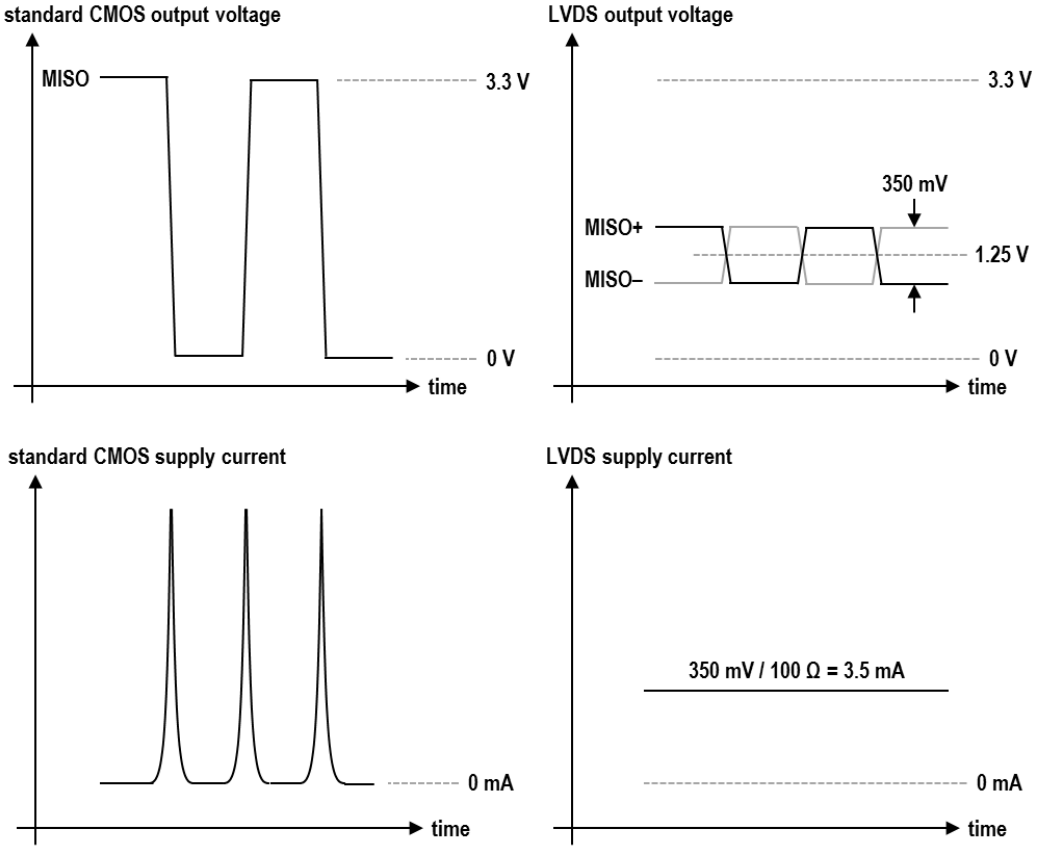
A recommended PCB footprint for QFN-packaged RHS2116 chips is shown on page 45. The center pad of the QFN package is connected to the VSTIM– power supply, so the center pad on the circuit board should be tied to the negative stimulation power supply. If a solder paste mask is used for reflow assembly, the paste mask for the center pad should be made smaller than the pad so excess solder is not deposited. When the QFN component is placed on the PCB, excess solder paste from the center pad can short to peripheral pins.

Leakage Currents Due to Residual Solder Flux

Solder contains flux, a chemical compound that helps to clean surfaces and facilitate solder flow and proper bonding. While flux is useful for the soldering process, residual flux left behind on the surface of the circuit board can be slightly conductive. Conductive paths between electrodes and power supply lines can cause leakage currents that may polarize electrodes and lead to oxidation or, in extreme cases, electrolysis of water near the electrodes.

If leakage currents are a concern, solder paste should be omitted on the center pad of the QFN. This is not a critical electrical connection, and since this pad is at the VSTIM– potential and very close to the electrode pads, it is an obvious concern due to residual solder flux that ends up underneath the QFN and cannot be cleaned effectively. Additionally, solder with water soluble flux should be used, and after assembly the boards should be thoroughly washed in warm deionized (DI) water. These are standard services that most circuit board assembly companies can provide on request.

Digital Signaling Modes



The RHS2116 chip communicates over a standard digital Serial Peripheral Interface (SPI) bus. The bus protocol and data structures used are described in later sections. The voltage levels used to send digital signals over this bus can assume one of two forms: standard CMOS signaling or low-voltage differential signaling (LVDS). The above figure illustrates the differences between a digital value (e.g., MISO) transmitted using these two signaling methods.

Standard CMOS Signaling

Standard CMOS signaling (upper left) transmits a digital one or zero by switching the voltage on a single output wire between ground and VDD. The current drawn from the power supply (lower left) is nearly zero until the output switches state; at this point, a burst of current is pulled from the power supply to charge or discharge the capacitance of the output wire. These bursts of supply current introduce high frequency noise to the on-chip power supply; this noise can adversely affect noise levels. For typical data streams containing similar numbers of ones and zeros, the dynamic power dissipation of a standard CMOS output driving a wire with capacitance C_{wire} at R bits/s is

$$P = \frac{1}{2} C_{\text{wire}} {V_{\text{DD}}}^2 R.$$

(The actual power dissipation will be slightly higher than this due to secondary effects like the momentary short-circuit current that leaks through CMOS circuits every time they switch state.)

If we operate an RHS2116 at the maximum sampling rate of 714 kS/s, the data rate R is 714 kHz × 32 bits = 22.8 Mbit/s. Typical coaxial cables have a capacitance of 100 pF/m. The power required to transmit 22.8 Mbit/s over a 2.0 m cable is approximately 25 mW.

Transmitting high-frequency data reliably over long wires is challenging due to the presence of reflections that occur when a propagating signal reaches the high-impedance input of a digital receiver. These reflections interfere with the transmitted signal and corrupt the data stream. The characteristic impedance Z_0 of a cable is given by

$$Z_0 = \sqrt{L/C}$$

where L is the cable inductance per unit length and C is the cable capacitance per unit length. For most common cable geometries (e.g., coaxial, twisted pair, ribbon), Z_0 falls in the range of 50 – 200 Ω. To eliminate reflections, the cable must be terminated with a parallel resistance equal to Z_0.

Standard CMOS digital outputs lack the current sourcing capability to drive the high DC currents necessary to support VDD-level signals (i.e., 3.3V) across such small resistances, so proper cable termination cannot be used in these cases. A series resistor with a value of Z_0 placed near a CMOS digital output can prevent multiple reflections from the high-impedance input at the far end of a cable by absorbing the first reflection, but this is an imperfect solution that fails with high data rates or long cables.

LVDS Signaling

LVDS signaling (upper right, previous page) uses a pair of wires (e.g., **MISO+** and **MISO–**) to transmit each digital signal; the wires are terminated with a 100 Ω resistor tied between them near the LVDS receiver. The average voltage on the wire pair is held roughly at 1.25V, and a 3.5 mA current is forced through the wires in one direction or the other, creating a ±350 mV differential voltage across the terminating resistor to signal a digital one or zero.

LVDS signaling offers several advantages over standard CMOS signaling. First, the use of terminated wires drastically reduces reflections, maintaining high signal integrity on long wires and at high data rates. Second, the use of small differential voltages greatly reduces crosstalk to other nearby wires in a cable bundle, especially if twisted pairs are used. Electromagnetic interference and emissions are also minimized using LVDS signaling. Finally, the current drawn from the power supply of the LVDS transmitter is nearly constant (lower right, previous page). This constant current draw does not introduce noise to the on-chip power supply. Thus, LVDS signaling is far better suited for low-noise operation on a chip containing both analog and digital components.

The minimum power dissipation of an LVDS transmitter is given by VDD·(3.5 mA) = 11.6 mW using a 3.3V power supply. At low frequencies and short wire lengths, standard CMOS signaling can operate at far lower power levels. However, as the calculations in the previous section demonstrate, LVDS can operate at lower power levels when data rates are high and wires are long.

Cables several meters in length can be used with LVDS signaling as long as the geometry of the cable is fairly consistent along its length. Twisted pairs are particularly good structures for LVDS signaling, and many standard cables contain multiple twisted pairs (e.g., USB, HDMI). The DC series resistance of the cable typically has no effect on the performance of the system as long as it is much less than the terminating resistance of 100 Ω. Signals propagate along standard cables at approximately two-thirds the speed of light, or 20 cm/ns, so a five-meter cable will introduce a round-trip delay of around 50 ns. As long as the SPI controller accounts for these delays, long cables may be used to communicate with RHS2116 chips reliably.

The LVDS inputs and outputs on the RHS2116 use industry-standard LVDS signal levels. Many commercially available FPGAs and microcontrollers have built-in LVDS I/O pins, and can be interfaced directly with the RHS2116. If a controller lacks LVDS I/O, a wide variety of commercially available LVDS-to-standard-CMOS driver and receiver interface chips may be used to translate signal levels (e.g., TI SN65LVDS, SN65LVDT, DS90LV, and DS90C lines; Fairchild FIN10xx line).

Selecting Signaling Modes on the RHS2116

If the **LVDS_en** pin on an RHS2116 is tied to GND, the SPI bus operates with standard CMOS signals, using a single wire for each digital signal. The digital input pins on the RHS2116 interpret any voltage below 0.7V as logic "low" and any voltage above 2.4V as logic "high", so the chip can be interfaced with standard 2.5V, 3.0V, or 3.3V signals. Digital inputs to the RHS2116 should not go below –0.4V, and should never exceed 3.6V. Digital outputs from the RHS2116 chip are driven to ground for logic "low" and to VDD for logic "high".

If the **LVDS_en** pin is tied to VDD, the SPI bus operates in LVDS mode, where every signal in the SPI bus is represented by a differential voltage across a pair of wires (e.g., **SCLK+** and **SCLK–**). The LVDS inputs on the RHS2116 expect a common-mode voltage near 1.25 V and differential signals near ±350 mV, but are fairly tolerant of moderate variations in these values. The LVDS inputs do not include on-chip termination, so a 100 Ω resistor should be placed between each LVDS input signal pair near the chip. Connection diagrams on the following pages provide examples of termination schemes.

Enabling LVDS mode on the RHS2116 increases current consumption by approximately 5.7 mA (from VDD to ground). This includes the 3.5 mA of current driven through the MISO output as well as current to power the three on-chip LVDS receivers for $\overline{CS}$, SCLK, and MOSI. (Commercial LVDS interface chips typically consume over 17 mA to perform the same functions as the RHS2116 LVDS I/O system.)

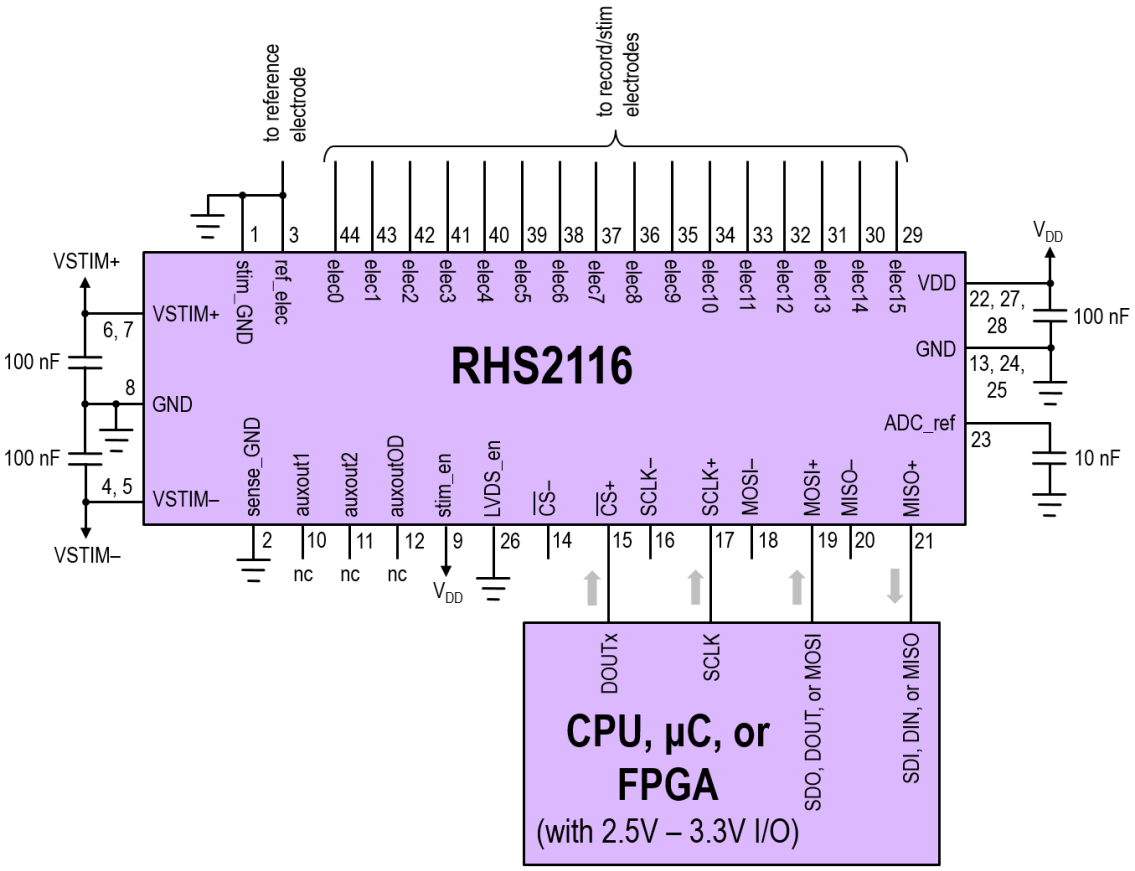
Increased Noise Levels with Standard CMOS Signaling

If standard CMOS signaling is used in combination with high ADC sampling rates, the amplifier noise level on the RHS2116 may rise above its nominal value of 2.4 μV_{rms}, particularly if long, high-capacitance wires are used for the SPI bus.

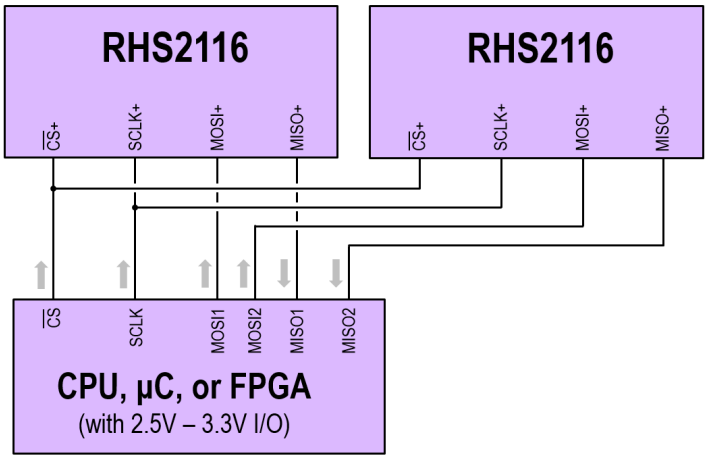
Typical Connection Diagram

STANDARD CMOS SPI INTERFACE (LVDS_en = 0)

The diagram below shows a typical circuit schematic for a single RHS2116 chip interfaced to a controller that is located in close proximity and uses a standard CMOS four-wire SPI interface. In addition to the chip, only four SMD (surface mount device) capacitors are required for a complete biopotential recording/stimulation front end.

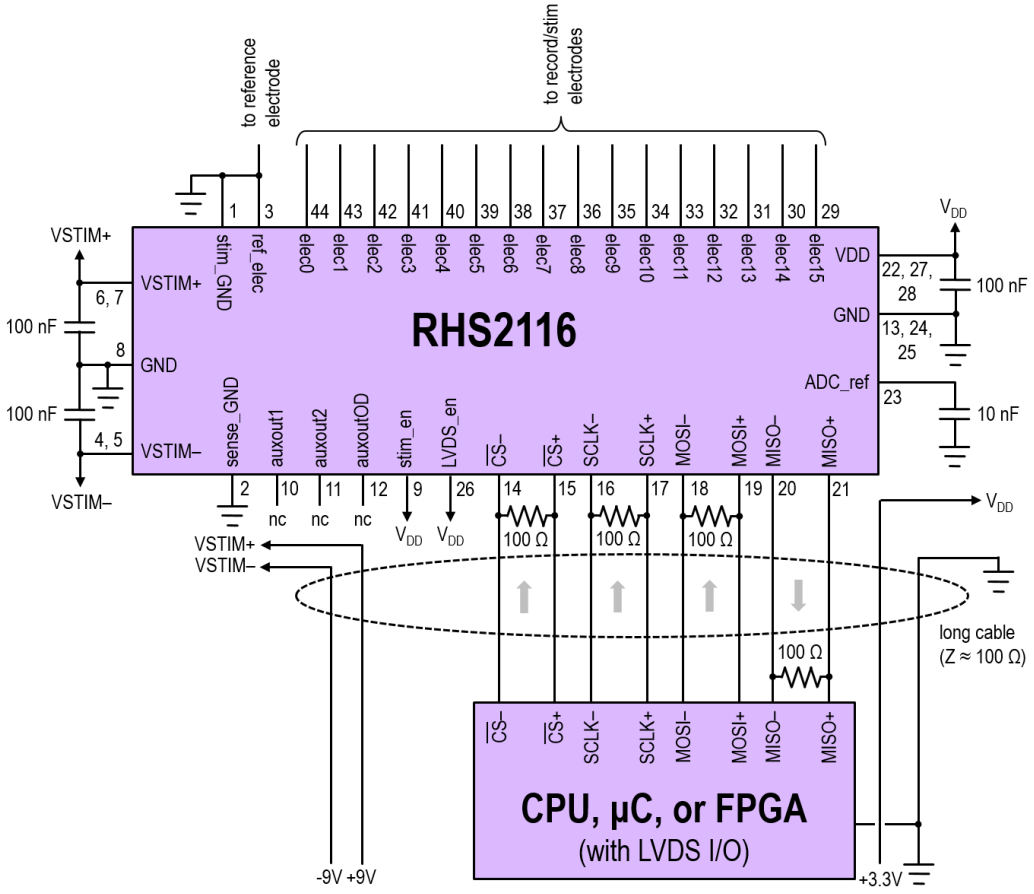


Additional RHS2116 chips can be added using only one additional MISO wire and MOSI wire per chip, provided that all chips receive commands using the same $\overline{CS}$ and SCLK signals, as shown below.

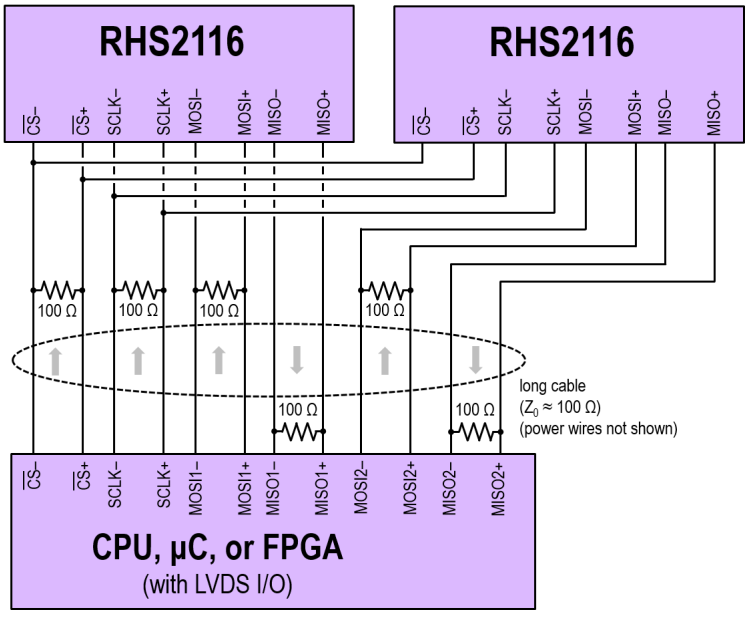


LVDS SPI INTERFACE (LVDS_en = 1)

The diagram below shows a typical circuit schematic for a single RHS2116 chip interfaced to a controller over a long cable, using an SPI interface with low-voltage differential signaling and 100 Ω termination resistors.



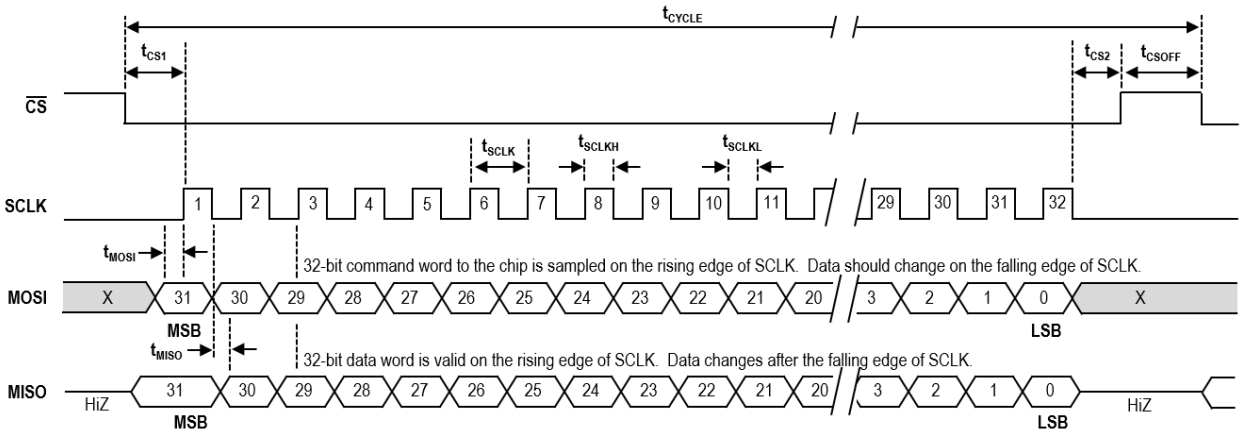
Additional RHS2116 chips can be added as shown below. Only one termination resistor should be used for each LVDS pair; this resistor should be located within 20 cm of LVDS input pins on the RHS2116 chips or the CPU or FPGA.



SPI Bus Signals

RHS2116 chips communicate using a standard SPI interface consisting of four signals: an active-low chip select ($\overline{CS}$); a serial data clock (SCLK) with a base value of zero; a "Master Out, Slave In" data line (MOSI) to receive commands from the master device; and a "Master In, Slave Out" data line (MISO) to send pipelined results from prior commands to the master device. The RHS2116 chip always functions as the SPI slave device. During each chip select cycle, 32-bit data words are transferred in each direction, MSB first. As shown below, the RHS2116 samples MOSI on the rising edge of SCLK. The master should sample MISO on the rising edge of SCLK. (The master device SPI interface should be configured with SPI options CPOL=0 and CPHA=0.) The $\overline{CS}$ line must be pulsed high between every 32-bit data transfer.

Timing Diagram



SPI BUS TIMING SPECIFICATIONS

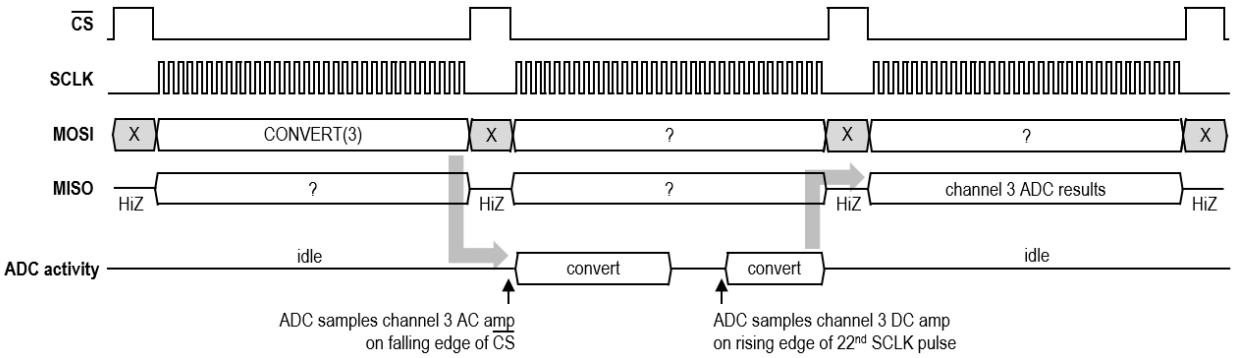
T_A = 25ºC, VDD = 3.3V unless otherwise noted.

SYMBOL	PARAMETER	MIN	MAX	UNIT	COMMENTS
t_{SCLK}	SCLK Period	40		ns	Maximum SCLK frequency is 25 MHz
t_{SCLKH}	SCLK Pulse Width High	20		ns	
t_{SCLKL}	SCLK Pulse Width Low	20		ns	
t_{CS1}	$\overline{CS}$ Low to SCLK High Setup	20		ns	
t_{CS2}	SCLK Low to $\overline{CS}$ High Setup	20		ns	
t_{CSOFF}	$\overline{CS}$ High Duration	100		ns	
t_{MOSI}	MOSI Data Valid to SCLK High Setup	10		ns	
t_{MISO}	SCLK or $\overline{CS}$ Falling Edge to MISO Data Valid		12	ns	
t_{CYCLE}	Total Cycle Time Between ADC Samples	1400		ns	Maximum sample rate is 714 kS/s, or 44.6 kS/s per channel for 16 multiplexed channels.

SPI Command Words

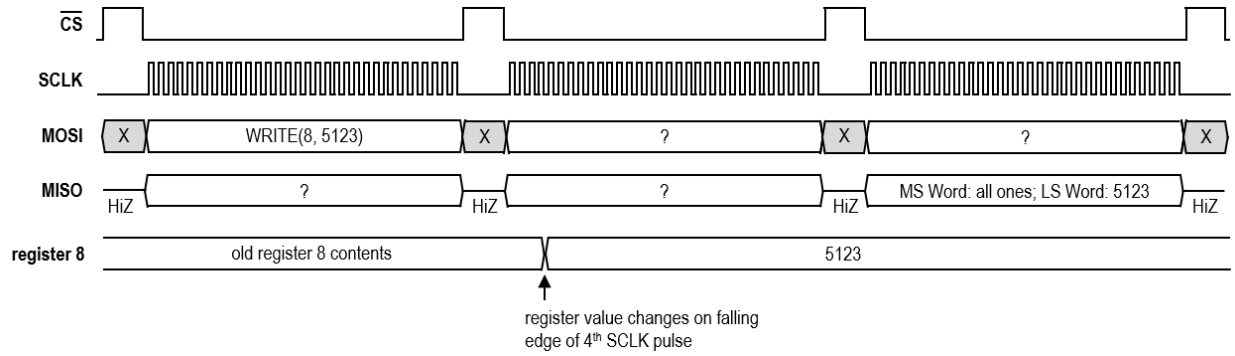
Each RHS2116 chip responds to four basic commands: perform an analog-to-digital conversion on amplifier signals from a particular channel; initialize ADC settings; write to a RAM register; or read from a RAM or ROM register. Each chip contains many 16-bit RAM registers that configure various aspects of chip behavior and several 16-bit ROM registers that store basic properties of the chip. In addition to the five commands, there are four one-bit flags present in some command words that also control various functions.

The RHS2116 uses a pipelined communication protocol; each command sent over the MOSI line generates a 32-bit result that is transmitted over the MISO line two commands later. Communication with the chip is illustrated in the following example diagram:



In the above diagram, a CONVERT command for channel 3 is issued during the first set of 32 SCLK pulses. Positive $\overline{CS}$ pulses separate successive SPI commands. The ADC conversion is executed during the following SPI communication cycle: the AC high-gain amplifier is sampled on the falling edge of $\overline{CS}$ following the CONVERT command. If the D flag in the CONVERT command is asserted, the DC low-gain amplifier is sampled on the rising edge of the 22nd SCLK pulse during this SPI cycle. The results of these ADC conversions are returned over the MISO line during the second SPI communication cycle following the original CONVERT command. See the full description of the CONVERT command below for more details.

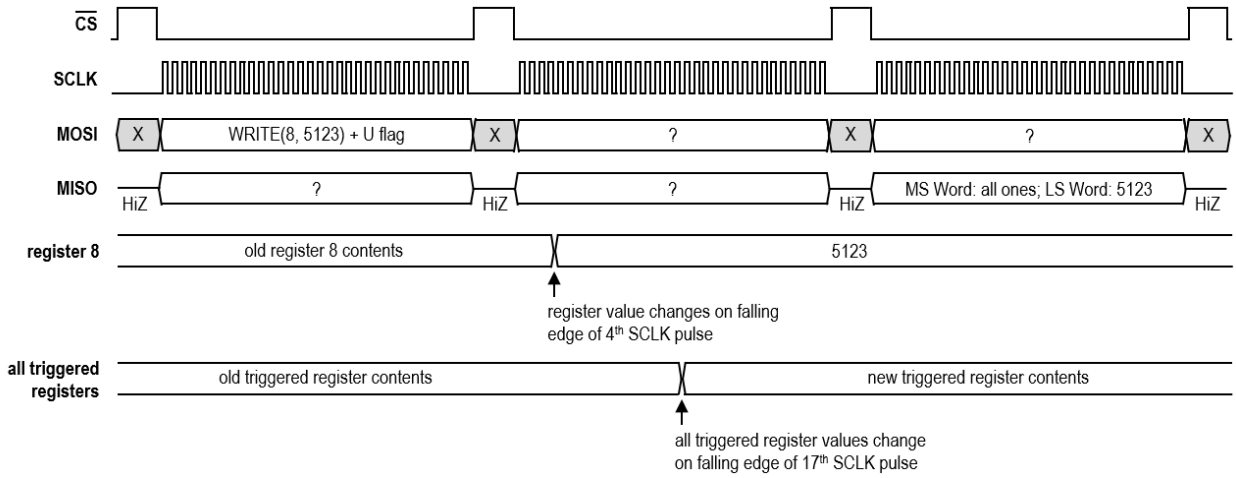
A register WRITE command is illustrated below:



Here, the MOSI line issues a command to the chip to write the value 5123 to Register 8. The on-chip register value is not updated until the falling edge of the 4th SCLK pulse during the following SPI communication cycle. The result of the WRITE command is returned via MISO during the following communication cycle.

Some registers on the RHS2216 are **triggered registers**. Triggered registers have internal buffers that are programmed with a WRITE command, but the new values do not become active to internal circuits until a command is sent that has the **U (Update) flag** asserted. When the U flag is asserted, **all** triggered registers across the chip update to their buffered values simultaneously. This allows complex, synchronized stimulation patterns to be created across multiple electrodes.

The diagram below shows an example of a WRITE command being issued with the U flag asserted:



Following a command with the U flag asserted, all triggered registers update their contents on the falling edge of the 17th SCLK pulse during the SPI communication cycle following the command.

Note that when reading a triggered register, the value returned is the value stored in the internal buffer, which is not necessarily the "active" value of this register unless the U flag has been asserted after the last WRITE command issued to this register.

The RHS2116 commands are described by the following bit patterns:

Command: CONVERT(C) – Run analog-to-digital conversion on channel C

MSB 31	30	29	28	27	26	25 – 22	21 – 16	LSB 15 – 0
0	**0**	**U**	**M**	**D**	**H**	**0000**	**C[5:0]**	**00000000 00000000**

Result:

MSB 31 – 16	15 – 10	LSB 9 – 0
A[15:0]	**000000**	**W[9:0]**

Comments:

The CONVERT(C) command executes an analog-to-digital conversion of analog channel C. Channels 0-15 correspond to the 16 amplifier channels sharing the chip with the ADC. The AC high-gain amplifier is sampled with 16 bits of resolution; its value is returned in the high 16 bits of the 32-bit result. If the D flag is set to one then the DC low-gain amplifier of channel C is sampled with 10-bit resolution, and its value is returned in the lower 10 bits of the result.

A special case of the CONVERT command with C = 63 can be used to cycle through successive amplifier channels. The CONVERT(63) command automatically increments the multiplexer to the next amplifier channel. After reaching the end of the amplifier array, the multiplexer rolls back to channel 0. (Note: The state of the chip is undefined at power-up, so at least one CONVERT(0) command should be sent before executing this variant of the command.)

Flags:

U flag: Setting the U (Update) flag to one updates all "triggered registers" to new values that were previously programmed.

M flag: Setting the M (Monitor) flag to one clears the compliance monitor register (Register 40).

D flag: If the D (DC amplifier) flag of a CONVERT command is set to one then the DC low-gain amplifier of channel C is also sampled (with 10-bit resolution), and its value is returned in the lower 10 bits of the result.

H flag: If the H (High-pass filter) flag of a CONVERT command is set to one when DSP offset removal is enabled (see "DSP High-Pass Filter for Offset Removal" section) then the output of the digital high-pass filter associated with amplifier channel C is reset to zero. This can be used to rapidly recover from a large transient and settle to baseline.

Command: CALIBRATE – Initiate ADC self-calibration routine (OBSOLETE)

MSB 31	30	29	28	27	26	25	24	23 – 0 LSB
0	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**00000000 00000000 00000000**

Result:

MSB 31	30 – 0 LSB
*	**0000000 00000000 00000000 00000000**

Comments:

The CALIBRATE command was included in the Intan Technologies RHD2000 family of amplifier-only chips to initiate an ADC self-calibration routine that was performed after chip power-up and register configuration. Although the command is included in this chip for continuity, **use of the CALIBRATE command is not recommended for the RHS2116**. Rather, a CLEAR command should be issued after the chip has been powered up (see next command).

Command: CLEAR – Set ADC calibration

MSB 31	30	29	28	27	26	25	24	23 – 0 LSB
0	**1**	**1**	**0**	**1**	**0**	**1**	**0**	**00000000 00000000 00000000**

Result:

MSB 31	30 – 0 LSB
*	**0000000 00000000 00000000 00000000**

Comments:

The CLEAR command initializes the ADC on the RHS2116 for normal operation. This command should be executed once after chip power-up to maximize the precision of the ADC.

The result returned by the RHS2116 consists of all zeros except for the MSB. The MSB will be zero if two's complement mode is enabled (see Register 1 description below); otherwise it will be one.

Command: WRITE(R,D) – Write data D to register R

MSB 31	30	29	28	27 – 24	23 – 16	LSB 15 – 0
1	**0**	**U**	**M**	**0000**	**R[7:0]**	**D[15:0]**

Result:

MSB 31 – 16	LSB 15 – 0
11111111 11111111	**D[15:0]**

Comments:

The WRITE(R,D) command writes a 16-bit data word D to chip register R. The data word D is echoed back to the master in the lower 16 bits of the result so that correct reception of the data word can be confirmed. The upper 16 bits of the result consist of all ones.

Any attempt to write to a read-only register (or non-existent register) will produce the same result, but in this case D will not be written to the register.

Flags:

U flag: Setting the U flag to one updates all "triggered registers" to new values that were previously programmed.

M flag: Setting the M flag to one clears the compliance monitor register (Register 40).

Command: READ(R) – Read contents of register R

MSB 31	30	29	28	27 – 24	23 – 16	LSB 15 – 0
1	**1**	**U**	**M**	**0000**	**R[7:0]**	**00000000 00000000**

Result:

MSB 31 – 16	LSB 15 – 0
00000000 00000000	**D[15:0]**

Comments:

The READ(R) command reads the contents of chip register R. The data word D is sent to the master in the lower 16 bits of the result. The upper 16 bits consist of all zeros.

Flags:

U flag: Setting the U flag to one updates all "triggered registers" to new values that were previously programmed.

M flag: Setting the M flag to one clears the compliance monitor register (Register 40).

Unknown Commands:

If an invalid command is sent (i.e., any command beginning with '01' that does not correspond to ADC calibration commands), the results returned by the chip will consist of all zeros except for the MSB. The MSB will be zero if two's complement mode is enabled (see Register 1 description below); otherwise it will be one.

On-Chip Registers

Each RHS2116 chip is capable of addressing up to 256 16-bit registers, in any combination of writable (RAM) registers and read-only (ROM) registers. **Upon power-up, all RAM registers contain indeterminate data and should be promptly configured by the SPI master device.** A CLEAR command should also be issued to set parameters that optimize ADC operation.

Individual bits in a register can be changed only by rewriting the entire 16-bit contents. Therefore, it is recommended that the SPI master device maintain a copy of RHS2116 register contents in its memory so bitwise operations can be performed there before writing the updated word to the chip using a WRITE command on the SPI bus.

The RAM registers present in each RHS2116 are described below. The detailed functions of some programmable variables were described previously in the datasheet. Note: All multi-bit variables have their most significant bits (MSBs) on the left in the diagrams below, towards the direction of the register MSB D[15]. Bits marked X have no function but should be set to zero for compatibility with any future chip versions.

Amplifier Control Registers

Register 0: Supply Sensor and ADC Buffer Bias Current

D[15:12]	D[11:6]	D[5:0]
XXXX	ADC buffer bias [5:0]	MUX bias [5:0]

MUX bias [5:0]: This variable configures the bias current of the MUX that routes the selected analog signal to the ADC input. The optimum value for this variable is a function of ADC sampling rate and is listed in a table in the "Analog-to-Digital Converter" section earlier in the datasheet.

ADC buffer bias [5:0]: This variable configures the bias current of an internal reference buffer in the ADC. The optimum value for this variable is a function of ADC sampling rate and is listed in a table in the "Analog-to-Digital Converter" section earlier in the datasheet.

Register 1: ADC Output Format, DSP Offset Removal, and Auxiliary Digital Outputs

D[15:13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3:0]
XXX	digoutOD	digout2	digout2 HiZ	digout1	digout1 HiZ	weak MISO	twoscomp	absmode	DSPen	DSP cutoff freq [3:0]

DSP cutoff freq [3:0]: This variable sets the cutoff frequency of the DSP filter used to for offset removal. See the "DSP High-Pass Filter for Offset Removal" section for details.

DSPen: When this bit is set to one, the RHS2116 performs digital signal processing (DSP) offset removal from all 16 amplifier channels using a first-order high-pass IIR filter. See the "DSP High-Pass Filter for Offset Removal" section for details.

absmode: Setting this bit to one passes all amplifier ADC conversions through an absolute value function. This is equivalent to performing full-wave rectification on the signals, and may be useful for implementing symmetric positive/negative thresholds or envelope estimation algorithms. This bit has no effect on ADC conversions from non-amplifier channels (i.e., C > 15). See the "Absolute Value Mode" section for more information.

twoscomp: If this bit is set to one, AC high-gain amplifier conversions from the ADC are reported using a "signed" two's complement representation where the amplifier baseline is reported as zero and values below baseline are reported as negative numbers. If this bit is set to zero, AC high-gain amplifier conversions from the ADC are reported using "unsigned" offset binary notation where the baseline level of a 16-bit conversion is represented as 1000000000000000. ADC conversions from DC low-gain amplifiers are always reported as unsigned binary numbers.

weak MISO: If this bit is set to zero and the **LVDS_en** pin is pulled low, the MISO line goes to high impedance mode (HiZ) when $\overline{CS}$ is pulled high, allowing multiple chips to share the same MISO line so long as only one of their chip select lines is activated at any time. If only one RHS2116 chip will be using a MISO line, this bit may be set to one, and when $\overline{CS}$ is pulled high the MISO

line will be driven weakly by the chip. This can prevent the line from drifting to indeterminate values between logic high and logic low. This variable has no effect when LVDS communication is enabled.

digout1 HiZ: The RHS2116 chips have an auxiliary digital output pin **auxout1** that may be used to activate off-chip circuitry (e.g., MOSFET switches, LEDs). Setting this bit to one puts this digital output into high impedance (HiZ) mode. See the "Auxiliary Digital Outputs" section for details.

digout1: This bit is driven out of the auxiliary CMOS digital output pin **auxout1**, provided that the **digout1 HiZ** bit is set to zero. See the "Auxiliary Digital Outputs" section for details.

digout2 HiZ: The RHS2116 chips have an auxiliary digital output pin **auxout2** that may be used to activate off-chip circuitry (e.g., MOSFET switches, LEDs). Setting this bit to one puts this digital output into high impedance (HiZ) mode. See the "Auxiliary Digital Outputs" section for details.

digout2: This bit is driven out of the auxiliary CMOS digital output pin **auxout2**, provided that the **digout1 HiZ** bit is set to zero. See the "Auxiliary Digital Outputs" section for details.

digoutOD: This bit controls an open-drain auxiliary high-voltage digital output pin **auxoutOD**. Setting this bit to one pulls the **auxoutOD** pin to VSTIM–. Setting this bit to zero puts the **auxoutOD** pin into a high impedance state. See the "Auxiliary Digital Outputs" section for details.

Register 2: Impedance Check Control

D[15:14]	D[13:8]	D[7]	D[6]	D[5]	D[4:3]	D[2:1]	D[0]
XX	Zcheck select [5:0]	X	Zcheck DAC power	Zcheck load	Zcheck scale [1:0]	XX	Zcheck en

Zcheck en: Setting this bit to one activates impedance testing mode, and connects the on-chip waveform generator to the amplifier selected by the **Zcheck select** variable. See the "Electrode Impedance Test" section for details.

Zcheck scale [1:0]: This variable selects the series capacitor used to convert the voltage waveform generated by the on-chip DAC into an AC current waveform that stimulates a selected electrode for impedance testing: 00 = 0.1 pF; 01 = 1.0 pF; 11 = 10 pF. See the "On-Chip AC Current Waveform Generator" section for more information.

Zcheck load: Setting this bit to one adds a capacitor load to the impedance checking network. This mode is only used for chip testing at Intan Technologies. This bit should always be set to zero for normal operation.

Zcheck DAC power: Setting this bit to one activates the on-chip digital-to-analog converter (DAC) used to generate waveforms for electrode impedance measurement. If impedance testing is not being performed, this bit can be set to zero to reduce current consumption (from VDD to GND) by 120 µA. See the "On-Chip AC Current Waveform Generator" section for more information.

Zcheck select [5:0]: This variable selects the electrode to be connected to the on-chip impedance testing circuitry if **Zcheck en** is set to one. In the RHS2116 16-channel chip, the two MSBs of this six-bit register is ignored. See the "Electrode Impedance Test" section for details.

Register 3: Impedance Check DAC

D[15:8]	D[7:0]
XXXXXXXX	Zcheck DAC [7:0]

Zcheck DAC [7:0]: This variable sets the output voltage of an 8-bit DAC used to generate waveforms for impedance checking. This variable must be updated at regular intervals to create the desired waveform. Note that this DAC must be enabled by setting **Zcheck DAC power** in Register 2. If impedance testing is not in progress, the value of this register should remain unchanged to minimize noise (although writing the same value to the register is acceptable). See the "On-Chip AC Current Waveform Generator" section for more information.

Registers 4-7: On-Chip Amplifier Bandwidth Select

Register 4:

D[15:11]	D[10:6]	D[5:0]
XXXXX	RH1 sel2 [4:0]	RH1 sel1 [5:0]

Register 5:

D[15:11]	D[10:6]	D[5:0]
XXXXX	RH2 sel2 [4:0]	RH2 sel1 [5:0]

Register 6:

D[15:14]	D[13]	D[12:7]	D[6:0]
XX	RL_A sel3	RL_A sel2 [5:0]	RL_A sel1 [6:0]

Register 7:

D[15:14]	D[13]	D[12:7]	D[6:0]
XX	RL_B sel3	RL_B sel2 [5:0]	RL_B sel1 [6:0]

RH1 sel1 [5:0], RH1 sel2 [4:0], RH2 sel1 [5:0], and **RH2 sel2 [4:0]:** These variables set the upper cutoff frequency of the biopotential amplifiers. A table in this datasheet provides appropriate register values for setting the upper cutoff frequency in the range of 100 Hz to 20 kHz.

RL_A sel1 [6:0], RL_A sel2 [5:0], and **RL_A sel3:** These variables set the "A version" of the lower cutoff frequency of the biopotential amplifiers. A table in this datasheet provides appropriate register values for setting the lower cutoff frequency in the range of 0.1 Hz to 1 kHz. The **amp fL select** variable in Register 12 allows users to rapidly switch amplifiers between two different lower cutoff frequencies as a means for rapidly recovering from stimulation artifacts.

RL_B sel1 [6:0], RL_B sel2 [5:0], and **RL_B sel3:** These variables set the "B version" of the lower cutoff frequency of the biopotential amplifiers. A table in this datasheet provides appropriate register values for setting the lower cutoff frequency in the range of 0.1 Hz to 1 kHz. The **amp fL select** variable in Register 12 allows users to rapidly switch amplifiers between two different lower cutoff frequencies as a means for rapidly recovering from stimulation artifacts.

Register 8: Individual AC Amplifier Power

D[15:0]
AC amp power [15:0]

AC amp power [15:0]: Setting these bits to zero powers down individual AC-coupled high-gain amplifiers, saving power if there are channels that don't need to be observed. Each amplifier consumes power in proportion to its upper cutoff frequency. Current consumption is approximately 7.6 µA/kHz per AC amplifier, from VDD to GND. Under normal operation, these bits should be set to one.

Register 9: reserved for future expansion

Register 10: Amplifier Fast Settle (TRIGGERED REGISTER)

D[15:0]
amp fast settle [15:0]

amp fast settle [15:0]: Setting any of these bits to one closes a switch in an AC high-gain amplifier that drives its analog output to the baseline "zero" level. This can be used to quickly recover from large transient events (e.g., stimulation) that may drive the amplifiers to their rails. The switch should be closed for a certain amount of time to settle the amplifiers (see "Fast Settle Function" section for details) and then this register should be reset to zero to resume normal amplifier operation. **Register 10 is a triggered**

register, meaning its value must first be programmed into an on-chip buffer using a WRITE command, and then the U flag must be asserted to update the active value of this register (and all other triggered registers on the chip).

Register 11: reserved for future expansion

Register 12: Amplifier Lower Cutoff Frequency Select (TRIGGERED REGISTER)

D[15:0]
amp fL select [15:0]

amp fL select [15:0]: These bits select between two different lower cutoff frequencies for each AC high-gain amplifier. If a particular bit is set to one, the corresponding amplifier has a lower cutoff frequency set by the **RL_A** setting in Register 6. If the bit is set to zero, the amplifier has a lower cutoff frequency set by the **RL_B** setting in Register 7. The ability to switch rapidly between two lower cutoff frequencies can be used to reduce the amplifier recovery time after stimulation artifacts. For example, under normal operation a user may wish to use a very low cutoff frequency (e.g., f_L = 0.1 Hz) to observe low-frequency signals like local field potentials (LFPs). The consequence of setting a very lot cutoff frequency is a slow recovery time with a time constant of $1/2\pi f_L$. A higher low-frequency cutoff (e.g., 250 Hz) may be used for brief periods during and/or following stimulation pulses to reduce this amplifier recovery time constant. See the "Amplifier Stimulus Artifact Recovery" section for more details. **Register 12 is a triggered register**, meaning its value must first be programmed into an on-chip buffer using a WRITE command, and then the U flag must be asserted to update the active value of this register (and all other triggered registers on the chip).

Registers 13-31: reserved for future expansion

Stimulation Control Registers

Registers 32-33: Stimulation Enable

Register 32: Stimulation Enable A

D[15:0]
stim enable A [15:0]

Register 33: Stimulation Enable B

D[15:0]
stim enable B [15:0]

stim enable A [15:0] and **stim enable B [15:0]:** These 32 bits must be set to particular "magic numbers" to enable the on-chip stimulators. If these exact values are not programmed, all stimulators are disabled. This prevents stimulators from being active when the chip is first powered up when all registers contain random data[1]. To enable stimulation, **stim enable A** must be set to binary 1010101010101010 (hex AAAA; decimal 43690) and **stim enable B** must be set to binary 0000000011111111 (hex 00FF; decimal 255). Note that the **stim_en** pin must also be pulled high (to VDD) for the on-chip stimulators to be enabled. When an RHS2116 chip is first powered up, at least one of these registers should be cleared to zero to ensure that stimulation is disabled. After all the stimulation registers have been written to and the triggered registers updated, then the proper values can be written to these two registers to enable stimulation.

[1] The chance of stimulation being enabled on power-up is not completely eliminated but is reduced to $1/2^{32}$, or approximately one in 4.3 billion. If this risk is too high, an external device can be used to hold **stim_en** low (at GND) until all on-chip registers have been properly initialized.

Register 34: Stimulation Current Step Size

D[15]	D[14:13]	D[12:7]	D[6:0]
X	step sel3 [1:0]	step sel2 [5:0]	step sel1 [6:0]

step sel1 [6:0], **step sel2 [5:0]**, and **step sel3 [1:0]:** This variable sets the step size of the 8-bit current-output DACs in each on-chip stimulator. A table earlier in the datasheet provides appropriate register values for setting the stimulation step size in the range of 10 nA/step (for a full-scale range of ±2.55 µA) to 10 µA/step (for a full-scale range of ±2.55 mA). This register is typically set once shortly after a chip is powered up, and then the stimulation current magnitudes on each channel are set to multiples of this current using Registers 64-79 and 96-111.

Register 35: Stimulation Bias Voltages

D[15:8]	D[7:4]	D[3:0]
XXXXXXXX	stim Pbias [3:0]	stim Nbias [3:0]

stim Pbias [3:0] and **stim Nbias [3:0]:** These variables configure internal bias voltages that optimize the compliance range of the stimulator circuits. The optimum values for these variables are a function of stimulation step size (set in Register 34) and are listed in a table earlier in the datasheet. This register is typically set once shortly after the chip is powered up.

Register 36: Current-Limited Charge Recovery Target Voltage

D[15:8]	D[7:0]
XXXXXXXX	charge recovery DAC [7:0]

charge recovery DAC [7:0]: This variable sets the output voltage of an 8-bit DAC used to generate a voltage in the range of -1.225V to +1.215V that is used by the current-limited charge recovery circuits. When current-limited (CL) charge recovery is enabled, an electrode is pulled toward this voltage. When this register is set to 128, the target voltage is zero. The DAC step size is 9.57 mV. When the register is set to 0, the target voltage reaches its minimum value of -1.225V. When the register is 255, the target voltage is at its maximum value of +1.215V. See the "Current-Limited Charge Recovery Circuit" section for more details.

Register 37: Charge Recovery Current Limit

D[15]	D[14:13]	D[12:7]	D[6:0]
X	Imax sel3 [1:0]	Imax sel2 [5:0]	Imax sel1 [6:0]

Imax sel1 [6:0], **Imax sel2 [5:0]**, and **Imax sel3 [1:0]:** These variables set the maximum current supplied (per channel) by the current-limited charge recovery circuit in each channel. When current-limited (CL) charge recovery is enabled, an electrode is pulled toward the voltage set by Register 36 with a current limited to the maximum current set by these variables. A table earlier in the datasheet provides appropriate register values for setting this current. See the "Current-Limited Charge Recovery Circuit" section for more details.

Register 38: Individual DC Amplifier Power

D[15:0]
DC amp power [15:0]

DC amp power [15:0]: This register was originally included on the chip to provide a modest power savings in cases where the DC-coupled low-gain amplifiers were not used. However, a hardware bug in the chip counterintuitively causes current drawn from VDD to **increase** when these amplifiers are powered down. For each DC amplifier channel that is powered down, the current from VDD increases by 1.93 mA. **It is therefore strongly recommended that Register 38 be set to all ones as soon as the chip is powered up.** This enables all DC-coupled low-gain amplifiers and reduces power consumption.

Register 39: reserved for future expansion

Register 40: Compliance Monitor (READ ONLY REGISTER WITH CLEAR)

D[15:0]
compliance monitor [15:0]

compliance monitor [15:0]: This is a read-only variable, but its contents can be cleared to zero by using the M flag during a CONVERT, READ, or WRITE command. Bits in this variable are set high when the corresponding stimulator exceeds its compliance voltage limit (either positive or negative) during stimulation and is unable to source or sink the requested current through an electrode. Typically this register is cleared prior to stimulation and checked periodically during or after stimulation to detect voltage compliance problems. See the "Compliance Monitor" section for more details.

Register 41: reserved for future expansion

Register 42: Stimulator On (TRIGGERED REGISTER)

D[15:0]
stim on [15:0]

stim on [15:0]: Bits in this variable turn on current sources in corresponding stimulators. A bit value of one activates the current source; a bit value of zero turns off the current. **Register 42 is a triggered register**, meaning its value must first be programmed into an on-chip buffer using a WRITE command, and then the U flag must be asserted to update the active value of this register (and all other triggered registers on the chip).

Register 43: reserved for future expansion

Register 44: Stimulator Polarity (TRIGGERED REGISTER)

D[15:0]
stim pol [15:0]

stim pol [15:0]: Bits in this variable set the polarity of current drive in corresponding stimulators. Setting a bit to zero produces negative current (i.e., cathodic current flowing into the chip that drives an electrode toward negative voltages). Setting a bit to one produces positive current (i.e., anodic current flowing out of the chip that drives an electrode toward positive voltages). **Register 44 is a triggered register**, meaning its value must first be programmed into an on-chip buffer using a WRITE command, and then the U flag must be asserted to update the active value of this register (and all other triggered registers on the chip).

Register 45: reserved for future expansion

Register 46: Charge Recovery Switch (TRIGGERED REGISTER)

D[15:0]
charge recovery switch [15:0]

charge recovery switch [15:0]: Bits in this variable control on-chip transistor switches that connect a selected electrode to the common **stim_GND** pin. If **stim_GND** is tied to ground, these switches can be used to reset the potential of an electrode to ground and recover any residual charge resulting from mismatched biphasic stimulation. Setting a bit to one closes the corresponding switch. Under normal operation, these bits should be set to zero. **Register 46 is a triggered register**, meaning its value must first be programmed into an on-chip buffer using a WRITE command, and then the U flag must be asserted to update the active value of this register (and all other triggered registers on the chip). See the "Charge Recovery Switch" section for more details.

Register 47: reserved for future expansion

Register 48: Current-Limited Charge Recovery Enable (TRIGGERED REGISTER)

D[15:0]
CL charge recovery enable [15:0]

CL charge recovery enable [15:0]: Bits in this variable connect a selected electrode to a current-limited driver that pulls the electrode to a voltage set by Register 36 with a maximum current set by Register 37. These drivers can be used to reset an electrode to a desired potential and recover any residual charge resulting from mismatched biphasic stimulation. Setting a bit to one connects an electrode to its current-limited driver. Under normal operation, these bits should be set to zero. **Register 48 is a triggered register**, meaning its value must first be programmed into an on-chip buffer using a WRITE command, and then the U flag must be asserted to update the active value of this register (and all other triggered registers on the chip). See the "Current-Limited Charge Recovery Circuit" section for more details.

Register 49: reserved for future expansion

Register 50: Fault Current Detector (READ ONLY REGISTER)

D[15:1]	D[0]
0000000 0000000	fault current detect

fault current detect: This read-only bit is set to one by internal circuitry if the current through the fault current detector exceeds approximately 20 µA in either direction. The exact threshold for fault current detection can vary between 10 µA and 35 µA from chip to chip. The fault current detector is typically wired in series with a common stimulation current return electrode (i.e., counter electrode), and this variable can be used to detect unintended current flow. Unlike **compliance monitor** in Register 40, the value of this variable is not latched; it reflects the real-time state of the current through the fault detector. See the "Fault Current Detector" section for more details.

Registers 51-63: reserved for future expansion

Registers 64-79: Negative Stimulation Current Magnitude (TRIGGERED REGISTERS)

D[15:8]	D[7:0]
negative current trim [7:0]	negative current magnitude [7:0]

negative current magnitude [7:0]: This variable sets the magnitude of the negative current on a particular stimulator. Registers 64-79 set negative current magnitudes on stimulation channels 0-15. The stimulation current step size is set by Register 34. **Registers 64-79 are triggered registers**, meaning values must first be programmed into on-chip buffers using a WRITE command, and then the U flag must be asserted to update the active value of these registers (and all other triggered registers on the chip). See the "Constant-Current Stimulator" section for more details.

negative current trim [7:0]: This variable can be used to trim the value of negative stimulation current over a range of approximately ±28%. This can be used to compensate for small variations in stimulation current across different stimulator channels. Normally this register should be set to a value of 128. Values less than 128 will reduce the current by about 0.2%/step; values greater than 128 will increase the current by about 0.22%/step.

Registers 80-95: reserved for future expansion

Registers 96-111: Positive Stimulation Current Magnitude (TRIGGERED REGISTERS)

D[15:8]	D[7:0]
positive current trim [7:0]	positive current magnitude [7:0]

positive current magnitude [7:0]: This variable sets the magnitude of the positive current on a particular stimulator. Registers 96-111 set positive current magnitudes on stimulation channels 0-15. The stimulation current step size is set by Register 34. **Registers 96-111 are triggered registers**, meaning values must first be programmed into on-chip buffers using a WRITE command, and then the U flag must be asserted to update the active value of these registers (and all other triggered registers on the chip). See the "Constant-Current Stimulator" section for more details.

positive current trim [7:0]: This variable can be used to trim the value of positive stimulation current over a range of approximately ±28%. This can be used to compensate for small variations in stimulation current across different stimulator channels. Normally this register should be set to a value of 128. Values less than 128 will reduce the current by about 0.2%/step; values greater than 128 will increase the current by about 0.22%/step.

Registers 112-250: reserved for future expansion

Note: All registers labeled as "reserved for future expansion" can be ignored. There are no registers on the RHS2116 corresponding to these addresses.

On-Chip Read-Only Registers

Each RHS2116 chip contains the following ROM registers that provide information on the identity and capabilities of the particular chip.

Registers 251-253: Company Designation

Register 251:

D[15:8]	D[7:0]
01001001 (ASCII 'I')	01001110 (ASCII 'N')

Register 252:

D[15:8]	D[7:0]
01010100 (ASCII 'T')	01000001 (ASCII 'A')

Register 253:

D[15:8]	D[7:0]
01001110 (ASCII 'N')	00000000

The read-only registers 251-253 contain the characters INTAN in ASCII. The contents of these registers can be read to verify the fidelity of the SPI interface.

Register 254: Number of Channels and Die Revision

D[15:8]	D[7:0]
die revision [7:0]	num of channels [7:0]

die revision [7:0]: This read-only variable encodes a die revision number which is set by Intan Technologies to encode various versions of a chip.

num of channels [7:0]: This read-only variable encodes the total number of amplifier/stimulation channels on the chip (i.e., 16).

Register 255: Intan Technologies Chip ID

D[15:8]	D[7:0]
00000000	chip ID [7:0]

chip ID [7:0]: This read-only variable encodes a unique Intan Technologies ID number indicating the type of chip. The chip ID for the RHS2116 is 32.

Example Chip Initialization Procedure

Following is a series of SPI commands that can be sent to the RHS2116 after power-up to initialize the chip for an application where all 16 channels will be sampled at a rate of 30 kS/s, along with comments. This details of these commands can be modified to suit particular uses. Consult the register descriptions on the preceding pages for more information on each operation.

SPI command	Comment
READ(255)	It is always good practice to send one "dummy" SPI command immediately following chip power-up to ensure that the on-chip digital controller in the proper state. Reading from ROM is a fine choice.
WRITE(32, 0x0000) WRITE(33, 0x0000)	Ensure that stimulation is disabled until we configure all the stimulation-related registers.
WRITE(38, 0xFFFF)	Power up all DC-coupled low-gain amplifiers to avoid excessive power consumption due to hardware bug. If this register is set to zero, an additional 30.9 mA will be drawn from VDD.
CLEAR	Initialize the on-chip ADC. Note that unlike the RHD2000 chips, the CALIBRATE command should not be used on the RHS2116 chip. Instead, the precision of the ADC is optimized by executing the CLEAR command. Unlike the CALIBRATE command, the CLEAR command does not need to be followed by dummy commands, and it can be executed prior to other register initialization.
WRITE(0, 0x00C7)	Configure the ADC and analog MUX for a total ADC sampling rate of 480 kS/s (i.e, 16 × 30 kS/s).
WRITE(1, 0x051A)	Set all auxiliary digital outputs to a high-impedance state. Set DSP high-pass filter to 4.665 Hz.
WRITE(2, 0x0040)	Power up DAC used for impedance testing, but disable impedance testing for now.
WRITE(3, 0x0080)	Initialize impedance check DAC to midrange value.
WRITE(4, 0x0016) WRITE(5, 0x0017)	Set upper cutoff frequency of AC-coupled high-gain amplifiers to 7.5 kHz.
WRITE(6, 0x00A8)	Set lower cutoff frequency of AC-coupled high-gain amplifiers to 5 Hz.
WRITE(7, 0x000A)	Set alternate lower cutoff frequency (to be used for stimulation artifact recovery) to 1000 Hz.
WRITE(8, 0xFFFF)	Power up all AC-coupled high-gain amplifiers.
WRITE(10, 0x0000) U flag = 1	Turn off fast settle function on all channels. (This command does not take effect until the U flag is asserted since Register 10 is a triggered register.)
WRITE(12, 0xFFFF) U flag = 1	Set all amplifiers to the lower cutoff frequency set by Register 6. Bits in this register can be set to zero during and immediately following stimulation pulses to rapidly recover from stimulation artifacts. (This command does not take effect until the U flag is asserted since Register 10 is a triggered register.)
WRITE(34, 0x00E2)	Set up a stimulation step size of 1 µA, giving us a stimulation range of ±255 µA on each channel.
WRITE(35, 0x00AA)	Set stimulation bias voltages appropriate for a 1 µA step size.
WRITE(36, 0x0080)	Set current-limited charge recovery target voltage to zero.
WRITE(37, 0x4F00)	Set charge recovery current limit to 1 nA.
WRITE(42, 0x0000) U flag = 1	Turn all stimulators off. (This command does not take effect until the U flag is asserted since Register 42 is a triggered register.)
WRITE(44, 0x0000) U flag = 1	Set all stimulators to negative polarity. (This command does not take effect until the U flag is asserted since Register 44 is a triggered register.)
WRITE(46, 0x0000) U flag = 1	Open all charge recovery switches. (This command does not take effect until the U flag is asserted since Register 46 is a triggered register.)
WRITE(48, 0x0000) U flag = 1	Disable all current-limited charge recovery circuits. (This command does not take effect until the U flag is asserted since Register 48 is a triggered register.)

Example chip initialization procedure (continued):

SPI command	Comment
WRITE(64, 0x8000) … WRITE(79, 0x8000) U flag = 1 in each	Write to registers 64-79, setting the negative stimulation current magnitudes to zero and the current trims to the center point. (These commands do not take effect until the U flag is asserted since Registers 64-79 are triggered registers.)
WRITE(96, 0x8000) … WRITE(111, 0x8000) U flag = 1 in each	Write to registers 96-111, setting the positive stimulation current magnitudes to zero and the current trims to the center point. (These commands do not take effect until the U flag is asserted since Registers 96-111 are triggered registers.)
WRITE(32, 0xAAAA) WRITE(33, 0x00FF)	Now that all the stimulators are initialized and turned off, enable stimulation (as long as the **stim_en** pin is pulled to VDD).
READ(255) M flag = 1	Dummy command with M flag set to clear the compliance monitor (Register 40).

The chip is now initialized. Note that it was not necessary to assert the U flag during every WRITE issued to a triggered register. Since the stimulators were disabled for most of this sequence, it would be fine to simply assert the U flag immediately prior to enabling stimulation by writing to registers 32 and 33.

Additional commands could include a series of READ commands to verify the contents of all RAM registers. Prior to executing the commands listed above, a series of READ commands to ROM registers could be issued to verify the integrity of the SPI interface and adjust the timing of MISO sampling, for example. This may be essential if the round-trip SPI bus delay is not known (e.g., due to the use of variable-length interface cables).

Following is a series of 20 commands that could be repeated in an infinite loop to sample all 16 amplifiers on the chip and update the stimulators at the amplifier sampling rate:

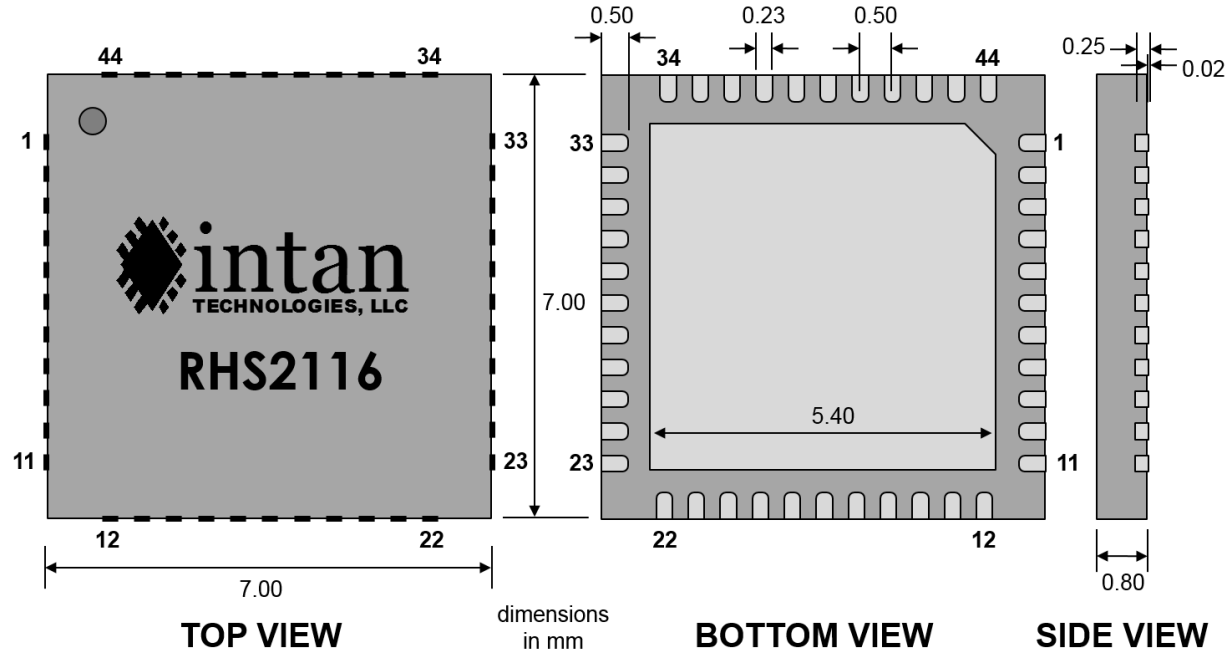
SPI command	Comment
CONVERT(0) … CONVERT(15) D flag = 1 in each	Perform ADC conversions on the AC and DC amplifiers in all 16 channels.
WRITE(?, ?) WRITE(?, ?)	Two open slots for miscellaneous tasks: updating stimulation magnitudes (Registers 64-79, 96-111), reading (and clearing) the compliance monitor (Register 40), managing artifact recovery (Register 10 and/or 12), or managing charge recovery (Register 46 and/or 48).
WRITE(44, ?)	Update polarity on all stimulators.
WRITE(42, ?) U flag = 1	Turn stimulators on or off, and trigger all changes from the last four WRITE commands.

The SPI command should be sent at a rate that sets the overall per-channel sampling rate to the desired frequency. If the sampling rate is set to 40 kS/s then the stimulators may be updated once every 25 µs. Note that if the amplifiers are not sampled and all command slots are used to control the stimulators then stimulation can be controlled with a much finer time scale. Other methods of interleaving the stimulation-related WRITE commands with ADC-related CONVERT commands are possible and may be better suited for particular applications.

Package Dimensions

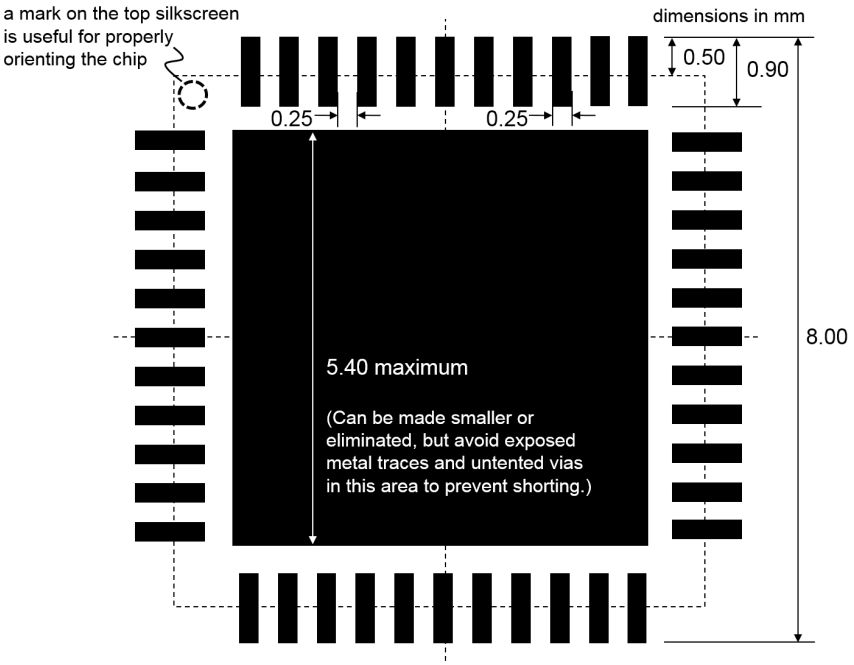
All dimensions are in millimeters.

44-Pin QFN Package



Printed Circuit Board Layout

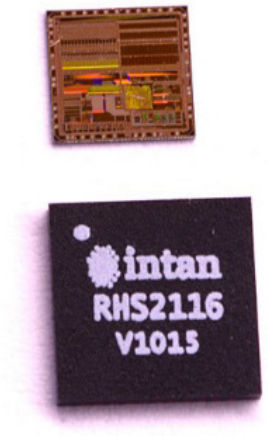
44-Pin QFN Package



Note: The center pad of the QFN is internally connected to VSTIM–. The center pad on the circuit board should tied to the negative stimulation power supply.

Pricing Information

See **www.intantech.com** for current pricing. All price information is subject to change without notice. Quantities may be limited. All orders are subject to current pricing at time of acceptance by Intan Technologies. Additional charges may apply for international purchases and shipping.



Contact Information

This datasheet is meant to acquaint engineers and scientists with the general characteristics of the RHS2116 digital electrophysiology stimulator/amplifier chip developed at Intan Technologies. We value feedback from potential end users. We can discuss your specific needs and suggest a custom integrated solution tailored to your applications.

For more information, contact Intan Technologies at:

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Document Revision History

20 January 2016:

- Original document released.

18 January 2018:

- Changed recommended value of **MUX bias** (in Register 0) for ADC sampling rates above 440 kS/s from 7 to 5 (see table, page 15).

2 February 2018:

- Added warning against leaving VSTIM+ and VSTIM– unconnected (see pages 4 and 23).

12 December 2018:

- Added soldering recommendations to minimize leakage currents (page 24).