8023A
MCC™ Manchester Code Converter

August 1985

Features

- **Compatible with IEEE 802.3 and Ethernet Rev. 1 Specification**
- **Compatible with the 8003 EDLC™ and Intel 82586 LAN Controller**
- **Directly Replaces SEEQ 8002 and 8023**
- **Manchester Data Encoding/Decoding and Receiver Clock Recovery with Phase Locked Loop (PLL)**
- **Receiver and Collision Squelch Circuit and Noise Rejection Filter**
- **Differential TRANSMIT Cable Driver**
- **Loopback Capability for Diagnostics and Isolation**
- **Fail-Safe Watchdog Timer Circuit to Prevent Continuous Transmission**
- **20 MHz Crystal Oscillator**
- **Transceiver Interface High Voltage (16 V) and Low Voltage Short Circuit Protection**
- **Low Power CMOS Technology with Single 5V Supply**
- **20 pin DIP Package**

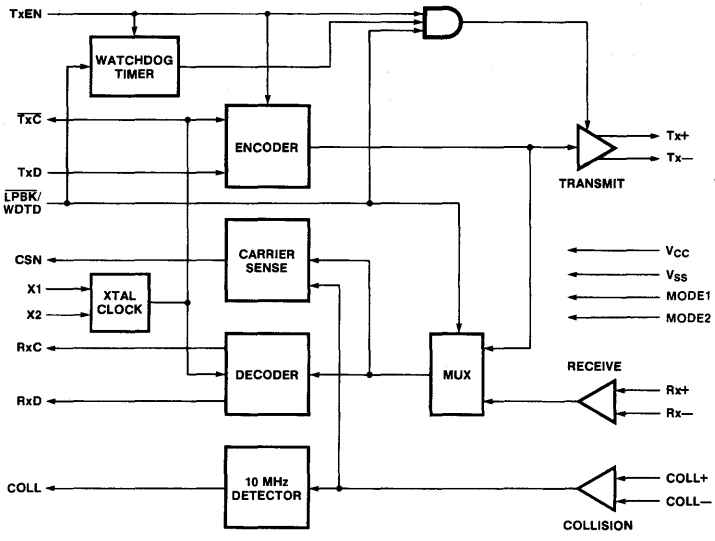
Description

The SEEQ 8023A Manchester Code Converter chip provides the Manchester data encoding and decoding functions of the Ethernet Local Area Network physical layer. It interfaces to the SEEQ 8003 Ethernet Data Link Controller or to the Intel 82586 LAN Controller and any standard Ethernet transceiver as defined by IEEE 802.3, and Ethernet Revision 1.

The SEEQ 8023A MCC™ is a functionally complete Encoder/Decoder including ECL level balanced driver and receivers, on board oscillator, analog phase locked loop for clock recovery and collision detection circuitry. In addition, the 8023A includes a 25 millisecond watchdog timer, a 4.5 microsecond window generator, and a loopback mode for diagnostic operation.

Together with the 8003 and a transceiver, the 8023A Manchester Code Converter provides a high performance minimum cost interface for any system to Ethernet.

Functional Block Diagram



Pin Configuration

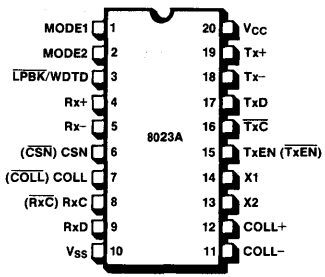


Figure 1. 8023A MCC™ Manchester Code Converter Block Diagram.

Functional Description

The 8023A Manchester Code Converter chip has two portions, transmitter and receiver. The transmitter uses Manchester encoding to combine the clock and data into a serial stream. It also differentially drives up to 50 meters of twisted pair transmission line. The receiver detects the presence of data and collisions. The 8023A MCC™ recovers the Manchester encoded data stream and decodes it into clock and data outputs. Manchester Encoding is the process of combining the clock and data stream so that they may be transmitted on a single twisted pair of wires, and the clock and data may be recovered accurately upon reception. Manchester encoding has the unique property of a transition at the center of each bit cell, a positive going transition for a "1", and a negative going transition for a "0" (See Figure 2). The encoding is accomplished by exlusive-ORing the clock and data prior to transmission, and the decoding by deriving the clock from the data with a phase locked loop.

Clock Generator

The internal oscillator is controlled by a 20 MHz parallel resonant crystal or by an external clock on X1. The 20 MHz clock is then divided by 2 to generate a 10 MHz ±0.01% transmitter clock. Both 10 MHz and 20 MHz clocks are used in Manchester data encoding.

Manchester Encoder and Differential Output Driver

The encoder combines clock and data information for the transceiver. In Manchester encoding, the first half of the bit cell contains the complementary data and the second half contains the true data. Thus, a transition is always guaranteed in the middle of a bit cell.

Data encoding and transmission begin with TxEN going active; the first is always positive for Tx(-) and negative for Tx(+). In IEEE mode, at the termination of a transmission, TxEN goes inactive and transmit pair approach to zero differential. In Ethernet mode, at the end of the transmission, TxEN goes inactive and transmit pair stay differentially high. The transmit termination can occur at bit cell center if the last bit is a one or at a bit boundary if the last bit is a zero.

To eliminate DC current in the transformer during idle, Tx ± is brought to 100 mV differential in 600 ns after the last transition (IEEE mode). The back swing voltage is guaranteed to be less than .1 V.

Watchdog Timer

A 25 ms watchdog timer is built on chip. It can be enabled or disabled by the $\overline{LPBK}$/WDTD signal. The timer starts counting at the beginning of the transmission. If TxEN goes inactive before the timer expires, the timer is reset and ready for the next transmission. If the timer expires before the transmission ends, transmission is aborted by disabling the differential transmitter. This is done by idling the differential output drivers (differential output voltage becomes zero) and deasserting CSN.

Differential Input Circuit (Rx+ and Rx–, COLL+ and COLL–)

As shown in Figure 3, the differential input for $\bar{R}x+$ and Rx- and COLL+ and COLL- are externally terminated by a pair of 39.2 Ω ± 1% resistors in series for proper impedance matching.

The center tap has a 0.01 μF capacitor, tied to ground, to provide the AC common mode impedance termination for the transceiver cable.

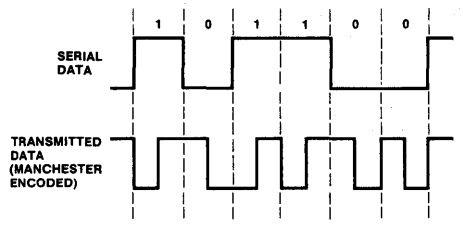


Figure 2. Manchester Coding

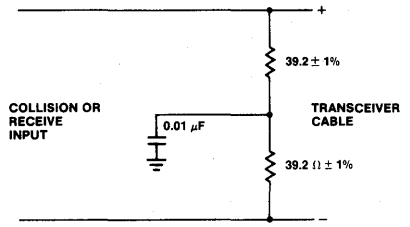


Figure 3. Differential Input Terminator

Both collision and receiver input circuits provide a static noise margin of -140 mV to -300 mV (peak value). Noise rejection filters are provided at both input pairs to prevent spurious signals. For the receiver pair, the range is 15 ns to 30 ns. For the collision pair, the range is 10 ns to 18 ns. The D.C. threshold and noise rejection filter assure that differential receiver data signal less than -140 mV in amplitude or narrower than 15 ns (10 ns for collision pair) is always rejected, signal greater than -300 mV and wider than 30 ns (18 ns for collision pair) is always accepted.

Manchester Decoder and Clock Recovery Circuit

The filtered data is processed by the data and clock recovery circuit using a phase-locked loop technique. The PLL is designed to lock onto the preamble of the incoming signal with a transition width asymmetry not greater than +8.25 ns to −8.25 ns within 12 bit cell time worst case and can sample the incoming data with a transition width asymmetry of up to +8.25 ns to −8.25 ns. The RxC high or low time will always be greater than 40 ns. If MODE2 is high or floating, RxC will be held low for 1.2 μs maximum while the PLL is acquiring lock. If MODE2 is low, RxC follows TxC for the first 1.2 μs and then switches to the recovered clock. In addition, the Encoder/Decoder asserts the CSN signal while it is receiving data from the cable to indicate the receiver data and clock are valid and available. At the end of frame, after node just finished transmitting, CSN is deasserted and will not be asserted again for a period of 4.5 μs regardless of the state of the receiver pair or collision pair. This is called the inhibit period. There is no inhabit period after packet reception. Also, RxD is held low if MODE2 is low or high if MODE 2 is high and RxC reverts to TxC. During clock switching, RxC may stay high for 200 ns maximum. ($\overline{RxC}$ stays low for 200 ns maximum, 40 ns minimum).

Collision Circuit

A collision on the Ethernet cable is sensed by the transceiver. It generates a 10 MHz ±15% differential square wave to indicate the presence of the collision. During the collision period, CSN is asserted asynchronously with RxC. However, if a collision arrives during inhabit period 4.5 μs from the time CSN was deasserted, CSN will not be reasserted.

Loopback

In loopback mode, encoded data is switched to the PLL instead of Tx+/Tx- signals. The recovered data and clock are returned to the Ethernet Controller. All the transmit and receive circuits, including noise rejection filter, are tested except differential output driver and differential input receiver circuits which are disabled during loopback. At the end of frame transmission, the 8023A also generates a 650 ns long COLL signal 550 ns after CSN was deasserted. The watchdog timer remains enabled in this mode.

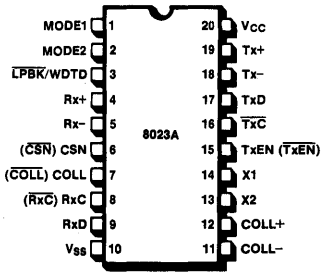


Figure 4. Pin Configuration

Pin Description

The MCC™ chip signals are grouped into four categories:

- *Power Supply and Clock*
- *Controller Interface*
- *Transceiver Interface*
- *Miscellaneous*

Power Supply

V_{CC} ..... +5V
V_{SS} ..... Ground

X1 and X2 Clock (Inputs): *Clock Crystal: 20 MHz crystal oscillator input. Alternately, pin X1 may be used as a TTL level input for external timing by floating pin X2.*

Controller Interface

RxC ($\overline{RxC}$) Receive Clock (Output): *This signal is the recovered clock from the phase decoder circuit. It is switched to TxC when no incoming data is present from which a true receive clock is derived. 10 MHz nominal and TTL compatible. If the MODE2 signal is high, RxC is inverted ($\overline{RxC}$) and there is a 1.25 μsec discontinuity at the beginning of frame reception.*

RxD Receive Data (Output) : *The RxD signal is the recovered data from the phase decoder. During idle periods, the RxD pin is LOW under normal conditions. However, if the MODE2 signal is HIGH, the RxD output will be HIGH during idle. TTL compatible. Active HIGH.*

CSN ($\overline{CSN}$) Carrier Sense (Output): *The Carrier Sense Signal indicates to the controller that there is activity on the coaxial cable. It is asserted when receive data is present or when a collision signal is present. It is deasserted at the end of frame or at the end of collision, whichever occurs later. It is asserted or deasserted synchronously with RxC. TTL compatible. Normally active HIGH, unless MODE2 is HIGH, in which case $\overline{CSN}$ is active LOW.*

$\overline{TxC}$ Transmit Clock (Output): *A 10 MHz signal derived from the internal oscillator. This clock is always active. TTL compatible.*

TxD Transmit Data (Input): *TxD is the serial input data to be transmitted. The data is clocked into the MCC by $\overline{TxC}$. Active HIGH, TTL compatible.*

TxEN ($\overline{TxEN}$) Transmit Enable (Input): *Transmit Enable, when asserted, enables data to be sent to the cable. It is asserted synchronously with $\overline{TxC}$. TxEN goes active with the first bit of transmission. TTL compatible. If MODE2 is HIGH, TxEN is inverted.*

COLL ($\overline{COLL}$) Collision (Output): *When asserted, indicates to the controller the simultaneous transmission of two or more stations on network cable. TTL compatible. If MODE2 is HIGH, COLL is inverted.*

Transceiver Interface

Rx+ and Rx- Differential Receiver Input Pair (Input): *Differential receiver input pair which brings the encoded receive data to the 8023A. The last transition is always positive-going to indicate the end of the frame.*

COLL+ and COLL- Differential Collision Input Pair (Input): *This is a 10 MHz ±15% differential signal from the transceiver indicating collision. The duty cycle should not be worse than 60%/40% —40%/60%. The last transition is positive-going.*

Tx+ and Tx- Differential Transmit Output Pair (Output): *Differential transmit pair which sends the encoded data to the transceiver. The cable driver buffers are source follower and require external 243 Ω resistors to ground as loading. 200 ns following the last transition, the differential voltage is slowly reduced to zero volts in 8 μs to limit the back swing of the coupling transformer to less than 0.1 V.*

Miscellaneous

MODE1 (Input): *This pin is used to select between AC or DC coupling. When it is tied high or left floating, the output drivers provide differential zero signal during idle (IEEE 802.3 specification). When pin 1 is tied low, then the output is differentially high when idle (Ethernet Rev. 1 specification).*

MODE2 (Input): *The MODE2 Input signal is normally active LOW. In this configuration, the 8023A operates in a mode compatible with the SEEQ 8003. An alternate mode of operation may be achieved by configuring the MODE signal active HIGH, or by allowing it to float HIGH with its internal pullup. In this configuration, RxC, TxEN, CSN and COLL become active LOW. In addition, RxD is HIGH during idle, and RxC has a 1.2 μs discontinuity during signal acquisition.*

$\overline{LPBK}$/WDTD Loopback/Watchdog Timer Disable (Input):

Normal Operation: *For normal operation this pin should be HIGH or tied to V_{CC}. In normal operation the watchdog timer is enabled.*

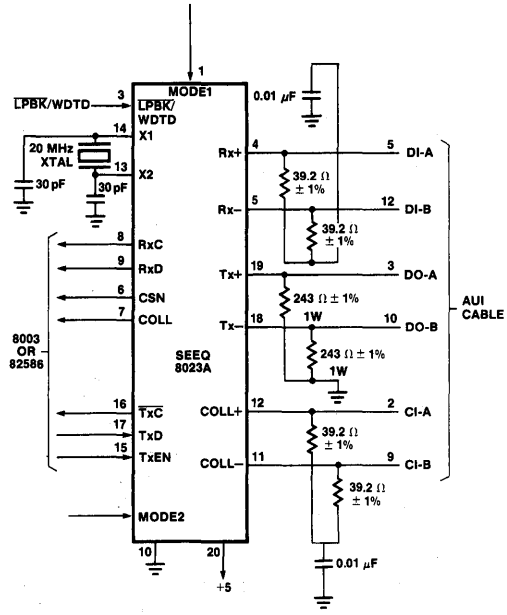


Figure 5. 8023A Interface

Loopback: *When this pin is brought low, the Manchester encoded transmit data from TxD and TxC is routed through the receiver circuit and sent back onto the RxD and RxC Pins. During loopback, Collision and Receive data inputs are ignored. The transmit pair is idled. At the end of transmission, the signal quality error test (SQET) will be simulated by asserting collision during the inhibit window. During loopback, the watchdog timer is enabled.*

Watchdog Timer Disable: *When this pin is between 10 V (Min.) and 16 V (Max.), the on chip 25 ms Watchdog Timer will be disabled. The watchdog timer is used to monitor the transmit enable pin. If TxEN is asserted for longer than 25 ms, then the watchdog timer (if enabled) will automatically deassert CSN and inhibit any further transmissions on the Tx+ and Tx− lines. The watchdog timer is automatically reset each time TxEN is deasserted.*

Interconnection to a Data Link Controller

Figure 6 shows the interconnections between the 8023A MCC™ and SEEQ's 8003 EDLC™. There are three connections for each of the two transmission channels, transmit and receive, plus the Collision Signal line (COLL).

Transmitter connections are:

Transmit Data, TxD
Transmit Clock, $\overline{TxC}$
Transmit Enable, TxEN
Collision, COLL

Receiver connections are:

Receive Data, RxD
Receive Clock, RxC
Carrier Sense, CSN

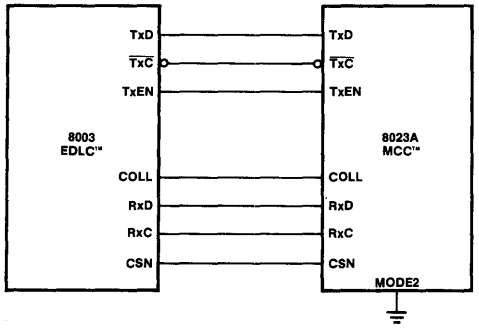


Figure 6. Interconnection of 8023A and 8003

Compatibility with Other LAN Controllers

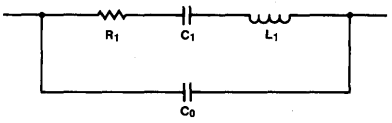
SEEQ's 8023A is compatible with other LAN Controllers, such as the 82586, when Pin 2 (MODE2) of the 8023A is floating or tied to V_{CC}. In this mode of operation, timing and polarity on the controller interface lines are compatible, with the 82586 specification dated March 1984.

Use of Time Domain Reflectometry in the 82586 is not recommended since the TDR transmission does not have a valid preamble.

D.C. and A.C. Characteristics and Timing

Crystal Specification

Resonant Frequency (C_L = 20 pF)	*20 MHz ± 0.005% 0–70° C and ± 0.003% at 25° C*
Type	*Fundamental Mode*
Circuit	*Parallel Resonance*
Load Capacitance (C_L)	*20 pF*
Shunt Capacitance (C_O)	*7 pF Max.*
Equivalent Series Resistance (R1)	*25 Ω Max.*
Motional Capacitance (C1)	*0.02 pF Max.*
Drive Level	*2 mW*



EQUIVALENT CIRCUIT OF CRYSTAL

Absolute Maximum Ratings*

Storage Temperature ..... −65° C to 150° C
All Input and Output Voltage ..... −0.3 to V_{CC} +0.3
V_{CC} ..... −0.3 to 7V
(Rx±, Tx±, COLL±) High Voltage Short Circuit Immunity ..... −0.3 to 16V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. Characteristics $T_A = 0°C$ –70° C; $V_{CC} = 5\ V \pm 10\%$

Symbol	Parameter	Min.	Max.	Units	Conditions
I_{IL}	Input Leakage Current (except MODE1, MODE 2 Receive and Collision Pairs)		10	µA	$0 \le V_{IN} \le V_{CC}$
	MODE1 and MODE2 Input Leakage Current		200	µA	$0 \le V_{IN} \le V_{CC}$
	Receive and Collision Pairs (Rx±, COLL±) Input Leakage Current		2	mA	$V_{IN} = 0$
I_{CC}	V_{CC} Current		100	mA	
V_{IL}	TTL Input Low Voltage	−0.3	0.8	V	
V_{IH}	TTL Input High Voltage (except X1)	2.0	V_{CC}	V	
	X1 Input High Voltage	3.5	V_{CC}	V	
V_{OL}	TTL Output Low Voltage except $\overline{TxC}$		0.4	V	$I_{OL} = 2.1$ mA
	$\overline{TxC}$ Output Low Voltage		0.4	V	$I_{OL} = 4.2$ mA
V_{OH}	TTL Output High Voltage (except RxC, $\overline{TxC}$, RxD	2.4		V	$I_{OH} = -400$ µA
	RxC, $\overline{TxC}$, RxD Output High Voltage	3.9		V	$I_{OH} = -400$ µA
V_{ODF}	Differential Output Swing	± 0.55	± 1.2	V	78Ω Termination Resistor and 243Ω Load Resistors
V_{OCM}	Common Mode Output Voltage	$V_{CC} - 2.5$	$V_{CC} - 1$	V	78Ω Termination Resistor and 243Ω Load Resistors
V_{BKSV}	Tx± Backswing Voltage During Idle		0.1	V	Shunt inductive load ≥ 27 µH
V_{IDF}	Input Differential Voltage (measured differentially)	±0.3	±1.2	V	
V_{ICM}	Input Common Mode Voltage	0	V_{CC}	V	
C_{IN}	Input Capacitance		15	pF	
C_{OUT}	Output Capacitance		15	pF	

A.C. Test Conditions

Output Loading TTL Output: — *1 TTL gate and 20 pF capacitor*

Differential Output: — *243Ω resistor and 10 pF capacitor from each pin to V_{SS} and a termination 78Ω resistor load resistor in parallel with a 27 µH inductor between the two differential output pins*

Differential Signal Delay Time Reference Level: — *50% point of swing*

Differential Output Rise and Fall Time: — *20% to 80% points*

RxC, $\overline{TxC}$, X1 High and Low Time: — *High time measured at 3.0V*
Low time measured at 0.6V

RxD, RxC, $\overline{TxC}$, X1 Rise and Fall Time: — *Measured between 0.6V and 3.0V points*

TTL Input Voltage (except X1): — *0.8V to 2.0V with 20 ns rise and fall time*

X1 Input Voltage: — *0.8V to 3.5V with 5 ns rise and fall time*

Differential Input Voltage: — *At least 300 mV with rise and fall time of 10 ns measured between -0.2V and +0.2V*

Transmit Timing $T_A = 0°C - 70°C$; $V_{CC} = 5\ V \pm 10\%$

Symbol	Parameter	Min.	Max.	Units
t_6	$\overline{TxC}$ Cycle Time	99.99	100.01	ns
t_7	$\overline{TxC}$ High Time	40		ns
t_8	$\overline{TxC}$ Low Time	40		ns
t_9	$\overline{TxC}$ Rise Time		5	ns
t_{10}	$\overline{TxC}$ Fall Time		5	ns
t_{11}	TxEN Setup Time if Mode2=0 TxEN Setup Time if Mode 2=1	 55		 ns
t_{12}	TxD Setup Time if Mode2=0 TxD Setup Time if Mode2=1	40 55		ns ns
t_{13}	Bit Center to Bit Center Time	99.5	100.5	ns
t_{14}	Bit Center to Bit Boundary Time	49.5	50.5	ns
t_{15}	Tx+ and Tx- Rise Time	49.5	5	ns
t_{16}	Tx+ and Tx- Fall Time		5	ns
t_{17}	Transmit Active Time From The Last Positive Transition	200		ns
t_{17A}	From Last Positive Transition of the Transmit Pair to Differential Output Approaches	400	600	ns
t_{17B}	From Last Positive Transition of the Transmit Pair to Differential Output Approaches Within 40 mV of 0 V		7000	ns
t_{18}	Tx+ and Tx- Output Delay Time		65	ns
t_{19}	TxD Hold Time if Mode2=0 TxD Hold Time if Mode2=1	5 0		ns ns
t_{20}	TxEN Hold Time if Mode2=0 TxEN Hold Time if Mode1=1	5 0		ns ns

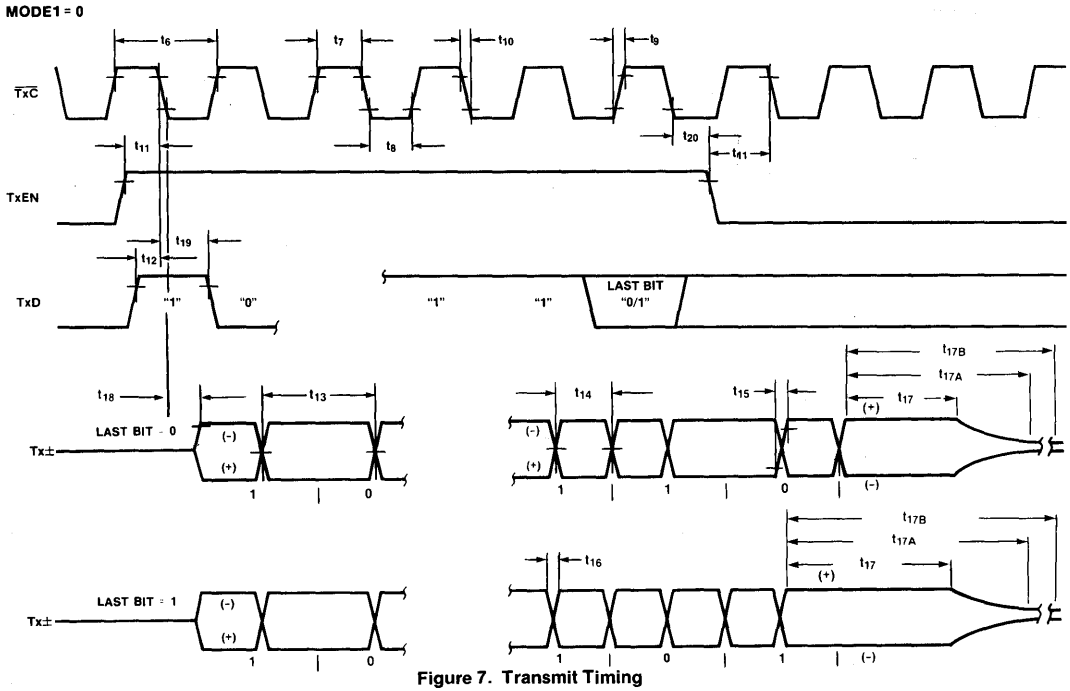


Figure 7. Transmit Timing

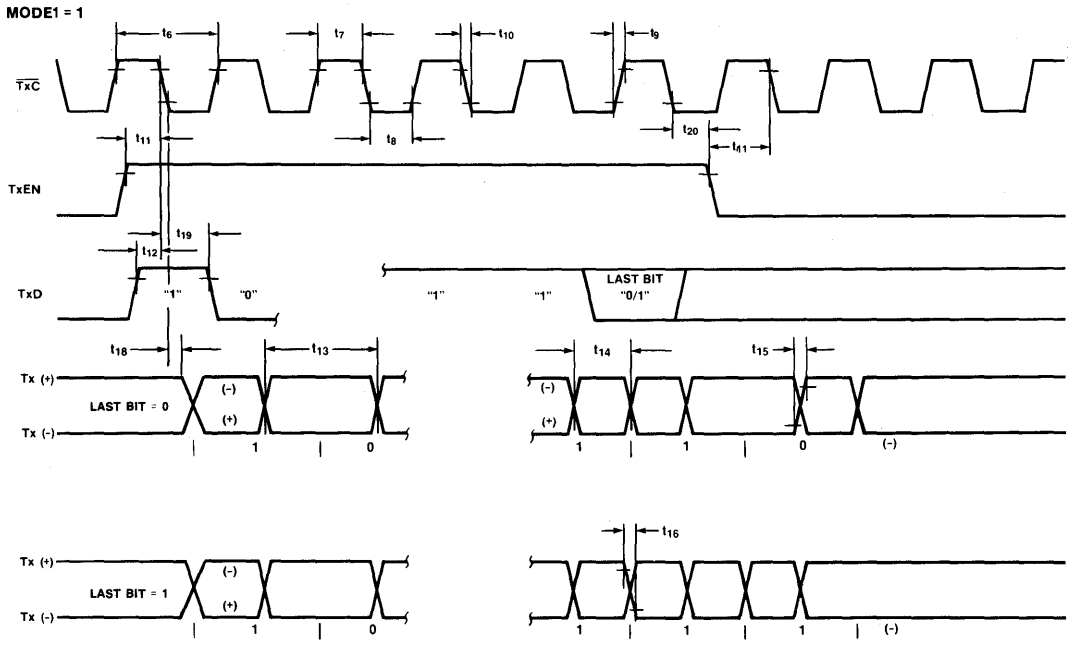


Figure 7. Transmit Timing

Receive Timing $T_A = 0°C$ –$70°C$; $V_{CC} = 5\ V \pm 10\%$

Symbol	Parameter	Min.	Max.	Units
t_{21}	CSN Asserts Delay Time		240	ns
t_{22}	CSN Deasserts Delay Time (measured from Last Bit Boundary)		240	ns
t_{23}	CSN Asserts and Deasserts Delay Time	30	70	ns
t_{23A}	$\overline{CSN}$ Deassertion Delay Time	10	35	ns
t_{24}	RxD Delay Time	30	70	ns
t_{26}	RxC, $\overline{RxC}$ Rise and Fall Time		5	ns
t_{27}	During Clock Switch RxC Keeps High, $\overline{RxC}$ Keeps Low Time	40	200	ns
t_{28}	RxC, $\overline{RxC}$ High and Low Time	40		ns
t_{29}	RxC, $\overline{RxC}$ Clock Cycle Time (during data period)	95	105	ns
t_{30}	CSN Inhibit Time (on Transmission Node only)	4.3	4.6	μs
t_{31}	Rx+/Rx– Rise and Fall Time		10	ns
t_{32}	$\overline{RxC}$ Held Low Duration from First Valid Negative-Going Transition	1.15	1.35	μs
t_{33}	$\overline{RxC}$ Stops Delay Time from First Valid Negative-Going Transition		240	ns
t_{34}	Rx+/Rx- Begin Return to Zero from Last Positive-Going Transition	160		ns
t_{35}	RxD Rise Time		10	ns
t_{36}	RxD Fall Time		10	ns

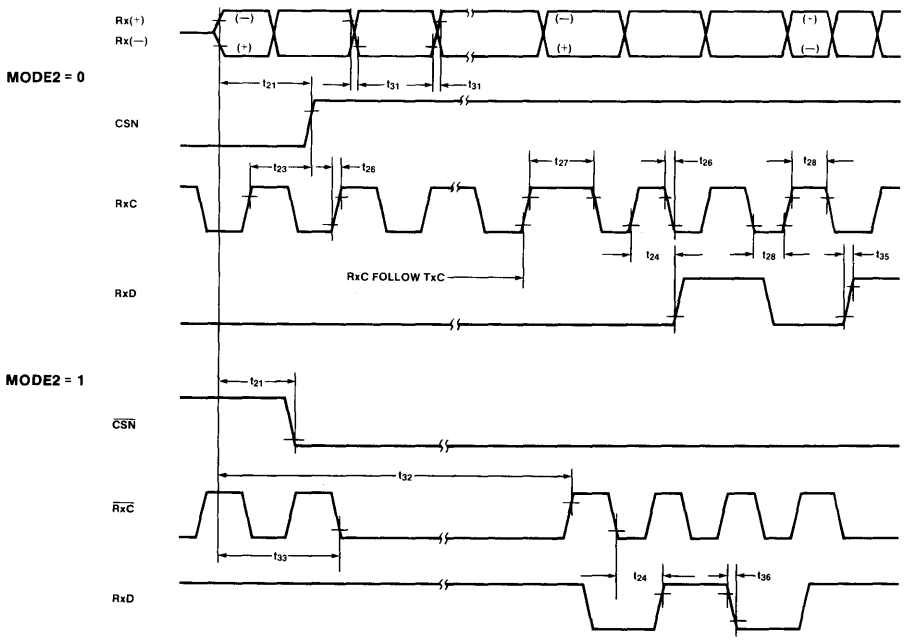


Figure 9. Receive Timing — Start of Packet

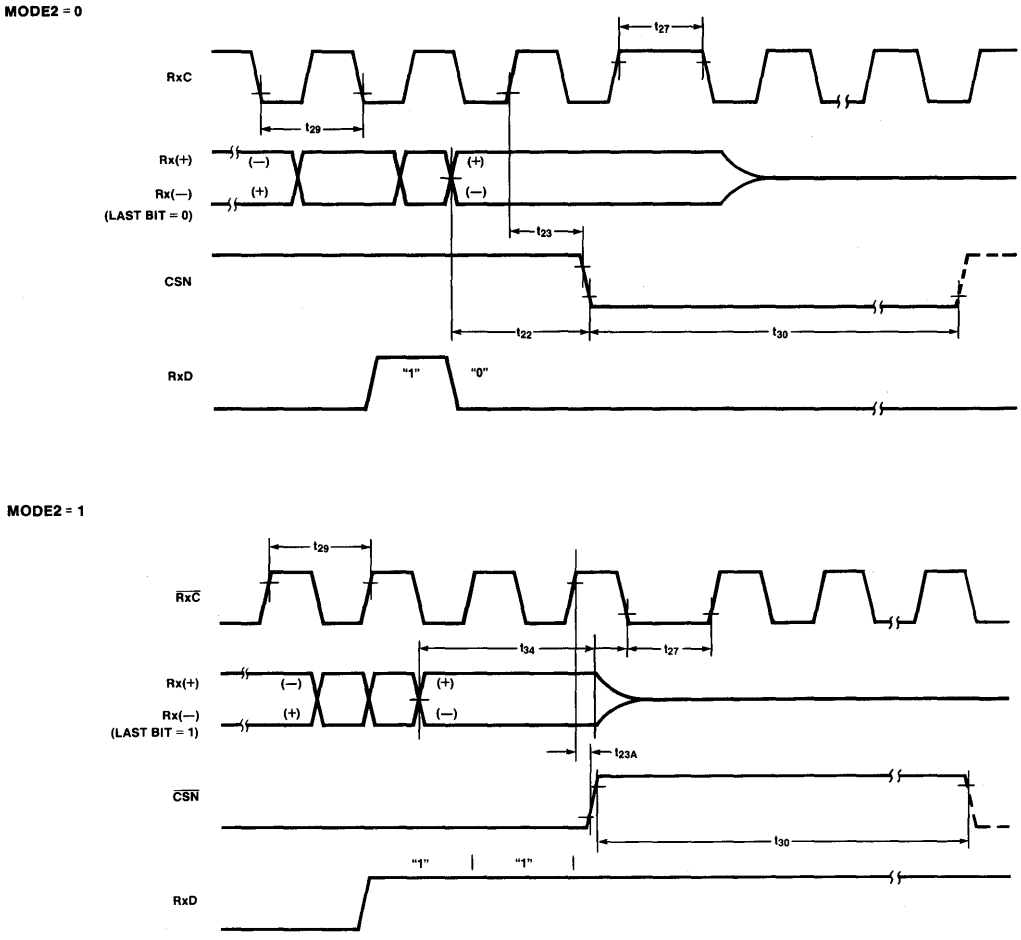


Figure 10. Receive Timing — End of Packet

Collision Timing $T_A = 0°C$ –$70°C$; $V_{CC} = 5\ V \pm 10\%$

Symbol	Parameter	Min.	Max.	Units
t_{51}	COLL+/COLL— Cycle Time	86	118	ns
t_{52}	COLL+/COLL— Rise and Fall Time		10	ns
t_{53}	COLL+/COLL— High and Low Time	35	70	ns
t_{54}	COLL+/COLL— Width (measured at –0.3V)	26		ns
t_{55}	COLL Asserts Delay Time		100	ns
t_{56}	COLL Deasserts Delay Time		180	ns
t_{57}	CSN Asserts Delay Time		200	ns
t_{58}	CSN Deasserts Delay Time		280	ns

Notes:

1. COLL+ and COLL- asserts and deasserts COLL, asynchronously, and asserts and deasserts CSN synchronously with RxC.
2. If COLL+ and COLL- arrives within 4.5μs from the time CSN was deasserted; CSN will not be reasserted (on transmission node only).
3. When COLL+ and COLL- terminates, CSN will not be deasserted if Rx+ and Rx- are still active.
4. When the node finishes transmitting and CSN is deasserted, it cannot be asserted again for 4.5 μs.
5. If MODE2 = 1, then COLL and CSN are inverted.

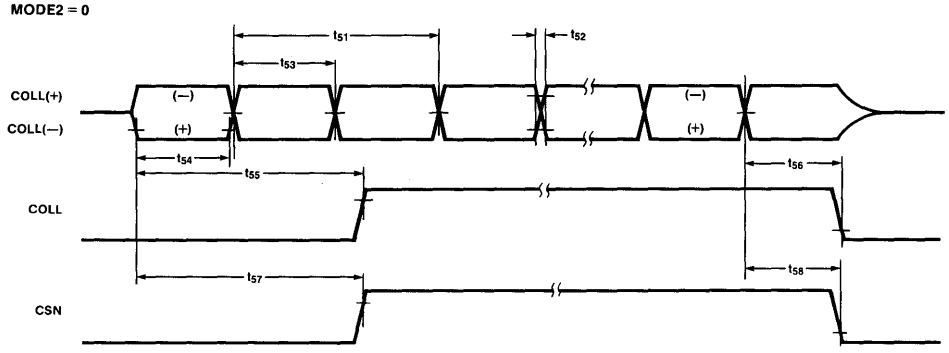


Figure 11. Collision Timing

20 MHz TTL Clock Input Timing $T_A = 0°C - 70°C$; $V_{CC} = 5\ V \pm 10\%$

Symbol	Parameter	Min.	Max.	Units
t_1	X1 Cycle Time	49.995	50.005	ns
t_2	X1 High Time	15		ns
t_3	X1 Low Time	15		ns
t_4	X1 Rise Time		5	ns
t_5	X1 Fall Time		5	ns
t_6	X1 to $\overline{TxC}$ Delay Time	10	30	ns

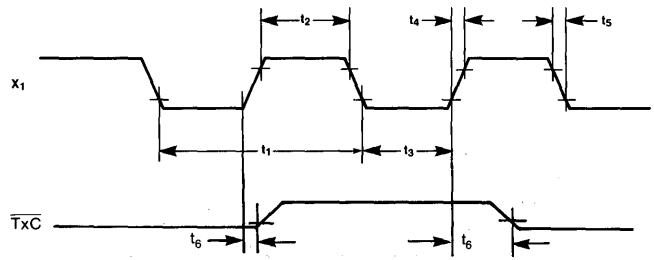


Figure 12. 20 MHz TTL Clock Timing

Loopback Timing $T_A = 0°C$ –$70°C$; $V_{CC} = 5\ V \pm 10\%$

Symbol	Parameter	Min.	Max.	Units
t_{61}	LPBK Setup Time	500		ns
t_{62}	LPBK Hold Time	5		μs
t_{63}	In Collision Simulation, COLL Signal Delay Time	475	625	ns
t_{64}	COLL Duration Time	600	750	ns

Note:

1. PLL needs 12-bit cell times to acquire lock, RxD is invalid during this period. RxC is low for 1.2 μs (max). RxD = 0 if MODE2 = 0. RxD = 1 if MODE2 = 1.

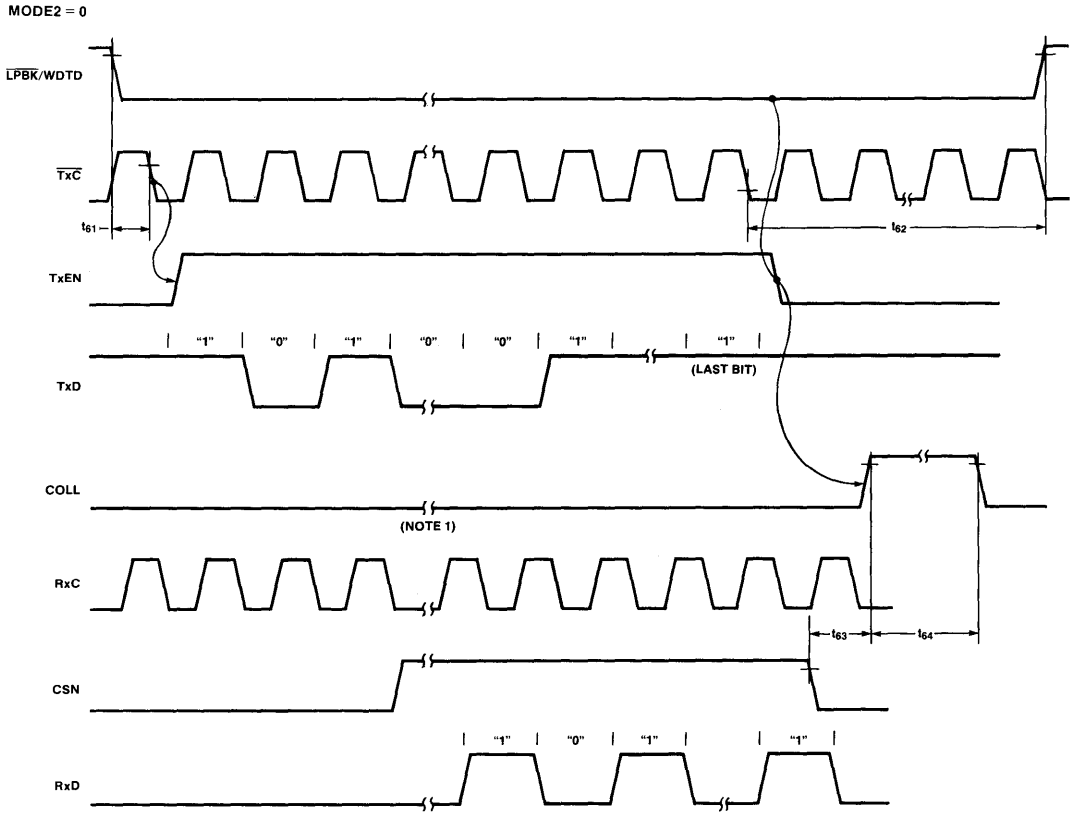


Figure 13. Loopback Timing

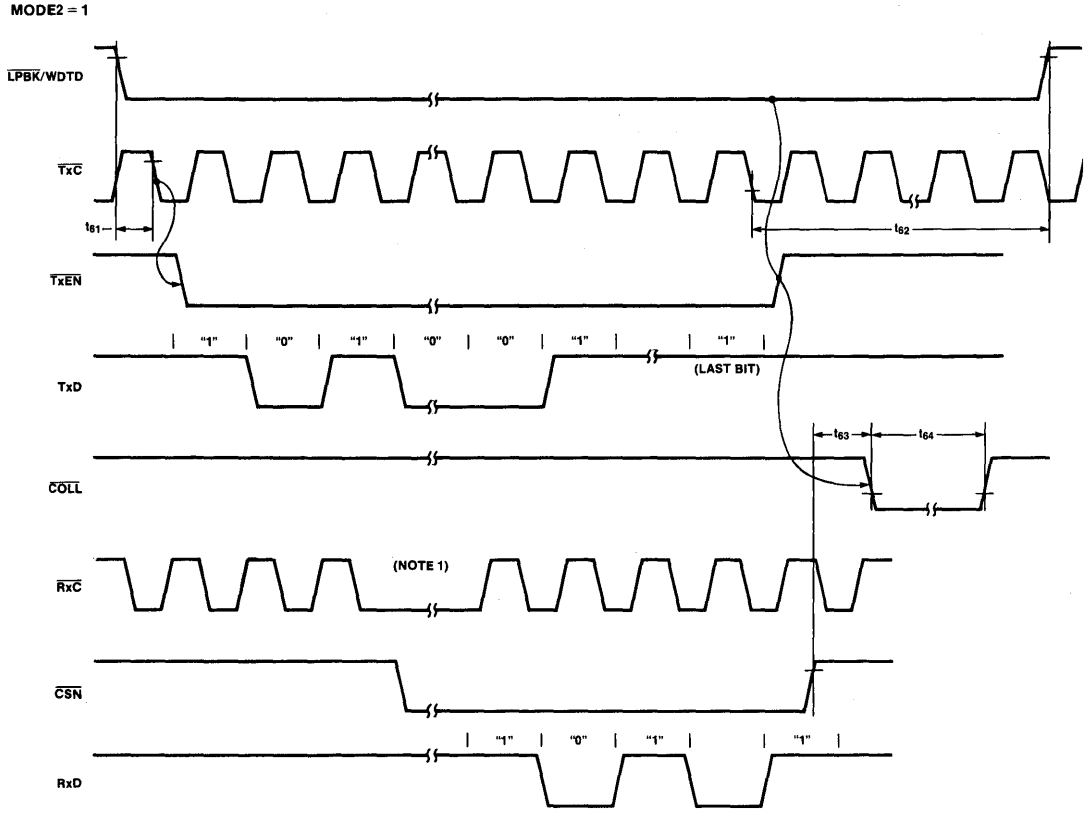


Figure 14. Loopback Timing — (Cont.)

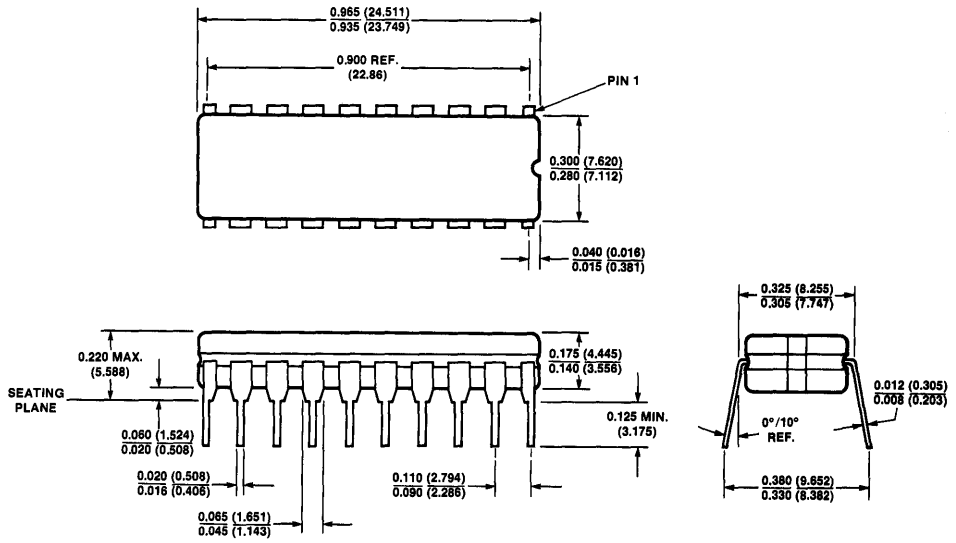
Ordering and Package Information

PART NUMBER

D Q 8023

- 8023 — PRODUCT: MCC™ MANCHESTER CODE CONVERTER
- Q — TEMPERATURE RANGE: 0° C TO 70° C
- D — PACKAGE: CERDIP

20-LEAD HERMETIC CERDIP
PACKAGE TYPE D



NOTES:
1. FOR SOLDER DIPPED LEADS, THICKNESS WILL BE 0.020 MAX.
2. ALL DIMENSIONS ARE IN INCHES AND (MILLIMETERS).