

CHAPTER 3

DECNA CONTROLLER OPTION MODULE

3.1 INTRODUCTION

This chapter is a physical and functional description of the Digital Ethernet CTI Bus Network Adapter (DECNA) controller option module. This chapter describes the DECNA option module, how it connects to other devices, and how it works on a hardware functional block level.

The DECNA option module is an Ethernet communications controller for Professional 300 series computer systems. It allows a computer to exchange data with other computers and work stations on a local area network that uses PRO/DECnet software, or with other networks that use the Ethernet communications system.

3.2 PHYSICAL DESCRIPTION

The DECNA option module (Figure 3-1) is a standard-size printed circuit board that installs into one option slot on a Professional 300 series computer system. This module has a single 90-pin zero insertion force (ZIF) connector (J1) and connects via the bus and system module to a 15-pin D-subminiature-type connector (NET 1) on the back of the Professional 300 Series system box.

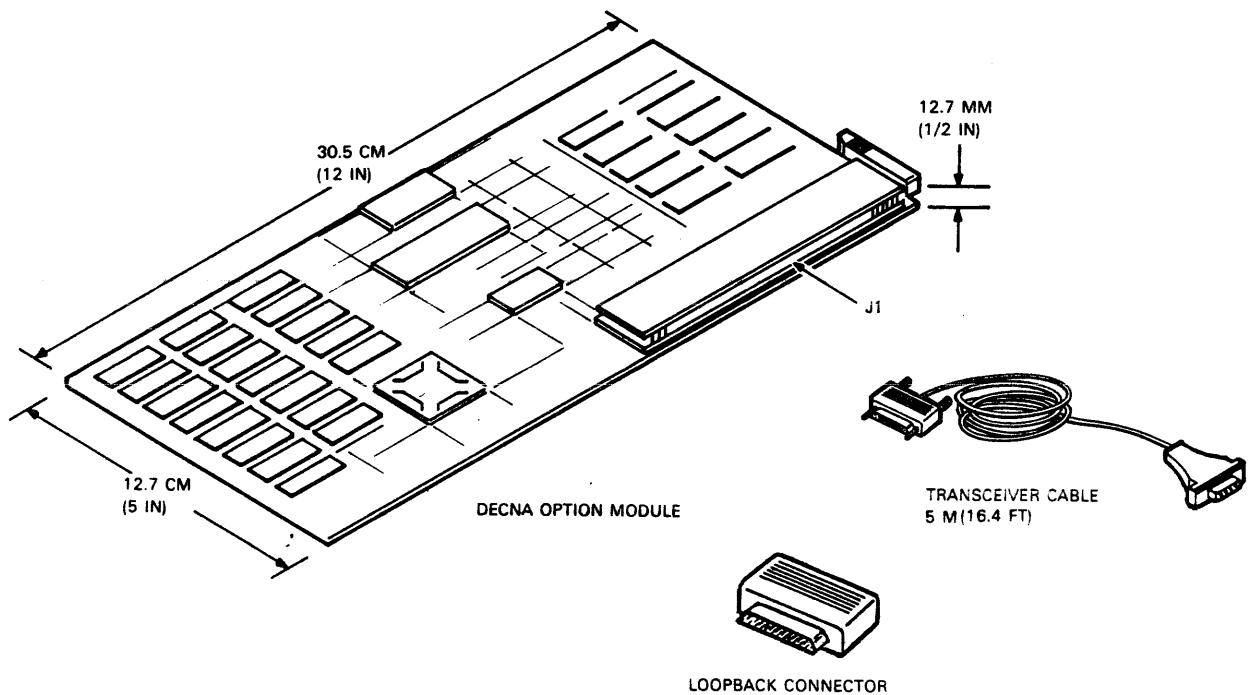


Figure 3-1 DECNA Option Module, Transceiver Cable 5 Loopback Connector

MA-0430-84

A 5 m (16.4 ft) PVC transceiver cable, with a thumbscrew connector on one end and a standard slide-lock connector on the other end, is supplied with the DECNA option module. A loopback connector and a maintenance diskette are also supplied.

3.3 SPECIFICATIONS

The DECNA option module performs specified data link and physical channel functions, which permit 10 Mbit/s data communications between stations separated by up to 2.8 km (4923 ft). The DECNA option module complies with the Xerox/Intel/Digital Ethernet Specification Version 2.0.

The DECNA option module uses less than 3.0 A at +5 V, and does not draw any current from the +12 V supply. The Professional 300 host system provides up to +12 V at 0.5 A to the transceiver via the transceiver cable connector.

Physical Specifications

Height	12.7 cm (5 in)
Length	30.5 cm (12 in)
Width	12.7 mm (1/2 in)

Environmental Specifications

Temperature	15°C (59°F) to 32°C (90°F)
Humidity	20% to 80%
Wet bulb reading	25°C (77°F) maximum
Dew point	2°C (36°F) minimum

3.4 ETHERNET OVERVIEW

Ethernet is a local area high-speed (10 Mbit/s) communications network extending from several hundred to several thousand feet.

3.4.1 Main Physical Components

Ethernet includes the following main physical components (Figure 3-2).

1. 50 ohm coaxial cable with 50 ohm terminators on each end
2. Transceivers that transmit and receive signals on the coaxial cable

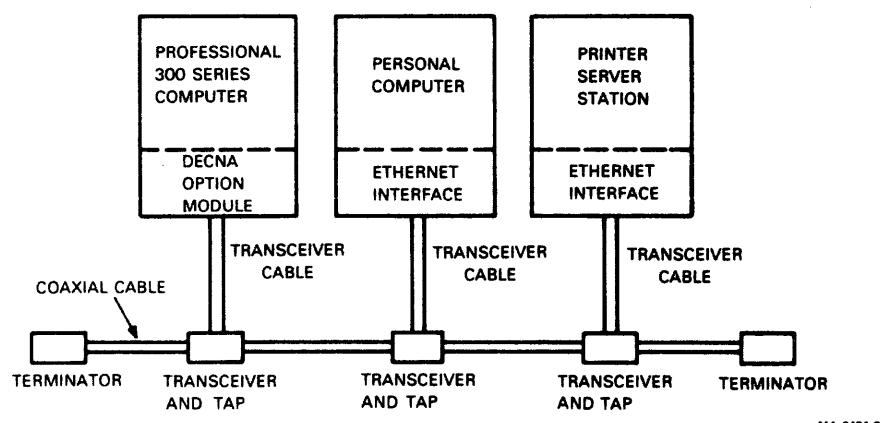


Figure 3-2 Ethernet Elements (Example)

3. Transceiver cables that connect the Ethernet interface to the transceivers
4. Ethernet interface (for example, the DECNA option module) that provides data encapsulation and decapsulation, network link management, and encoding/decoding of the signal to and from the transceivers

3.4.2 Ethernet Protocol

The Ethernet specifications, key elements are the rules for using the coaxial cable. These rules determine how a station transmits information over the coaxial cable. These rules are called CSMA/CD rules (Carrier Sense, Multiple Access, with Collision Detection). The Ethernet interface was designed to adhere to these rules.

Carrier Sense means that any station that wants to transmit monitors the line first to see if the cable is busy. The station waits until the cable is idle before transmitting.

Multiple Access means that any station can transmit. There is no central controller that decides which station can transmit and when it can transmit. This is distributed control, where all stations are equal and have equal access to the cable.

Collision Detection means that when the cable is free, a station can start transmitting. Any transmitting station monitors the line to detect any other station that is transmitting at the same time and causing a collision. If such a collision is detected, the transmitting station continues transmitting for a fixed time to make sure all other transmitting stations also detect the collision. This is called a "jam." After a jam, transmitting stations stop transmitting for a random period of time before trying again. The random wait period increases by an algorithm defined in the protocol so that collisions are resolved even if many terminals are colliding.

3.4.3 Transmission Frame Format

Figure 3-3 shows the Ethernet frame format for transmitting on the coaxial cable. The following text describes the Ethernet frame format.

The *Preamble* (64 bits) provides receive synchronization.

The *Destination Address* field (48 bits) specifies the station(s) for which the frame is intended. The address value can be: the physical address of one station, a multicast group address associated with one or more stations, or the broadcast address for simultaneous transmission to all network stations.

The *Source Address* field (48 bits) specifies the transmitting station's physical address. Each Ethernet interface has a unique physical address assigned to it when it is built. During transmission, the interface inserts its unique physical address into the source address field.

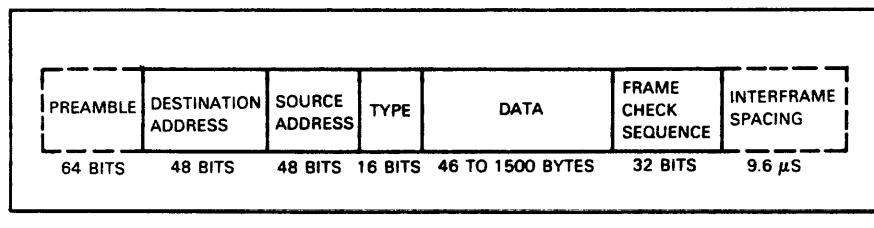


Figure 3-3 Ethernet Frame Format

The *Type* field is specified by the user for use by high level network protocols. This field tells the receiving station how to interpret the contents of the data field.

The *Data* field can contain a variable number of data bytes ranging from 46 to 1500 bytes. This field can accept less than 46 bytes by automatically inserting null characters to complete a 46-byte minimum frame size.

The *Frame Check Sequence* field (32 bits) contains a 32-bit cyclic redundancy check (CRC) value generated by the interface during transmission.

The *Interframe Spacing* consists of a minimum of $9.6\mu s$ quiet period at the end of the data packet.

3.5 DECNA FUNCTIONAL OVERVIEW

The DECNA option module accepts data from the Professional 300 series computer system, groups the data into message packets according to the Ethernet frame format, then sends the packets through the Ethernet network. The module also receives, decodes, and stores incoming message packets for computer system access.

The DECNA option module is functionally divided into the following three major circuits (Figure 3-4).

- CTI Bus interface
- Dual-ported memory
- Ethernet interface

The *CTI BUS interface* is a slave interface. It provides buffers, latches, registers, and decoding logic for interfacing between the host system and the DECNA option module. It has direct link memory access to the dual-ported memory. The CTI Bus accesses registers via the I/O page. Paragraph 3.6 describes the CTI Bus Interface in detail.

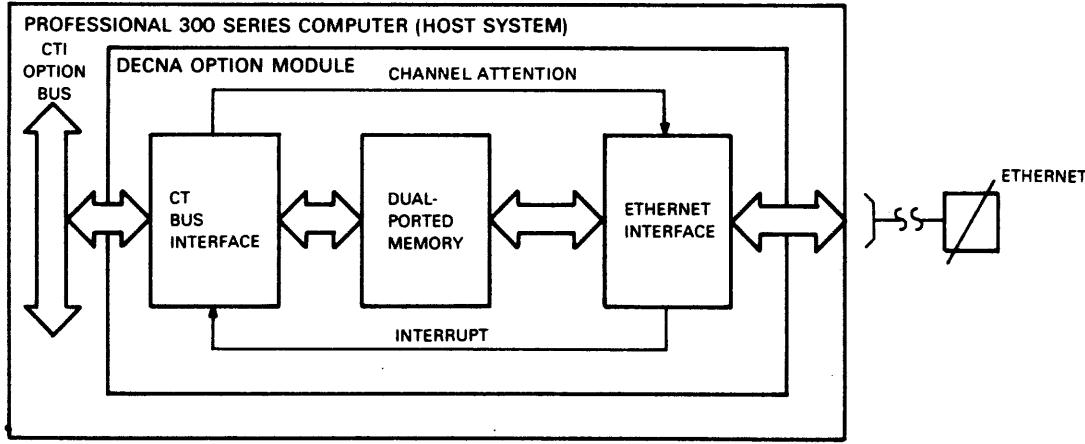


Figure 3-4 DECNA Option Module Major Functional Block Diagram

The *dual-ported memory* (128 kilobytes) provides a shared access area for the memory resident command, status, and data buffers. It is an extension of host system memory. The host system can use parts of the dual-ported memory to store data and Ethernet commands. The dual-ported memory appears in the 22-bit address space outside of the I/O page. It has large buffering capability and looks like slave memory on the CTI Bus. For transmission the host system loads the dual-ported memory. The Ethernet interface then transfers the stored data at any rate it wants. For reception, the dual-ported memory stores large amounts of incoming data, which the host system can access. The dual-ported memory is enabled or disabled by a software-accessible bit through the CTI Bus interface. Paragraph 3.7 describes the dual-ported memory in detail.

The *Ethernet interface* is further divided into two major circuits: the Ethernet communications controller and the Ethernet serial interface (Figure 3-5). The Ethernet communications controller handles the Ethernet data link layer protocol and controls how the DECNA option module uses the link. During transmission, the Ethernet interface collects information from shared memory, prepares packets for transmission, and controls packet transmission. During reception, the Ethernet interface assembles data received into word format and loads messages into shared memory. The Ethernet interface provides the Ethernet physical layer cable interface. This circuit generates 10 Mbits/s data rates, performs Manchester encoding/decoding of packet information, and monitors channel access. Paragraph 3.8 describes the Ethernet interface in detail.

3.5.1 Initialization

The entire DECNA option module is reset during power-up and can also be reset via software-controlled bits in a control register that is part of the CTI Bus interface. A memory reset bit in the control register resets the DECNA memory and an Ethernet interface reset bit resets the DECNA Ethernet interface. Paragraph 3.6 describes the CTI Bus interface control register.

3.5.2 Transmission Overview

During transmission, the host system processor writes the transmit command block and data packet into the dual-ported memory via the CTI Bus interface. The host system then raises and lowers the channel attention signal (CA) (Figure 3-5) to instruct the Ethernet Interface to locate, read, and process the next command. The Ethernet interface, after processing the command, gains access to the serial link, moves the data from the dual-ported memory, forms the data into Ethernet-formatted packets, then transmits the data packets to the destination node. When transmission is complete (or an attempt is complete), the Ethernet interface writes the transmit status into the dual-ported memory and asserts an interrupt signal to the host system. This signal tells the system to check transmission status.

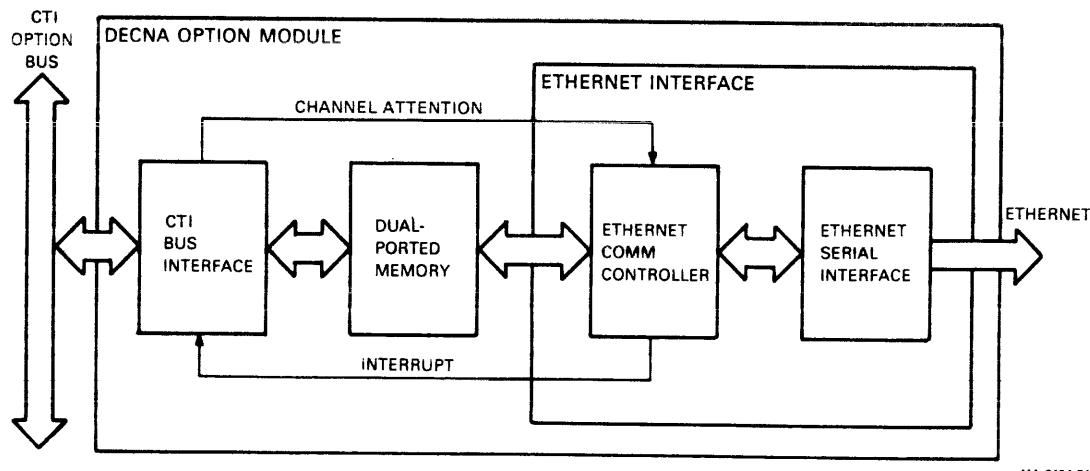


Figure 3-5 DECNA Ethernet Interface

3.5.3 Reception Overview

To receive, the host system gains access to the dual-ported memory to set up the receive buffer area(s) and the receive command block(s). The host system then raises and lowers the channel attention (CA) signal to instruct the Ethernet interface to locate, read, and process the command. The Ethernet interface then works without further intervention from the host system. The interface detects the beginning of packets, performs address checking, moves data and status to the dual-ported memory, maintains error counters, and provides an interrupt signal (Figure 3-5) to notify the host of the received packet(s).

3.6 CTI Bus INTERFACE

The CTI Bus interface (Figure 3-6) is a slave interface between the CTI Bus and the rest of the DECNA option module. The CTI Bus provides the bus transceivers, registers, control circuitry, and decoding logic needed to communicate with the Professional 300 series system module.

NOTE

Refer to the Professional 300 Series Technical Manual Volume 1 for a description of the Professional 300 Series system module.

The CTI Bus interface includes the following components.

- Bus transceivers
- Bus command register
- Control circuitry
- Memory read address register
- Base address comparator
- Memory access register
- Control register
- Option ROM
- Address ROM
- ROM address logic

The rest of Paragraph 3.6 describes these circuits to a functional block level. All block diagrams and signal descriptions in this section refer to *DECNA Field Maintenance Print Set (MP 5415987-0-1)*.

3.6.1 Bus Transceivers, Bus Command Register, and Control Circuitry

Figure 3-7 shows the bus transceivers, bus command register, and control circuitry. These circuits enable read/write operations through the host system option bus. Paragraphs 3.6.1.1 through 3.6.1.7 describe read/write bus cycle timing and circuits. See Table 3-1 for signal descriptions.

3.6.1.1 Read/Write – Read/write operations occur in two distinct forms: memory access and I/O page access.

Memory access is a direct link of data address lines 0 through 16 (DAL 0-16) to the dual-ported memory.

I/O page access provides access to CTI Bus interface read/write registers via the uppermost 4-kilobyte segment of the host computer's addressing capability. Only the system module can gain access to the DECNA option module. The DECNA option module cannot communicate with other option modules through I/O page. The host computer allows the address of the DECNA option module in the I/O page to be assigned by the host system when the module is installed. The slot in which the option module is installed determines the address of the option. I/O references are decoded by the system module and a unique slot select (SS) signal is wired to the DECNA option module through the bus. The DECNA option module uses the slot select signal to determine if it is being accessed. Refer to the Professional 300 Series Technical Manual Volume 1 for the DECNA option module addressing range.

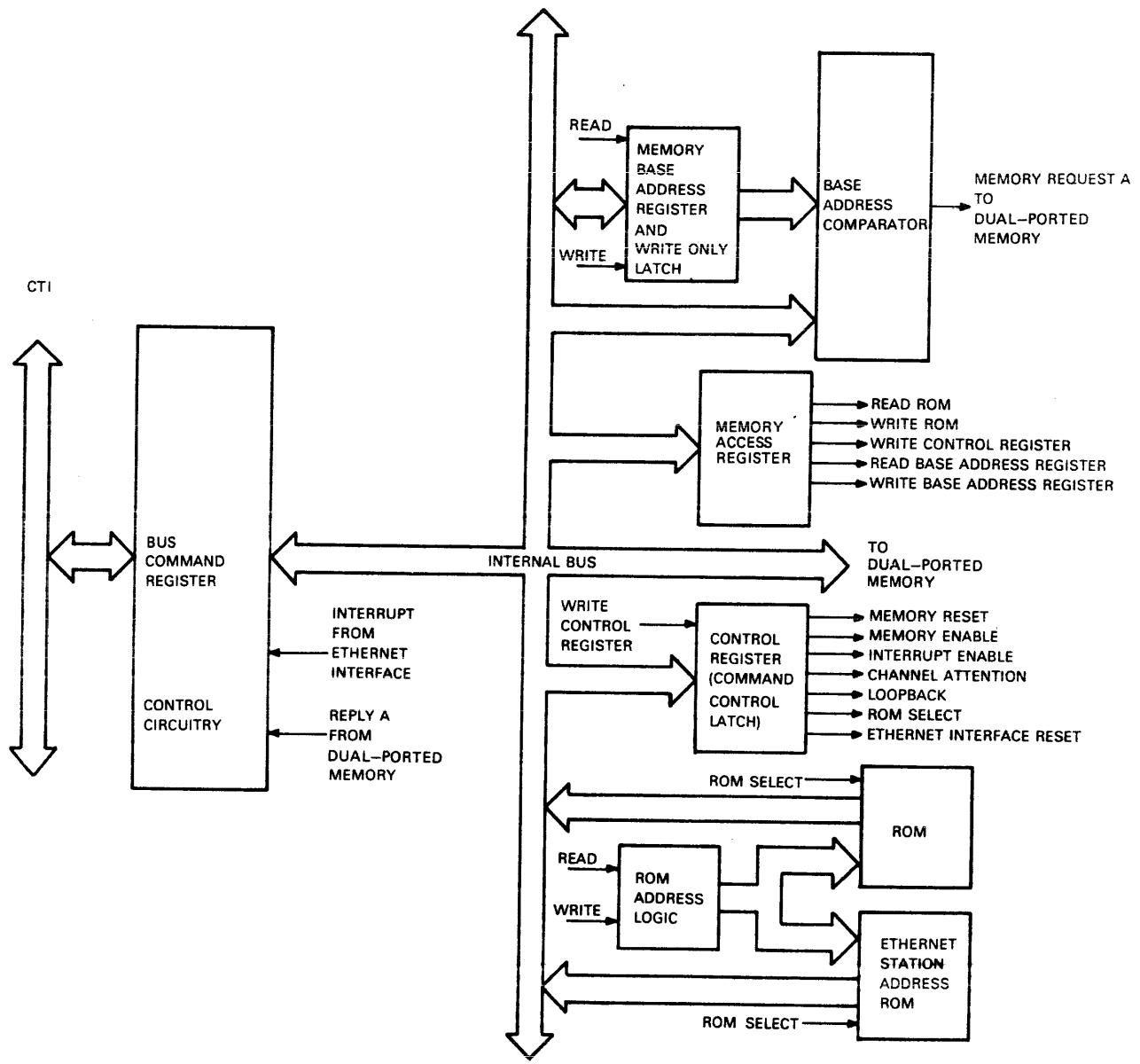
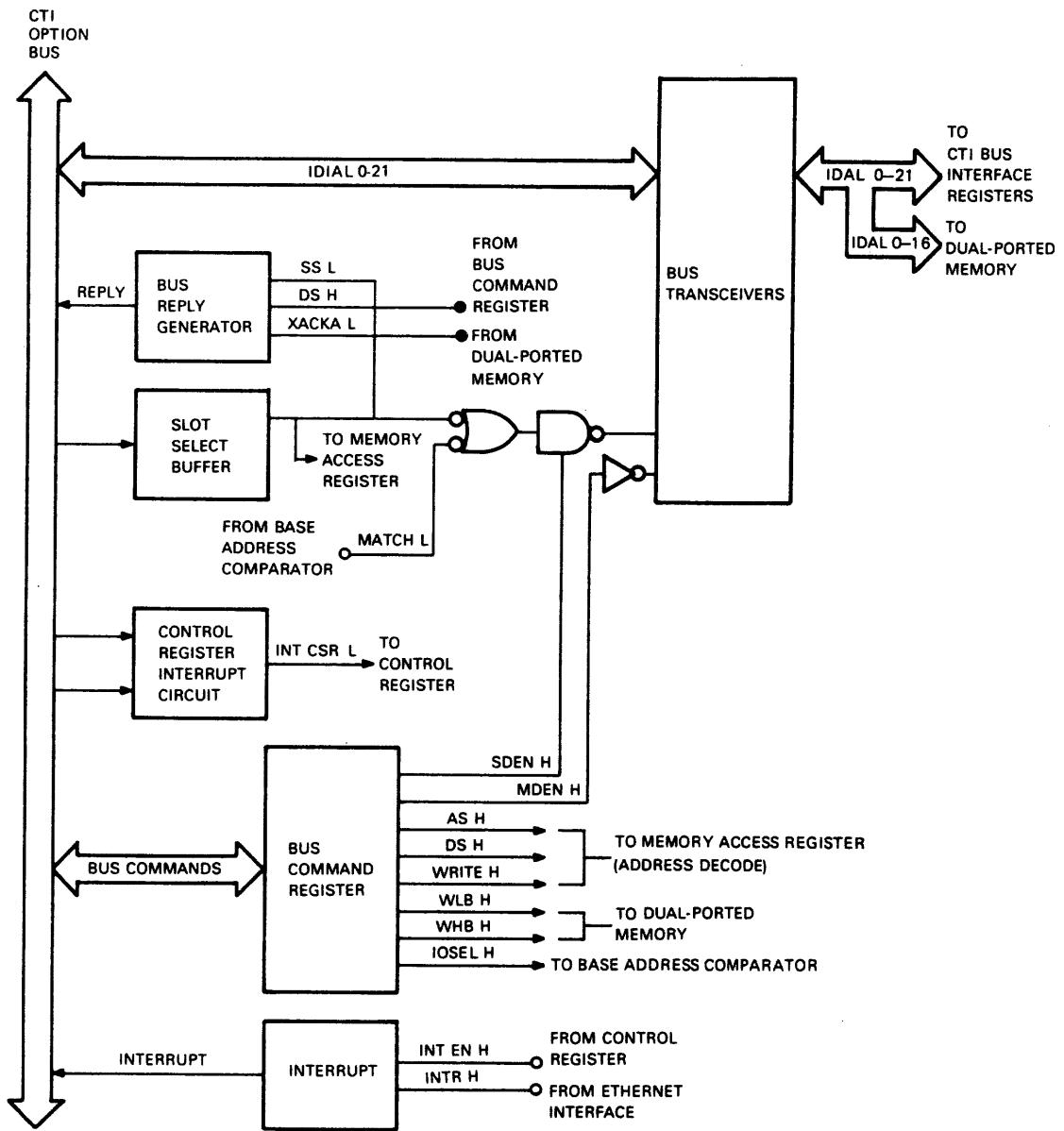


Figure 3-6 CTI Bus Interface



MA-0436-64

Figure 3-7 Bus Transceivers, Bus Command Registers, and Control Circuitry

Table 3-1 Bus Transceivers, Bus Command Register, and Control Circuitry Signal Description

Mnemonic	Signal Name	Active State (True)	Description
SDEN	Slave data Enable	H	SDEN is bus command register output. It enables bus transceivers to send data to the host system when SS L or MATCH L are true.
MATCH	Match low	L	MATCH is base address comparator output. It enables bus transceivers to send data to the host system.
MDEN	Master data enable	H	MDEN is bus command register output. It enables bus transceivers to receive address or data from the host system.
AS	Address strobe	H	AS is bus command register output. It enables address data latching from the host system into the memory access register.
DS	Data strobe	H	DS is bus command register output. It enables data transfer between the registers, memory, and host system.
WRITE	Write	H	WRITE is bus command register output. It enables the host processor to write words to the DECNA option module.
WLB	Write low byte	H	WLB is bus command register output. It enables the host processor to write low bytes to the DECNA memory.
WHB	Write high byte	H	WHB is bus command register output. It enables the host processor to write high bytes to the DECNA memory.

Table 3-1 Bus Transceivers, Bus Command Register, and Control Circuitry Signal Description (Cont)

Mnemonic	Signal Name	Active State (True)	Description
IOSEL	I/O select	H	IOSEL is bus command register output to the base address comparator. It is asserted by the host processor when accessing a location in the I/Opage of the address space. IOSEL disables access to the dual-ported memory.
SS	Slot select	H	SS enables the host processor to gain access to the DECNA registers. It is also used with XACKA L and DS H to generate a bus reply (RPLY L).
INT EN	Interrupt enable	H	INT EN is control register output. It gates the interrupt signal (INTR H) from the Ethernet interface to the host processor (BIRQA L).
INTR	Interrupt	H	INTR is Ethernet interface output gated by INT EN H to the host processor to signal the end of an operation.

3.6.1.2 Bus Transceivers – The bus transceivers (Figure 3-7) consist of buffers that provide an interface between the CTI Bus and the DECNA internal multiplex bus. In combination, the buffers drive and receive 22 data address lines (0 through 21) including 16 bits of data per byte to the dual-ported memory. See Table 3-1 for signal descriptions.

3.6.1.3 Bus Command Register – The bus command register (Figure 3-7) transfers bus commands to the DECNA option module bus transceivers, memory access register, base address comparator, bus reply generator, and dual-ported memory. See Table 3-1 for signal descriptions.

3.6.1.4 Slot Select Buffer – The slot select buffer (Figure 3-7) buffers the slot select signal (SS L) from the CTI Bus. The host system module asserts SS L while the address is being generated on the bus. SS L is true on the bus before the assertion of the address strobe signal (AS H). This allows SS L to be used in address decoding that occurs on the DECNA option module. See Table 3-1 for signal descriptions.

3.6.1.5 Bus Reply Generator – The bus reply generator (Figure 3-7) generates a reply signal for the host computer whenever the host computer gains access to the dual-ported memory via memory access or the DECNA read/write registers via the I/O page. See Table 3-1 for signal descriptions.

3.6.1.6 Control Register Interrupt Circuit – The control register interrupt circuit (Figure 3-7) uses signals from the system module to generate an initialize signal (INIT CSR L) that clears the control register. See Table 3-1 for signal descriptions.

3.6.1.7 Host Interrupt Circuit – The host interrupt circuit (Figure 3-7) gates an interrupt enable signal (INT EN H) from the control register with an interrupt signal (INTR H) from the Ethernet interface. The host interrupt circuit's output puts BIRQA L on the CTI Bus to notify the host computer that the Ethernet interface has completed an operation. See Table 3-1 for signal descriptions.

3.6.2 Memory Access Register

The memory access register (Figure 3-8) is an address decoder that provides read and/or write commands to the ROM address logic, control register, and base address comparator. See Table 3-2 for signal descriptions.

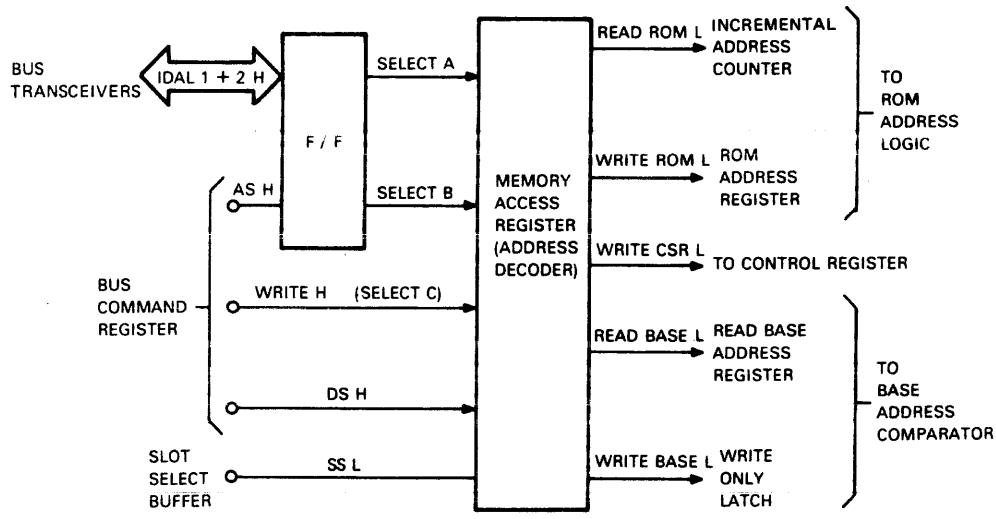


Figure 3-8 Memory Access Register

Table 3-2 Memory Access Register Signal Description

Mnemonic	Signal Name	Active State (True)	Description
AS	Address strobe	H	AS is bus command register output. It latches the input state of the flip-flops.
WRITE	Write	H	WRITE is bus command register output. It selects a write operation when true, and a read operation when not true.
DS	Data strobe	H	DS is bus command register output. It enables data decoding when SS L is true.
SS	Slot select	L	SS is slot select buffer output. It enables address decoding when DS H is true.
READ ROM	Read ROM	L	READ ROM is output to the ROM address logic. It enables the contents of the option ROM or Ethernet station address ROM to be read by the host system.
WRITE ROM	Write ROM	L	WRITE ROM is output to the ROM address logic. It enables the host system to reset the ROM pointer to zero.
WRITE CSR	Write control register	L	WRITE CSR is output to the control register. It enables a write to the control register.
READ BASE	Read base address	L	READ BASE is output to the base address comparator. It enables the host system to read the contents of the base address register.
WRITE BASE	Write base address	L	WRITE BASE is output to the base address comparator. It enables the host system to write the contents of the base address register.

3.6.3 Control Register (Command Control Latch)

The control register (Figure 3-9) is a software-accessible, write-only, byte-wide, command control latch. It controls the DECNA option module's main functions. The control register is accessed via WRITE CSR L from the memory access register and cleared (reset) by INIT CSR L from the control circuit. This register uses IDAL 0 through 7 to perform the following functions.

Reset memory

Enable dual-ported memory

Enable interrupts

Sends a channel attention (CA) signal to the Ethernet interface

Enable the Ethernet interface loopback

Select option ROM (self-test) or the address ROM

Reset the Ethernet interface

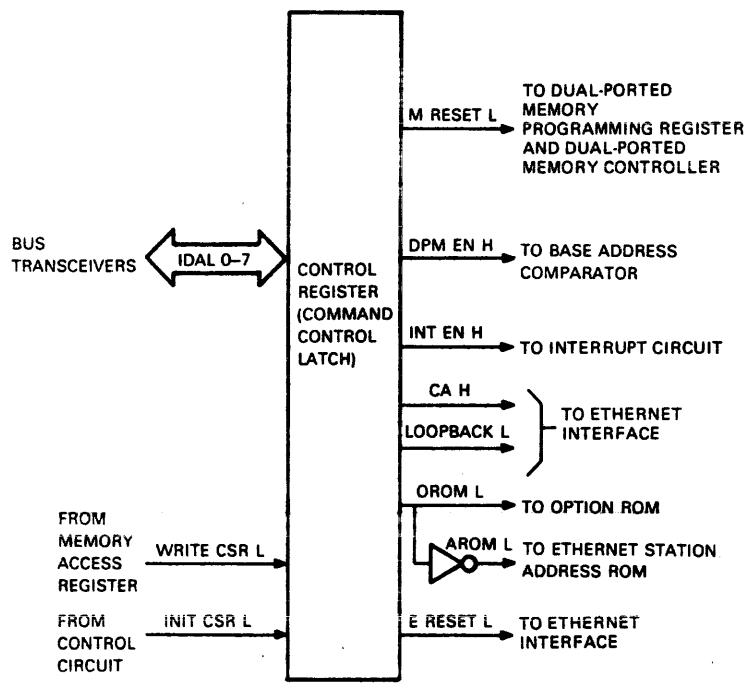


Figure 3-9 Control Register (Command Control Latch)

Figure 3-10 shows the control register signals and bit values.

At system power-up, reset, or bus reset, INIT CSR L is true and all seven bits in this register are set to 0, which resets the DECNA option module.

NOTE

**The state of M RESET (bit 0) or E RESET (bit 7)
does not affect the other control register bits.**

See Table 3-3 for signal descriptions.

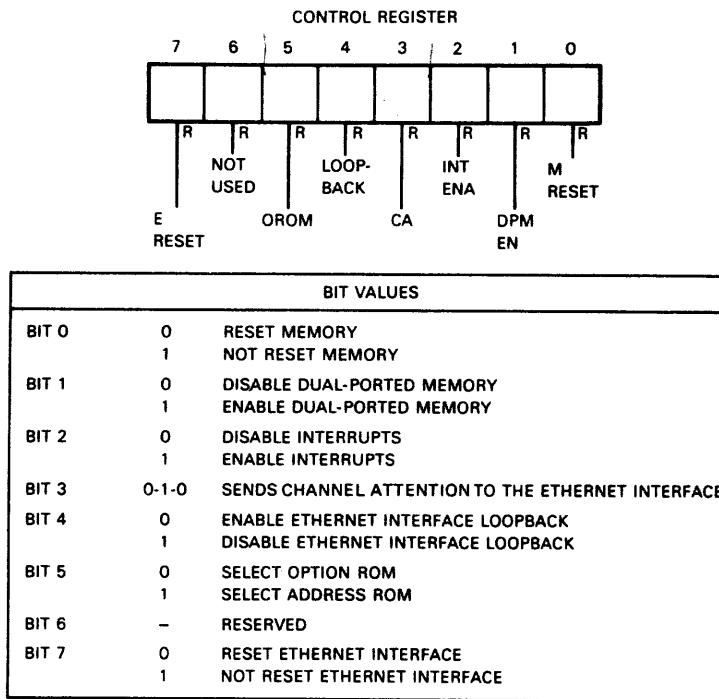


Figure 3-10 Control Register Bit Values

Table 3-3 Control Register Signal Description

Mnemonic	Signal Name	Active State (True)	Description
WRITE CSR	Write control register	L	WRITE CSR is memory access register output. It enables a write to the control register.
INIT CSR	Initiate (clear) control register	L	INIT CSR is memory access register output. It resets the control register.
M RESET	Memory reset	L	M RESET is output to the dual-ported memory. It resets the dual-ported memory only.
DPM EN	Dual-ported memory enable	H	DPM EN is output to base address comparator. It enables bus access to the dual-ported memory.
INT ENA	Interrupt enable	H	INT ENA is output to the BIRQA interrupt circuit. It gates the interrupt signal from the Ethernet interface to the host system.
CA	Channel attention	H	CA is output to the Ethernet interface. It alerts the Ethernet interface to process the next command.
LOOPBACK	Loopback	L	LOOPBACK is output to the Ethernet interface. It places the Ethernet interface in loopback mode.
OROM	Option ROM select	L	OROM is output to the option ROM. It selects the option ROM for a read by the host system.
AROM	Address ROM select	L	AROM is output to the address ROM. It selects the address ROM for a read by the host system.

3.6.4 Memory Base Address Register and Write-Only Latch, and Base Address Comparator

The memory base address register and write-only latch (Figure 3-11) is a software-accessible read/write register. It stores the high order address bits of the memory page. The base address comparator (Figure 3-12) compares the high order address bits in the base address register with the high order address bits from memory access (IDAL 17-21), which are coming in on the bus. If the bits match, the 128K block of dual-ported memory is accessible. The lower five bits of the dual-ported memory base address register determine the five high order address bits for the location of the 64K word dual-ported memory in the host system address space.

The high order bit (bit 7) of the base address register is a read-only bit that is set by the Ethernet interface. It indicates an error condition for a previously transmitted packet. This bit indicates that the no carrier sense signal (NCRS H) was present for an entire transmission. Once set, this error bit remains set until the base address register is read. See Table 3-4 for signal descriptions.

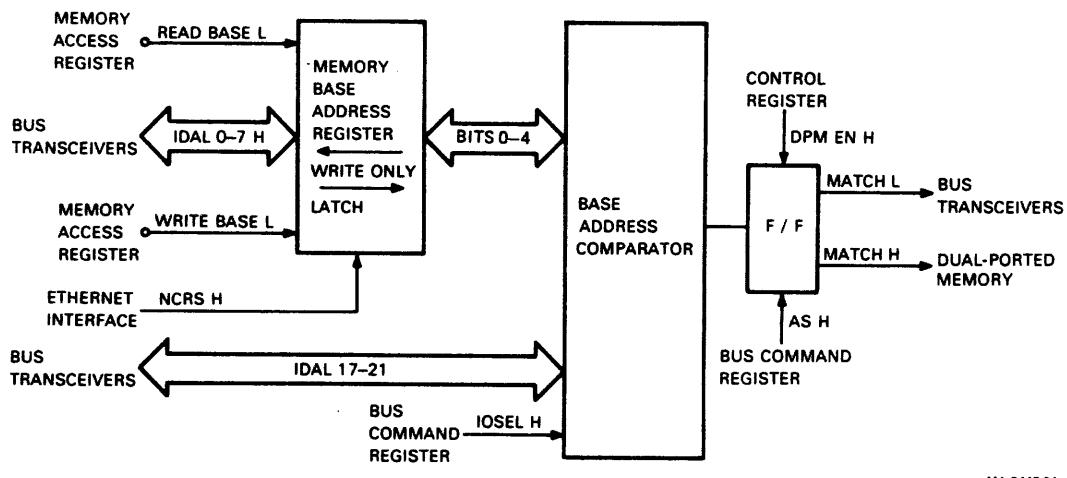


Figure 3-11 Memory Read Base Address Register and Write-Only Latch, and Base Address Comparator

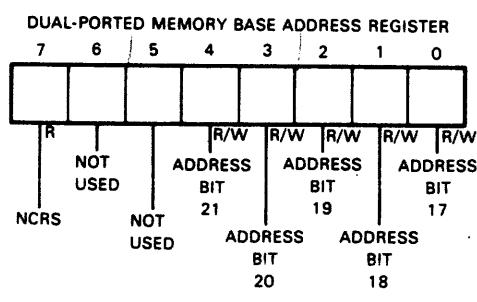


Figure 3-12 Dual-Ported Memory Base Address Register Bit Value

Table 3-4 Dual-Ported Memory Read Base Address Register, Write-Only Latch, and Base Address Comparator Signal Description

Mnemonic	Signal Name	Active State (True)	Description
READ BASE	Read base	L	READ BASE is memory access register output. It enables the host system to read the contents of the base address register.
WRITE BASE	Write base	L	WRITE EASE is memory access register output. It enables the host system to write the contents of the base address register.
NCRS	No carrier	H	NCRS is Ethernet interface output. It indicates an error condition on a previous transmission attempt.
IOSEL	I/O select	H	IOSEL is bus command register output. It disables the base address comparator.
DPM EN	Dual-ported memory enable	H	DPM EN is control register output. It enables the flip-flop operation to enable access to the dual-ported memory.
AS	Address strobe	H	AS is bus command register output. It changes the state of the flip-flop to generate MATCH H.
MATCH	Match low	L	MATCH L is output to the bus transceivers. It enables data transmission to the host system.
	Match high	H	MATCH H is output to the dual-ported memory. It enables data transmission from the host system to the dual-ported memory.

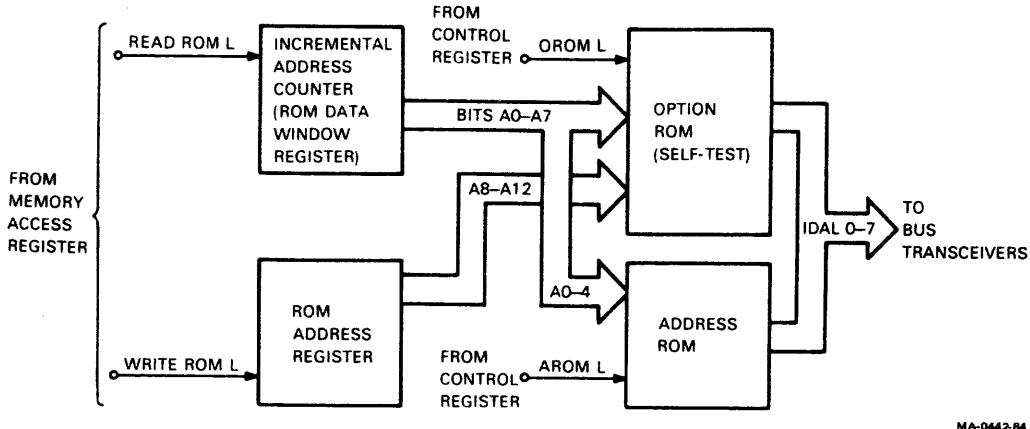


Figure 3-13 Option ROM, Address ROM and ROM Address Logic

3.6.5 Option ROM, Address ROM, and ROM Address Logic

This circuitry (Figure 3-13) provides access to the ROM for down-line loading boot code and diagnostics (option ROM). It also stores the unique Ethernet address of this particular DECNA option module (Ethernet station address ROM).

3.6.5.1 Option ROM – The option ROM (8 kilobytes) provides for down-line loading and storage of bootstrap code and diagnostic code for the DECNA option module. This code is host system processor code that can be read by the host through the ROM data window register, assembled into words in memory, and executed. The bootstrap procedure conforms to the Professional 300 Series boot specification. See Table 3-5 for signal descriptions.

3.6.5.2 Address ROM – The address ROM (32-byte PROM) stores the unique physical address (Ethernet station address) of this particular DECNA option module. The address is software readable. The first six bytes contain the unique address and are accessible via the ROM data window register. The next two bytes contain a checksum value for PROM contents and are also accessible through the ROM data window register. Checksum is calculated according to Ethernet Specification Version 2.0. See Table 3-5 for signal descriptions.

3.6.5.3 ROM Address Logic – ROM address logic consists of the ROM data window register and ROM address register. See Table 3-5 for signal descriptions.

The *ROM data window register* is a read-only, byte-wide register. In response to successive read operations, it provides sequential access to bytes of data stored in the option ROM or Ethernet station address ROM. This register increments by one for each read operation. Either the option ROM or Ethernet station address ROM can be selected for access by a bit (OROM L/AROM L) from the control Register. See Table 3-5 for signal descriptions.

The *ROM address register* is a software-accessible, write-only register. When WRITE ROM L is asserted, the ROM address logic resets and points to the first location of the option ROM or the Ethernet station address ROM. See Table 3-5 for signal descriptions.

Table 3-5 Option ROM, Address ROM, and ROM Address Logic Signal Description

Mnemonic	Signal Name	Active State (True)	Description
READ ROM	Read ROM	L	READ ROM is memory access register output. It enables the host system to read the contents of the option ROM or address ROM, depending on which ROM is selected (OROM L or AROM L). Sequential reads increment the ROM address pointer.
WRITE ROM	Write ROM	L	WRITE ROM is memory access register output. It enables the host system to write to the option ROM if the option ROM is selected (OROM L).
OROM	Option ROM select	L	OROM is control register output. It selects the option ROM for a read by the host system.
AROM	Address ROM select	L	AROM is control register output. It selects the address ROM for a read by the host system.

3.7 DUAL-PORTED MEMORY

The dual-ported memory (Figure 3-14) stores host instructions, data, and Ethernet controller commands. The host system gains access to the dual-ported memory through the CTI Bus interface and port A (asynchronous). The Ethernet accesses the dual-ported memory through the Ethernet interface and port B (synchronous). Port arbitration is accomplished as follows. The port most recently used for memory access has access priority in case both ports try to gain access at the same time.

The dual-ported memory includes the following components.

- 64K × 16 dynamic ram
- CTI write network interface (NI) write selector
- Dual-ported memory controller
- CTI read/write decoder
- Port a (CTI data-to-memory buffer, data latch, and address latch)
- Port B (NI data-to-memory buffer, data latch, and address latch)

The rest of Paragraph 3.7 describes these circuits to a functional block level. All block diagrams and signal descriptions in this section are derived from the *DECNA Field Maintenance Print Set* (MP-01895-01).

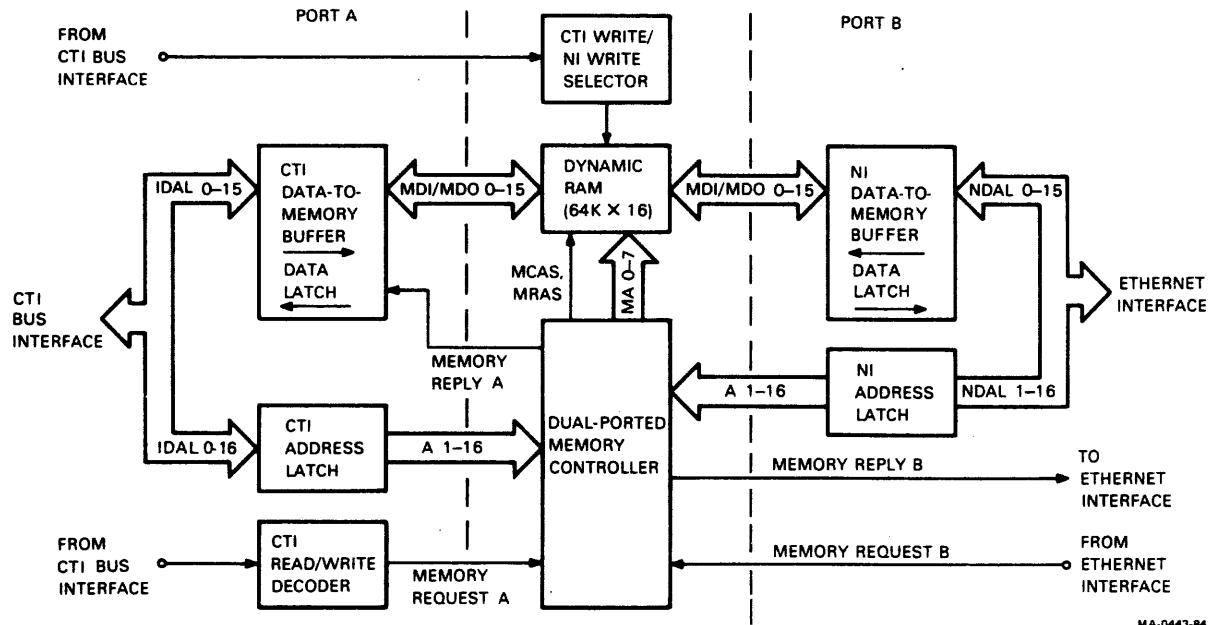


Figure 3-14 Dual-Ported Memory

3.7.1 Dynamic RAM

The dynamic RAM (Figure 3-15) is a $64K \times 16$ (128 kilobyte) array divided into two banks: a low-byte bank and high-byte bank. There are 16 memory data in (MDI 0-15) and 16 memory data out (MDO 0-15) lines to provide access to and from memory via port A or port B. Eight memory address (MA 0-7) lines provide row and column addressing from the dual-ported memory controller. Four memory row address strobe (MRAS 0-3) and four memory column address strobe (MCAS 0-3) signals from the dual-ported memory controller latch the row and column address present on the MA 0-7 lines. The CTI write/NI write selector selects a low and/or high byte. See Table 3-6 for signal descriptions.

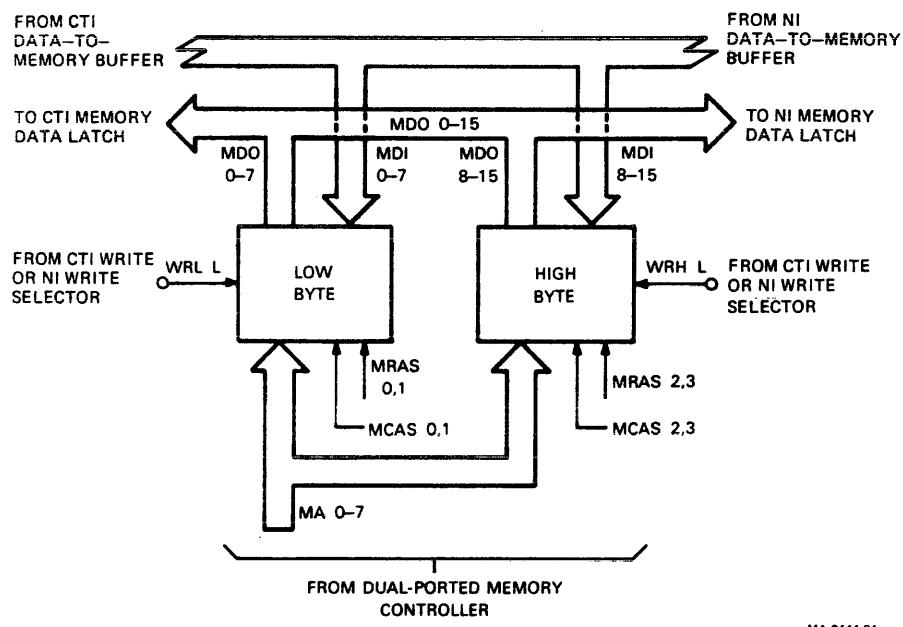


Figure 3-15 Dynamic RAM

Table 3-6 Dynamic RAM Signal Description

Mnemonic	Signal Name	Active State (True)	Description
MDI 0-15	Memory data input	H	MDI 0-15 are memory data input lines to RAM from port A or port B.
MDO 0-15	Memory data output	H	MDO 0-15 are memory data output lines from RAM to port A or port B.
MA 0-7	Memory address	H	MA 0-7 are dual-ported memory controller output. These memory address lines provide the row and column address.
MRAS 0-3	Memory row address strobe	L	MRAS 0-3 are dual-ported memory controller outputs. They latch the row address present on MA 0-7.
MCAS 0-3	Memory column address strobe	L	MCAS 0-3 are dual-ported memory controller outputs. They latch the column address present on MA 0-7 lines.
WRL	Write low byte	L	WRL is CTI write/NI write selector output. It writes a low byte.
WRH	Write high byte	L	WRH is CTI write/NI write selector output. It writes a high byte.

3.7.2 CTI Write/NI Write Selector

The CTI write/NI write selector (Figure 3-16) is a decoder that selects which port can gain access to memory for a write operation. When PSEL is true, the decoder outputs are determined by the states of the RWHB and RWLB inputs. When PSEL is not true, both decoder outputs are low. See Table 3-7 for signal descriptions.

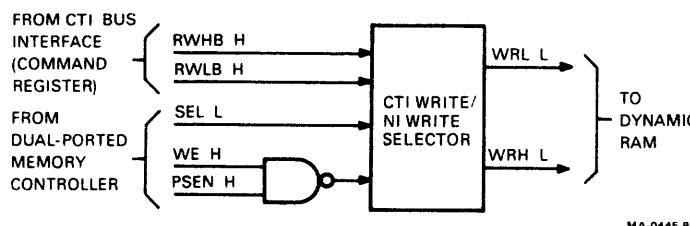


Figure 3-16 CTI Write/NI Write Selection

Table 3-7 CTI Write/NI Write Selector Signal Description

Mnemonic	Signal Name	Active State (True)	Description
RWHB	Read/write high byte	H	RWHB is CTI Bus interface command register output. It enables the host processor to write high bytes to the DECNA memory.
RWLB	Read/write low byte	H	RWLB is CTI Bus interface command register output. It enables the processor to write low bytes to the DECNA memory.
PSEL	Port select	L	PSEL is dual-ported memory controller output. It selects a port for the data transfer. When true, PSEL selects port A; when not true, it selects port B.
WE	Write enable	H	WE is dual-ported memory controller output. It enables a write operation when PSEN is true.
PSEN	Port select enable	H	PSEN is dual-ported memory controller output. It provides contention-free port exchange. When PSEN is true, PSEL cannot change state; when PSEN is not true, PSEL can change state.
WRL	Write low byte	L	WRL is output to the dynamic RAM low byte. It enables a write low byte operation.
WRH	Write high byte	L	WRH is output to the dynamic RAM high byte. It enables a write high byte operation.

3.7.3 Dual-Ported Memory Controller

The dual-ported memory controller (Figure 3-17) is the heart of the dual-ported memory. It is a microcomputer that is programmed at power-up and driven by an 8 MHz clock. The dual-ported memory controller provides the necessary signals to address, refresh, and directly drive the dynamic RAM. It also provides arbitration circuitry to support dual-port access to the dynamic RAM. The controller controls asynchronous operation on port A and synchronous operation on port B. A programming register with a M RESET signal from the CTI Bus interface control register resets the controller chip and memory. See Table 3-8 for signal descriptions.

3.7.3.1 Clock and TTL-to-MOS Level Converter – The 8 MHz clock and TTL-to-MOS level converter provides the timing circuit that drives the dual-ported memory controller chip (8207). The 8 MHz is derived from a flip-flop that divides the output of a 16 MHz crystal by two. The 8 MHz signal is fed to a TTL-to-MOS level converter, which generates the MCLK signal to drive the controller chip.

3.7.3.2 8207 Programming Register – The 8207 programming register is a serial-shift register that allows various designer-selectable options in the 8207 chip. When M RESET is asserted, the register is loaded with octal value 000176. When M RESET is deasserted, the contents of this register is loaded into the dual-ported memory controller chip via the PDI signal. The MUX signal provides a clock for shifting the register contents.

3.7.3.3 Arbiter Circuit – The arbiter circuit is a multiplexer that uses the 8207 chip MUX signal to provide enable signals to the port A and port B address latches.

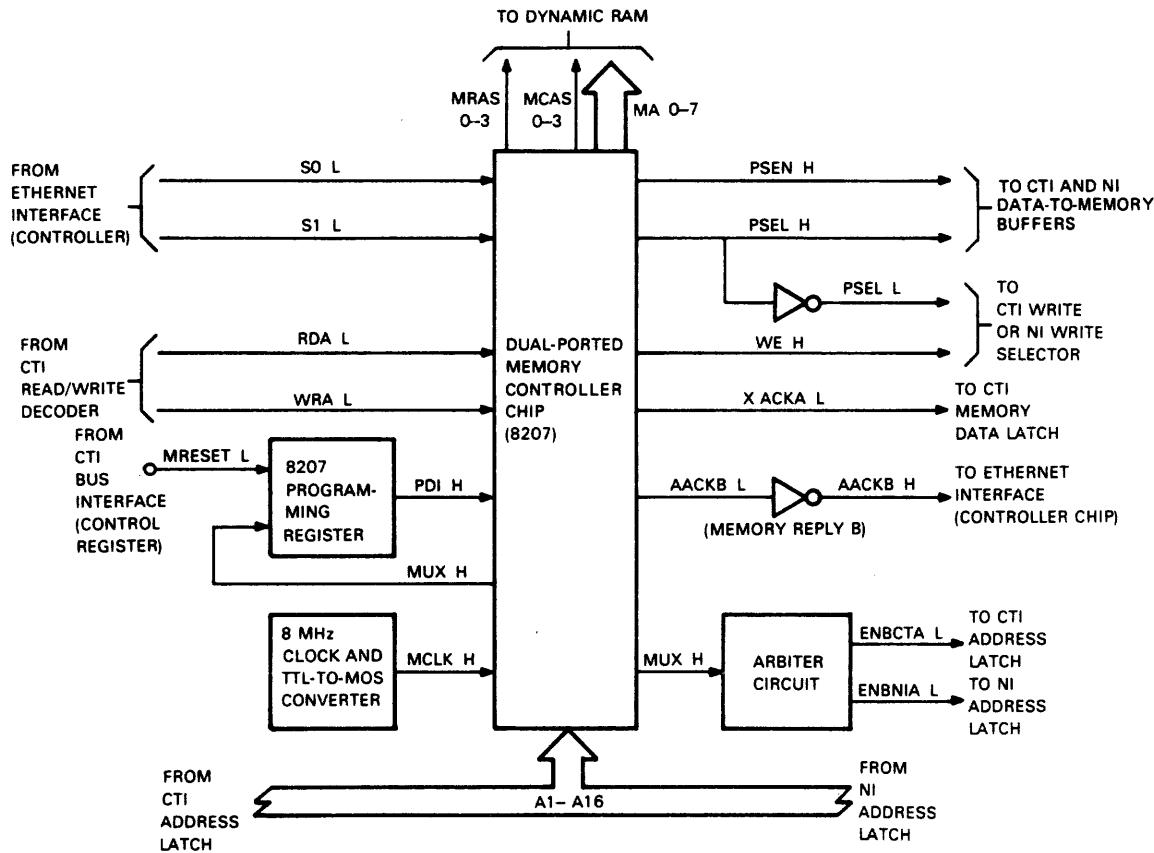


Figure 3-17 Dual-Ported Memory Controller

Table 3-8 Dual-Ported Memory Controller Signal Description

Mnemonic	Signal Name	Active State (True)	Description
A1-A16	Address low/high	H	A1-A8 provide low-order address inputs to generate a row address A9-A16 provide high-order address inputs to generate a column address
MA 0-7	Memory address	H	MA 0-7 are output to the dynamic RAM. They provide the row and column addresses of the selected port to the dynamic RAM.
MRAS 0-3	Memory row address strobe	H	MRAS 0-3 are output to the dynamic RAM. They latch the row address present on MA 0-7.
MCAS 0-3	Memory column address strobe	H	MCAS 0-3 are output to the dynamic RAM. They latch the column address present on MA 0-7.
M RESET	Memory reset	L	M RESET is CTI Bus interface control register output. It loads octal value 000176 into the programming register and resets the controller chip.
MUX	Multiplexor control	H	MUX provides serial-shifting of the value in the programming register during the initial programming phase after M RESET. During normal operation, it drives the arbiter circuit.
PDI	Program data input	H	PDI provides the initial programming value to the 8207 chip.

Table 3-8 Dual-Ported Memory Controller Signal Description (Cont)

Mnemonic	Signal Name	Active State (True)	Description
S0	Status 0	L	S0 is Ethernet interface controller output. It provides the write memory request command input for port B.
S1	Status 1	L	S1 is Ethernet interface controller output. It provides a read memory request command input for port B.
RDA	Read for port A	L	RDA is CTI read/write decoder output. It provides a read memory request command for port A.
WRA	Write for port A	L	WRA is CTI read/write decoder output. It provides a write memory request command for port A.
PSEN	Port select enable	H	PSEN is output to the CTI or NI data-to-memory buffers (port A or B). With PSEL, PSEN provides contention-free port exchange. When PSEN is not true, PSEL can change its state.
PSEL	Port select	H/L	PSEL is output to the CTI and NI data-to-memory buffers and the CTI write/NI write selector. It selects port A or B.
WE	Write enable	H	WE is output to the CTI write/NI write selector. It provides a write enable for the write operation.

Table 3-8 Dual-Ported Memory Controller Signal Description (Cont)

Mnemonic	Signal Name	Active State (True)	Description
XACKA	Transfer acknowledge port A	L	XACKA is output to the port A memory data latch. It enables the memory data latch and indicates that data on the bus is valid during a read cycle or can be removed from the bus during a write cycle via port A.
AACKB	Advanced acknowledge port B	H	AACKB is output to the Ethernet controller. It indicates that the processor can continue processing and that data will be available when required.
ENBCTA	Enable port A address	L	ENBCTA enables the port A address latch.
ENBNIA	Enable port B address	L	ENBNIA enables the port B address latch.
M CLOCK	Memory clock	H	M CLOCK provides timing for the dual-ported memory controller and the Ethernet interface controller.

3.7.4 CTI Read/Write Decoder

The CTI read/write decoder (Figure 3-18) decodes, for the dual-ported memory controller, which type of operation (read or write) that the host system is trying to perform. The decoder is gated by MATCH H and RDS H signals from the CTI Bus interface. When WRITE H from the CTI Bus interface command register is true, the decoder output WRA L is true, which specifies a write operation. When WRITE H is not true, the decoder output RDA L is true, which specifies a read operation. See Table 3-9 for signal descriptions.

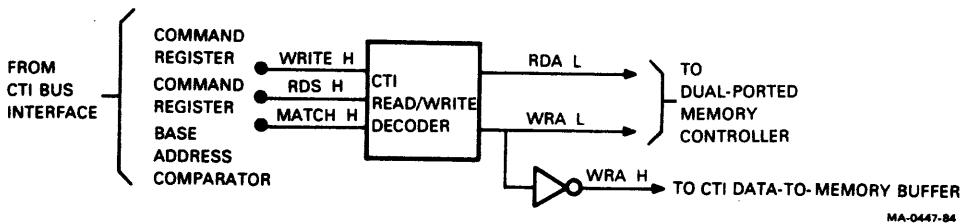


Figure 3-18 CTI Read/Write Decoder

Table 3-9 CTI Read/Write Decoder Signal Description

Mnemonic	Signal Name	Active State (True)	Description
WRITE	Write	H	WRITE is CTI Bus interface command register output. When true, WRITE specifies a write operation; when not true, WRITE specifies a read operation.
DS	Data strobe	H	DS is CTI Bus interface command register output. It enables the CTI read/write decoder.
MATCH	Match	H	MATCH is CTI Bus interface address comparator output. It enables the CTI read/write decoder.
RDA	Read port A	L	RDA is output to the dual-ported memory controller. It provides a read memory request command for port A.
WRA	Write port A	L	WRA L is output to the dual-ported memory controller. It provides a write memory request command for port A.
		H	WRA H is output to the port A data-to-memory buffer. It enables a host system write-to-memory operation.

3.7.5 Port A (CTI Data-to-Memory Buffer, Data Latch, and Address Latch)

Port A (Figure 3-19) consists primarily of a CTI data-to-memory buffer, a CTI memory data latch, and a CTI address latch. The host system, via the CTI Bus interface, accesses DECNA memory through port A. Communication between the host system and DECNA memory through port A is asynchronous. See Table 3-10 for signal descriptions.

3.7.5.1 CTI Data-to-Memory Buffer – The CTI data-to-memory buffer, when enabled by PSEL H, PSEN H, and WRA H, pass signals on internal data address lines 0–15 from the host system to the dynamic RAM via memory data input lines 0–15.

3.7.5.2 CTI Memory Data Latch – The CTI memory data latch, when enabled by XACKA L AND RDA L, pass signals on memory data output lines 0–15 from the dynamic RAM to the host processor via internal data address lines 0–15.

3.7.5.3 CTI Address Latch – The CTI address latch, when enabled by AS H and ENBCTA L, pass signals on internal data address lines 1–16 from the host system to the dual-ported memory controller via address lines 1–16.

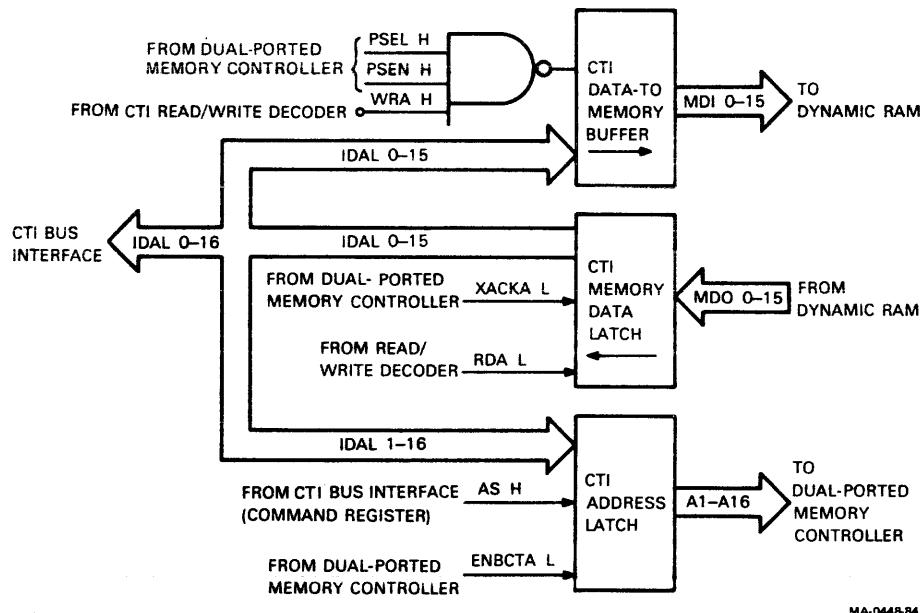


Figure 3-19 Port A

Table 3-10 Port A (CTI Data-to-Memory Buffer, Data Latch, and Address Latch) Signal Description

Mnemonic	Signal Name	Active State (True)	Description
IDAL 0-16	Internal data address lines	H	IDAL 0-16 are internal data address lines.
MDI 0-15	Memory data input	H	MDI 0-15 output to the dynamic RAM. They provide the memory data to the dynamic RAM.
MDO 0-15	Memory data output	H	MDO 0-15 are dynamic RAM output. They provide the memory data from the dynamic RAM.
A1-A16	Address low/high	H	A1-A16 are output to the dual-ported memory controller. A1-A8 provide the lower order address. A9-A16 provide the high order address.
PSEL	Port select	H	PSEL is dual-ported memory controller output. When true, PSEL selects port A; when not true, PSEL selects port B.
PSEN	Port select enable	H	PSEN is dual-ported memory controller output. It provides contention-free port exchange. When PSEN is not true, PSEL cannot change state; when PSEN is not true, PSEL can change state.
WRA	Write port A	H	WRA is CTI read/write decoder output. It is used with PSEL H and PSEN H to enable the data-to-memory buffer.
XACKA	Transfer acknowledge port A	L	XACKA is dual-ported memory controller output. It indicates that data on bus are valid during a read cycle, or that data can be removed from the bus during a write cycle.

Table 3-10 Port A (CTI Data-to-Memory Buffer, Data Latch, and Address Latch) Signal Description (Cont)

Mnemonic	Signal Name	Active State (True)	Description
RDA	Read port A	L	RDA is CTI read/write decoder output. It enables the memory data latch.
AS	Address strobe	H	AS is CTI Bus interface command register output. It enables latching of address data from the host system into the address latch.
ENBCTA	Enable CTI address	L	ENBCTA is dual-ported memory controller output. It enables the CTI address on A1-A16.

3.7.6 Port B (Network Interface Data-to-Memory Buffer, Memory Data Latch, and Address Latch)
 Port B (Figure 3-20) consists primarily of a network interface (NI) data-to-memory buffer, an NI memory data latch, and an NI address latch. The Ethernet, via the Ethernet interface, accesses the DECNA memory through port B. Communication between the Ethernet and DECNA memory through port B is synchronous. See Table 3-11 for signal descriptions.

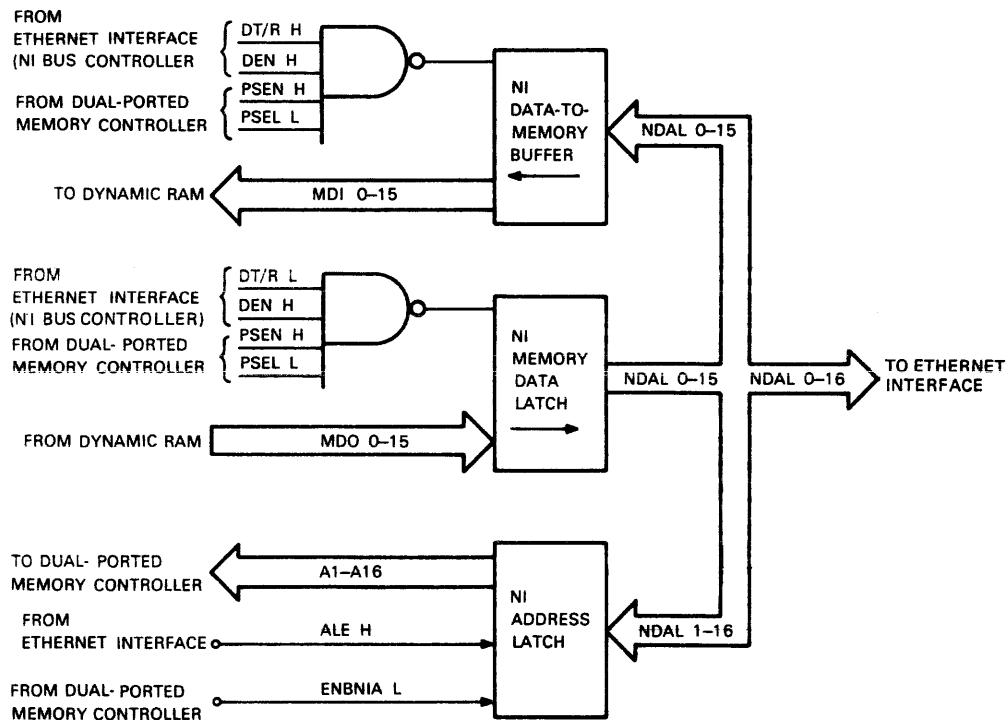


Figure 3-20 Port B

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Table 3-11 Port B (NI Data-to-Memory Buffer, Data Latch, and Address Latch) Signal Description

Mnemonic	Signal Name	Active State (True)	Description
NDAL 0-16	Network data address lines	H	NDAL 0-16 are network data address lines.
MDI 0-15	Memory data input	H	MDI 0-15 are output to the dynamic RAM. They provide memory data to the dynamic RAM.
MDO 0-15	Memory data output	H	MDO 0-15 are dynamic RAM output. They provide memory data from the dynamic RAM.
A1-A16	Address low/high	H	A1-A16 are output to the dual-ported memory controller. A1-A8 provide the lower-order address. A9-A16 provide the higher-order address.
DT/R	Data transmit receive	H	DT/R H is Ethernet interface internal bus controller output. It establishes the direction of the data flow. When true (high), DT/R H enables data transmission from the Ethernet interface to memory.
		L	DT/R L is Ethernet interface internal bus controller output. It establishes the direction of the data flow. When true (low), DT/R L enables data transmission from memory to the Ethernet interface.
DEN	Data enable	H	DEN is Ethernet interface internal bus controller output. It enables data transfer between memory and the Ethernet interface.

Table 3-11 Port B (NI Data-to-Memory Buffer, Data Latch, and Address Latch) Signal Description (Cont)

Mnemonic	Signal Name	Active State (True)	Description
PSEN	Port select enable	H	PSEN is dual-ported memory controller output. It provides contention-free port exchange. When PSEN is true, PSEL cannot change state; when PSEN is not true, PSEL can change state.
PSEL	Port select	L	PSEL is dual-ported memory controller output. When true, PSEL selects port B; when not true, PSEL selects port A.
ALE	Address latch enable	H	ALE is Ethernet interface output. It strobes an address into the address latch. Latching occurs on the falling (high to low) transmission.

3.7.6.1 NI Data-to-Memory Buffer – The NI data-to-memory buffer, when enabled by DT/R, DEN H, PSEN H, and PSEL L, passes signals on network data address lines 0–15 from the Ethernet to the dynamic RAM via memory data input lines 0–15.

3.7.6.2 NI Memory Data Latch – The NI memory data latch, when enabled by DT/R, DEN H, PSEN H, and PSEL L, passes signals on the memory data output lines 0–15 from the dynamic RAM to the Ethernet via network data address lines 0–15.

3.7.6.3 NI Address Latch – The NI address latch, when enabled by ALE H and ENBNIA L, passes signals on the network data address lines 1–16 from the Ethernet to the dual-ported memory controller via address lines 1–16.

3.8 ETHERNET INTERFACE

The Ethernet interface (Figure 3-21) provides the Ethernet cable interface and handles the Ethernet data link layer protocol. The interface generates 10 Mbytes/s data rates, performs Manchester encoding/decoding of packet information, monitors channel access, and generally controls how the DECNA option module uses the link. The Ethernet interface includes the following major circuits.

- Ethernet controller
- Ethernet serial interface
- Broadband compatibility circuit

The rest of Paragraph 3.8 describes these circuits to a functional block level. All block diagrams and signal descriptions in this section relate to *DECNA Field Maintenance Print Set* (MP-01895-01).

3.8.1 Ethernet Controller

The Ethernet controller (Figure 3-22) consists primarily of an Ethernet communications controller chip (82586) driven by an 8 MHz clock, a fail-safe time-out circuit, and an NI internal bus controller. Paragraph 3.8.1.1 through 3.8.1.4 describe these circuits. See Table 3-11 for signal descriptions.

3.8.1.1 Clock and TTL-to-MOS Level Converter – The 8 MHz clock and TTL-to-MOS level converter (Figure 3-22) provide the timing circuit that drives the Ethernet communications controller chip (82586). The 8 MHz is derived from a flip-flop that divides the output of a 16 MHz crystal by two. The 8 MHz signal that results is fed to the TTL-to-MOS level converter, which generates the MCLK signal to drive the controller chip. The TTL-to-MOS level converter also provides a TCLK signal to provide timing for the NI internal bus controller. See Table 3-11 for signal descriptions.

3.8.1.2 Ethernet Communications Controller Chip (82586) – The Ethernet communications controller chip (82586) (Figure 3-22) is a microcomputer that is programmed at system power-up. This controller chip handles the Ethernet data link layer protocol and generally controls how the DECNA option module uses the link. This chip is the controlling interface between the Ethernet serial interface, dual-ported memory, and CTI Bus interface.

During transmission, memory resident command blocks begin execution when the chip receives the channel attention signal (CA H) from the CTI Bus interface control register. A transition of CA from low to high to low instructs the controller chip to locate, read, and process the next command. The controller chip, after processing a transmit command, gains access to the serial link, moves the data from the dual-ported memory, forms the data into Ethernet-formatted packets, then transmits the data packets to the destination node. When transmission is complete (or an attempt is complete), the controller chip writes the transmit status into the dual-ported memory and asserts an interrupt signal (INTR H) to tell the host system to check transmit status.

To receive, the host system raises and lowers the channel attention signal (CA) after setting up the receive buffer areas and receive command blocks in the dual-ported memory. The controller chip then begins to process commands without further intervention from the host system. The chip detects the beginning of incoming packets, performs address checking, moves data and status to the dual-ported memory, maintains error counters, and asserts the interrupt signal (INTR H) to notify the host system of received packet(s).

See Table 3-12 for signal descriptions.

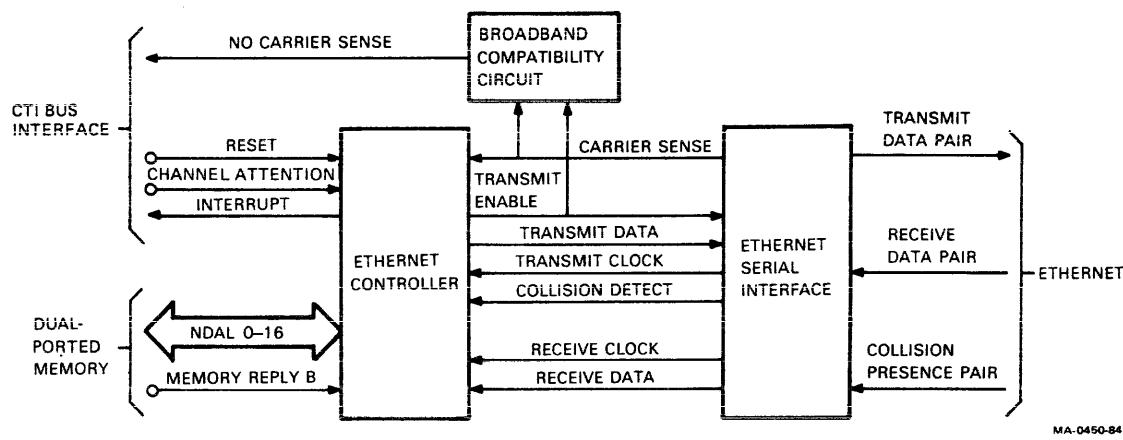


Figure 3-21 Ethernet Interface

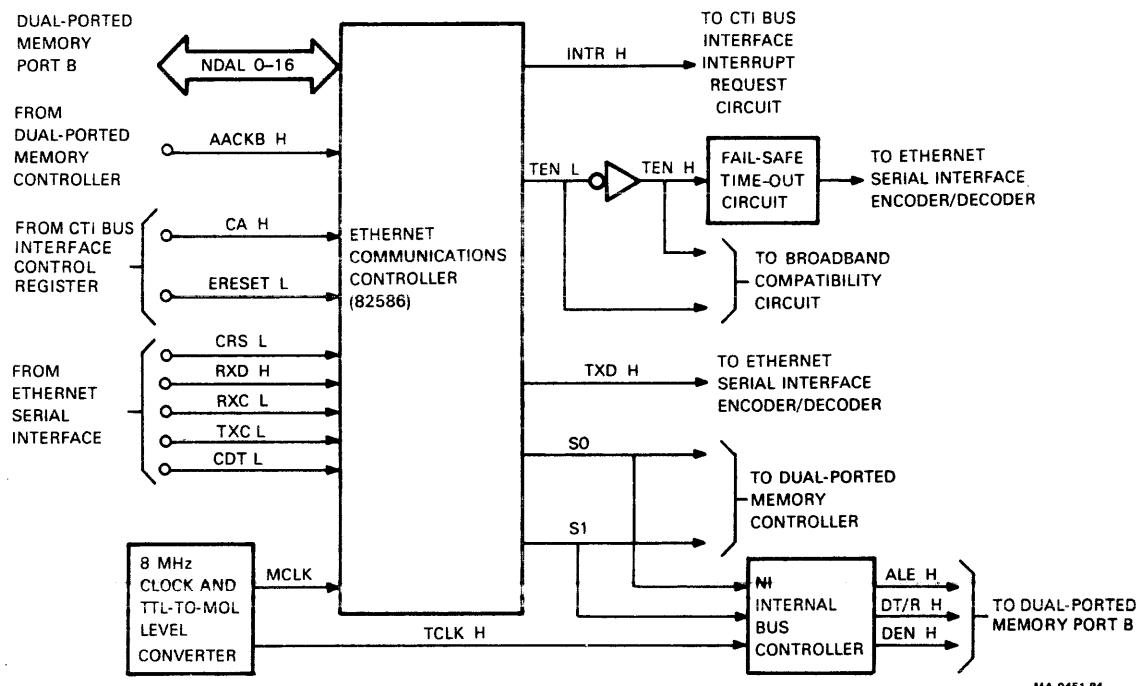


Figure 3-22 Ethernet Controller

Table 3-12 Ethernet Controller Signal Description

Mnemonic	Signal Name	Active State (True)	Description
NDAL 0-16	Network data address lines	H	NDAL 0-16 are network data address lines 0-16.
AACKB	Acknowldege	H	AACKB is dual-ported memory controller output. It provides an indication from addressed memory that the transfer cycle can be completed. When not true (low), AACKB causes wait states.
CA	Channel attention	H	CA is CTI Bus interface control register output. It starts the execution of memory resident command blocks. CA is true for at least one system clock period.
E RESET	Ethernet reset	L	E RESET is CTI Bus interface control register output. It causes a total reset of the controller chip.
CRS	Carrier sense	L	CRS is Ethernet serial interface output. It notifies the controller that there is traffic on the serial link.
RXD	Receive data	H	RXD is Ethernet serial interface output. It decodes the receive serial data.
RXC	Receive data clock	L	RXC is Ethernet serial interface output. It is a clock signal derived from the receive data input. RCX provides timing information for the Ethernet controller.
TXC	Transmit data clock	L	TXC is Ethernet serial interface output. It provides transmit timing for the Ethernet controller.

Table 3-12 Ethernet Controller Signal Description (Cont)

Mnemonic	Signal Name	Active State (True)	Description
CDT	Collision detect	L	CDT is Ethernet serial interface output. It indicates that a collision has occurred on the link.
MCLK	System clock	H	MCLK provides system clock timing.
TCLK	Clock	H	TCLK provides clock timing for the NI internal bus controller. It establishes when the command and control signals are generated.
INTR	Interrupt request	H	INTR is output to the CTI Bus interface. It interrupts the host computer.
TEN	Transmit enable	L	TEN enables the serial interface to transmit data. It is forced high after a reset.
TXD	Transmit data	H	TXD is output to the Ethernet serial interface encoder/decoder. It is serial data to be encoded.
S0, S1	Status	L	S0 and S1 are output to the dual-ported memory controller and the NI internal bus controller. They define the type of memory transfer during the current memory cycle. S0 and S1 generate memory control and timing signals in the NI internal bus controller.
ALE	Address latch enable	H	ALE is output to the dual-ported memory port B. It strobes an address into the port B address latch. Latching occurs on the falling (high to low) transition.

Table 3-12 Ethernet Controller Signal Description (Cont)

Mnemonic	Signal Name	Active State (True)	Description
DT/R	Data transmit/receive	H	DTR is output to the dual-ported memory port B. It establishes the direction of the data flow. When true (high), DT/R enables data transmission from the Ethernet interface to memory. When not true (low), DT/R enables data transmission from memory to the Ethernet interface.
DEN	Data enable	H	DEN is output to the dual-ported memory port B. It enables data transfers between memory and the Ethernet interface.

3.8.1.3 Fail-Safe Time-Out Circuit – The fail-safe time-out circuit (Figure 3-22) provides a timer function. This circuit prevents the station from transmitting continuously for long periods of time. This circuit is important because long transmissions can disable the Ethernet communications link. The timer starts at the beginning of an Ethernet frame transmission and has a time-out of 28 ms. The timer resets each time transmission stops as a result of the transmit enable signal (TEN) being deasserted. If the timer runs out before TEN is deasserted, the Ethernet frame being transmitted is terminated. The timer then resets only when TEN is deasserted. See Table 3-12 for signal descriptions.

3.8.1.4 NI Internal Bus Controller – The NI internal bus controller (Figure 3-22) is clocked by the 8 MHz clock. The controller decodes status inputs S0 and S1 to provide control timing for port B to enable the data flow and establish the direction of the data flow. See Table 3-12 for signal descriptions.

3.8.2 Ethernet Serial Interface

The Ethernet serial interface (Figure 3-23) is the interface between the Ethernet controller and the Ethernet transceiver cable. The interface provides the Ethernet physical layer cable interface and performs Manchester encoding/decoding. It also provides carrier detection, collision detect signal processing, transmit and receive clock timing for the Ethernet controller, and a loopback capability.

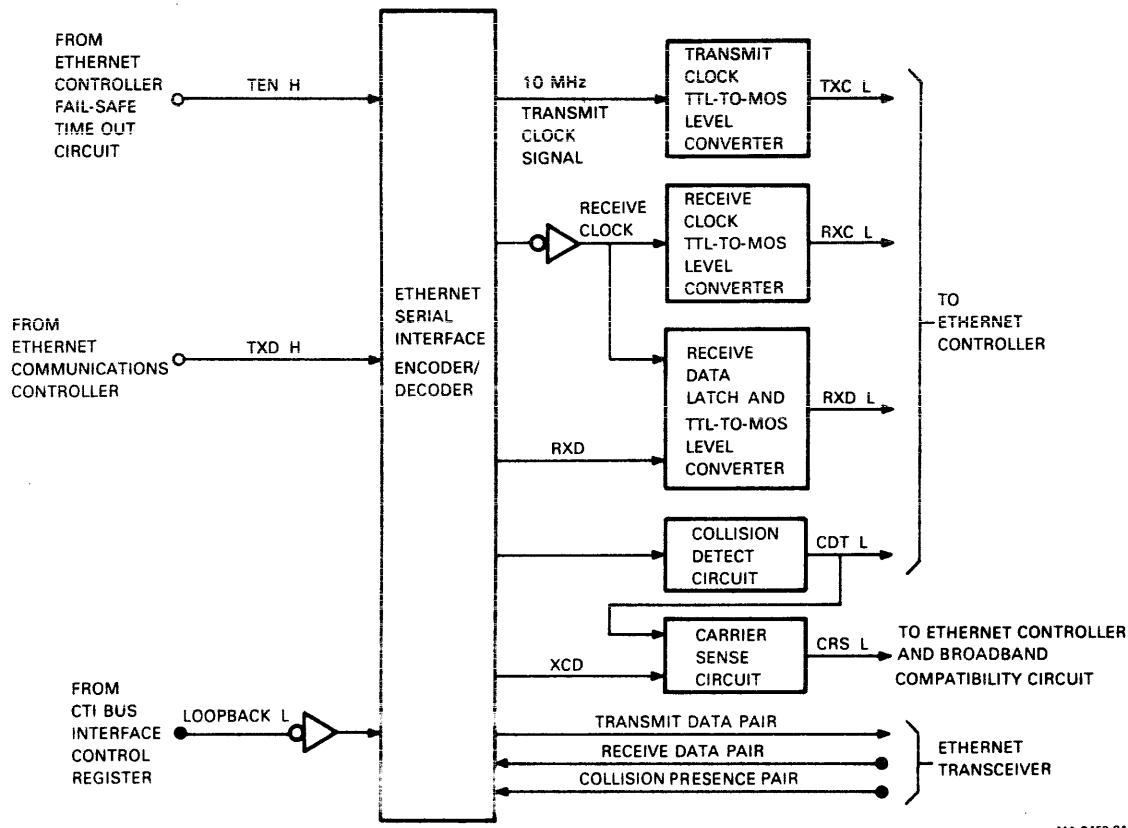


Figure 3-23 Ethernet Serial Interface

The Ethernet serial interface includes the following circuitry.

- Ethernet serial interface encoder/decoder (MB502A)
- Transmit clock TTL-to-MOS level converter
- Receive clock TTL-to-MOS level converter
- Receive data latch and TTL-to-MOS level converter
- Collision detect circuit
- Carrier sense circuit

The rest of Paragraph 3.8.2 describes these circuits to a functional block level. All block diagrams and signal descriptions in this section are derived from the *DECNA Field Maintenance Print Set* (MP5415987-0-1).

Refer to Table 3-13 for signal descriptions.

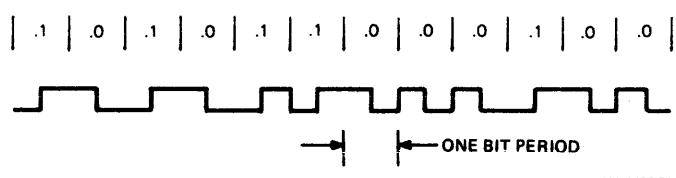
Table 3-13 Ethernet Serial Interface Signal Description

Mnemonic	Signal Name	Active State (True)	Description
TEN	Transmit enable	H	TEN is Ethernet fail-safe time-out circuit output. It enables transmit data pair. When TEN is not true (low), the transmit data pair signal is idle (high).
TXD	Transmit data	H	TXD is Ethernet controller output. It provides the serial data to be encoded. Serial data is supplied synchronously with the falling edge of the transmit data clock signal.
LOOPBACK	Loopback	L	LOOPBACK is CTI Bus interface control register output. It controls loopback mode operation.
TXC	Transmit data clock	L	TXC is output to the Ethernet controller. It provides the transmit timing for the Ethernet controller.
RXC	Receive data clock	L	RXC is output to the Ethernet controller. It provides receive timing for the Ethernet controller.
RXD	Receive data	L	RXD is output to the Ethernet controller. It receives serial data.
CRS	Carrier sense signal	L	CRS is output to the Ethernet controller and broadband compatibility circuit. It notifies the controller that there is traffic on the serial link.
CDT	Collision detect	L	CDT is output to the Ethernet controller. It notifies the controller that a collision has occurred.

Table 3-13 Ethernet Serial Interface Signal Description (Cont)

Mnemonic	Signal Name	Active State (True)	Description
TRANSMIT + and -	Transmit data pair		TRANSMIT is output to the Ethernet transceiver. It transmits Manchester encoded signals to the Ethernet transceiver.
RECEIVE + and -	Receive data pair		RECEIVE is Ethernet transceiver output. It receives Manchester encoded signals from the Ethernet transceiver.
COLLISION + and -	Collision presence pair		COLLISION is Ethernet transceiver output. It receives a 10 MHz square wave signal generated by the Ethernet transceiver.

3.8.2.1 Manchester Code – Manchester code is a signalling method that combines data and timing clock pulses into a single serial-encoded data stream (Figure 3-24). Each bit is split into two halves with the second half containing the inverse of the first half. A transition always occurs in the middle of each bit. During the first half of the bit, the encoded signal is the logical complement of the bit value being encoded. During the second half of the bit, the encoded signal is the uncomplemented value of the bit being encoded.



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Figure 3-24 Manchester Encoded Data

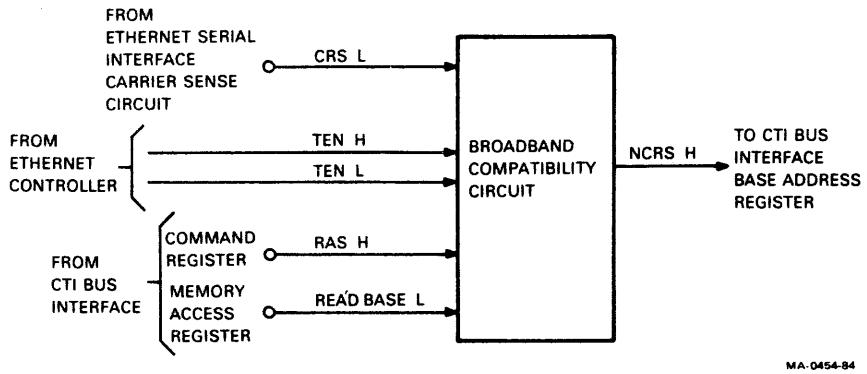


Figure 3-25 Broadband Compatibility Circuit

3.8.2.2 Ethernet Serial Interface Encoder/Decoder – The Ethernet serial interface encoder/decoder (Figure 3-25) is an MB502A chip. The encoder portion of this chip converts serial binary data into Manchester code. The decoder portion of this chip converts Manchester code into binary data and synchronous clock signals.

The *encoder* sends a 10 MHz transmit clock signal, which is converted to the MOS level, to the Ethernet controller. The Ethernet controller sends the TEN signal and transmit data signal (TXD) to the serial interface. The encoder transmits data on differential transmit data pair outputs to the transceiver cable.

The *decoder* receives data on the differential receive data pair inputs from the transceiver cable. It performs a carrier detect function and separates data and clock from the Manchester signal. (The carrier is derived from the receive inputs and passed to the ethernet controller via the carrier sense circuit.)

The encoder/decoder chip converts the collision detect inputs to a TTL output signal, which goes to the Ethernet controller and carrier sense circuit as a collision detect signal (CDT L). The incoming CDTL signal on the collision presence pair input is generated by the Ethernet transceiver. The Ethernet transceiver also simulates a collision at the end of each packet to test the DECNA collision detect circuitry.

The encoder/decoder chip also provides for a loopback operating mode. The loopback signal from the CTI Bus interface control register controls the loopback operating mode. In this mode, encoded data are routed internally to the decoder, the transmit outputs are idle, and the receive collision inputs are ignored. See Table 3-13 for signal descriptions.

3.8.2.3 Transmit Clock TTL-to-MOS Level Converter – The transmit clock TTL-to-MOS level converter (Figure 3-23) converts the 10 MHz transmit clock signal from the encoder/decoder to the MOS level. The converter then feeds the transmit clock signal that results (TXC L) to the Ethernet controller. Refer to Table 3-13 for signal descriptions.

3.8.2.4 Receive Clock TTL-to-MOS Level Converter – The receive clock TTL-to-MOS level converter (Figure 3-23) converts the receive clock signal from the encoder/decoder to the MOS level. The converter then feeds the receive clock signal that results (RXC L) to the Ethernet controller. Refer to Table 3-13 for signal descriptions.

3.8.2.5 Receive Data Resynchronizer and TTL-to-MOS Level Converter – The receive data resynchronizer and TTL-to-MOS level converter (Figure 3-23) supports Manchester encoded data reception. This circuit takes receive clock pulses and receive data from the serial interface encoder/decoder. Then, this circuit positions the data relative to RXC L so that a transition from RXC L to RXC H is centered on a data cell. See Table 3-13 for signal descriptions.

3.8.2.6 Collision Clock Detect Circuit – The collision clock detect circuit (Figure 3-23) is a level converter. It changes the 10 MHz collision signal from the serial interface encoder/decoder to a level (CDT L) required by the Ethernet controller chip. See Table 3-13 for signal descriptions.

3.8.2.7 Carrier Sense Circuit – The carrier sense circuit (Figure 3-23) generates the carrier sense (CRS L) signal for the Ethernet controller chip. It ORs the CDT L and XCD signals from the encoder/decoder to produce CRS L. When CRS L is deasserted, a 5 μ s one-shot time-out reinforces the CRS L deassertion so that CRS is not allowed to go active for the one-shot time-out period.

3.8.3 Broadband Ethernet Compatibility Circuit

The broadband Ethernet compatibility circuit (Figure 3-25) provides DECNA compatibility with a broadband Ethernet transceiver. In a broadband Ethernet system, the assertion of the carrier detected signal can be delayed up to 17 μ s from the beginning of the transmission. During carrier detect in transmission mode, the Ethernet controller does not provide valid carrier sense status. To determine the carrier sense status from a transmission on a broadband Ethernet system, a read-only error bit is provided in the CTI Bus interface memory base address register. This bit indicates that for some previously transmitted packet, the carrier sense was never asserted during the transmission. See Table 3-14 for signal descriptions.

Table 3-14 Broad-Band Compatibility Circuit Signal Description

Mnemonic	Signal Name	Active State (True)	Description
CRS	Carrier sense signal	L	CRS is Ethernet serial interface output. It indicates that traffic is on the link.
TEN	Transmit enable	H	TEN is Ethernet controller output. It indicates the beginning of transmission.
RAS	Read address strobe	H	RAS is CTI Bus interface command register output. It clocks the circuit's final stage.
NCRS	No carrier sense signal	H	NCRS is output to the CTI Bus interface memory read base address register. It indicates that, for a previously transmitted packet, CRS L was never asserted during the transmission.
READ BASE	Read base	L	READ BASE is CTI Bus interface memory access register output. It resets the broadband compatibility circuit.