2240 BIT

MOS Read-Only Memory Character Generators

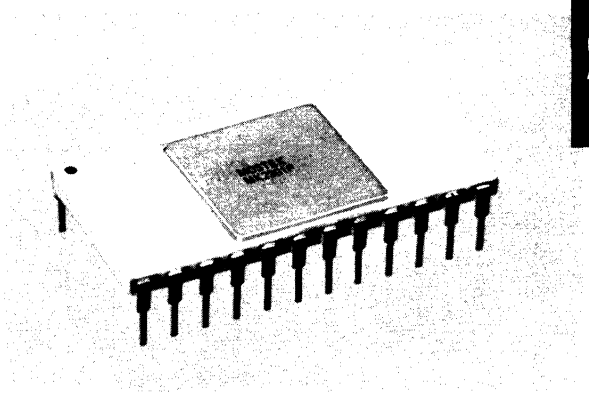
MOSTEK

FEATURES

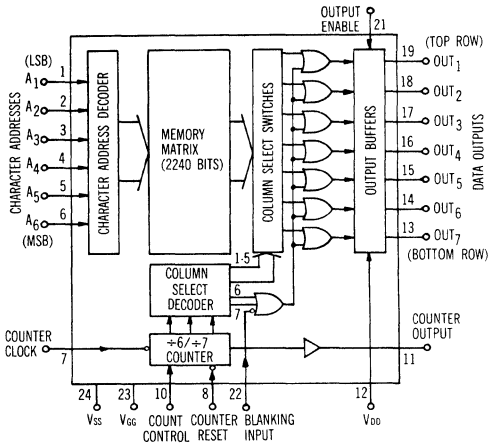
- ☐ Ion-implantation processing for full TTL/DTL compatibility
- ☐ 2240 bits of storage organized as 64 5x7 dot matrix characters with column-by-column output
- ☐ MK 2302 P is pre-programmed with ASCII encoding
- ☐ Internal counter provides clocked column selection
- ☐ Counter output for updating external character address registers
- ☐ Internal provision for one- or two-column intercharacter spacing
- ☐ Output enable and blanking capability
- ☐ Operates from +5V and —12V supplies

APPLICATIONS

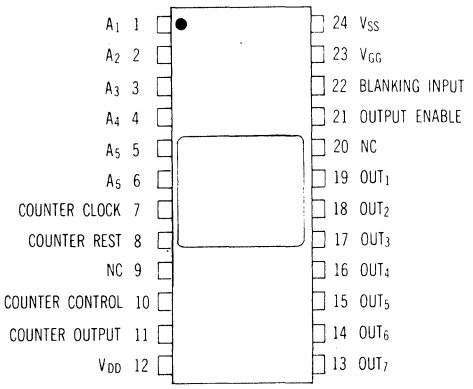
- ☐ CRT alphanumeric displays
- ☐ Light-Emitting Diode (LED) array driver
- ☐ Billboard and stock market displays



FUNCTIONAL DIAGRAM



PIN CONNECTIONS



NC = NO CONNECTION

DESCRIPTION

The MK 2300 P Series MOS, TTL / DTL-compatible read-only memories (ROMs) are designed specifically for dot-matrix character generation. Each ROM provides 2240 bits of programmable storage, organized as 64 characters each having 5 columns of 7 bits. A row output capability for 64 7x10 characters is possible, as illustrated on the back page.

Low threshold-voltage processing, utilizing ion-implantation, is used with P-channel, enhancement-mode MOS technology to provide direct input/output interface with TTL and DTL logic families. All inputs are protected to prevent damage from static charge accumulation.

The MK 2302 P is preprogrammed with ASCII-encoded characters (font shown on back page). Other ROMs in the series are programmed during manufacture to customer specifications by modification of a single mask.

Characters are selected by a six-bit binary word at the Character Address inputs. Each character consists of five columns, the columns selected by an internal counter which is clocked by the Counter Clock input. Column information appears sequentially beginning with the left-most column. Two additional intercharacter spacing columns are available, selectable for one or two spaces by the Count Control Input. During spacing, the Data Outputs are high (+5V), or the "dot-off" condition. After the last space, the modulo counter automatically increments to the leftmost column.

Synchronizing other system components with the ROM is possible using the Counter Reset Input to reset the counter to the last intercharacter spacing column, or using the Counter Output which occurs only on the last spacing column.

The Blanking Input allows all Data Outputs to be driven high (+5V) without affecting any other ROM functions. The Output Enable input allows the outputs to be open-circuited for wire-ORing.

Memory operation is static; refresh clocks are not required to maintain output information. The Counter Clock input is used only to select columns and need not be pulsed continuously.

ABSOLUTE MAXIMUM RATINGS

Voltage on any terminal relative to V_{SS} ..... +0.3V to −20V
Operating temperature range ..... 0°C to +75°C
Storage temperature range ..... −55°C to +150°C

RECOMMENDED OPERATING CONDITIONS ($0°C \leq T_A \leq 75°C$)

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply voltage	+4.75	+5.0	+5.25	V	
	V_{DD}	Supply voltage	—	0.0	—	V	See note 1
	V_{GG}	Supply voltage	−12.6	−12.0	−11.4	V	
INPUTS	$V_{in(0)}$	Input voltage, logic "0"			+0.6	V	See note 2
	$V_{in(1)}$	Input voltage, logic "I"	$V_{SS}-1.5$			V	Count control input should be returned to V_{GG} for ÷ 6 operation, or V_{SS} for ÷ 7 operation
	$V_{in(cc)}$	Count Control input voltage, ÷ 6		−12.0	−11.4	V	
		÷ 7	+4.75	+5.0		V	
COUNTER TIMING	f_{clk}	Counter Clock input frequency	0		200	kHz	
	$t_{clk(0)}$	Clock time at logic "0"	2			μs	
	$t_{clk(1)}$	Clock time at logic "I"	2			μs	See timing diagrams
	$t_{r(clk)}$	Clock rise time			0.1	μs	
	$t_{f(clk)}$	Clock fall time			0.1	μs	
	t_{rp}	Reset pulse width	1.0			μs	
	t_{crd}	Clock-to-reset pulse delay	0.4			μs	See note 4

ELECTRICAL CHARACTERISTICS

(V_{SS} = +5.0V ±0.25V, V_{GG} = −12.0V ±0.6V, $0°C \leq T_A \leq +75°C$, unless noted otherwise)

		PARAMETER	MIN	TYP*	MAX	UNITS	CONDITIONS
POW	I_{SS}	Supply current (V_{SS})		20	40	mA	Outputs unconnected
	I_{GG}	Supply current (V_{GG})		20	40	mA	f_{clk} = 200 kHz
INPUTS	C_{in}	Input capacitance			10	pF	$V_{in}=V_{SS}$, f_{meas} = 1MHz
	I_{in}	Input leakage current			10	μA	$V_{in}=V_{SS}-6V$, $T_A=25°C$
							See note 2
OUTPUTS	$V_{out(0)}$	Output voltage, logical "0"		0.2	0.4	V	I_{out} = 2.0 mA (into output)
	$V_{out(1)}$	Output voltage, logical "I"	2.4			V	I_{out} = 0.6 mA (out of output)
							See note 3
	I_{out}	Data Output leakage current	−10		+10	μA	$V_{SS}-6V \leq V_{out} \leq V_{SS}$, $T_A=25°C$ (outputs disabled)
DYNAMIC CHARACTERISTICS	t_{AO}	Address-to-output delay time			1	μs	
	t_{CO}	Clock-to-output delay time			1	μs	
	t_{CCO}	Clock-to-counter output delay time			1	μs	Rise and fall times included in delay times — See timing diagrams
	t_{BO}	Blanking/unblanking delay time			1	μs	
	t_{OEO}	Output enable/disable delay time			1	μs	
	t_{CRO}	Counter reset delay time			1	μs	R_L = 4 kΩ to V_{SS}
	t_{CRCO}	Reset-to-counter output delay time			1	μs	C_L = 15 pF to V_{DD}
	t_F	Output fall time			0.3	μs	T_A = 25°C
	t_R	Output rise time			0.3	μs	

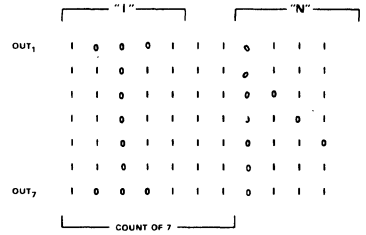
*Typical values apply at V_{SS} = +5.0V, V_{GG} = −12.0V, T_A = 25°C

NOTES:
1. Supply voltages shown are for operation in a TTL/DTL system. Other supply voltages may be used if V_{DD} and V_{GG} maintain the same relationship to V_{SS}, e.g., V_{SS} = 0V, V_{DD} = −5V, V_{GG} −17V. Input voltages would also need to be adjusted accordingly.
2. These parameters apply to the character address, counter clock, counter reset, blanking, and output enable inputs.
3. These parameters apply to both the data outputs and counter output.
4. The counter clock must not make a negative transition within the period tcrd, before or after a positive counter reset transition. The counter reset negative edge may occur any time.

TIMING

(waveforms not to scale)

Timing diagram (1) shows the time relationships between character address, data output, counter clock, and counter output during typical operation of an MK 2300 P Series character generator. An output sequence from the MK 2302 P is shown to help clarify operation. This sequence can be seen from the top rows (OUT_1) of the characters "I" and "N".



All timing relationships shown in diagram (1) apply to any other output or combination of characters as well.

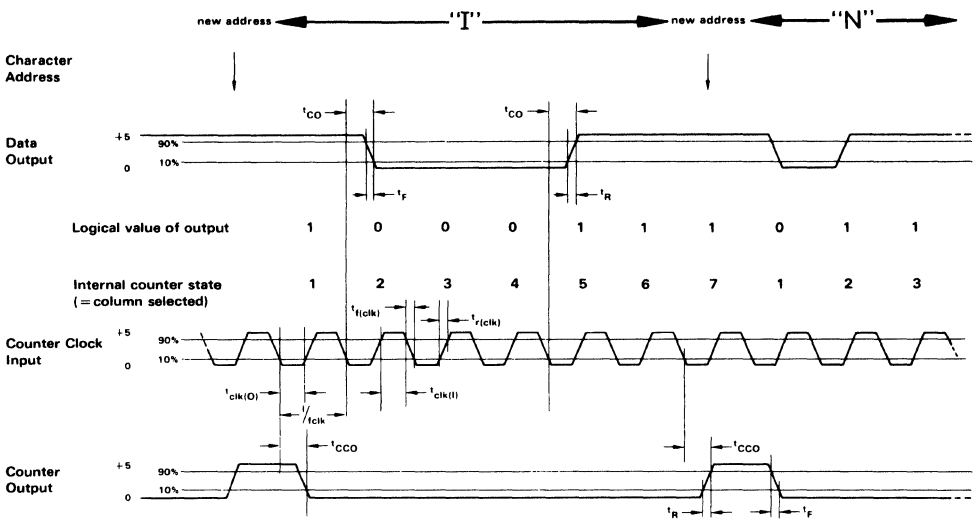
Relevant input conditions assumed but not shown in timing diagram (1) are as follows:

Count Control,	+5V
Counter Reset,	+5V
Blanking Input,	+5V
Output Enable,	+5V

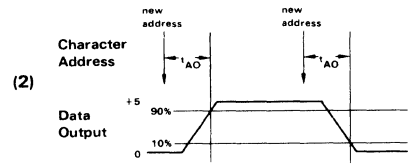
Had the Count Control input been at −12V, the counter sequence would have been six positions instead of seven and the Counter Output would have been high during the sixth position.

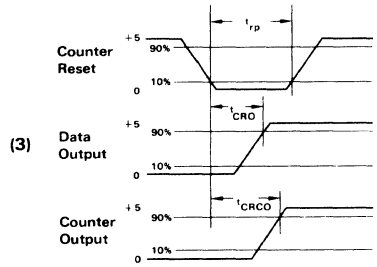
New character addresses are shown coinciding with the rising edge of the Counter Output waveform in diagram (1). This condition was selected to demonstrate use of the Counter Output to advance an external input register to a new character address. Character addresses can be changed at any other time as well. Timing diagram (2) depicts output response to a character address change when, for example, the counter is stationary in one of the five character column positions.

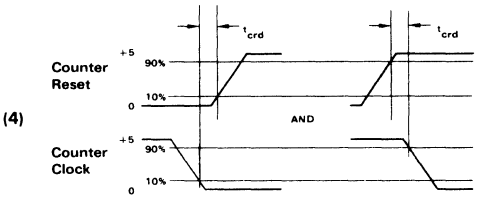
Timing diagrams (3) through (6) show timing relationships for the Counter Reset, Blanking Input, and Output Enable. The "open" condition in (6) implies that both the pull-up and pull-down devices in each data output push-pull buffer are turned off.

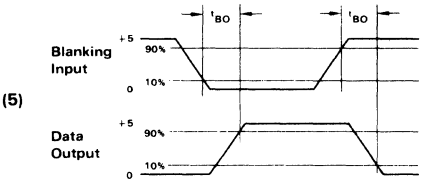


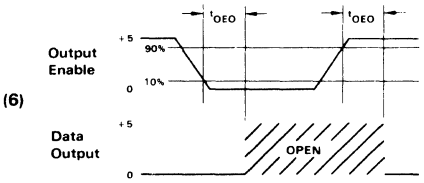
(1)











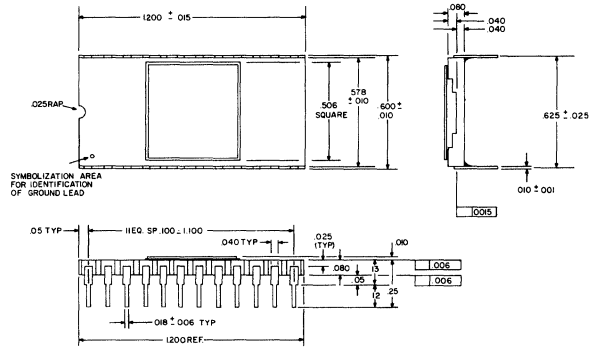
OPERATING NOTES

The following table summarizes the MK 2300 P Series input control states and corresponding drive levels:

Count Control	
÷6	−12V
÷7	+5V
Counter Reset	
operate	+5V
reset	0V
Blanking Input	
unblank	+5V
blank*	0V
Output Enable	
enable	+5V
disable**	0V

*All data outputs high (+5V)
**All data outputs open-circuited

PHYSICAL DESCRIPTION (24 lead ceramic dual-in-line hermetic package)

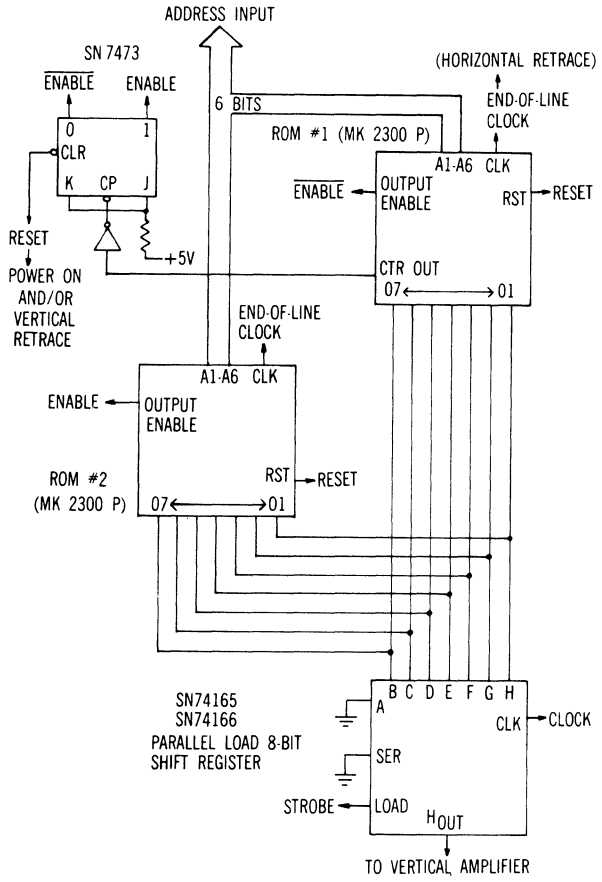


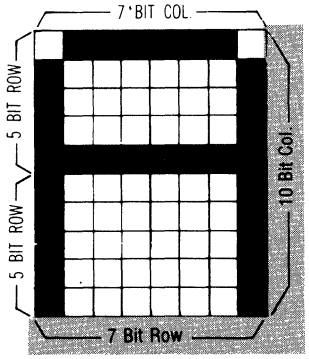
APPLICATION: 7x10 CHARACTER GENERATOR

ROM CODING

7x10 Non-Interlace Configuration: (As illustrated) For row-out (7-bit) horizontal raster-scan application, code ROM #1 for Rows 1 through 5; and ROM #2 for Rows 6 through 10.

7x10 Interlace (525-line): Code ROM #1 for Rows 1, 3, 5, 7, 9; Code ROM #2 for Rows 2, 4, 6, 8, 10. The Enable Flip-flop should be changed to clock only at vertical retrace time, thus allowing ROM #1 to be enabled for the 1st page sweep (262 ½ lines) and then allowing ROM #2 to be enabled for the interlaced 2nd page sweep of 262 ½ lines.



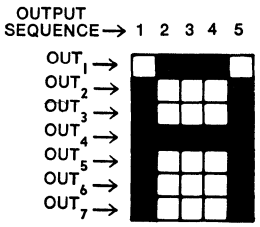


Combining two 5x7 column-output ROMs provides a 7x10 row output.

MK 2302 P

Logic 1 = input @ +5V
Logic 0 = input @ 0V

Output dot "on" = 0V
Output dot "off" = +5V



A_4	A_3	A_2	A_1	A_6 1 1 0 0 / A_5 0 1 0 1
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

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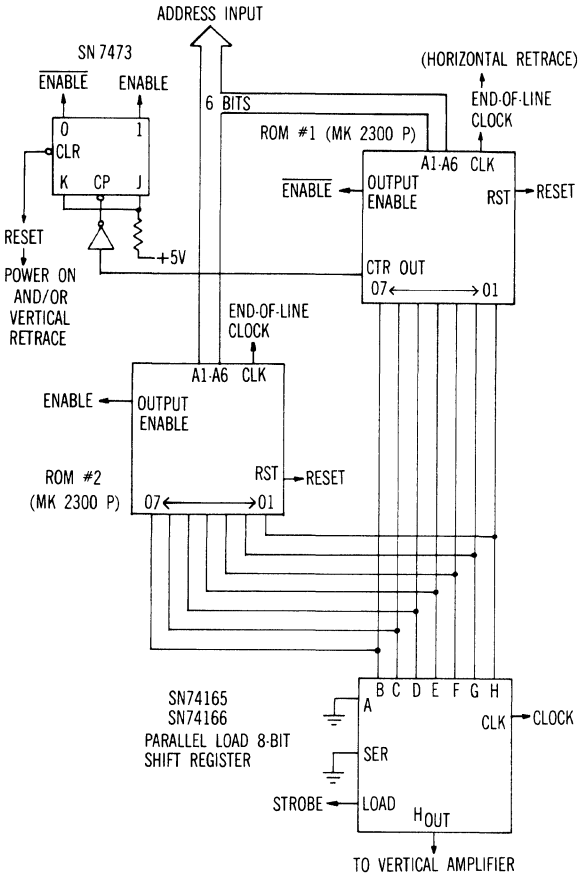
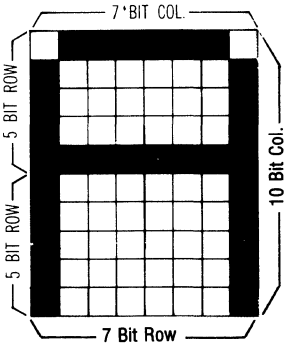


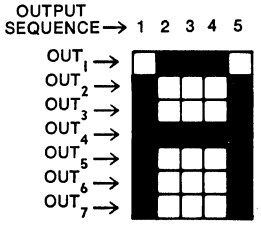


Combining two 5x7 column-output ROMs provides a 7x10 row output.

MK 2302 P

Logic 1 = input @ +5V
Logic 0 = input @ 0V

Output dot "on" = 0V
Output dot "off" = +5V



A_4	A_3	A_2	A_1	A_6 1 1 0 0 / A_5 0 1 0 1
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

MOSTEK ROM PUNCHED-CARD CODING FORMAT[1]

MK 2300 P

Cols. Information Field

First Card

1-30 Customer
31-50 Customer Part Number
60-72 Mostek Part Number[2]

Second Card

1-30 Engineer at Customer Site
31-50 Direct Phone Number for Engineer

Third Card

1-5 Mostek Part Number[1]
10-15 Organization[2]

Fourth Card

1-6 Data Format[3] — "MOSTEK"
15-28 Logic[4] — "Positive Logic" or
35-57 Verification Code[5]

Data Cards [4]

1-6 Binary Address
8-12 First row of character
14-18 Second row of character
20-24 Third row of character
26-30 Fourth row of character
32-36 Fifth row of character
38-42 Sixth row of character
44-48 Seventh row of character

Notes: 1. Assigned by Mostek Marketing Department; may be left blank.

2. Punched as 64x5x7.
3. "MOSTEK" format only is accepted on this part.
4. A dot "ON" should be coded as a "1".
5. Punched as: (a) VERIFICATION HOLD — i.e. the customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS — i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification.
   (c) VERIFICATION NOT NEEDED — i.e. the customer will not receive a CVDS and production will begin immediately.