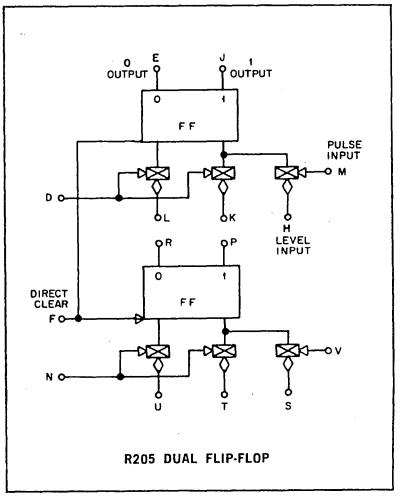
DUAL FLIP-FLOP
TYPE R205

R SERIES



R205 DUAL FLIP-FLOP

The R205 contains two identical flip-flops with a common direct clear input. Each has three DCD gates, and can be collector-triggered at either output by a diode-transistor gate or a diode network. The R205 can be used in any of the following applications without additional gating: up counter, down counter, shift register, ring counter, or jam transfer register.

INPUT: Direct Clear — A standard 100-nsec pulse or a ground level of 100 nsec minimum duration activates the input; the load at ground is 1 ma. When not in use, the direct clear terminal must be at —3v. If the flip-flop is used in an up counter with carry gates enabled, direct clear pulses must be at least 400 nsec long to suppress carry propagation. **DCD Gates, Level** — Standard levels of —3v and ground. Because DCD gates are internally conditioned by the state of the flip-flop, complement inputs may be formed by tying 1 and 0 DCD gate inputs together. A DCD gate is enabled by a ground level and disabled by a —3v level. The conditioning level must be present for at least 400 nsec before the gate is pulsed. The level input represents 2 ma of load at ground. When 1 and 0 DCD gates are connected in parallel to form a complement input, the total load is 3 ma at ground. **Pulse** — Standard 100-nsec pulses (—3v to ground) at any frequency up to 2 mc. It can also be driven by positive-going level changes (—3v to ground) with rise times of 60 nsec max and duration of 100 nsec min. Prior to operation the input must have been at —3v for at least 400 nsec. The pulse input represents 3 ma of load at ground. When a pair of 1 and 0 DCD gates have a common pulse input as in complementing or shifting, the total pulse load is 4 ma at ground. **Collector Triggering** — Triggering circuit load is the external load on the terminal being driven plus the internal load on that terminal. Internal load for the 1 terminal is 6 ma; for the 0 terminal, 8 ma.

OUTPUT: Standard levels. Carry propagation time is 70 nsec. The 0 terminal can drive a 13-ma external load at ground; the 1 terminal, 15 ma at ground. Internal load on the 1 terminal is 6 ma; for the 0 terminal, 8 ma. If more than 18 in. of wire is attached to an output, additional clamped loads (see the W002, W005) should be connected to decrease the output fall time. The load is sufficient if the positive transition at the opposite terminal reaches —1v within 80 nsec after the flip-flop is pulsed.

Note: Additional driving capability at —3v is required by some circuits outside the R series. Auxiliary clamped loads W002 and W005 are available for this purpose.

POWER: +10 v(A)/0.5 ma, —15 v(B)/36 ma.

R205 — $29.00