High-Speed Low-Power FinFET Based Domino Logic

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Abstract—This paper introduces a novel FinFET based domino logic, which exploits the exclusive property of the FinFET device (capacitive coupling between front-gate and back-gate in a four-terminal (4T) FinFET) to simultaneously achieve higher performance and lower power consumption. Using a new implementation of the resistive gate, the keeper device is made weaker at the beginning of the evaluation phase to reduce its contention with the pull-down network, but gradually becomes stronger to provide high noise margin. The strength of the keeper device is controlled by the differential gate voltage, which guarantees low gate-source voltage at the beginning of the evaluation phase and high gate-source voltage during rest of the time.

I. INTRODUCTION

Scaling of CMOS technology has traditionally improved performance, increased transistor density, and reduced power consumption [1]. However, scaling of bulk MOSFET becomes substantially difficult for technology nodes below 32 nm, where proximity of source and drain reduces the control of the gate over the channel leading to unacceptable short channel effects (SCEs). To maintain strong gate control over the channel in bulk MOSFETs, several techniques such as utilization of ultra-thin gate oxide, and higher channel dopant concentration are used, which are now approaching fundamental physical limitations. Using ultra-thin gate dielectric leads to higher gate leakage current due to small physical barrier to gate-oxide tunneling. On the other hand, increased channel dopant concentration, which is needed to eliminate leakage paths far from the channel surface [2], reduces carrier mobility due to impurity scattering, increases sub-threshold slope, and enhances band-to-band tunneling leakage [3]. While high-k/metal-gate and SOI technologies can solve some of these problems, however, beyond the 22 nm technology node, a single gate can not effectively control the channel to suppress the short channel effects.

1.1 Double Gate (FinFET) Transistors

Non-classical silicon devices such as Double-gate (DG) transistors have been proposed to substitute bulk MOSFETs for ultimate scaling [4]. In DG-FETs, electrically-coupled front and back gates effectively control SCEs, resulting in reduced drain induced barrier lowering (DIBL), thereby lowering sub-threshold leakage current. Among the various types of DG devices, FinFETs are easier to manufacture and have been proposed as the most likely candidate to substitute bulk MOSFETs for ultimate scaling [5]. FinFET structures can alleviate SCEs and reduce both gate and sub-threshold leakage currents significantly due to better control of the channel by two gates, very low channel doping concentration and allowed thicker gate oxide. Additionally, near-intrinsic channel doping

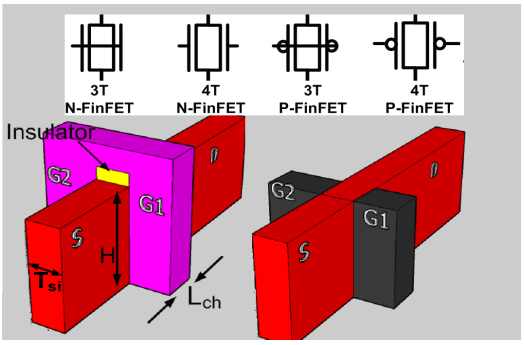

Fig.1. In a 3T FinFET, gate 1 (G1) and gate 2 (G2) are connected to each other while in a 4T FinFET G1 and G2 are separated.

eliminates any threshold voltage variation due to random dopant fluctuations that are prevalent in planar MOSFETs. The FinFET devices can be employed either with two gates tied together (3T structure) or with two independently biased gates (4T structure) [6] (Fig. 1). The width of the FinFET device is quantized and can be obtained from

$$Width = 2 \times n \times H \quad (1)$$

Where, H is the height and n is the number of the fins. This property (width quantization) restricts the design (including performance/power characteristics) optimization typically achieved via continuous device sizing, which is widely employed in bulk CMOS technology.

1.2 Domino Logic

Domino logic circuit techniques are extensively applied in high-performance microprocessors due to the superior speed and area characteristics of dynamic CMOS circuits as compared to static CMOS circuits [7]. In a standard domino logic gate, a feedback PMOS "keeper" device is employed to maintain the state of the dynamic node against coupling noise, charge sharing, and sub-threshold leakage of the pull-down devices. The keeper device requires careful sizing to optimize the noise margin and performance of the domino logic. However, due to width quantization, optimization of performance and noise margin of FinFET based domino logic with continuous keeper sizing is difficult. This paper introduces a novel FinFET based domino logic, which exploits the exclusive property of the FinFET (capacitive coupling between the front-gate and the back-gate of a 4T FinFET device) to simultaneously achieve higher performance and lower power consumption without noise margin degradation.

This paper is organized as follows. In Section II, structure of domino logic and previous works are explained, while in Section III, capacitive coupling in 4T FinFET is discussed. Section IV presents the new methodology in keeper design of

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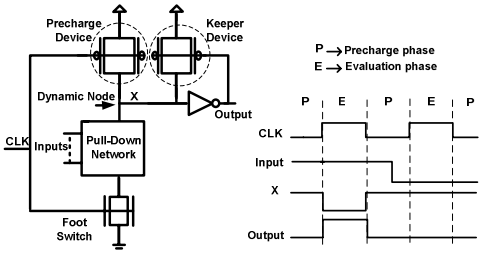

Fig.2. Standard domino logic consists of a precharge block, a keeper device, and a pull-down network. In the precharge mode, dynamic node charges to V_{DD}, output is '0'. In evaluation phase, dynamic node either discharges or remains at '1' depending on the input combination.

FinFET domino logic. Design analysis and simulation results are presented in Section V. Finally, concluding remarks are made in Section VI.

II. PREVIOUS WORKS

Structure of a standard 3T FinFET based domino logic is similar to bulk CMOS based domino logic except that all the bulk transistors are replaced by 3T FinFET devices (Fig. 2). A domino gate consists of a precharge device, a pull-down network, a PMOS keeper device and an inverter. During the precharge phase, clock is low, the precharge transistor (PMOS) is 'ON', and the dynamic node ('X') is charged to V_{DD}, driving output to ground and turning on the "keeper" PFET device. The "foot switch" NFET device is off during the precharge phase, and disconnects any discharging path from 'X' to ground. In a footless domino logic, the inputs to the gates should all have '0' logic value in the precharge phase, which is also desirable in normal domino logic to eliminate the charge sharing problem. During the evaluation phase, the foot switch transistor turns on and provides a discharging path from node 'X' to ground depending on the input values. However, the keeper circuit stays 'ON' during the time when the pull-down network begins to discharge the dynamic node until voltage of output node reaches a certain high voltage to turn off the PFET keeper device. This contention between the keeper and the pull-down network increases both delay of the gate and its power consumption and forms a trade-off between achievable performance, power consumption and noise margin of the dynamic logic [8]. This trade off is becoming more and more demanding in sub-100 nm technologies; because, as technology scales, leakage current of transistors increases tremendously, which implies that dynamic gates require larger keepers [9]. Moreover, process variation results in significant variation in leakage current of gates located on different regions of a die. As a result, to maintain appropriate level of noise margin for different gates spread over a chip, designers must use large p-type keepers such that sufficient amount of current is supplied to the dynamic node even in worst case scenarios [9].

In bulk CMOS technology, several works have been reported in keeper design to achieve high performance as well as high reliability. However, keeper design in FinFET is particularly challenging due to width quantization in FinFET structures that prevents simultaneously achieving good performance and reliability by continuous keeper sizing. Existing FinFET based domino logic design in [10] (Fig. 3) and [11] use a dual purpose 4T device to function as both keeper and precharge block, which reduces the dynamic power consumption by reduction of clock load capacitance (gate of precharge device), however, there is no optimization for performance and noise margin in the evaluation phase, since the keeper strength is fixed during the evaluation phase. Another domino logic proposed in [12] (Fig. 4) also uses a 4T device as keeper, where area overhead of the keeper block restricts the design to the high fan-in gates implementation. In [12], at the beginning of the evaluation phase, keeper device operates in single-gate (the gate connected to the output of the NAND gate has logic value '1') mode to reduce the contention between the keeper and the pull-down network. After a period equal to the delay produced by the delay elements, the keeper operates in double-gate (both gates have '0' logic value) mode to increase the noise margin. It is important to note that these ideas proposed in previous works can be implemented in bulk technology using body biasing or dual threshold devices. In this paper, we propose a new FinFET based domino logic that employs the exclusive

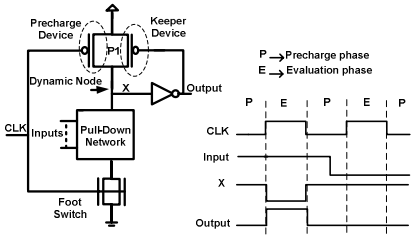

Fig.3. FinFET domino logic with dual purpose 4T FinFET used as precharge and keeper blocks [10]. The front-gate of P1 is the precharge device and the back-gate is the keeper device. Using merged precharge/keeper device (P1), reduces the clock load capacitance, leading to lower dynamic power. However, short-circuit current is same as in standard domino logic. Keeper strength does not change during the evaluation phase, hence there is no optimization with regards to performance and noise margin of the domino logic.

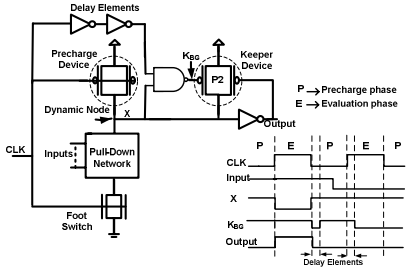

Fig.4. FinFET domino logic with 4T FinFET as keeper blocks [12]. At the beginning of evaluation phase, P2 operates in single-gate mode since the front-gate of P2 has logic value '1' (due to the delay elements), leading to lower contention between the keeper and pull-down network. Due to area overhead of the keeper block, the idea is only suitable for high fan-in gates. Similar design (using body biasing or dual-threshold devices) can be found in bulk CMOS technology.

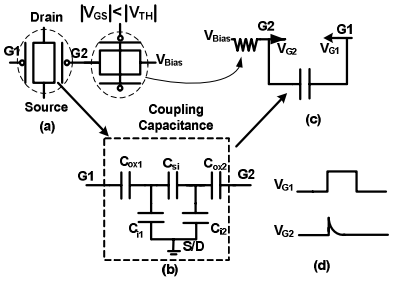

Fig.5. Resistive gate 4T FinFET structure. A 3T FinFET, which operates in sub-threshold regime and acts as a resistor is added to the back-gate (G2) of symmetric 4T FinFET. (b) Small-signal capacitance equivalent circuit of a FinFET [14]. (c) Circuit model of resistive gate 4T FinFET. By capacitive coupling of two gates, a differential circuit is formed. (d) Differential pulse on G2 (V_{G2}) formed due to transition in G1 (V_{G1}) for V_{Bias}=0.

property of FinFET devices (capacitive coupling between the front-gate and the back gate of 4T FinFET) to make the keeper transistor weaker at the beginning of the evaluation phase. This strategy reduces the contention between the keeper and the pull-down network, leading to higher performance and lower short-circuit power consumption. Using a resistive gate, a differential waveform at the gate of the keeper dynamically controls the gate-source voltage of the keeper transistor. At the beginning of the evaluation phase, lower gate-source voltage reduces the drive capability of the keeper, while the gate-source voltage gradually becomes V_{DD} (if pull-down network does not discharge the dynamic node) to achieve high noise margin. In the next two subsections, we explain the structure of the resistive gate FinFET device and its exploitation in FinFET based domino logic design.

III. RESISTIVE GATE FINFET

Fig. 5 illustrates the operation of the resistive gate FinFET, which is formed by a 4T FinFET and a 3T FinFET transistor that operates in sub-threshold regime (instead of a fixed resistor [13]) (Fig. 5(a)). The coupling capacitances between the two gates of the 4T FinFET are shown in Fig. 5(b), where C_{OX1} and C_{OX2} are the gate oxide capacitance of the front-gate and the back-gate respectively, C_{si} is fin capacitance, C_{i1} and C_{i2} are the inversion capacitances. Note that coupling capacitances are shown in equilibrium condition, i.e., no current flow between the source and the drain is assumed [14]. As a result, a differential voltage waveform appears on gate 2 (G2) due to transition (step) in gate 1 (G1), as shown in Fig. 5(d) and can be estimated from equation (2).

$$V_{G2} = V_{BIAS} + \alpha V_{G1} \exp(\frac{-t}{RC}) \quad (2)$$

Where R is resistance and C is the effective coupling capacitance between the two gates, and t is time. Values of C_{i1} and C_{i2} are negligible compared to those of the other capacitances in Fig. 5(b) for low gate voltage, which is desirable to have higher pulse at the resistor side (higher value of α). Fig. 6 shows implementation of the resistive gate FinFET (formed by P1 and P2), where P2 is a symmetric 3T FinFET in Fig. 6(a) and is an asymmetric 4T

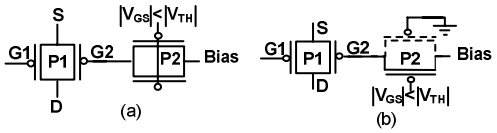

Fig.6. Resistive gate 4T FinFET structure implementation. P2 is a 3T FinFET in (a) and an asymmetric 4T FinFET in (b). high-V_{th} channel of P2 is shown with dashed line in (b).

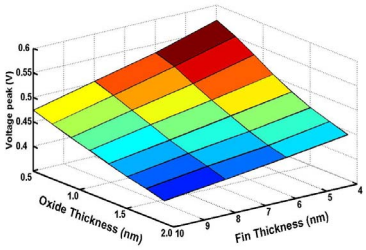

Fig.7. Peak value of the differential waveform at the back-gate (G2) of asymmetric resistive gate 4T FinFET (Fig. 6(b)) for 0→0.8V transition in the front-gate (G1). The sensitivity of the peak value (and hence the time constant of the differential waveform) to the fin and oxide thickness variation of P1 is low.

FinFET in Fig. 6(b) (due to different oxide thickness and gate work-function of the front-gate and the back-gate). In terms of fabrication, it has been demonstrated that 3T and 4T FinFETs as well as 3T and asymmetric 4T FinFET can be co-fabricated [15], [16]. The value of the resistor, and hence the waveform peak and time-constant for the back-gate (G2), can be controlled by the applied voltage (V_{GS}), and the threshold voltage or size of P2 in Fig. 6. As explained in the next section, we use the asymmetric resistive gate FinFET (Fig. 6(b)) in the new domino logic, which requires more fabrication steps, but provides higher noise margin. We also explain in section IV, why the resistive gate with fixed resistor [13] is not suitable for keeper design.

Variability of fin and oxide thickness is very important and should be considered in FinFET based circuit design. Fig. 7 shows the peak value of the differential waveform at the back-gate of P1 (G2) (in Fig. 6) for various fin and gate oxide thickness of P1. The sensitivity of the peak value (and the time constant) is low, which is helpful for reliable keeper design. Fig. 8 shows the differential waveform for different fin thickness of P1. Both peak value and time constant of differential waveform increases for thinner fins, however, they can also be controlled by the bias voltage of P2. This over-drive differential voltage pulse reduces the drive current of the p-type resistive gate, which is helpful at the beginning of the evaluation phase to reduce the contention between the keeper and the pull-down network. On the other hand, the input capacitance of the 4T resistive gate is smaller than the input capacitance of the 3T FinFET, since the gate capacitance of the second gate is decoupled from the input signal. Hence, the switching power can be reduced if resistive gate FinFET is used instead of 3T FinFET, especially for clock signal, since it has highest switching activity in VLSI systems.

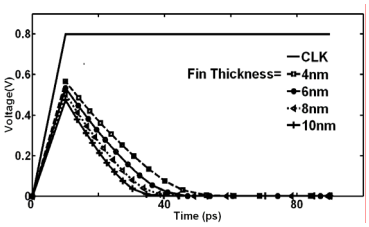

Fig.8. Differential waveform at the back-gate (G2) of P1 in resistive gate 4T FinFET (Fig. 6(b)) for 0→0.8V transition in the front-gate (G1). The peak value and time constant of the waveform can also be modulated by adjusting the size, threshold voltage, and gate voltage of P2 in Fig. 6.

IV. PROPOSED FINFET BASED DOMINO LOGIC

The structure of the proposed FinFET based domino logic is shown in Fig. 9, where a 4T p-type device (P1) is used as both the precharge and keeper device. The front-gate of P1 (FG1) is connected to *CLK* and acts as a precharge device, while the back-gate of P1 (BG1) plays the role of a keeper device. P2 is an asymmetric 4T FinFET, where the front-gate (FG2) (which is connected to the dynamic node 'x') is the low-V_{th} channel and the back-gate (BG2) (which is connected to the output) is the high-V_{th} channel.

In the precharge phase, *CLK* is '0', dynamic node is '1', and the output is '0'. P2 operates in single gate mode (front-gate (FG2) is biased to '1' and back-gate (BG2) is biased to '0'), and connects the back-gate of P1 (BG1) to the output, hence P1 operates in double gate mode (both front-gate and back-gate are biased to '0'). Note that the back-gate of P1 (BG1) can not completely discharge to zero voltage (V_{BG1} reaches a minimum value, which we call V_{BGMIN}), since P2 is diode connected in this structure. In the evaluation phase, if the dynamic node is discharged through the pull-down network, output makes a 0→1 transition. In this case, the front-channel of P2 (FG2) (channel near the front-gate), connects the back-gate of P1 (BG1) to the output instantly.

As explained, at the beginning of the evaluation phase, P1 and P2 form a resistive gate FinFET (as shown in Fig. 6(b)), and 0→1 transition of the clock, creates a differential waveform at the back-gate of P1 (BG1), which reduces the gate-source voltage of back-gate of P1 (BG1) (keeper device), thereby making P1 weaker than the pull-down network. Since the minimum voltage of BG1 is V_{BGMIN}, the differential waveform happens on top of V_{BGMIN}. However, upsizing or reducing the threshold voltage of P1 solves the driving degradation of P1 (since its back-gate voltage (BG1) does not reach zero voltage), and the proposed domino logic retrains it advantages.

Alternatively, to create a path for the back-gate of P1 to reach zero voltage, N1 is added to the design (Fig 10). N1 operates in sub-threshold regime, and helps P2 to discharge the back-gate of P1 completely (if input combination is '0') and increases the drive capability of P1, and hence increases noise margin of domino logic. In this structure, the asymmetric 4T FinFET (P2) can be replaced by 3T FinFET

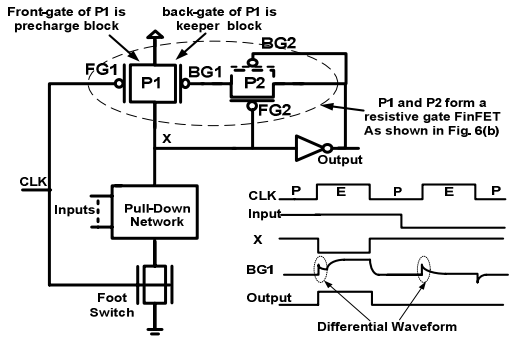

Fig.9. Structure of the proposed domino logic, where P1 and P2 are symmetric and asymmetric 4T FinFET, respectively. Front-gate of P1 plays the role of precharge device, while the back-gate of P1 and P2 form the keeper device. P2 acts as a resistor at the beginning of the evaluation phase, and forms the resistive gate 4T FinFET with P1. Differential waveform at the back-gate of P1 (Fig. 8) due to low to high transition of the clock, makes the keeper weaker at the beginning of the evaluation phase, and reduces the contention between the keeper and the pull-down network. The voltage at the back-gate of P1 can not reach zero, since a p-type device connects this node to the output. To solve this issue, N1 is added to the proposed domino logic as shown in Fig. 10.

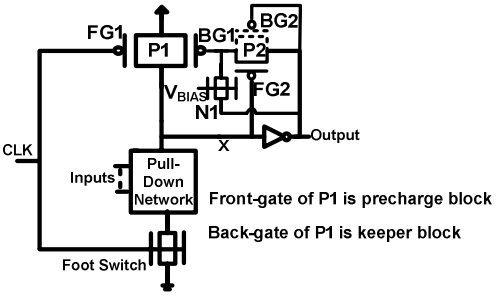

Fig.10. N1 is added to the domino logic proposed in Fig. 9 to help P2 in discharging the back-gate of P1, if needed. In this structure, the voltage of back-gate of P1 can go to V_{DD} or ground as shown in Fig. 11.

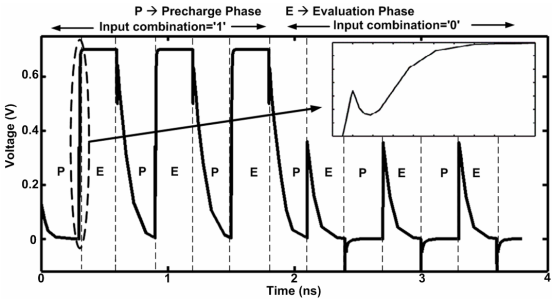

Fig.11. MEDICI predicted waveform at the back-gate of resistive gate 4T FinFET (BG1) for 0→0.7V transition in the front-gate. The peak value and time constant of the waveform can be adjusted by size, threshold voltage, and of P2 and gate voltage of N1 in Fig. 10. Inset shows the zoomed low-to-high transition.

(both gates connected to the dynamic node, as shown in Fig 6(a)), which makes the fabrication process easier at the cost of noise margin degradation. Note that, resistive gate with fixed resistor can not be used in keeper design, since the back-gate of P1 will be charged very slowly (through low pass filter consisting of the fixed resistor and gate capacitance of P1) and thereby increase the short-circuit power consumption. However, this is not the case in

proposed domino logic, since the back-gate of P1 is charged through front-channel (channel near the front-gate (FG2)) of P2, which has almost zero resistivity due to low V_{th}.

V. Analysis and Simulation Results

A mixed-mode device simulator [17] was used to analyze the proposed FinFET domino logic. FinFET parameters including 25 nm channel length, 1 nm gate oxide thickness, and 10 nm fin thickness were used in this work. Mid-gap metal gates were used for all p-type and n-type FinFETs, except that the work-function and the gate oxide thickness of the high-V_{th} gate for the asymmetric 4T FinFET was chosen to be 4.2 eV and 4 nm, respectively.

Fig. 11 shows the voltage waveform at the back-gate of P1 (in Fig. 10), for different input combinations. It can be observed that the differential voltage waveform at the beginning of the evaluation phase reduces the contention between the keeper (BG1) and the pull-down network. Fig. 12 shows the same waveform if a resistive gate with fixed resistor [13] is used in keeper design. The voltage of back-gate of P1, in this case, is charged very slowly (when pull-down network discharges the dynamic node), leading to high short-circuit current. Note that in precharge phase, the voltage of back-gate of P1 is not too important since the dynamic node is charged through front-channel of P1 (precharge block). For the same noise margin, Fig. 13 shows the short-circuit current of 2-input domino OR gates implemented with standard and proposed domino logic, for two different output load (1fF & 20fF). It can be observed that the proposed keeper reduces the contention between the pull-down network and the keeper block, leading to less short-circuit power during evaluation phase. The new design is more beneficial in high fan-in logic, where keeper size should increase (leading to higher capacitive coupling) to compensate the leakage current of the pull-down network and provide high noise margin.

In multi-level domino logic (Fig. 14), the size of N1 (in Fig. 10) should be smaller than that in the previous level (stage) to guarantee weak keeper when the pull-down network starts to discharge. However, with a conservative keeper design for the first stage, the same keeper can be used for all stages. Proposed domino logic is well suited for clock-delay domino logic, where all the logic gates in a level receive the data and the delayed clock from the previous level only. The delay for each stage is determined by the evaluation time of the previous stage. Fig. 15 shows the output waveform of two input OR-gate in standard and proposed domino logic for C_L=50fF, when one input makes 0→1 transition. Table 1, compares the delay and power consumption of the proposed and standard domino logic for the same noise margin, clock frequency of 2.5 GHz and V_{DD} of 0.8V. It can be observed that the proposed domino logic has better performance compared to that of the standard domino logic, since contention between the keeper and the pull-down network is reduced by using resistive gate keeper.

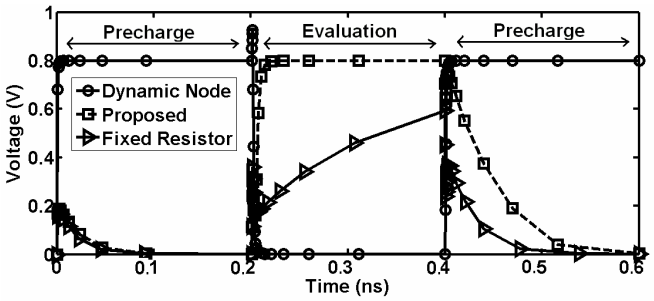

Fig.12. MEDICI predicted waveforms at the back-gate of P1 (in Fig. 10) for 0→0.8V transition in its front-gate, when the resistive gate with fixed resistor and is used in the keeper design. In this case, voltage of back-gate of P1 goes very slowly to '1', leading to high short-circuit current. Voltage of the dynamic node is also shown as a reference.

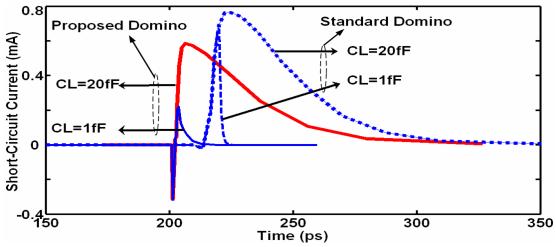

Fig.13. MEDICI predicted short-circuit current at the evaluation phase, in proposed and standard domino logic design. New keeper reduces the contention between the keeper and the pull-down network, and hence improves the performance of the domino logic and reduces the short circuit power consumption.

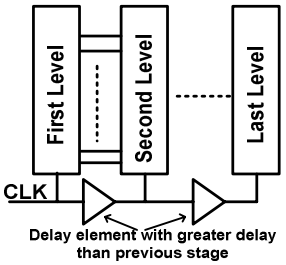

Fig.14. Structure of a multi-level clock-delay domino logic, where the delay of the clock-network between stages is slightly bigger than the previous stage. Proposed domino logic is suited for clock-delay domino logic.

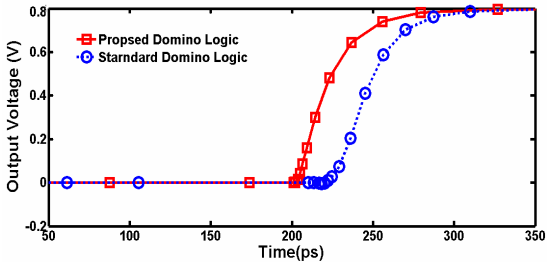

Fig.15. Output waveform of the proposed and the standard domino logic NOR gate. The proposed domino logic is faster, since the contention between the keeper and the pull-down network is reduced without penalty in noise margin (C_L=50fF).

It is worth noting that the delay of both proposed domino logic and standard domino logic can be reduced by using skewed output inverter (for fast low-to-high transition) [18]. Lower power consumption of proposed domino logic comes from lower short-circuit power, and lower switching power

Table 1. Comparison between delay and power of different domino logic gates for the same noise margin.

	Delay (ps)				Power (μW)			
	Standard		Proposed		Standard		Proposed	
Load	1fF	10fF	1f	10fF	1f	10fF	1f	10fF
AND2	8	35	4	18	3	7	1.6	5
OR2	6	28	3	15	5	11	4	9
AND4	13	42	9	23	2	5	1	4
OR4	9	47	6	25	7	13	5	10
OR8	13	53	7	26	9	17	6	12
OR16	18	62	10	29	12	28	8	19

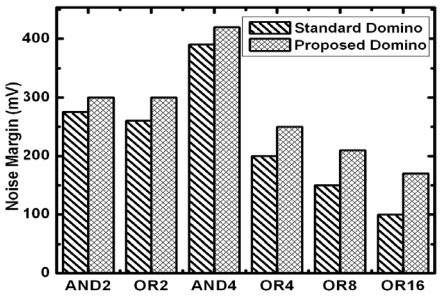

Fig.16. For same delay, the proposed domino logic has higher noise margin compared to the standard domino logic. Note that for same keeper drive capability, standard domino logic will have slightly higher noise margin at the cost of lower performance.

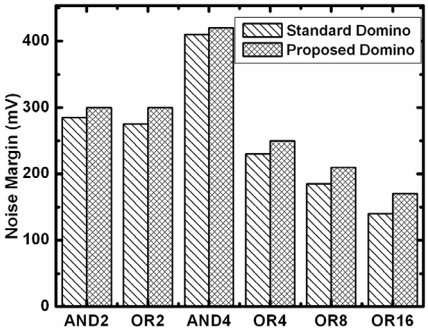

Fig.17. For same power consumption, proposed domino logic has higher noise margin compared to the standard domino logic. Again, for same keeper drive capability, standard domino logic has slightly higher noise margin at the cost of higher power consumption.

due to reduction of clock load capacitance by using resistive gate in the precharge and the keeper blocks. Note that, for equivalent drive capability of the keeper (in proposed and standard domino), standard domino has slightly higher noise margin, since in the proposed structure, keeper is weaker at the beginning of the evaluation phase. However, as shown in Fig. 16 and Fig. 17, for same performance and/or power constraints, the proposed structure has better noise margin, since to satisfy the delay and/or power constraints, smaller keeper device should be employed in standard domino logic, leading to noise margin degradation.

VI. CONCLUSION

A novel FinFET based domino logic is proposed that exploits the exclusive FinFET property (capacitive coupling between front-gate and the back-gate) and has higher performance and lower power consumption, with negligible area overhead compared to standard domino logic. The new design is more beneficial in high fan-in logic, where larger keeper is needed to compensate for the leakage current of the pull-down network and provide sufficient noise margin.

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