WIP: Open-Source Standard Cell Characterization Process Flow on 45 nm (FreePDK45), 0.18 μm, 0.25 μm, 0.35 μm and 0.5 μm

Rabin Thapa and Samira Ataei and James E. Stine
Electrical and Computer Engineering Department, VLSI Computer Architecture Research Group,
Oklahoma State University, Stillwater, OK 74078
{rabin.thapa, ataei, james.stine}@okstate.edu

***Abstract*—This paper describes the design flow of the standard cell characterization on five different technologies and integration of its results with other VLSI tools processes that can be duplicated and implemented for the research and education in the academia. In this proposed work, one design flow is on non-fabricable technology of open-source false-technology FreePDK45 of 45 nm CMOS technology [1]. The other design flows are in the fabricable technology in 0.18 μm, 0.25 μm, 0.35 μm and 0.5 μm. The design flow are automated to simplify the students with intricacy of the tools. This design flows in this work are automated for the tool, Virtuoso `Liberate` from Cadence Design Systems and students can easily adopt it as part of the VLSI design class curriculum. This characterization flow precisely models the electrical characteristics of the cell that has been subjected to different input variables as explained below. The characterized models are of high demand in other design tools used in between RTL to GDSII process flow.**

I. Introduction

Many in the academia find it difficult to characterize standard cells, mostly because there are very few open source standard-cells libraries available to begin with. Many of the IC Companies have their own standard-cell libraries which they use for their own internal purposes. The use of these libraries outside the companies are restricted due the proprietary information contained within. So, an open source standard-cell library on various technologies, which would be very helpful for the research and education in the academia, is the need of the time. With this objective in mind, a previously introduced standard-cell library in 0.5 μm technology [2], [3] was introduced. Couple of years later, in 2007, the same author along with a joint team from Oklahoma State University and North Carolina State University jointly published the open source FreePDK 45nm Standard cells [1]. Each library for each technologies consists of multiple cells of different drive strength. This proposed work has borrowed the standard cells for characterization from these works. The main purpose here is to provide an updated mechanism for characterization for these standard-cell libraries. Moreover, repeatable characterization scripts are given to help researchers redo or characterize new cells for their flows [1]. The tools used for characterization for this proposed work is Virtuoso Liberate from Cadence Design Systems (CDS). To the best of our knowledge, this is the only open source standard cell characterization process flows available to the public that works on this tool.

II. The Process Flow

A. Characterization Flow

The standard cell characterization flow begins with three basic input files. First, a netlist layout of the cell in SPICE format is required. The layout tool, magic was used to generate the files in this work. Second, information on the device technology that is dependent on the specific technology and the process utilized is required. Finally, a file is required that consists of information on the operational temperature and voltage used on the cells along with the two dimensional table with input slew on one axis and output capacitive load on another. For this work, open-source non-fabricable FreePKD45 of 45 nm CMOS technology [1] and the fabricable standard cells in 0.18 μm, 0.25 μm, 0.35 μm and 0.5 μm are included in this characterization flow. Each of these libraries are characterized for at least three process corners: typical, best and worst cases.

Upon characterization of the cells, detailed views on the electrical behavior of each of the cells are generated. These views of the cell differ when exposed to different processes and environmental variations, the variation of the input slew and the various output load capacitance. The database is created by the tool and stores all these informations and generates the characterization reports. The characterization report models the electrical behavior of the standard cell; it consists of timing, power and signal integrity (noise) results based on variation of input parameters. One of the generated files is an electric view of Non-Linear Delay model (NLDM). The NLDM with timing/power information are further used as

[1]The original FreePDK45 standard-cell library from Oklahoma State University had some issues with its characterization despite detailed scripts available within the library. Although researchers could have realized these errors and rerun the characterization, this work fixes some of those errors and updates the scripts with the new characterization tool.

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TABLE I
INPUT FILES USED FOR THE CHARACTERIZATION

Directory or File	Contains Information on
MODELS	Device technology
NETLIST	Transistor netlist in SPICE format
TEMPLATE	Slew, output load, cell names
.tcl	Various files with tcl commands

a baseline for other delay models such as Composite Current Source, (CCS) and Effective Current Source (ECS) models.

Although standard-cell libraries are useful, they are difficult to integrate into design flows because most of the electronic design automation softwares are complex. However, the innate educational value to have a design flow along with standard-cell libraries and memories is paramount to educating future engineers. Therefore, the process designed here would be incomplete without any design flow integration. The methodology is to integrate both the characterized standard-cell libraries, along with the work from OpenRAM [4], to create a complete element that can be manipulated by different Universities and research programs. OpenRAM is an open-source, portable and flexible memory compiler that generates different size and configuration of SRAMs for FreePDK45 [1] and Scalable CMOS [5] technologies. Figure 1 shows a sample design that has been placed and routed using the library. The design flow and all scripts are available for free academic use at http://vlsiarch.ecen.okstate.edu.

III. CHARACTERIZATION FLOW WITH AN EXAMPLE

The input files are summarized in Table I and list of cells used are illustrated in Table II. Below, steps are introduced for creating standard cell characterization of an inverter in 45nm technology. These steps can be duplicated for any cells in any technology by using proper related files. The base files can be downloaded from http://vlsiarch.ecen.okstate.edu.

- Within the MODELS sub folder, the file with *.sp* extension has the correct device technology file with the process corners used for both pMOS and nMOS CMOS transistors.

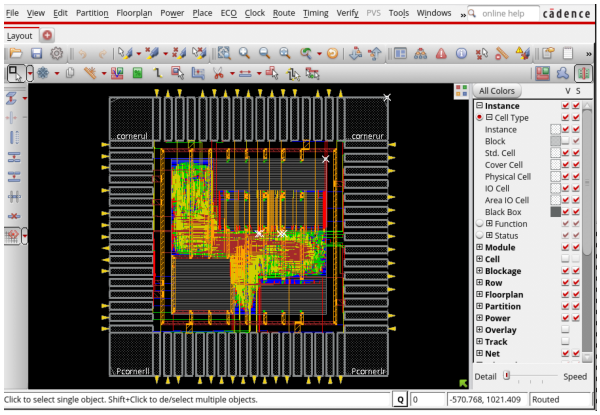

Fig. 1. FreePDK45 Placement and Routing.

TABLE II
STANDARD CELLS LIST IN CHARACTERIZATION FLOW.

Cells
INVX1, INVX2, INVX4, INVX8
OR2X1, OR2X2, NOR2X1,NOR3X1,
AND2X1, AND2X1, AND2X2, NAND2X1, NAND3X1,
XNOR2X1, XOR2X1,
BUFX2, BUFX4, CLKBUF1, CLKBUF2, CLKBUF3
FAX1, HAX1,
OAI21X1, OAI22X1, AOI21X1, AOI22X1,
DFFNEGSQ, DFFPOSSQ, DFFSRSQ, LATCHSQ
Xn indicates drive strength, where n=1, 2, 3, 4
SQ indicates sequential circuit

- Within the NETLIST sub folder, netlists contains the layout netlist in SPICE format.
- Within the TEMPLATE sub folder, the template_OSU.*tcl* file contains all the input signal slew and output capacitive loads, the lower and upper slew values, the name of the cell used.
- Within the char.*tcl* file, all the environmental variables like voltage, temperature are included. Some Tcl scripts provided by the CDS have been modified and reused to create the necessary results.
- Next, the CCS and/or ECSM results are created. The file rechar.*tcl* has been modified to accomodate this. CCS and ECSM related files are placed in separate folders to create separate results.
- A `Makefile` has been created to hide the intricacy of calling different commands and making it easy to run the complete process.

IV. CONCLUSIONS

This paper introduces the design flow of the characterization and integration with other VLSI tools for academia. The first part is the characterization flow for non-fabricable FreePDK45 standard cells using the Virtuoso Liberate tool from Cadence. The fabricable standard cells from other technologies (0.5 μm, 0.35 μm, 0.25 μm and 0.18 μm) are also included in this characterization flow. The main motivation behind this open-source standard cells characterization process flow and integration is to promote research and education in academia.

REFERENCES

[1] J. Stine, I. Castellanos, M. Wood, J. Henson, F. Love, W. Davis, P. Franzon, M. Bucher, S. Basavarajaiah, J. Oh, and R. Jenkal, "FreePDK: An open-source variation-aware design kit," in *International Conference on Microelectronic Systems Education*, pp. 173–174, June 2007.

[2] J. Grad and J. E. Stine, "A standard cell library for student projects," 2003.

[3] J. Grad, J. E. Stine, and D. D. Neiman, "Real world SoC experience for the classroom," in *2005 IEEE International Conference on Microelectronic Systems Education (MSE'05)*, pp. 49–50, June 2005.

[4] M. R. Guthaus, J. E. Stine, S. Ataei, B. Chen, B. Wu, and M. Sarwar, "Openram: An open-source memory compiler," in *2016 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 1–6, Nov 2016.

[5] MOSIS, "MOSIS scalable CMOS (SCMOS) design rules." https://www.mosis.com/files/scmos/scmos.pdf, 2017.