Politecnico di Torino

TAMTAMS Web

Integrated System Technology

NAND/AND MODULES:

Delay_Pow_nand2_cmos, Delay_Pow_nand3_cmos, Delay_Pow_nand4_cmos
Delay_Pow_nor2_cmos, Delay_Pow_nor3_cmos, Delay_Pow_nor4_cmos

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Contents

1 Introduction

Analysis and parameters estimation in terms of power and delay of different single logic gates. To do that *NAND2, NAND3, NAND4* and *NOR2, NOR3, NOR4* logic gates implemented in *CMOS-logic* are analysed.
This *OCTAVE* files are implemented for *TAMTAMS*:

- **Delay_Pow_nand2_cmos.m**: CMOS-logic 2-inputs NAND;
- **Delay_Pow_nand3_cmos.m**: CMOS-logic 3-inputs NAND;
- **Delay_Pow_nand4_cmos.m**: CMOS-logic 4-inputs NAND;
- **Delay_Pow_nor2_cmos.m**: CMOS-logic 2-inputs NOR;
- **Delay_Pow_nor3_cmos.m**: CMOS-logic 3-inputs NOR;
- **Delay_Pow_nor4_cmos.m**: CMOS-logic 4-inputs NOR;

where the following parameters are estimated:

- **Delay_nand_and**: input to output delay;
- **Pnand_and_dyn**: dynamic power;
- **Pnand_and**: static power;

2 Logic Implementation

The different logic gates involved into the analysis are represented in form of schematic.
The dimension of the transistor are forced in order to have a resistance (and an I_{on}) equal to the inverter of minimal dimension.
In figure 1 is possible to see the reference schematic for the *CMOS* logic. The structure is the most known one based on a pull-up and a pull-down structure.

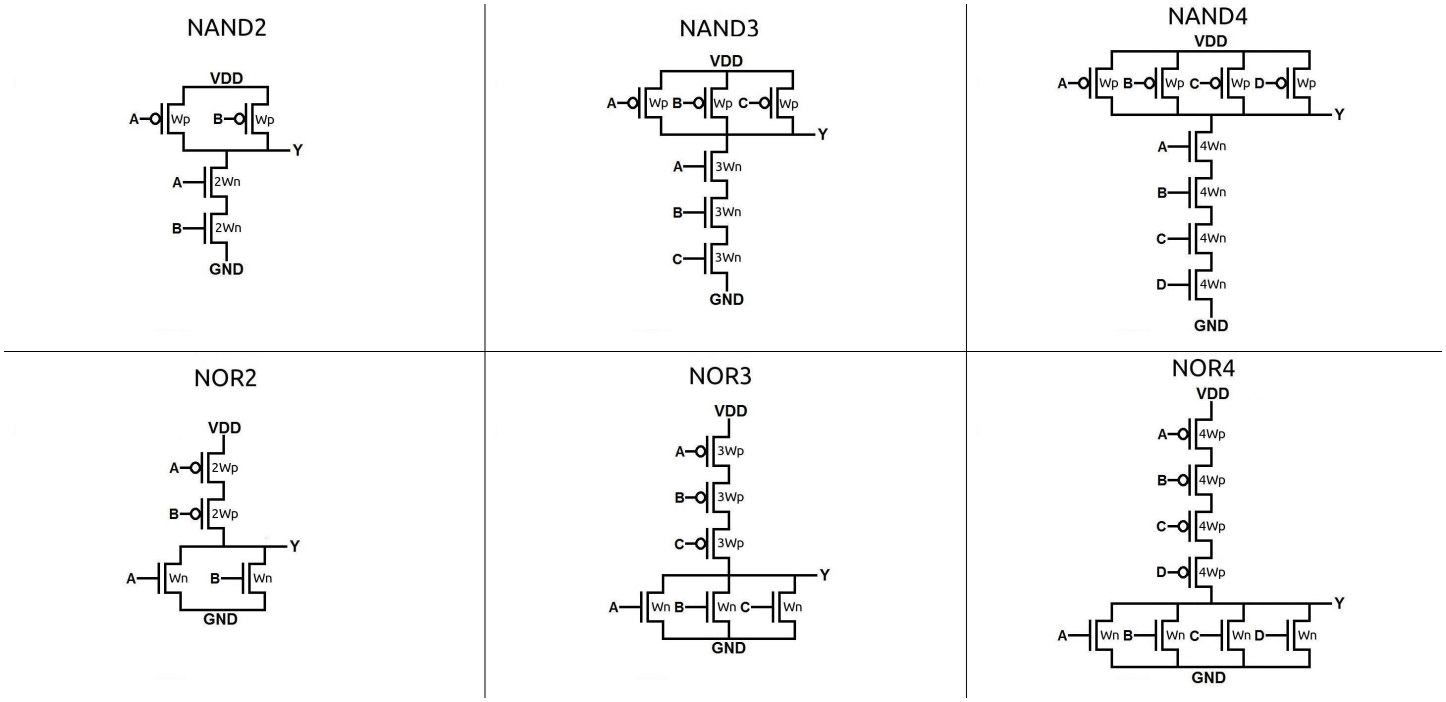

Figure 1: CMOS schemes

3 Delay

3.1 Theoretical Analysis

The delay analysis of the different gates is implemented exploiting the *Elmore* Delay model, taking into account that it is an optimistic model. Moreover it could be used to easily compare different technological implementation.
Necessary technological parameters in order to evaluate the delay are reported below.
The analysis is done on gate with a load made of a minimum inverter or multiple of it. Is possible compute input capacitance of *n-MOS* and *p-MOS* transistors per unit length:

$$C_{in_N} = C_{OX} + C_{overlapN} \quad [pF/\mu m] \tag{1}$$
$$C_{in_P} = C_{OX} + C_{overlapP} \quad [pF/\mu m] \tag{2}$$

where the two overlap capacitances are due to the overlap size between the gate and drain/source areas:

$$C_{overlapN} = 10^6 \cdot C_{GDOn} \quad [pF/\mu m] \tag{3}$$
$$C_{overlapP} = 10^6 \cdot C_{GDOp} \quad [pF/\mu m] \tag{4}$$

The junction capacitances between source and drain are:

$$C_{jN} = C_{bottomN} + C_{sidewallN} \quad [pF/\mu m] \tag{5}$$
$$C_{jP} = C_{bottomP} + C_{sidewallP} \quad [pF/\mu m] \tag{6}$$

C_{bottom} is the capacitance due to the area of the pool of the source/drain and $C_{sidewall}$ is the one due to the edge of the same pool.

$$C_{bottomN} = C_{j0_N} \cdot \left(1 + \frac{V_{DD}}{2 \cdot P_{bN}}\right)^{-M_{jN}} \cdot 2.5 \cdot L_{drawn} \quad [pF/\mu m] \tag{7}$$
$$C_{bottomP} = C_{j0_P} \cdot \left(1 + \frac{V_{DD}}{2 \cdot P_{bP}}\right)^{-M_{jP}} \cdot 2.5 \cdot L_{drawn} \quad [pF/\mu m] \tag{8}$$
$$C_{sidewallN} = 10^6 \cdot C_{sw_N} \cdot \left(1 + \frac{V_{DD}}{2 \cdot P_{bswN}}\right)^{-M_{jswN}} \quad [pF/\mu m] \tag{9}$$
$$C_{sidewallP} = 10^6 \cdot C_{sw_P} \cdot \left(1 + \frac{V_{DD}}{2 \cdot P_{bswP}}\right)^{-M_{jswP}} \quad [pF/\mu m] \tag{10}$$

Moreover for the estimation of parasitic capacitances C_{jN} and C_{jP}, it is necessary to evaluate the perimeter.

$$\text{perim}_N = 2 \cdot \text{lungh\_diff} + W_N[\mu m] \tag{11}$$
$$\text{perim}_P = 2 \cdot \text{lungh\_diff} + W_P[\mu m] \tag{12}$$

We consider only one side for the W, because the internal one does not touch a conductor, but just a spatial charge.
Therefore C_{jN} and C_{jP} are:

$$C_{jN} = C_{bottomN} \cdot W_N + C_{sidewallN} \cdot \text{perim}_N \quad [pF] \tag{13}$$
$$C_{jP} = C_{bottomP} \cdot W_P + C_{sidewallP} \cdot \text{perim}_P \quad [pF] \tag{14}$$

Now we have to evaluate the equivalent resistance of the *MOS* that contributes in the delay calculation:

$$R_n = \frac{1}{\mu_n \cdot C_{OX} \cdot \frac{W_N}{L_{eff}} \cdot (V_{DD} - V_{tn})} \quad [\Omega] \tag{15}$$

$$R_p = \frac{1}{\mu_p \cdot C_{OX} \cdot \frac{W_P}{L_{eff}} \cdot (V_{DD} - V_{tp})} \quad [\Omega] \tag{16}$$

Another parameters used in our analysis is h. It's simply the multiplier of the number of inverter linked in output, the parametrized fan-out.

3.2 Delay calculation

In figure:2 the *Elmore* model of *NAND2-CMOS* gate is shown. The computation are made by summing partial product between parasitic capacitance and resistance. To compute the delay of all gates in analysis the same model it's applied.

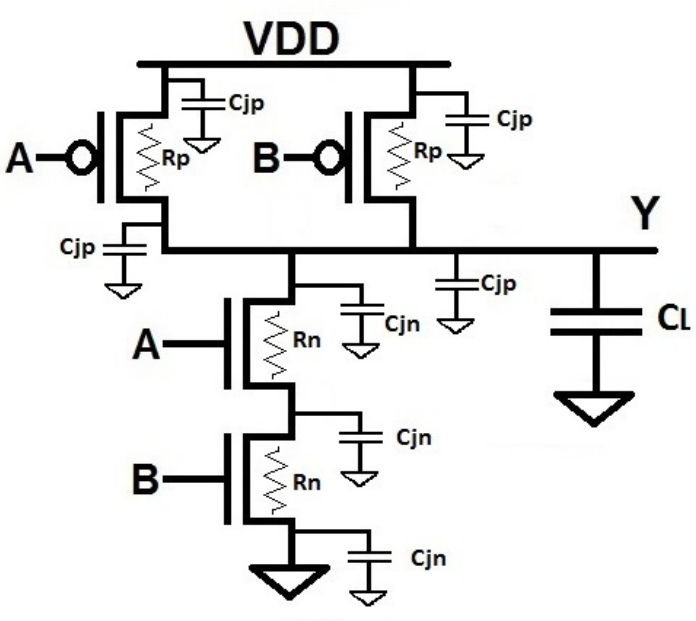

Figure 2: CMOS-NAND2 Elmore Model

Obviously there are different delay depending on the inputs combinations, we take in account the worst case that produce the maximum delay for the gate. For example is easy to see that the worst case for the rise time in the *NAND2* is when only one of the inputs it's low, because in case of all input in *low-state* the resistance is halved. While for the fall time there is only one case. All these reasoning are specular in the *NOR* gates.

- **NAND2-CMOS**

$$tr_{cnand2} = R_p \cdot (C_{jp} + C_{jp} + C_{jn} + h \cdot C_L) = R_p \cdot (2 \cdot C_{jp} + C_{jn} + h \cdot C_L) \tag{17}$$

$$tf_{cnand2} = R_n \cdot (C_{jn} + C_{jn} + C_{jp} + C_{jp} + h \cdot C_L) + R_n \cdot (C_{jn} + C_{jp} + C_{jp} + h \cdot C_L) = R_n \cdot (3 \cdot C_{jn} + 4 \cdot C_{jp} + 2 \cdot h \cdot C_L) \tag{18}$$

- **NAND3-CMOS**

$$tr_{cnand3} = R_p \cdot (3 \cdot C_{jp} + C_{jn} + h \cdot C_L) \tag{19}$$

$$tf_{cnand3} = R_n \cdot (6 \cdot C_{jn} + 9 \cdot C_{jp} + 3 \cdot h \cdot C_L) \tag{20}$$

- **NAND4-CMOS**

$$tr_{cnand4} = R_p \cdot (4 \cdot C_{jp} + C_{jn} + h \cdot C_L) \tag{21}$$

$$tf_{cnand4} = R_n \cdot (10 \cdot C_{jn} + 16 \cdot C_{jp} + 4 \cdot h \cdot C_L) \tag{22}$$

- **NOR2-CMOS**

$$tr_{cnor2} = R_p \cdot (C_{jn} + C_{jn} + C_{jp} + C_{jp} + h \cdot C_L) + R_p \cdot (C_{jn} + C_{jp} + C_{jp} + h \cdot C_L) = R_p \cdot (3 \cdot C_{jn} + 4 \cdot C_{jp} + 2 \cdot h \cdot C_L) \tag{23}$$

$$tf_{cnor2} = R_n \cdot (C_{jn} + C_{jn} + C_{jp} + h \cdot C_L) = R_p \cdot (2 \cdot C_{jn} + C_{jp} + h \cdot C_L) \tag{24}$$

- **NOR3-CMOS**

$$tr_{cnor3} = R_p \cdot (6 \cdot C_{jp} + 9 \cdot C_{jn} + 3 \cdot h \cdot C_L) \tag{25}$$

$$tf_{cnor3} = R_n \cdot (3 \cdot C_{jn} + C_{jp} + h \cdot C_L) \tag{26}$$

- **NOR4-CMOS**

$$tr_{cnor4} = R_p \cdot (10 \cdot C_{jp} + 16 \cdot C_{jn} + 4 \cdot h \cdot C_L) \tag{27}$$

$$tf_{cnor4} = R_n \cdot (4 \cdot C_{jn} + C_{jp} + h \cdot C_L) \tag{28}$$

4 Dynamic Power

4.1 Theoretical Analysis

The dynamic power can be evaluated through the following:

$$P_{dynamic} = \frac{1}{2} \cdot f \cdot C \cdot \alpha \cdot V_{DD}^2 \quad [W] \tag{29}$$

Where α is the switching activity, f the frequency and C the total capacitance.
This analysis was made imposing two assumption in order to get simplified expression to easily make consideration on the technological behaviour of described gates:

- The input probability is always considered as $\frac{1}{2}$;
- The computation of the switching activity for every single node is based on a *probabilistic model* (shown in detail later).

All the necessary technological parameters involved into this analysis are detailed in 3.1.

4.2 Dynamic power calculation

For demonstrative purpose a procedure to calculate the dynamic power of the *NAND2-CMOS* gate is reported.
In Figure 3 the scheme of the *NAND2* gate is shown.

$$C \cdot \alpha = C_{IN} \cdot (\alpha_A + \alpha_B) + C_M \cdot \alpha_M + C_X \cdot \alpha_X \tag{30}$$

The considered capacitances are the following:

- C_{IN} is the input capacitance associate at only one input:

$$\begin{aligned} C_{IN} &= C_{OX} \cdot 2W_N \cdot L_{eff} + C_{OX} \cdot W_P \cdot L_{eff} + 2C_{overlapN} + 2C_{overlapP} = \\ &= 2C_{OXN} + C_{OXP} + 2C_{overlapN} + 2C_{overlapP} \quad [pF] \end{aligned} \tag{31}$$

- C_M is the output capacitance:

$$C_M = 2C_{jN} + 2C_{jP} + C_L \quad [pF] \tag{32}$$

  C_{jP} is multiplied by 2 because we have different pools for the two drains and C_{jN} is also multiplied by 2 because the *n-MOS* have dimension $2W_N$.

- C_X is the internal capacitance between the two *n-MOS* transistors in the pull-down network, supposing that source and drain are common for the two *n-MOS*:

$$C_X = 2C_{jN} \quad [pF] \tag{33}$$

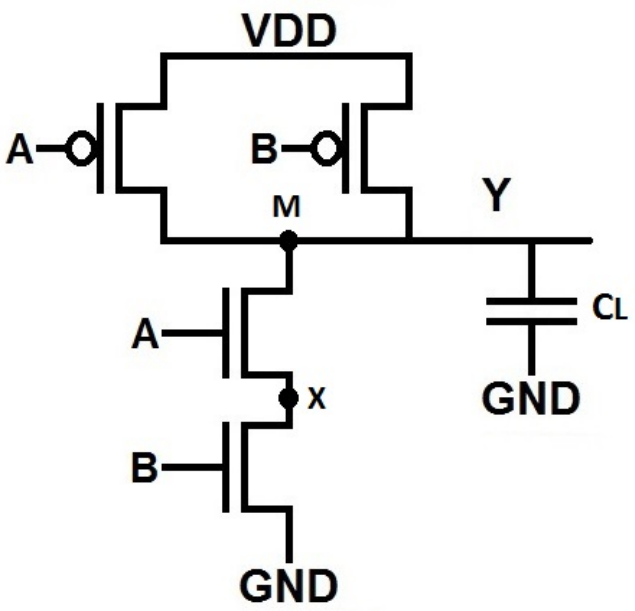

Figure 3: CMOS 2-input NAND architecture

Regarding the switching activity it can be computed in the following way if the *probabilistic model* is considered :

$$\alpha = 2P(1-P) \tag{34}$$

Where P is the probability that the generic node is at *one*. Supposing that the probability of each input to be at *one* is $\frac{1}{2}$ we get:

$$\alpha_A = \alpha_B = \frac{1}{2} \tag{35}$$

For the node M:

$$P_M = 1 - P_A \cdot P_B \rightarrow \alpha_M = \frac{3}{8} \tag{36}$$

For the internal node X, the probability is given by:

$$P_X = P_A(1-P_B) \rightarrow \alpha_X = \frac{1}{2} \tag{37}$$

Summing up the final expression is the following:

$$C \cdot \alpha = 2C_{OXN} + C_{OXP} + 2C_{overlapN} + 2C_{overlapP} + \frac{3}{8} \cdot (2C_{jN} + 2C_{jP} + C_L) + \frac{1}{2} \cdot 2C_{jN} \tag{38}$$

The other logic gates are analysed in similar way.
Here are reported just the final expression for $C \cdot \alpha$ in those cases:

- **NAND3-CMOS**:

$$C \cdot \alpha_{CNAND3} = \frac{3}{2} \cdot (3C_{OXN} + C_{OXP} + 2C_{overlapN} + 2C_{overlapP}) + \frac{7}{32} \cdot (3C_{jN} + 3C_{jP} + C_L) + \frac{19}{32} \cdot 3C_{jN} \tag{39}$$

- **NAND4-CMOS**:

$$C \cdot \alpha_{CNAND4} = 2 \cdot (4C_{OXN} + C_{OXP} + 2C_{overlapN} + 2C_{overlapP}) + \frac{11}{94} \cdot (4C_{jN} + 4C_{jP} + C_L) + \frac{5}{9} \cdot 4C_{jN} \quad (40)$$

- **NOR2-CMOS**:

$$C \cdot \alpha_{CNOR2} = C_{OXN} + 2C_{OXP} + 2C_{overlapN} + 2C_{overlapP}) + \frac{3}{8} \cdot (2C_{jN} + 2C_{jP} + C_L) + \frac{3}{8} \cdot 2C_{jP} \quad (41)$$

- **NOR3-CMOS**:

$$C \cdot \alpha_{CNOR3} = \frac{3}{2} \cdot (C_{OXN} + 3C_{OXP} + 2C_{overlapN} + 2C_{overlapP}) + \frac{7}{32} \cdot (3C_{jN} + 3C_{jP} + C_L) + \frac{19}{32} \cdot 3C_{jP} \quad (42)$$

- **NOR4-CMOS**:

$$C \cdot \alpha_{CNOR4} = 2 \cdot (C_{OXN} + C_{OXP} + 2C_{overlapN} + 2C_{overlapP}) + \frac{11}{94} \cdot (4C_{jN} + 4C_{jP} + C_L) + \frac{59}{83} \cdot 4C_{jP} \quad (43)$$

5 Static Power

5.1 Theoretical Analysis

The static power can be evaluated as shown below:

$$P_{static} = V_{DD} \cdot I_{leak} \quad [W] \tag{44}$$

where I_{leak} is the total leakage current and V_{DD} is the supply voltage. For the leakage current we consider two factors:

- **I_{OFF} - Subthreshold current**: is the leakage current that flows drain-source when $V_{GS} = 0$ and $|V_{DS}| = V_{DD}$ as shown in figure 4.

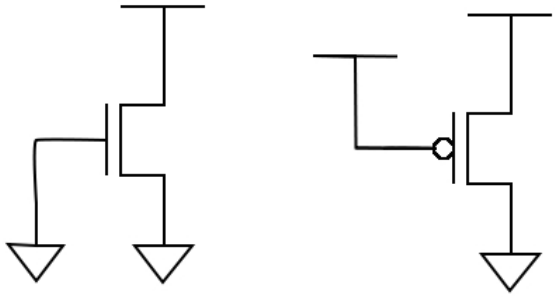

Figure 4: Leakage drain/source current when MOS are off

- **I_{GATE} - Gate Current**: is the leakage current that flows from drain and source to gate or vice versa when $|V_{GS}| = V_{DD}$ and $V_{DS} = 0$ as can be seen in fig 5. Also in other condition a small gate current could appear but is possible to say that in those other cases the contribution is negligible.

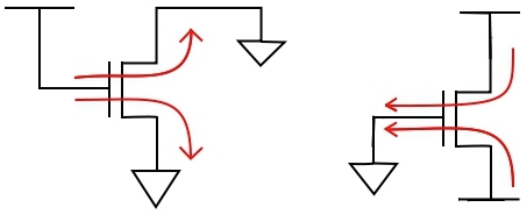

Figure 5: Leakage gate current

5.2 Static power calculation

As example the detailed procedure used to estimate the static power of the *NAND2-CMOS* is presented. Every possible combination of the two inputs are considered and for each of those cases the different appearing leakages contribution are taken into account. The table 1 is used to show this operation.

A	B	Y	LEAKAGE CURRENT
0	0	1	$I_{OFFn}2W_N + 2 \cdot I_{GATEp}W_P$
0	1	1	$I_{OFFn}2W_N + I_{GATEn}2W_N + I_{GATEp}W_P$
1	0	1	$I_{OFFn}2W_N + I_{GATEp}W_P$
1	1	0	$2 \cdot I_{OFFp}W_P + 2 \cdot I_{GATEn}2W_N$

Table 1: Leakage current contributes for each combination of inputs

I_{OFF} is the drain/source off current and I_{GATE} is the gate current. Those contribution are multiplied by the effective dimension of transistor.
Considering the inputs as equally probable is possible to found the total leakage current as the mean value:

$$I_{leakCNAND2} = \frac{1}{4} \cdot (2 \cdot I_{OFFp}W_P + 4 \cdot I_{GATEp}W_P + 3 \cdot I_{OFFn}2W_N + 3 \cdot I_{GATEn}2W_N) \quad [nA] \tag{45}$$

Exploiting the same analysis is possible to found an expression for the static current for all the other gates. Only the final expression are reported below.

- **NAND3-CMOS**:
  $I_{leakCNAND3} = \frac{1}{8} \cdot (3 \cdot I_{OFFp}W_P + 12 \cdot I_{GATEp}W_P + 7 \cdot I_{OFFn}3W_N + 7 \cdot I_{GATEn}3W_N) \quad [nA]$
- **NAND4-CMOS**:
  $I_{leakCNAND4} = \frac{1}{16} \cdot (4 \cdot I_{OFFp}W_P + 32 \cdot I_{GATEp}W_P + 15 \cdot I_{OFFn}4W_N + 15 \cdot I_{GATEn}4W_N) \quad [nA]$
- **NOR2-CMOS**:
  $I_{leakCNOR2} = \frac{1}{4} \cdot (3 \cdot I_{OFFp}2W_P + 3 \cdot I_{GATEp}2W_P + 2 \cdot I_{OFFn}W_N + 4 \cdot I_{GATEn}W_N) \quad [nA]$
- **NOR3-CMOS**:
  $I_{leakCNOR3} = \frac{1}{8} \cdot (7 \cdot I_{OFFp}3W_P + 7 \cdot I_{GATEp}3W_P + 3 \cdot I_{OFFn}W_N + 12 \cdot I_{GATEn}W_N) \quad [nA]$
- **NOR4-CMOS**:
  $I_{leakCNOR4} = \frac{1}{16} \cdot (15 \cdot I_{OFFp}4W_P + 15 \cdot I_{GATEp}4W_P + 4 \cdot I_{OFFn}W_N + 32 \cdot I_{GATEn}W_N) \quad [nA]$

6 Octave Implementation

In table 2 the variables used into the modules are reported and in table 3 there are the output parameters estimates.

Code variable	Source file	Physical quantity
Lgate	Technology file	nm
Wgate	Technology file	μm
Vdd	Technology file	V
Xj	Technology file	nm
Cox	Technology file	F/cm^2
Cj0n	Technology file	$pF/\mu m^2$
Cjswn	Technology file	$pF/\mu m^2$
Cj0p	Technology file	$pF/\mu m^2$
Cjswp	Technology file	$pF/\mu m^2$
Cgd0n	Technology file	F/m
Cgd0p	Technology file	F/m
Gamma	Technology file	–
Mjn	Technology file	%
Mjp	Technology file	%
Mswn	Technology file	%
Mswp	Technology file	%
Pbn	Technology file	V
Pbp	Technology file	V
Pbswn	Technology file	V
Pbswp	Technology file	V
mueff_n	Mobility module	cm^2/Vs
mueff_p	Mobility module	cm^2/Vs
Vth_n	Vth module	V
Vth_p	Vth module	V
Ioff_n	Ioff module	$\mu A/\mu m$
Ioff_p	Ioff module	$\mu A/\mu m$
Igate_n	Igate module	$\mu A/\mu m$
Igate_p	Igate module	$\mu A/\mu m$

Table 2: Variables required and used by the module

Code variable	Physical quantity	Meaning
Delay_nand_and	ns	input to output delay of selected module
Pnand_and_dyn	W	Dynamic power of selected module
Pnand_and	W	Static power of selected module

Table 3: Variables provided in output of selected module

6.1 Text Results

An example of the output provided by the TAMTAMS analysis using the *Print text results* is provided below. The computed values of delay, dynamic and static power are reported for four possible value of *Fan Out* where this quantity just means the number of inverter considered as output load for the gate.

```
Technology: bulk/HP_2005

System Setup: 2016-04-17 13:37:08
Cox =  2.8776e-06
Vtlong =  0.61691
SCE =  0.18990
DIBL =  0.24118
mueff_n =  252.01
mueff_p =  61.319
Ecrit_n =  7.9360e+04
Ecrit_p =  3.2616e+05
Vdsat_n =  0.15325
Vdsat_p =  0.41401
Cdep =  5.0656e-07
m =  1.2831

Module 0 : Delay_Pow_nand2_cmos

Fan Out = 1:
I/ODelay[ns]  DynPower[W]  StaticPower[W]
 6.1742e+00   1.5764e-06   3.8419e-09

Fan Out = 2:
I/ODelay[ns]  DynPower[W]  StaticPower[W]
 9.6946e+00   1.8727e-06   3.8419e-09

Fan Out = 3:
I/ODelay[ns]  DynPower[W]  StaticPower[W]
 1.3215e+01   2.1691e-06   3.8419e-09

Fan Out = 4:
I/ODelay[ns]  DynPower[W]  StaticPower[W]
 1.6735e+01   2.4654e-06   3.8419e-09
```

6.2 Graphical Results

Using the *Show graphical results* three different graph are provided as output. The first one represents the delay; an example is reported in fig. 6. There are four different lines, one for each value of *Fan Out*.
The figure 7 shows the second graph provided and it represent the dynamic power.
The last graph shows the static power (fig. 8). This value does not depends on output load so all the lines are overlapped.

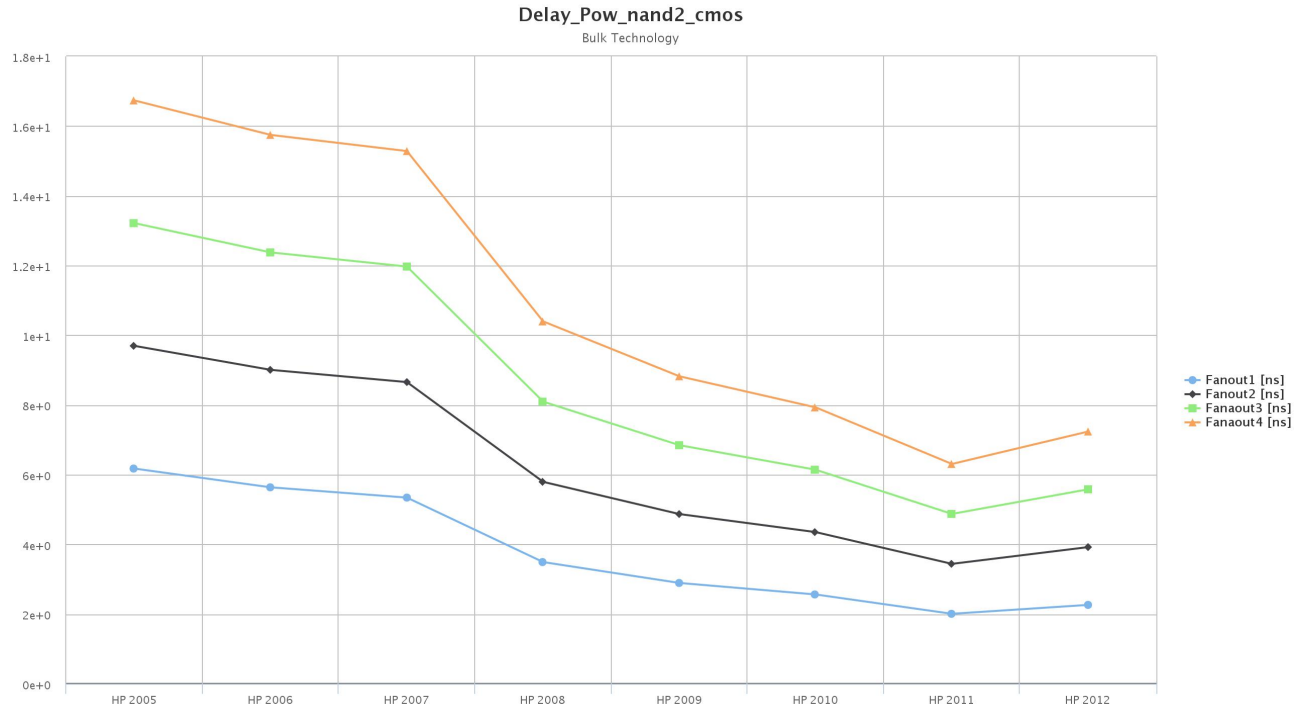

Figure 6: Delay graphical output

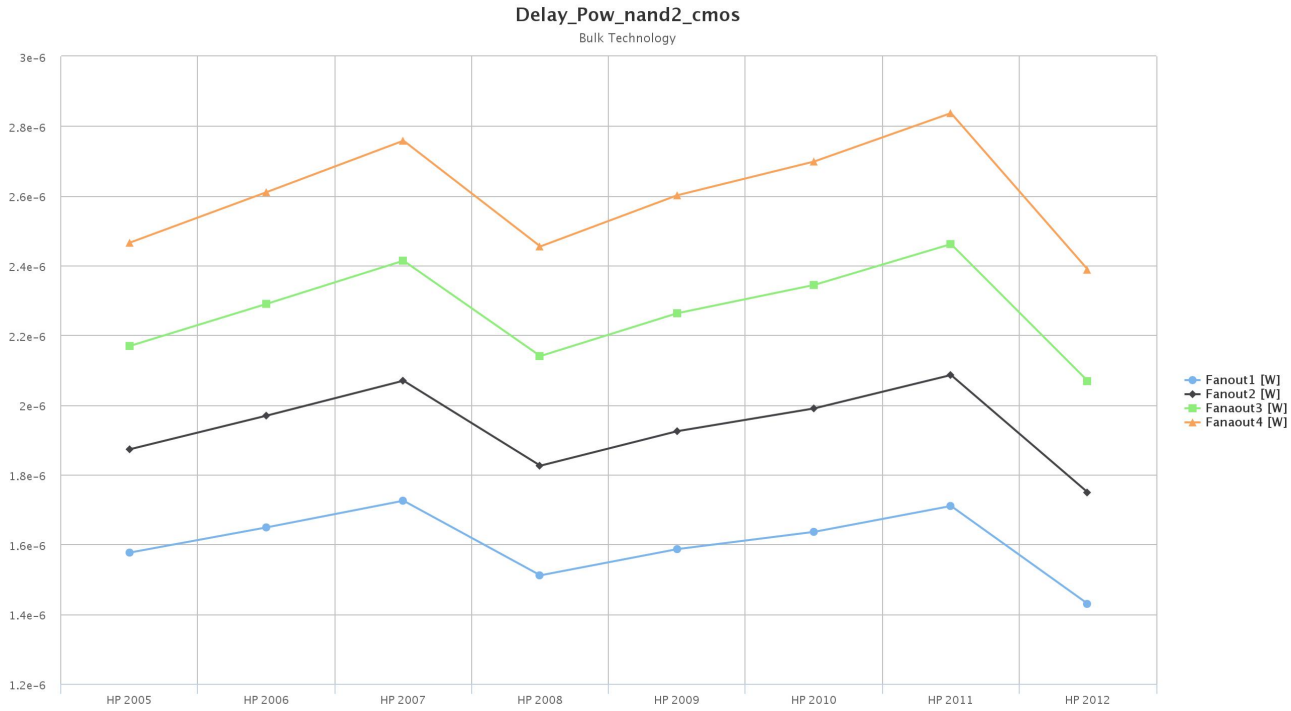

Figure 7: Dynamic power graphical output

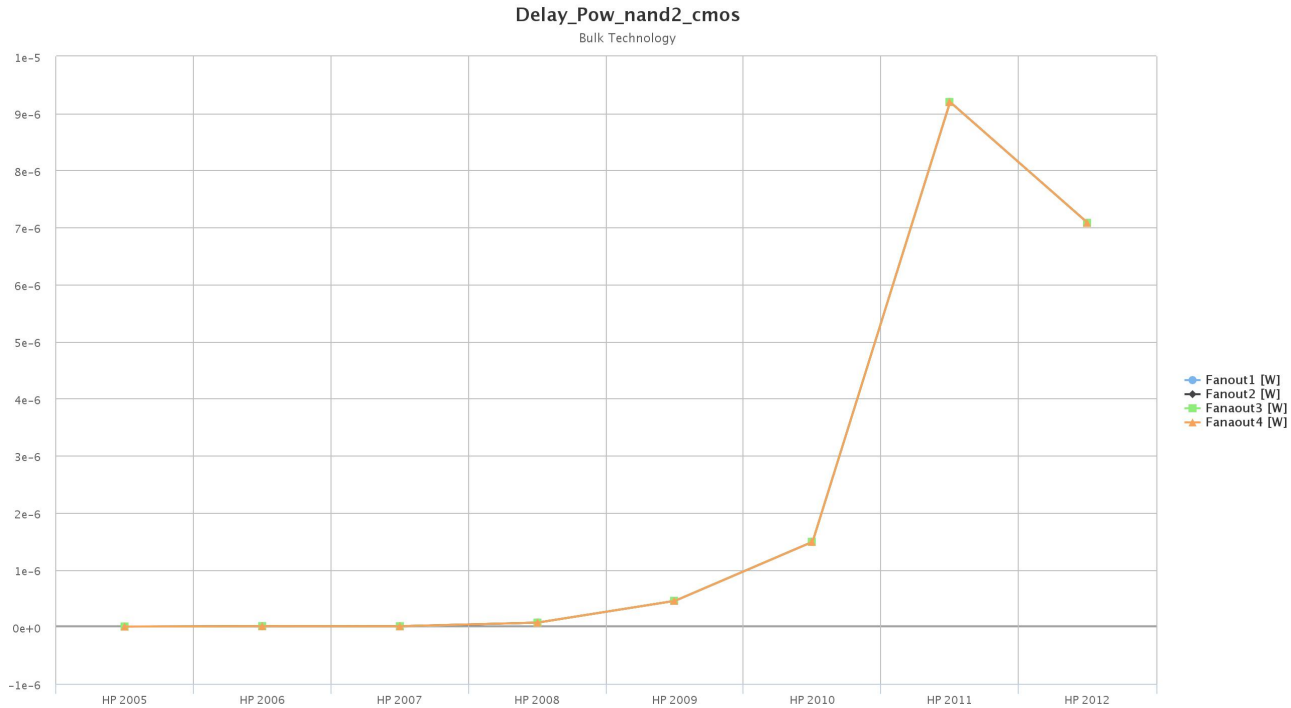

Figure 8: Static power graphical output