High speed Low power Multiple Bit Subtractor Circuit Design Using High performance domino Logic

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***Abstract*—The domino logic style is very attractive for designing high performance digital logic circuits in Very Large Scale Integrated microprocessor chips. In this paper a four bit subtractor circuit is designed using different domino logic styles and its performance is compared with one another. The simulations were performed using L=0.12µm technology along with a supply voltage V_{DD} =1.2V. The simulation results show that the delay of the subtractor circuit is very low compared to the conventional four bit subtractors. The delay is in the order of Pico seconds. These new multiple bit subtractors show improved noise immunity low leakage and low power consumption without much speed penalty. In this paper the performance of multiple bit subtractors designed using high speed domino technique, conditional keeper technique and leakage current mirror technique is analyzed in detail. Also the layout level simulations were performed to study the performance of multiple bit subtractor circuits.**

***Key words*—Domino logic, high-speed domino circuit, leakage power, noise tolerance, transistor sizing.**

I. INTRODUCTION

DOMINO logic gates and circuits have been excellent choice in the design of high-performance modules in modern VLSI microprocessors[1]-[4].The only limitation of domino circuits is their relatively low noise margin compared to that of standard CMOS gates. That is dynamic logic families are more sensitive to noise than static logic families. This limitation can be overcome by employing a P-type MOSFET called keeper transistor in the pull up network that compensates for leakage current of the pull-down NMOS network. Employing the keeper transistor at the pull up network improves reliability of the domino logic circuits but it degrades the performance of the logic circuit in terms of speed. As the technology scales down, the supply voltage V_{DD} is reduced for low power, and the threshold voltage (V_{th}) is also scaled down to achieve high performance [2][5]. But reducing the threshold voltage exponentially increases the subthreshold leakage current and increasing leakage currents seriously limits the robustness of wide fan in dynamic gates [6][7]. Therefore reduction of this subthreshold leakage current and improving noise immunity are the major concern in robust and high-performance designs in modern microprocessor chips especially for wide fan-in dynamic gates.

One method to minimize the leakage current in dynamic logic gates is proper gate sizing [8][9]. In this paper a four bit subtractor is implanted using three types of dynamic domino techniques. In the first method a 4-bit subtractor is implemented using leakage current mirror (LCR) technique. In this technique a leakage current replica (LCR) keeper is used. This LCR keeper uses an analog current mirror to replicate the leakage current of a dynamic gate pull-down network and thus tracks process, voltage, and temperature[10]-[12]. In the second method, the 4-bit full subtractor is implemented using two conditional keepers for improving the robustness and noise tolerance [13]. In this case, a weak keeper maintains the state of the dynamic node during the transition window - when NMOS logic pulls down and a strong keeper is conditionally activated based on the state of the dynamic node after a certain delay. This reduces contention during the evaluation period, thereby enabling high speed and minimizing the short circuit power dissipation. The third type of 4-bit subtractor is implemented using high speed domino technique. All these three types of subtractors are implemented in 120nm technology with a supply voltage of 1.2V.

The delay of the dynamic domino modules can be controlled by varying the sizes of transistors in the circuit. The circuit delay can be minimized by increasing the transistor sizes in the circuit. This implies that high speed circuits require larger area. So for dynamic domino circuits, there is a trade off exist between speed and area. Domino logic circuits are the most widely used dynamic logic style. Domino logic circuits have two phases of operations. The first phase is called precharge phase and second phase called evaluation phase. During the precharge phase of the domino logic circuits, the clock goes low and the dynamic node is precharged to V_{DD} through a p-type pull up transistor. The evaluation phase starts when the clock goes high. During the evaluation period, the pull down network evaluates the logic function and the dynamic node will either be charged to V_{DD} or it will be pulled low based on the state of inputs.

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In this paper the performance of 4-bit ripple carry subtractor is analysed in detail with the help of layout level simulation results. The transistor level circuits are implemented first and then went for module level analysis. The paper is organized as follows. Section II details the circuit implementation and operation of the 4-bit subtractor using three different domino techniques. Section III compares the performance of these full subtractor circuits using the simulated results. Section IV concludes the paper.

II.CIRCUIT DESIGN

The circuit diagram of a full subtractor circuit implemented using high speed domino (HSD) technique is shown in fig.1 and its layout is shown in fig.2. In this design the clock signal is connected to the gate of the keeper transistor through two inverters. The purpose of the inverters is to introduce some delay. The keeper is connected to the output node through a NMOS transistor. This will reduce the delay by minimizing the parasitic capacitance of the pull down network. The block diagram of the 4- bit subtractor circuit implemented using the HSD technique is shown in fig.3. The timing diagram of the 4-bit subtractor using HSD technique is shown in Fig.4 and its layout is shown in fig.5.

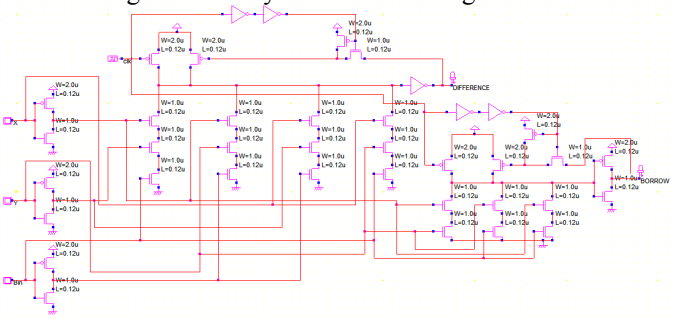

Fig.1. Full Subtractor circuit using High Speed domino logic

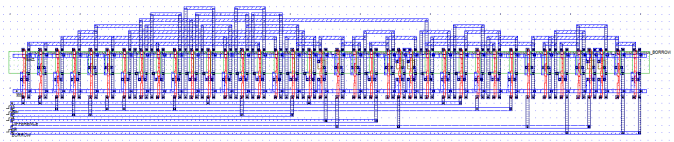

Fig.2. Layout of the Full Subtractor circuit using High Speed domino logic

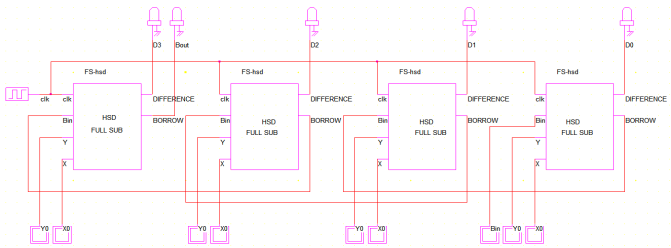

Fig.3 Block diagram of 4-bit subtractor using high speed domino logic

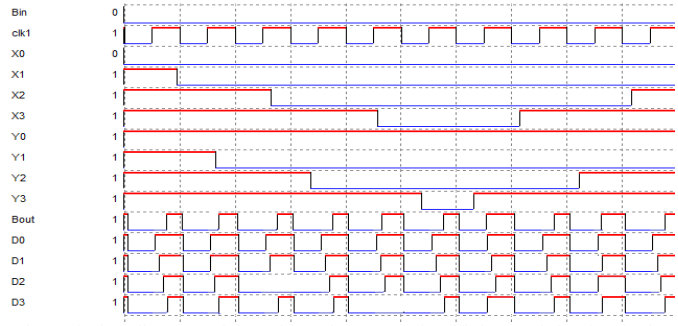

Fig.4 Timing diagram of the 4-bit Subtractor using high speed domino logic

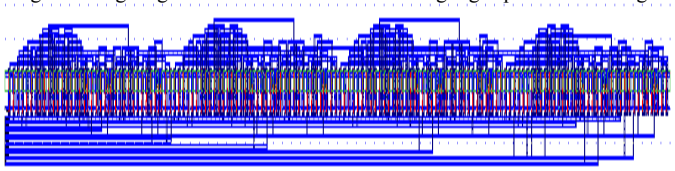

Fig.5 Layout of the 4-bit subtractor using high speed domino logic

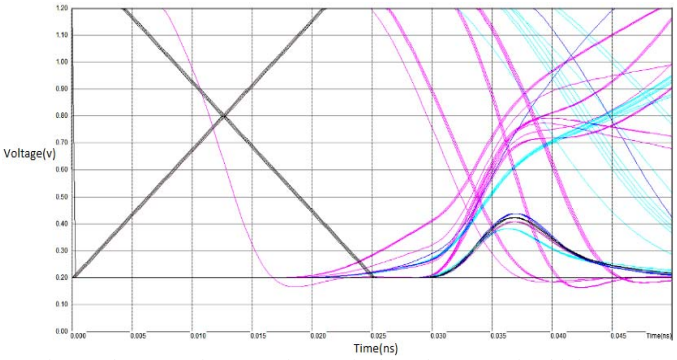

Fig.6 Voltage Vs Time waveforms of 4-bit subtractor using high speed domino

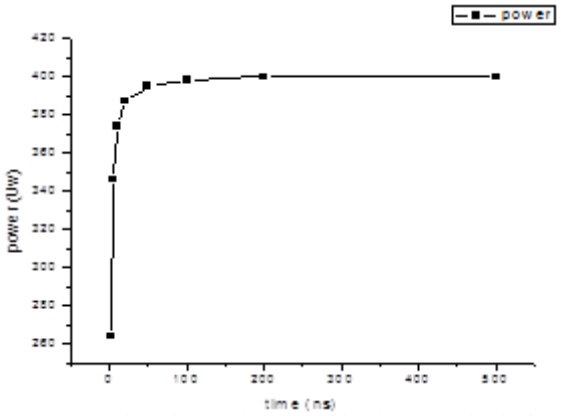

Fig.7 Power Vs Time characteristics of 4-bit subtractor using high speed domino

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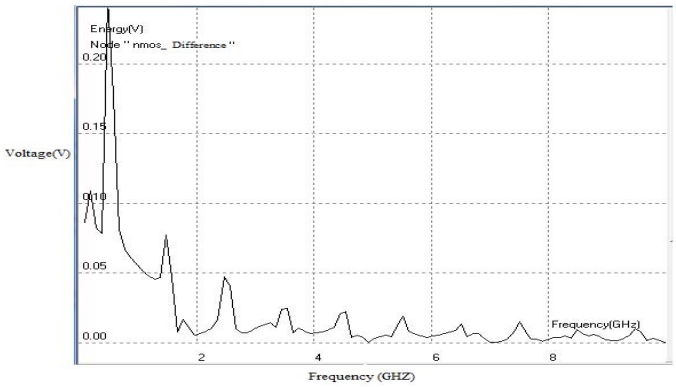

Fig.8 Output voltage Vs Frequency characteristics of 4-bit subtractor using HSD

The output voltage Vs Time characteristic of the 4-bit subtractor is shown in fig.6. This diagram shows the precharing and evaluation of the circuit. The delay of this circuit is in the order of pico seconds. The power–time characteristic of the 4-bit subtractor is shown in figure-7. The power of the circuit depends on the frequency of the clock signal and also the switching activity of the input signals. This circuit need proper selection of clock signal. If the clock frequency exceeds 500MHz, the performance degrades which is shown in fig.8. The circuit is implemented using L=0.12µm technology with V_{DD} =1.2V. The simulation results shows that the circuit performance is superior in terms of speed and delay compared to the subtractor circuits implemented using standard static logic circuit techniques.

The full subtractor circuit implemented using leakage current replica technique is shown in fig.9 and its layout is shown in fig.10. In this full subtractor circuit a current mirror is connected to the keeper transistor which compensates for the subthreshold leakage current of the pull-down network. This current mirror circuit can be shared for all the logic gates in the circuit. In this configuration the keeper and current mirror circuit minimizes the delay of the circuit by minimizing the effect of charge sharing. The 4-bit full subtractor circuit implemented using leakage current replica technique is shown in fig.11 and its layout is shown in fig.12. Since the keeper transistor is strongly ON during the beginning of the evaluation phase, the contention is still high in this circuit. Also the replica transistor does not track the leakage current due to noise and DIBL in the pull down NMOS network. The area overhead of the replica and mirror PMOS transistors becomes very high which intern leads to excess static power dissipation in the replica circuit. The timing diagram of the 4-bit subtractor implemented using LCR technique is shown in fig.13.

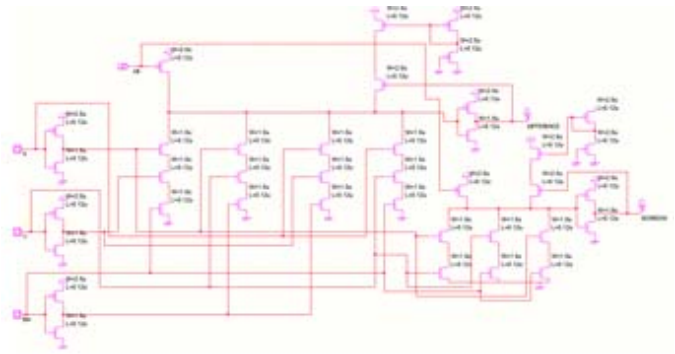

Fig.9. Full subtractor circuit using leakage current replica (LCR) domino

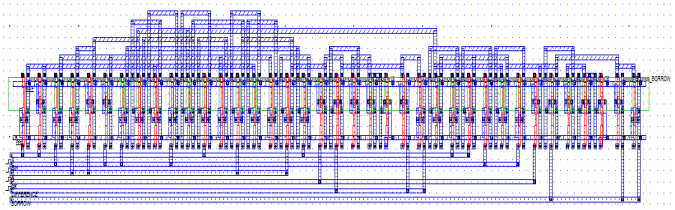

Fig10. Layout of the Full subtractor circuit using leakage current replica domino

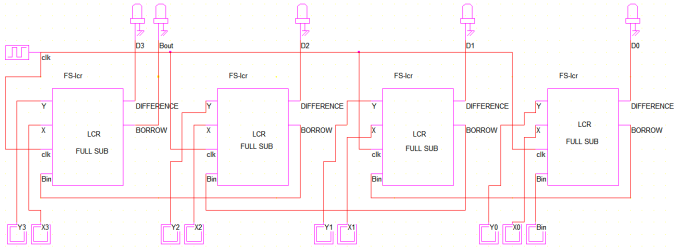

Fig.11. Block diagram of 4-bit subtractor using LCR domino

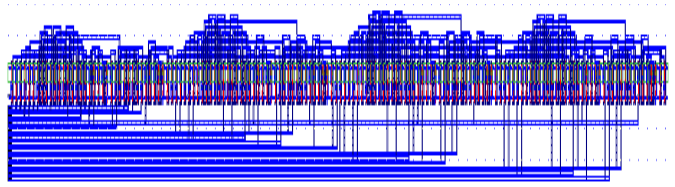

Fig.12. Layout diagram of 4-bit subtractor using LCR domino

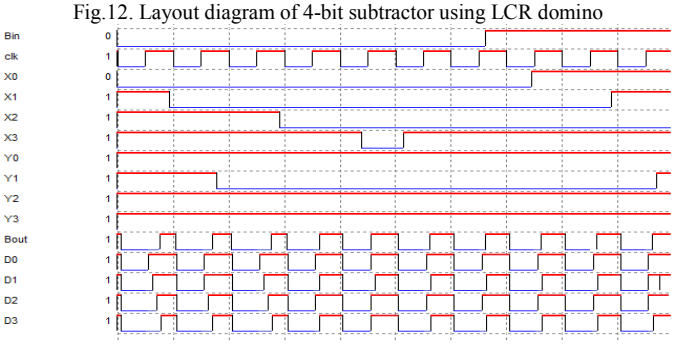

Fig.13.Timing diagram of the 4-bit subtractor using LCR domino

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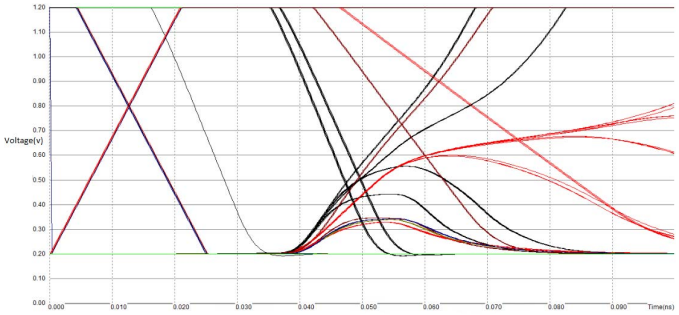

Fig.14. Voltage Vs Time waveforms of 4-bit subtractor using LCR domino

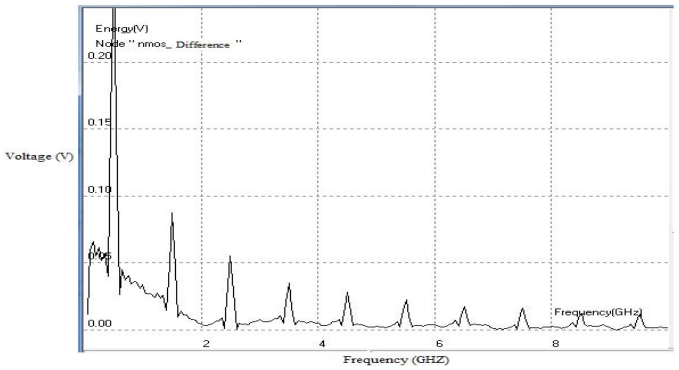

Fig.15.Output voltage Vs Frequency characteristics of 4-bit subtractor using LCR

Since a single current mirror structure can be shared among more than one domino logic circuits, this design technique is useful for constructing wide fan in circuits such as multiple bit subtractors, adders, registers, multiplexers etc. The output voltage Vs Time characteristic of the 4-bit subtractor implemented using LCR domino style is shown in fig.14. The frequency dependence of the 4-bit subtractor circuit designed using leakage current replica domino logic style is shown in fig.15. The clock frequency used in this design is 500MHz. As the clock frequency increases the output voltage decreases due to the parasitic capacitances. When clock goes low, the dynamic node will be precharged to V_{DD} (precharge phase) and the output remains low in this condition. When the clock signal changes the state from low to high the circuit evaluate the logic function (evaluation phase).

The full subtractor circuit implemented using conditional keeper technique is shown in fig.16 and its layout is shown in fig.17. Conditional keeper domino (CKD) circuits use two keepers to improve the performance of the domino circuits having wide fan in. The pull up network contain a weak keeper, which maintains the state of the dynamic node during the evaluation phase of the circuit and a strong keeper which is conditionally activated based on the state of the dynamic node after some delay. The clock signal can be delayed by employing two inverters in its path and the delayed clock signal is connected to the strong keeper through a NAND gate. These two keepers reduce the contention during the evaluation phase and thereby increasing the speed of the circuit and decrease the power dissipation. The block diagram of the 4-bit subtractor circuit designed using CKD technique is shown in fig.18 and its layout is shown in fig.19.The circuit is also simulated using L=0.12µm technology with V_{DD}=1.2V. When clock is low, the dynamic node will be precharged to V_{DD} and the output remains low in this condition. When the clock signal changes the state from low to high the circuit evaluate the logic function. The output voltage Vs Time characteristic of the 4-bit subtractor implemented using CKD domino style is shown in fig.20. The frequency dependence of the 4-bit subtractor circuit designed using conditional keeper domino logic style is shown in fig.21.

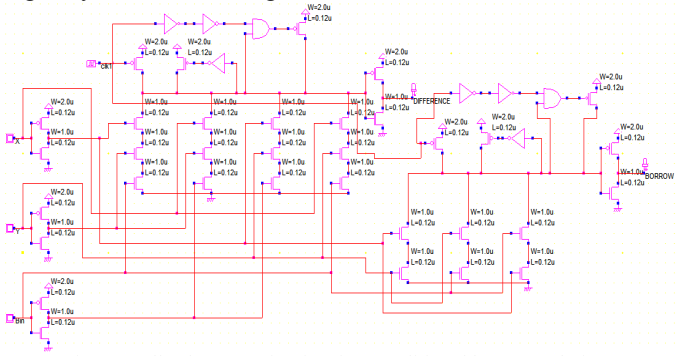

Fig.16. Full subtractor circuit using conditional keeper technique

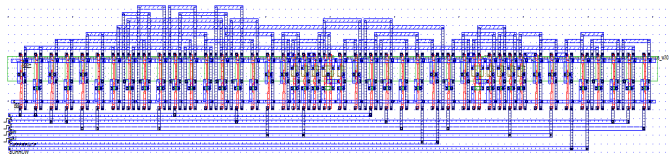

Fig.17. Layout of Full subtractor using conditional keeper technique

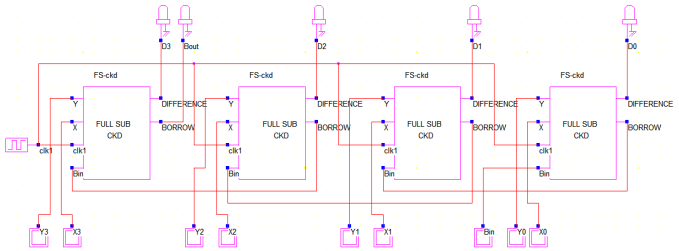

Fig.18. Block diagram of the 4-bit subtractor circuit using CKD logic style

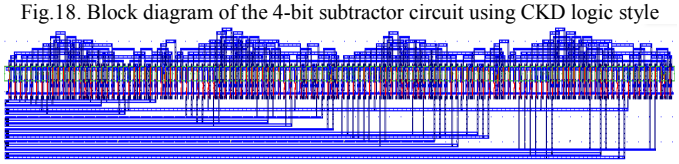

Fig.19. Layout diagram of the 4-bit subtractor circuit using CKD logic style

In this paper three types of multiple bit subtractors are presented with L=0.12µm technology and with a supply voltage of 1.2V. These high performance domino styles improve the scalability of multiple bit domino logic subtractors. Using these methods it is possible to implement the subtractor circuits with a transistor gate length of L=32nm along with a supply voltage of 0.8V. These subtractor circuits are superior in performance compared to conventional static logic subtractors. These subtractor circuits minimize the chip area, minimize the leakage power, and improve the noise tolerance without much speed degradation. Also the delay between the gates is now reduced to the order of pico seconds.

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These types of domino logic circuits can be used in high performance microprocessors.

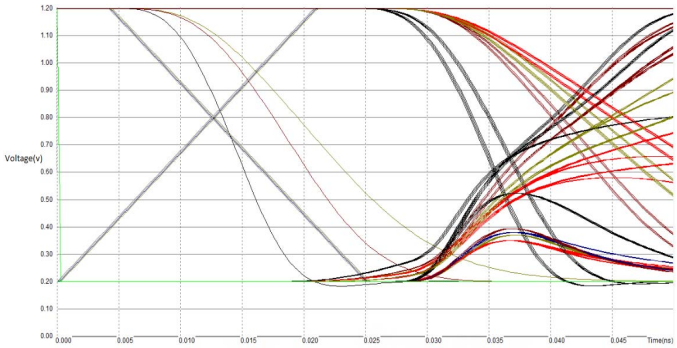

Fig.20. Voltage Vs Time waveforms of 4-bit subtractor using CKD domino

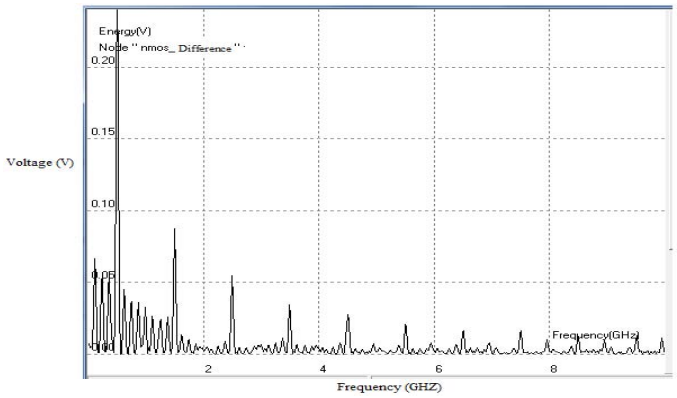

Fig.21.Output voltage Vs Frequency characteristics of 4-bit subtractor using CKD

III.SIMULATION RESULTS

The simulations were performed using L=0.12µm technology along with the supply voltage V_{DD}=1.2V. The timing diagram of the 4-bit subtractor circuit designed using HSD technique is shown in fig.4 and its output voltage Vs time characteristics is shown in fig.6, power–time characteristics is shown in fig.7 and frequency–output voltage characteristics is shown in fig.8. The simulation results for HSD subtractor shows that these subtractors show improved noise immunity and low power consumption, along with high speed. The voltage Vs time diagram clearly shows the precharging and evaluation phases of the circuit. At higher clock frequencies the parasitic capacitance is high which leads to charge sharing problem. That is at very high frequencies the output voltage during the evaluation period decreases due to parasitic effects. The timing diagram of the 4-bit subtractor circuit designed using LCR technique is shown in fig.13 and its output voltage Vs time characteristics is shown in fig.14 and frequency–output voltage characteristics is shown in fig.15. Since a single current mirror structure can be shared among more than one domino logic circuits, this design technique is useful for constructing wide fan in circuits such as multiple bit subtractors, adders, registers, multiplexers etc. This circuit has the area overhead of an extra NMOS transistor which is connected to the keeper from the current mirror circuit. This subtractor circuit has much better noise margin, low leakage current and low power consumption compared to the adder circuits designed using domino logic styles with traditional feedback keepers.

IV.CONCLUSION

As the technology scales down, the leakage current of the pull down evaluation network increases especially in wide fan in dynamic gates. This will increase the power consumption and reduce the noise immunity. In this paper the performance of 4-bit subtractor circuit designed using three domino circuit techniques (HSD, LCR, and CKD) is analysed in detail and its performance is compared with other subtractor circuits. The 4-bit subtractor circuit is simulated using L=0.12µm technology along with supply voltage V_{DD}=1.2V. The experimental results shows that these subtractor circuits gives superior performance compared to subtractor circuits designed using conventional domino techniques.

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