Politecnico di Torino

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NAND-2 inputs analysis
Integrated system technology

GROUP: 15

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1 Introduction

In this project we made an analysis and parameters estimation in terms of power and delay of a single logic gate, CMOS NAND-2 inputs. The analysis has been made for different fan-out to check the behaviors of parameters estimated.
The matlab files implemented for TAMTAM are:

- nand-2input_fanout_1;
- nand-2input_fanout_2;
- nand-2input_fanout_3;
- nand-2input_fanout_4;
- nand-2input_fanout_n;

2 Theoretical analysis

In this section we explain the technological parameters estimation and analysis for a single MOSFET and NAND-2 input.

2.1 Technological Parameters

We have estimated necessary technological parameters in order to evaluate:

- Static power
- Dynamic power
- Input-to-output delay
- Maximum frequency

The static power can be evaluated as shown below

$$P_{static} = V_{DD} \cdot I_{leak} \tag{1}$$

where I_{leak} is the leakage current and V_{DD} is the voltage supply.
The dynamic power can be computed as

$$P_{dynamic} = \alpha \cdot C_{gate} \cdot V_{DD}^2 \cdot f \tag{2}$$

where α is the switching activity, $\alpha \cdot C_{gate}$ is the switching capacitance and f is the frequency.
The oxide capacitance per unit length is the same for pMOS and nMOS transistors.

$$C_{OX} = \frac{10^9 \cdot (\epsilon_0 \cdot \epsilon_r)}{t_{OX}} \cdot L_{eff} \quad [pF/\mu m] \tag{3}$$

where L_{eff} is the effective gate length and t_{OX} is the thickness of the oxide.
The input capacitance of nMOS and pMOS transistors per unit length are:

$$C_{in_N} = C_{OX} + C_{overlapN} \quad [pF/\mu m] \tag{4}$$
$$C_{in_P} = C_{OX} + C_{overlapP} \quad [pF/\mu m] \tag{5}$$

where the two overlap capacitances are due to the overlap size between the gate and drain/source areas:

$$C_{overlapN} = 10^6 \cdot C_{GDOn} \quad [pF/\mu m] \tag{6}$$
$$C_{overlapP} = 10^6 \cdot C_{GDOp} \quad [pF/\mu m] \tag{7}$$

The junction capacitances between source and drain are:

$$C_{jN} = C_{bottomN} + C_{sidewallN} \quad [pF/\mu m] \tag{8}$$
$$C_{jP} = C_{bottomP} C_{sidewallP} \quad [pF/\mu m] \tag{9}$$

C_{bottom} is the capacitance due to the area of the pool of the source/drain and $C_{sidewall}$ is the one due to the edge of the same pool.

$$C_{bottomN} = C_{j0_N} \cdot \left(1 + \frac{V_{DD}}{2 \cdot P_{bN}}\right)^{-M_{jN}} \cdot 2.5 \cdot L_{drawn} \quad [pF/\mu m] \tag{10}$$

$$C_{bottomP} = C_{j0_P} \cdot \left(1 + \frac{V_{DD}}{2 \cdot P_{bP}}\right)^{-M_{jP}} \cdot 2.5 \cdot L_{drawn} \quad [pF/\mu m] \tag{11}$$

$$C_{sidewallN} = 10^6 \cdot C_{sw_N} \cdot \left(1 + \frac{V_{DD}}{2 \cdot P_{bswN}}\right)^{-M_{jswN}} \quad [pF/\mu m] \tag{12}$$

$$C_{sidewallP} = 10^6 \cdot C_{sw_P} \cdot \left(1 + \frac{V_{DD}}{2 \cdot P_{bswP}}\right)^{-M_{jswP}} \quad [pF/\mu m] \tag{13}$$

Moreover for the estimation of parasitic capacitances C_{jN} and C_{jP}, it is necessary to evaluate the perimeter.

$$\text{perim}_N = 2 \cdot \text{lungh\_diff} + W_N [\mu m] \tag{14}$$
$$\text{perim}_P = 2 \cdot \text{lungh\_diff} + W_P [\mu m] \tag{15}$$

We consider only one side for the W, because the internal one doesn't touch a conductor, but just a spatial charge.
Therefore C_{jN} and C_{jP} are:

$$C_{jN} = C_{bottomN} \cdot W_N + C_{sidewallN} \cdot \text{perim}_N \quad [pF] \tag{16}$$
$$C_{jP} = C_{bottomP} \cdot W_P + C_{sidewallP} \cdot \text{perim}_P \quad [pF] \tag{17}$$

For the leakage current we consider two factors

- **Subthreshold current**: is the leakage current that flows drain/source when $V_{gate_{nMOS}} = 0$ and $V_{gate_{pMOS}} = V_{DD}$ as shown in figure 1.
- **Gate Current**: is the leakage current that flows from drain and source to gate or viceversa when drain and source are tied at the same potential and gate is tied at the opposite potential for nMOS and pMOS as shown in figure 2.

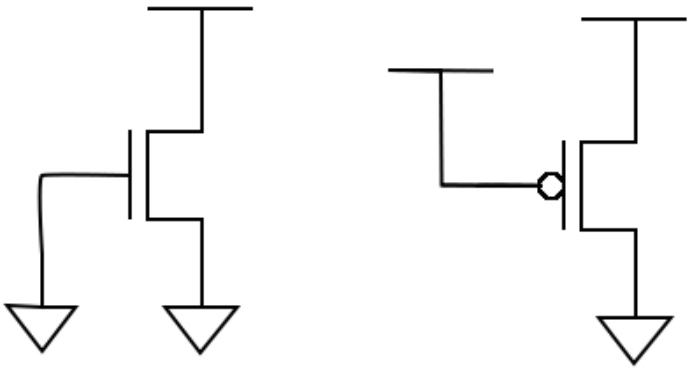

Figure 1: Leakage drain/source current when MOS are off

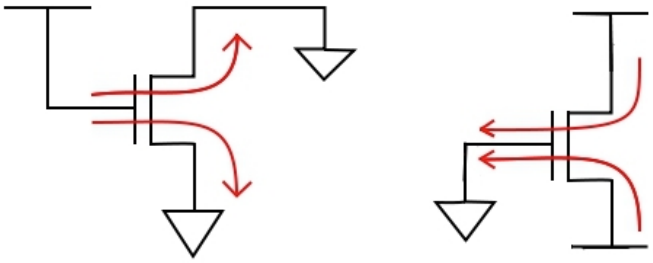

Figure 2: Leakage gate current

2.2 Dynamic Analysis

For the 2-input NAND in CMOS technology, the architecture is shown in figure 3. In order to compute

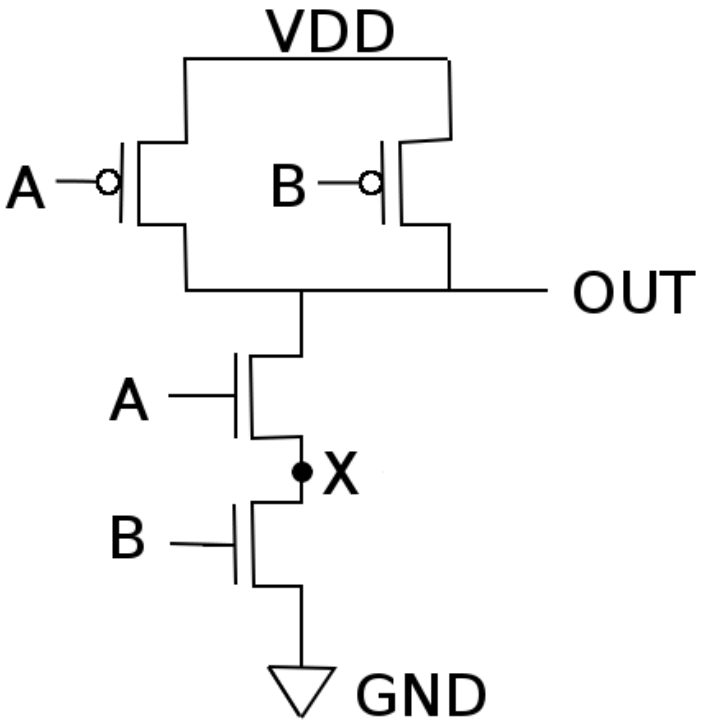

Figure 3: CMOS 2-input NAND architecture

the dynamic power, we have to calculate the total switching capacitance.
We have to consider three different capacitance:

- C_{IN} is the input capacitance associate at only one input

$$C_{IN} = C_{OX} \cdot 2W_N \cdot L_{eff} + C_{OX} \cdot W_P \cdot L_{eff} + 2C_{overlapN} + 2C_{overlapP} \quad [pF] \tag{18}$$

- C_{OUT} is the output capacitance

$$C_{OUT} = C_{jN} + 2C_{jP} \quad [pF] \tag{19}$$

  C_{jP} is multiplied by 2 because we have different pools for the two drains.

- C_{INT} is the internal capacitance between the two nMOS transistors in the pull-down network

$$C_{INT} = C_{jN} \quad [pF] \tag{20}$$

  We have only one C_{jN} because we consider that source and drain are common for the two nMOS.

To calculate the dynamic power is necessary to compute the switching activity for each node, using the probability that each node is equal to one.

$$P_{X1} = \frac{P_A \cdot (1 - P_B)}{1 - (1 - P_A) \cdot (1 - P_B)} \tag{21}$$

P_{X1} is the probability that the internal node in equal to one. The probability P_{OUT} at the output node is

$$P_{OUT} = 1 - (1 - P_A) \cdot (1 - P_B) \tag{22}$$

The switching activities are computed from probabilities as follow

$$\alpha_A = P_A \cdot (1 - P_A) \tag{23}$$
$$\alpha_B = P_B \cdot (1 - P_B) \tag{24}$$
$$\alpha_X 1 = P_{X1} \cdot (1 - P_{X1}) \tag{25}$$
$$\alpha_{OUT} = P_A \cdot (1 - P_{OUT}) \tag{26}$$

where P_A and P_B are the probabilities of the two inputs.
Finally, the total switching capacitance is

$$C_{NAND-2} = C_{IN} \cdot (\alpha_A + \alpha_B) + C_{X1} \cdot \alpha_{X1} + C_{OUT} \cdot \alpha_{OUT} \quad [pF] \tag{27}$$

2.3 Static Analysis

In the table 1 we present the four contributes due to the four combination of inputs of leakage power for the architecture in figure 3. where I_{OFF} is the drain/source leakage current and I_{GATE} is the gate leakage

A	B	Y	I_{leak} contribute
0	0	1	$I_{OFFn} + 2 \cdot I_{GATEp}$
0	1	1	$2 \cdot I_{OFFn} + 2 \cdot I_{GATEn} + I_{GATEp}$
1	0	1	$2 \cdot I_{OFFn} + I_{GATEp}$
1	1	0	$2 \cdot I_{OFFp} + 2 \cdot 2 \cdot I_{GATEn}$

Table 1: Leakage current contributes for each combination of inputs

current.
Finally, using P_A and P_B probabilities of inputs, I_{leak} results

$$\begin{aligned} I_{leak} = {} & (1 - P_A) \cdot (1 - P_B) \cdot (I_{OFFn} + 2 \cdot I_{GATEp}) + (1 - P_A) \cdot P_B \cdot (2 \cdot I_{OFFn} + 2 \cdot I_{GATEn} + I_{GATEp}) \\ & + P_A \cdot (1 - P_B) \cdot (2 \cdot I_{OFFn} + I_{GATEp}) + P_A \cdot P_B \cdot (2 \cdot I_{OFFp} + 2 \cdot 2 \cdot I_{GATEn}) \end{aligned} \tag{28}$$

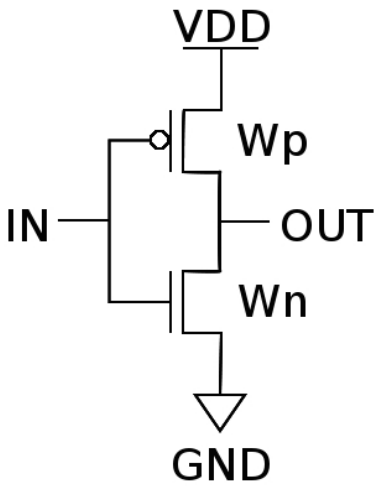

Figure 4: Architecture of CMOS inverter

2.4 Delay Analysis

The 2-input NAND gate, is projected starting from inverter gate that is made to have the same rise and fall time obtained dimensioning $W_P = 1.29 \cdot W_N$ to compensate different mobility between electrons and holes. Now, from inverter in figure 4, imposing $I_{INV} = I_{NAND2}$ we obtain

$$C_{INV}\frac{V_{DD}}{t_{INV}} = C_{NAND2}\frac{V_{DD}}{t_{NAND2}} \tag{29}$$

simplifying V_{DD} we obtain

$$\frac{C_{INV}}{t_{INV}} = \frac{C_{NAND2}}{t_{NAND2}} \tag{30}$$

$$t_{NAND2} = t_{INV}\frac{C_{NAND2}}{C_{INV}} \tag{31}$$

where t_{INV} is calculated in the same way as

$$t_{INV} = t_{MOS}\frac{C_{INV}}{C_{MOS}} \tag{32}$$

where t_{MOS} can be computed as τ

$$t_{MOS} = C_{MOS}\frac{V_{DD}}{I_{ONn} \cdot W_N} \tag{33}$$

The capacitances are:

$$C_{MOS} = C_{OX} \cdot L_{eff} \cdot W_N \tag{34}$$

$$C_{INV} = C_{jN} + C_{jP} + C_{f01} \tag{35}$$

$$C_{NAND2} = C_{OUT} + C_L \tag{36}$$

where C_{INV} is the sum of its intrinsic capacitance and an input capacitance of an inverter of the same type C_{f01}.
The NAND capacitance C_{NAND2} is composed by the sum of its intrinsic capacitance C_{OUT} and one or more gate of the same type C_L depending of chosen fan-out.

$$C_{f01} = C_{OX} \cdot L_{eff} \cdot W_N + C_{OX} \cdot L_{eff} \cdot W_P + C_{overlapN} + C_{overlapP} \tag{37}$$

$$C_L = C_{IN} \cdot \text{fan\_out} \tag{38}$$

From t_{NAND2}, maximum frequency can be computed as

$$f_{max} = \frac{1}{t_{NAND2}} \tag{39}$$

2.5 Elmore Delay

We have chosen to implement another delay model to have a comparison to the previous one. To do this we adopted the Elmore model which is an optimistic model. To evaluate the delay of 2-input NAND we started from [1] and [2], for 3-input NAND we have architecture shown in figure 5. A 3-input NAND

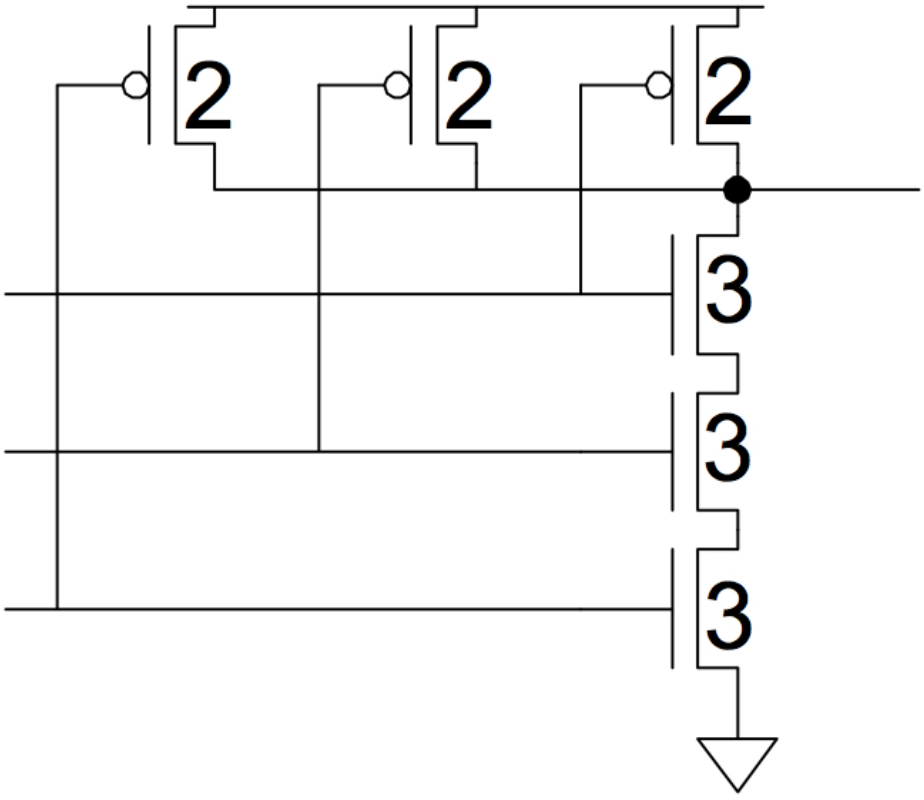

Figure 5: Architecture for 3-input NAND gate

gate with transistor widths chosen to achieve effective rise and fall resistance equal to that of a unit inverter (R). In this case pMOS has a width of $2 \cdot W_N$ (in the worst case, current flows only in one pMOS) to compensate the difference between mobility of electrons and holes, while for nMOS, width is $3 \cdot W_N$ because are in series.
Now we have to compute the capacitance at each node (neglecting capacitances effect due to layout) shown in figure 6. As we can see, at each input nodes, capacitances is $5C$ because the aspect ratio is 2 for pMOS

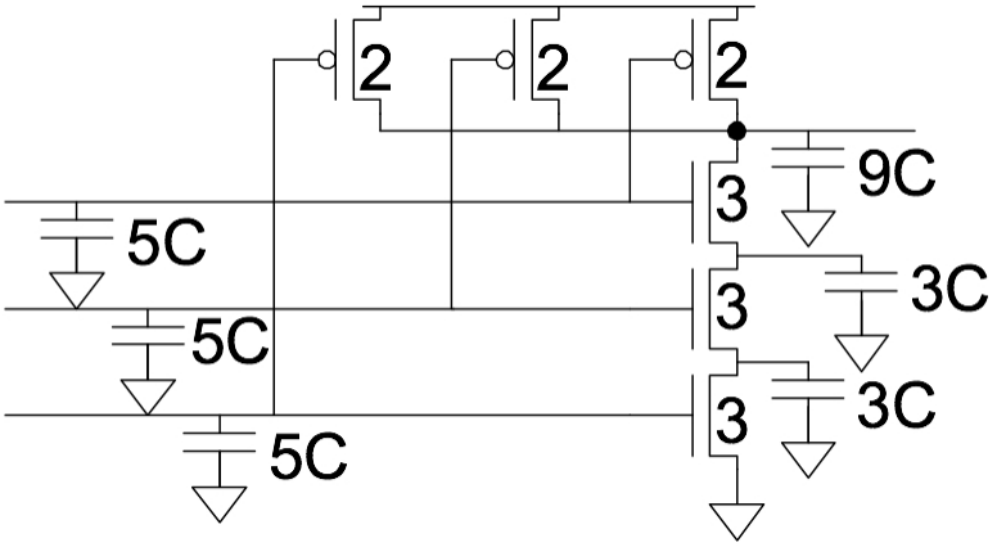

Figure 6: Capacitances for 3-input NAND gate

and 3 for nMOS, while the output capacitance is $9C$ because the output node is loaded with 3 pMOS and 1 nMOS. Considering layout, the situations is different. In figure 7, the source of 2 pMOS are common, so capacitance at output node due to pull-up network is reduced to $4C$, finally the total capacitance is $7C$.

For 2-input NAND, we use layout in figure 8, so the resultant model of capacitances is that in figure 9 where h is the fan-out. Now, let's focus on our formulas to evaluate the delay. First of all it is necessary to estimate equivalent resistance of MOSFET as

$$R = \frac{1}{\mu_n \cdot C_{OX} \cdot \frac{W_N}{L_{eff}} \cdot (V_{DD} - V_{tn})} \tag{40}$$

capacitance C is C_{OUT} previously estimated. The rise propagation delay t_{pdr} is

$$t_{pdr} = \left(\left(2\frac{\mu_p}{\mu_n} + 2 \right) + 4 \right) \cdot R \cdot C \tag{41}$$

and the fall propagation delay t_{pdf} is

$$t_{pdf} = 2 \cdot C \cdot \frac{R}{2} + \left(\left(2\frac{\mu_p}{\mu_n} \right) + 2 + 4 \cdot h \right) \cdot C \cdot R \tag{42}$$

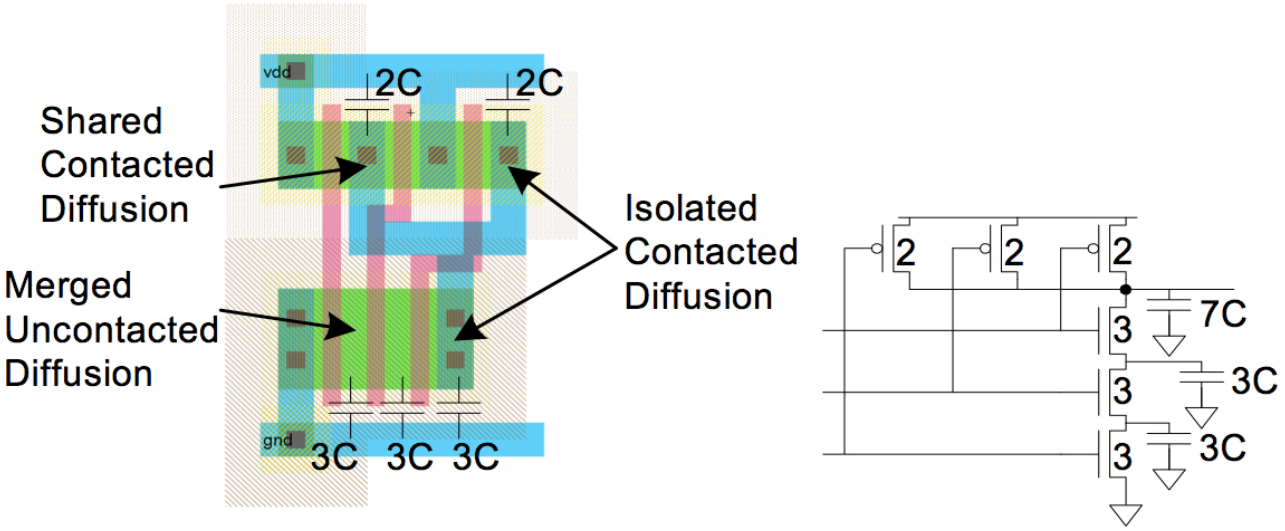

Figure 7: Layout example for 3-input NAND gate

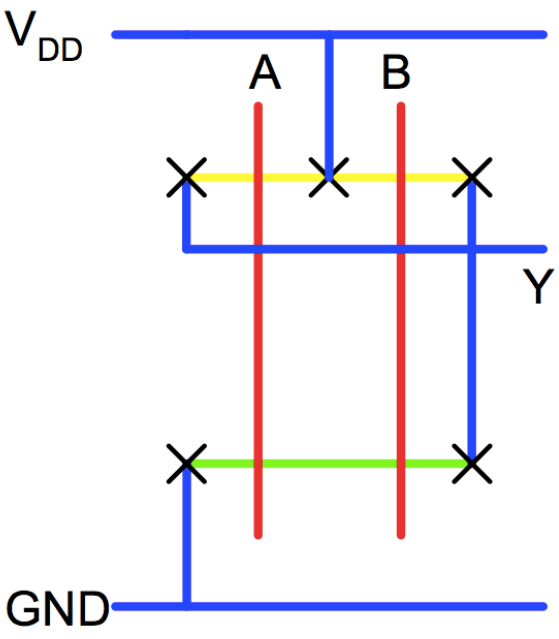

Figure 8: Layout for 2-input NAND gate

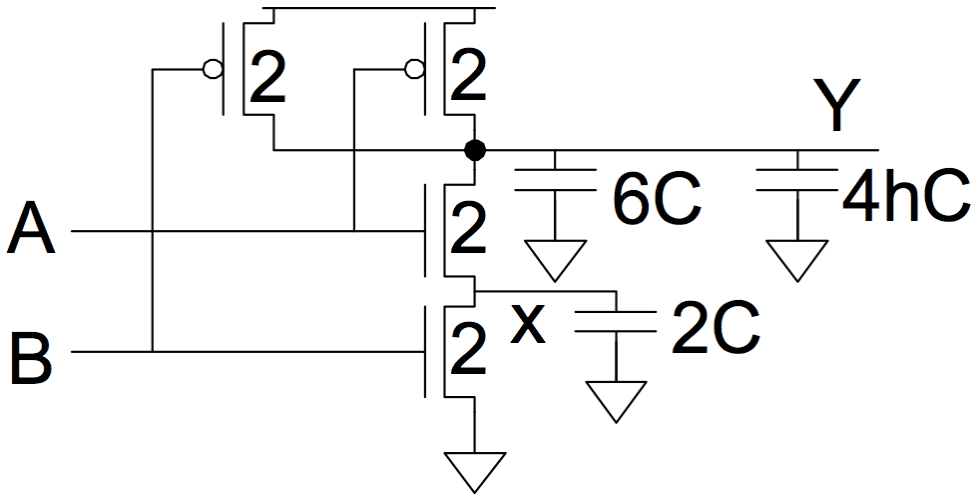

Figure 9: Capacitances for 2-input NAND gate

3 Octave implemetation

In table 2 there are the used variables in our model, and in table 3 there are the output parameters estimates.

- *CMOS_NAND2_fanout1.m*
- *CMOS_NAND2_fanout2.m*
- *CMOS_NAND2_fanout3.m*
- *CMOS_NAND2_fanout4.m*
- *CMOS_NAND2_generic_fanout.m*

Code variable	Source file	Physical quantity
Cox	Technology file	$pF/\mu m^2$
Lgate	Technology file	nm
Cj0n	Technology file	$pF/\mu m^2$
Vdd	Technology file	V
Cjswn	Technology file	F/m
Cj0p	Technology file	$pF/\mu m^2$
Cjswp	Technology file	F/m
Cgd0n	Technology file	F/m
Cgd0p	Technology file	F/m
Ion_n	Ion_mas.m	$\mu A/\mu m$
Ion_p	Ion_mas.m	$\mu A/\mu m$
Ioff_n	Ioff_mas.m	$\mu A/\mu m$
Ioff_p	Ioff_mas.m	$\mu A/\mu m$
Igate_n	Igate_mas.m	$\mu A/\mu m$
Igate_p	Igate_mas.m	$\mu A/\mu m$

Table 2: Variables used in NAND2 module

Code variable	Physical quantity	Meaning
P_static_nd2	W	Static power of 2-input NAND gate
P_dyn	W	Dynamic power of 2-input NAND gate
t_nd2	s	Propagation delay across 2-input NAND gate
f_max	Hz	Maximum frequency of 2-input NAND gate
tpd	s	Elmore model propagation delay across 2-input NAND gate

Table 3: Variables provided in output in NAND2 module

4 Results

To test our module that computes power and delay, we run some simulation changing V_{DD} and fan-out according the three different technology families in the same year. In figure 10 is plotted the behavior of delay in function of fan-out. As we expected, increasing the fan-out, the delay increases too and find out

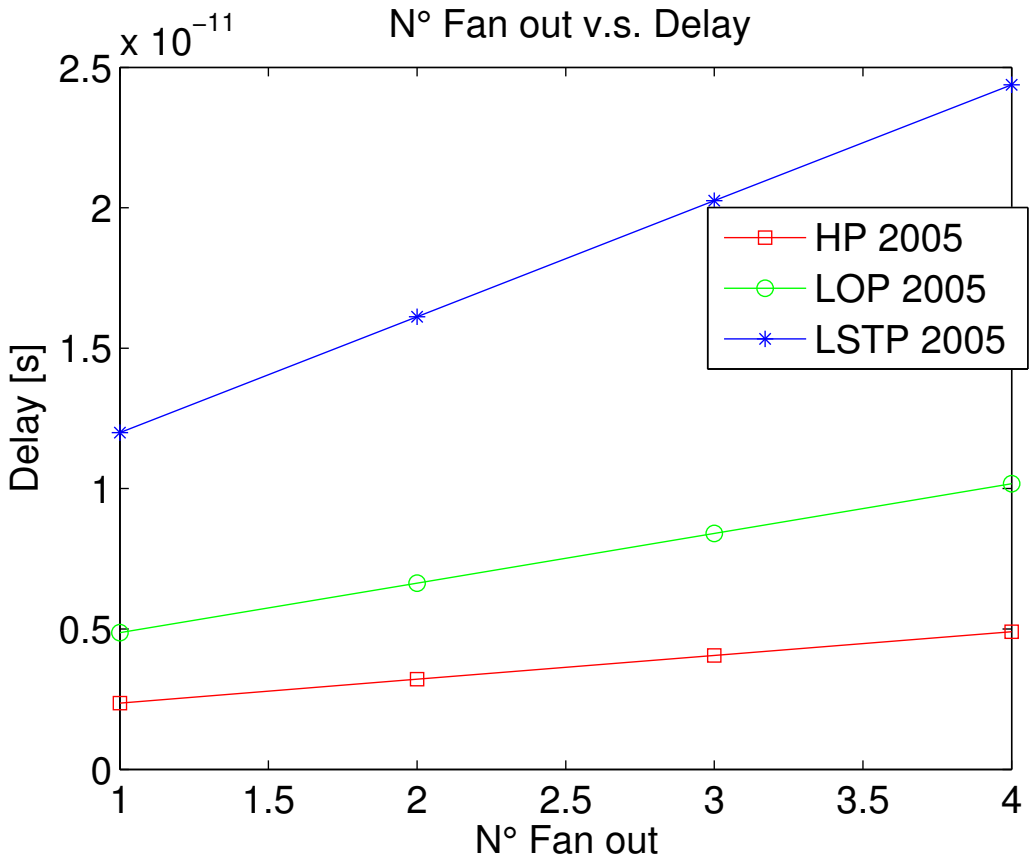

Figure 10: Fan-out vs delay

also that HP technology has lower delay respect to LOP and LSTP, moreover its slope is less than other two.
In figure 11 is shown the delay variations for different V_{DD} values according the three technology families. As we expected, delay increases as V_{dd} decreases. As before, the slope of HP is lower than the other two but less compared to fan-out plot.
About power, in table 4 are reported static and dynamic power for the three families at 2005.

NOTE: Variable Cox received in input at our module should be in $pF/\mu m^2$, but we have verified that must be multiplied by 10 to have a correct Cox.

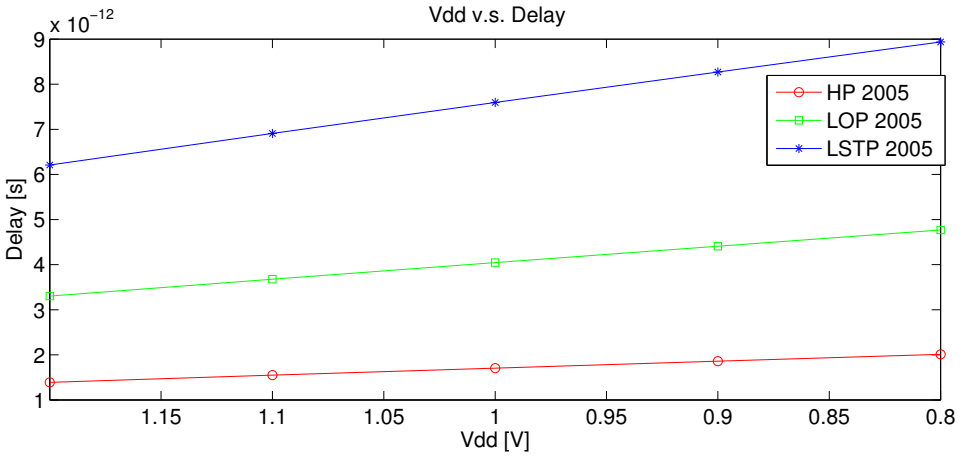

Figure 11: V_{DD} vs delay

	HP [W]	LOP [W]	LSTP [W]
P static	$3.7411 \cdot 10^{-4}$	$2.3884 \cdot 10^{-6}$	$1.6137 \cdot 10^{-8}$
P dynamic	$2.518 \cdot 10^{-6}$	$1.3937 \cdot 10^{-6}$	$2.4310 \cdot 10^{-6}$

Table 4: Static and dynamic power for 2005 technological node

References

[1] N.H.E. Weste and D. Harris, *"CMOS VLSI design, A circuits and systems perspective"*

[2] Rabaey, Chandrakasan and Nikolic, *"Digital integrated circuits, a design perspective"*