A High-Performance Circuit Technique For CMOS Dynamic Logic

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Abstract ----Dynamic logic style is used in high performance circuit design because of its fast speed and less transistors requirement as compared to CMOS logic style. But it is not widely accepted for all types of circuit implementations due to its less noise tolerance and charge sharing problems. A small noise at the input of the dynamic logic can change the desired output. Domino logic uses one static CMOS inverter at the output of dynamic node which is more noise immune and has less capacitance at the output node. In this paper we have proposed a novel circuit for domino logic which is more noise robust and has very less power-delay product (PDP) as compared to previous reported articles. Low PDP is achieved by reducing the short circuit current during evaluation phase when PDN is conducting and also the leakage current when PDN is not conducting.

Keywords: Dynamic logic, domino logic, Delay, diode-footed domino, noise tolerance, power consumption, robustness, technology scaling, semi-dynamic logic

I. INTRODUCTION

The rapid advancement in VLSI circuit is due to increased use of portable and wireless systems with low power budgets and microprocessors with higher speed. To achieve this, the size of transistors and supply voltages are scaled down along with technology. Due to larger number of devices per chip the interconnection density increases. The interconnection density along with high clock frequency increases capacitive coupling of the circuit. Therefore, noise pulses known as cross-talk are generated leading to logic failure and delay of the circuit [1]. Again, when supply voltage is scaled, threshold voltage of the device needs to be scaled to preserve the circuit performance, which in turn leads to increase in the leakage current of the device.

Due to high speed and low device count especially compared to complementary CMOS, dynamic-logic circuits are used in a wide variety of applications including microprocessors, digital signal processors and dynamic memory[2]. Dynamic circuit contains a pull-down network (PDN) which realizes the desired logic function. According to the basic theory, the dynamic logic circuit will precharge at every clock cycle. Due to the high frequency of the clock signal a lot of extra noise is introduced in the circuit that consumes additional power and slows down the circuit.

In this paper we propose a new circuit technique which can reduce the noise of dynamic logic dramatically. This circuit increases speed and decreases the power dissipation of the circuit as compared to other domino logic styles.

II. PROBLEM STATEMENT

Fig. 1 is an example of footless domino gate. During the precharge phase when the clock is LOW, the pre-charging PMOS switches ON and the dynamic node is connected to the V_{DD} and gets precharged to V_{DD}. When clock goes high, the evaluation phase starts and the output gets evaluated with the pull-down network and conditionally gets discharged if any one of the input is at logic 1. At the evaluation period, when all the inputs are at logic 0, the dynamic node should remain at logic 1. The wide fan-in NMOS pull-down leaks the charge stored in the capacitance at the dynamic node because of subthreshold leakage. This is again compensated by the PMOS keeper, which aims to restore the voltage of the dynamic node. When a noise voltage impulse occurs at any gate input, the keeper may not be able to restore the voltage level of the dynamic node. The subthreshold leakage current is exponentially dependent on V_{GS}. In presence of noise impulse, the gate voltage increases which increases V_{GS} and the dynamic node gets wrongly discharged.

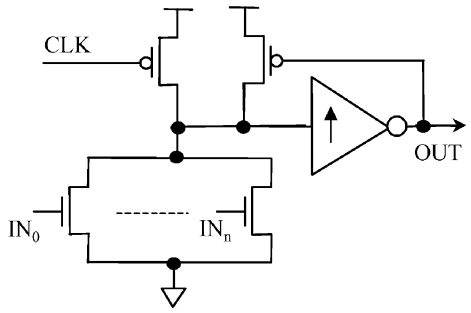

Fig. 1. A typical footless Domino OR gate

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As noise is more important issue than area, energy dissipation and delay in a domino gate, so recently several techniques have been proposed to reduce the noise of dynamic circuits. All the techniques have reduced noise sensitivity but there are many drawbacks with area, power dissipation and delay.

III. BACKGROUND AND RELATED WORK

Diode-Footed domino[3] contains an NMOS transistor in a diode configuration i.e. gate and drain terminals connected together in series with the evaluation network, as shown in Fig. 2. A diode footed transistor is exploited in this design in which the leakage current flowing through the PDN in the evaluation phase causes voltage drop across the diode footed transistor. This makes V_{GS} negative and hence leakage reduces. The performance degradation can be compromised by the mirror network. By varying the size of mirror, noise immunity can be achieved. When we compare it with standard footless domino, this scheme is very slow. Furthermore, the inverse clock increases the capacitive load of the clock driver.

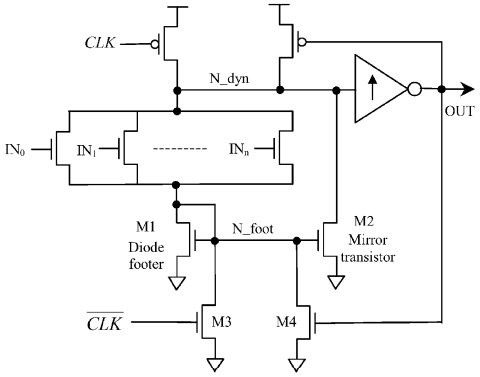

Fig. 2. Diode footed Domino [3]

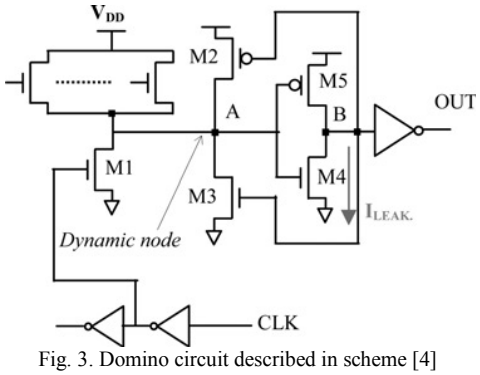

Fig. 3. Domino circuit described in scheme [4]

In [4], the circuit based on a pull up network constitutes only the NMOS transistors as depicted in Fig. 3. This style doesn't have precharge PMOS transistors. When the clock is low i.e. at the precharge stage, M1 is switched on and the dynamic node is precharged to 0 V. When clock is high i.e. at evaluation phase, M1 is OFF and the pull up network can conditionally charge the dynamic node. When one or more input signals are there, the dynamic node has to charge up to V_{DD}, but due to the absence of pull up network it only charges to V_{DD}-V_{TH}. This drop is compensated by the PMOS M2.The noise is decreased by NMOS pull up network, the leakage through pull up network charges dynamic node. But again it needs an inverting clock which increases the capacitive load. Also it uses extra inverter like structure which increases the area and complexity of the circuit.

IV. NOVEL APPROACH

This proposed circuit is designed for low power consumption and faster operation which reduces the delay of circuit exponentially. The exponential reduction of the delay reduces the power-delay-product (PDP) of the circuit thousand times. It takes the advantage of the semi dynamic logic, in which the source of the NMOS buffer transistor is connected to the drain of NMOS clock transistor instead of ground; it operates in semi dynamic state. Also the Diode footer decreases the leakage and certain drawbacks of the circuit are further compensated by the presence of the current mirror circuit.

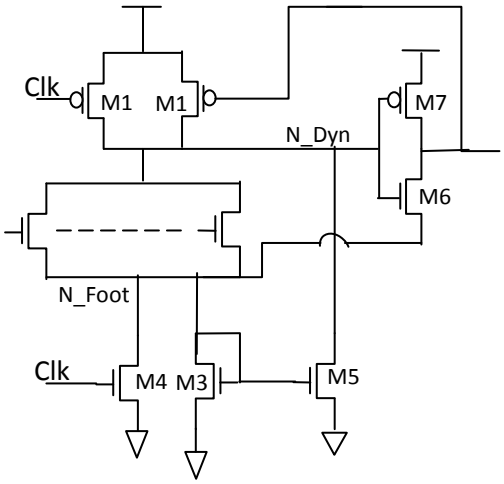

Fig. 4. Proposed scheme

A. Circuit analysis:-

The circuit has been added with a diode footed domino in series with the PDN, one current mirror circuit parallel to the diode foot and also the semi-dynamic buffer in which the buffer of the domino logic is not grounded and is connected to the PDN foot. To make the diode footer, the drain and gate terminal of the three transistors are shorted. Due to stacking effect of the diode footer, the subthreshold leakage also decreases [3]. There is a voltage drop across the diode footer in evaluation phase. Due to this voltage drop V_{GS} becomes negative. This causes exponential reduction in threshold voltage.

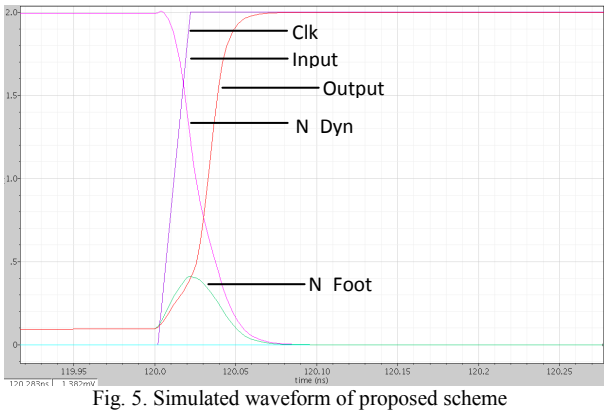

Fig. 5. Simulated waveform of proposed scheme

But according to H M Meimand et al, the disadvantage of the diode footer is that, it increases the switching threshold voltage of gate by the threshold of NMOS and the new threshold voltage is about $2V_{TN}$ of the original. So there will be a performance degradation of the circuit. The performance degradation is then optimized by putting a current mirror that mirrors the current. The current is now drained easily to the ground.

$$I_{total\_eval}=I_{PDN}+I_{MIRROR}$$

I_{total_eval} = Total evaluation current
I_{PDN}= Current through the evaluation network
I_{MIRROR}= Current through the mirror transistor

B. Noise Analysis:-

When the PDN is OFF and the N_Dyn is at high voltage and the N_Foot is at low voltage, the high level of dynamic node makes the gate of the NMOS M6 of the buffer to V_{DD} and the low level of N_Foot makes the source of the M6 to 0. This makes M6 ON and the voltage of buffer output of buffer same as the voltage of N_Foot. It can be easily verified that if the NOMS transistor of the buffer can always be turned off, the pulses propagating to the output can be avoided [5].

In the evaluation period, when the NMOS clock transistor M4 is ON, N_Foot gets discharged to 0. When the PDN is ON the N_Dyn also gets discharged to ground. This makes the VGS of buffer NMOS M6 to 0 as VGS=VG-VS=0. This makes the NMOS OFF and the buffer output gets completely charged thru PMOS M7.

During precharge the dynamic node will get charged to high, when the PDN is ON the voltage of the N_Foot is nearly same as N_Dyn, as the NMOS M4 is OFF. The VGS of the buffer NMOS will be VG-VS<VTH which keeps the NMOS of the buffer at turned OFF stage. The PMOS of the buffer is also OFF due to the high level of N_dyn node. This makes the output of buffer LOW.

So by making the NMOS of the buffer switched OFF during the operation during precharge avoids the pulses propagating to the output. This makes the performance of the circuit better than other circuits. This also limits the sampling time and the power consumption will be decreased.

C. Power Analysis:-

The proposed structure uses the semi-dynamic buffer structure. So the output node OUT has no pulses in the precharge stage as shown in fig. 6. In the figure the 1st waveform shows the clock the second and third wave form shows the inputs of the 2 inputs or gate. The 4th waveform shows the output plotted for the basic domino gate. The 5th and 6th waveform shows the outputs of the two reference circuit structures. The last or the 7th waveform shows the output of the proposed circuit.

It can be seen that the 4 5 and 6 waveforms contains the pulses in the precharge period, but the proposed output does not contain such pulses, which means the buffer does not get on and off frequently, so the current through the buffer reduced sufficiently then the counterpart.

If there many pulses the buffer gets ON and OFF frequently. The power consumption of the logic circuit in conventional circuit is given by [5]

$$P_{avg1}= K.V_{DD}^{2}.C_{dyn}+ r.f.V_{DD}.V_{noise}.C_{dyn} \quad (1)$$

Power consumption of the buffer in conventional stage is given by

$$P_{avg2}=K.V_{DD}^{2}.(C_{load}+C_{buffer})+r.f.V_{DD}.V_{noise}.(C_{load}+Cbuffer \quad (2)$$

As $C_{load} \gg C_{buffer}$, equation 2 becomes

$$P_{avg2}=K.V_{DD}^{2}.C_{load}+r.f.V_{DD}.V_{noise}.C_{load} \quad (3)$$

$$P_{avg}=K.V_{DD}^{2}.(C_{load}+C_{dyn})+r.f.V_{DD}.V_{noise}.(C_{load}+Cdyn \quad (4)$$

In the proposed logic the power is given by

$$P_{prop}= K.V_{DD}^{2}.C_{load}+ r.f.V_{DD}.V_{noise\_p}.C_{load} \quad (5)$$

So the finally the amount of power which the proposed circuit saves is

$$P_{avg}\text{-}P_{prop}=K.V_{DD}^{2}.(C_{load}+C_{dyn})+ r.f.V_{DD}.V_{noise}.(C_{load}+C_{dyn})-K.V_{DD}^{2}.C_{load}- r.f.V_{DD}.V_{noise\_p}.C_{load}$$

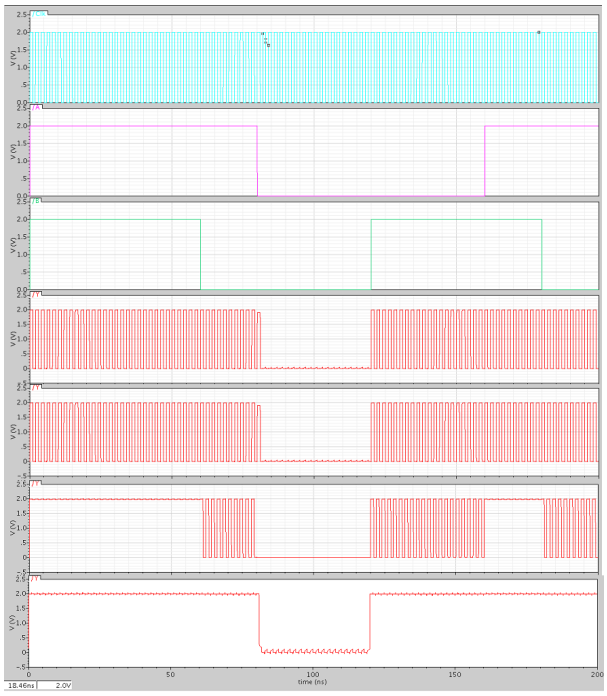

Fig.6. Waveform simulated for the OR gate
1. Clock Input 2. Input A 3. Input B 4. Output for basic circuit
5. Output for [4] 6. Output for [3] 7. Output for Proposed circuit

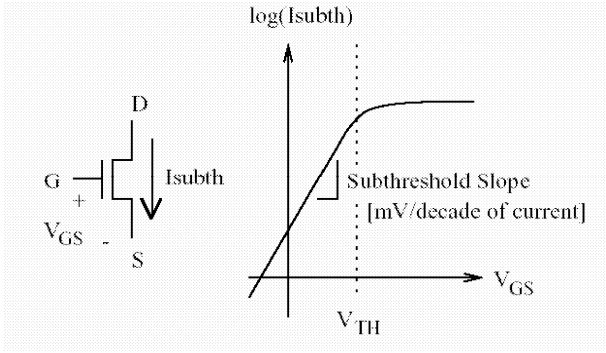

Fig.7. Subthreshold leakage in a metal–oxide–semiconductor (NMOS) transistor [7]

Power saved due to semidynamic logic is

$$P_{saved}=\mathrm{K}.{V_{DD}}^2.C_{dyn}+r.f.V_{DD}.V_{noise}.C_{dyn}+ r.f.V_{DD}.V_{noise}.C_{load} \quad (6)$$

As $V_{noise} \gg V_{noise_p}$

Also the power can be reduced due to the voltage drop across the diode footer, which makes the V_{GS} of the OFF evaluation network negative, causing exponential reduction in subthreshold leakage. This phenomena reduces the power consumption of the circuit.

.IV. SIMULATION AND COMPARISON OF RESULTS

These circuits are simulated with Cadence Specter using 90nm technology and 2V. The circuit was being compared with the OR gate previous techniques. The OR gate was implemented because it is a typical example of wide pull-down network. The proposed circuit was being implemented for comparator circuit and was compared with the comparator circuits of other reference circuits and also investigated with different values of fan-in. It was found that the proposed circuit performs better than the previous proposed circuits.

The proposed circuit also shows advantage in having less number of transistors as compared to the previous. As compared to the basic domino the proposed circuit contains only 3 extra transistors where the other circuits contain more number of extra transistors with the disadvantage of having the inverting clock.

This technique reduces up to 95% of power from the existing technique and the speed of the circuit increases exponentially because of the elimination of pulses during the precharge phase and reduction of subthreshold leakage current in the PDN.

Table.1. Comparison of comparator circuit for proposed domino logic with comparator designed with Basic circuit and other reference circuits

Comparator fan-in	Parameters	Basic	Scheme on paper [3]	Scheme on paper [4]	Proposed scheme
1-Bit	Delay	4.106 E-8	4.109 E-8	3.98 E-8	2.84 E-11
	Power	5.0 E-6	5.6 E-6	5.2 E-6	1.5 E-6
2-Bit	Delay	4.00 E-8	4.10 E-8	3.72 E-8	4.66 E-11
	Power	7.2 E-6	9.6 E-6	8.5 E-6	1.6 E-6
4-Bit	Delay	4.107 E-8	4.111 E-8	3.56 E-8	6.43 E-11
	Power	2.28 E-5	2.8 E-5	2.5 E-5	1.9 E-6
8-Bit	Delay	4.00 E-8	4.00 E-8	3.84 E-8	9.68 E-11
	Power	2.07 E-5	1.14 E-5	1.67 E-5	2.3 E-6
16-Bit	Delay	4.00 E-8	4.01 E-8	3.54 E-8	1.55 E-11
	Power	3.88 E-5	1.4 E-5	1.2 E-5	3.14 E-6
32-Bit	Delay	4.02 E-8	4.16 E-8	3.22 E-8	2.65 E-11
	Power	7.5 E-5	1.7 E-5	1.3 E-5	4.4 E-6

Table.2. Comparison of PDP of the proposed circuit with the basic domino and other reference domino logic

fan-in	Basic	[3]	[4]	Proposed
1-Bit	2.05E-13	2.30E-13	2.06E-13	4.26E-17
2-Bit	2.88E-13	3.93E-13	3.16E-13	7.45E-17
4-Bit	9.36E-13	1.15E-12	8.90E-13	1.22E-16
8-Bit	8.28E-13	4.56E-13	6.41E-13	2.22E-16
16-Bit	1.55E-12	5.61E-13	4.24E-13	4.86E-17
32-Bit	3.01E-12	7.07E-13	4.18E-13	1.11E-17

IV. CONCLUSION

In this paper, we have proposed a high-speed and low-power domino logic circuit. The simulation is carried out with 90 nm and 2 V process technology. The results indicate that the proposed scheme can work at very high speed while consuming very low power, which in turn reduces the PDP of the circuit exponentially. The proposed circuit also shows noise efficiency compared to previous work in the literature. The circuit is flexible and quite applicable for large fan-in gates.

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