Politecnico di Torino

Project report
Integrated System Technology

Master degree in Electronic Engineering

Group 2

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February 15, 2019

Contents

Introduction

In this project analysis on logic gates have been carried out, estimating power and delay; dynamic logic CMOS NAND2, NAND3, NOR2, NOR3 have been implemented. The analyses have been made for different fan-in and fan-out parameters, making parametric the whole system: then, *MATLAB* simulations have been processed in order to test the models implemented,

CHAPTER 1

Theoretical analysis

1.0.1 Delay analysis

First of all, the delay analysis has been considered by exploiting the Elmore Delay: it is an optimistic model but it could be a starting point in order to compare different technological nodes, highlighting the variations between them.
Since the following theoretical discussion is the same for each gate, it has been considered that would be better doing it once for each case, in order to avoid redundancy inside the report. Eventually, all the capacitances per unit of length/area have been multiplied per the corresponding unit, scaling them in order to obtain fixed units of measurement (e.g. $[pF]$, $[\mu m]$).

The first step is to evaluate the input capacitance of nMOS and pMOS transistors:

$$C_{in_N} = C_{OX} + C_{overlapN} \quad [pF] \tag{1.1}$$

$$C_{in_P} = C_{OX} + C_{overlapP} \quad [pF] \tag{1.2}$$

where overlap capacitances are caused by the overlap region between the gate and drain/source areas during the fabrication process:

$$C_{overlapN} = W_n \cdot C_{GDOn} \quad [pF] \tag{1.3}$$

$$C_{overlapP} = W_p \cdot C_{GDOp} \quad [pF] \tag{1.4}$$

It's clear how important is to minimise the overlap capacitance but since it's very difficult to guarantee the perfect alignment between gate and drain/source, it's better having them, instead of an area where neither the gate nor the source/drain areas overlap (no functional MOS).

The junction capacitances between source and drain are:

$$C_{jN} = C_{bottomN} \cdot W_n + C_{sidewallN} \cdot perimeter_n \quad [pF] \tag{1.5}$$

$$C_{jP} = C_{bottomP} \cdot W_p + C_{sidewallP} \cdot perimeter_p \quad [pF] \tag{1.6}$$

The former refers to the capacitance of the pool area of the source/drain and the latter is the one due to the edge of the same pool. Usually parasitic capacitances C_{jN} and C_{jP} are per unit length, here expressed multiplying by the perimeter computed as:

$$\text{perim}_N = 2 \cdot \text{lungh\_diff} + W_n \quad [nm] \tag{1.7}$$

$$\text{perim}_P = 2 \cdot \text{lungh\_diff} + W_p \quad [nm] \tag{1.8}$$

taking into account just one side of W, because across the other one there's only spatial charge.

Junction capacitance contributions are computed as:

$$C_{bottomN} = C_{j0_N} \cdot \left(1 + \frac{V_{DD}}{2 \cdot P_{bN}}\right)^{-M_{jN}} \cdot 2.5 \cdot L_{diff} \quad [pF/\mu m] \tag{1.9}$$

$$C_{bottomP} = C_{j0_P} \cdot \left(1 + \frac{V_{DD}}{2 \cdot P_{bP}}\right)^{-M_{jP}} \cdot 2.5 \cdot L_{diff} \quad [pF/\mu m] \tag{1.10}$$

$$C_{sidewallN} = C_{sw_N} \cdot \left(1 + \frac{V_{DD}}{2 \cdot P_{bswN}}\right)^{-M_{jswN}} \quad [pF/\mu m] \tag{1.11}$$

$$C_{sidewallP} = C_{sw_P} \cdot \left(1 + \frac{V_{DD}}{2 \cdot P_{bswP}}\right)^{-M_{jswP}} \quad [pF/\mu m] \tag{1.12}$$

Now we have to evaluate the equivalent resistance of the MOS that contributes in the delay calculation:

$$R_n = \frac{1}{\mu_n \cdot C_{OX} \cdot \frac{W_N}{L_{eff}} \cdot (V_{DD} - V_{tn})} \quad [\Omega] \tag{1.13}$$

$$R_p = \frac{1}{\mu_p \cdot C_{OX} \cdot \frac{W_P}{L_{eff}} \cdot (V_{DD} - V_{tp})} \quad [\Omega] \tag{1.14}$$

Another parameter used in our analysis is h. It's simply the multiplier of the number of inverter linked in output, the parametric fan-out.

1.0.2 Static power estimation

Static power can be calculated as

$$P_{static} = V_{DD} \cdot I_{leak} \quad [nW] \tag{1.15}$$

where I_{leak} is the leakage current and V_{DD} is the voltage supply. In order to estimate leakage contribution, two figures of merit have to be considered:

- *Subthreshold current*: contribution that flows from drain to source when $V_{gate_{nMOS}} = 0$ and $V_{gate_{pMOS}} = V_{DD}$ (reference fig. 1.2);
- *Gate current*: contribution flowing from drain/source to gate or viceversa when terminals are tied at the same potential, opposite to the gate one (reference fig. 1.1).

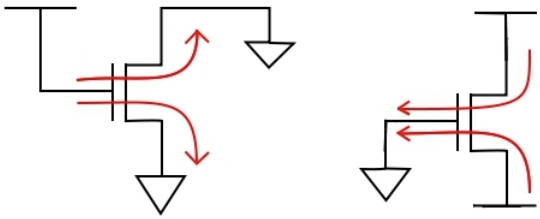

Figure 1.1: Leakage current example

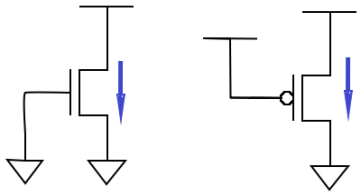

Figure 1.2: Subthreshold current example

1.0.3 Dynamic power estimation

The dynamic power can be evaluated through the following expression:

$$P_{dynamic} = \frac{1}{2} \cdot f \cdot C \cdot \alpha \cdot V_{DD}^2 \quad [\mu W] \tag{1.16}$$

where f means operating frequency, C the total capacitance while α is the switching activity of the considered node.

CHAPTER 2

NAND2/NAND3 realised in Dynamic Logic

First of all, in order to be clear during explanation, it could be useful to show the circuit of the gates under testing:

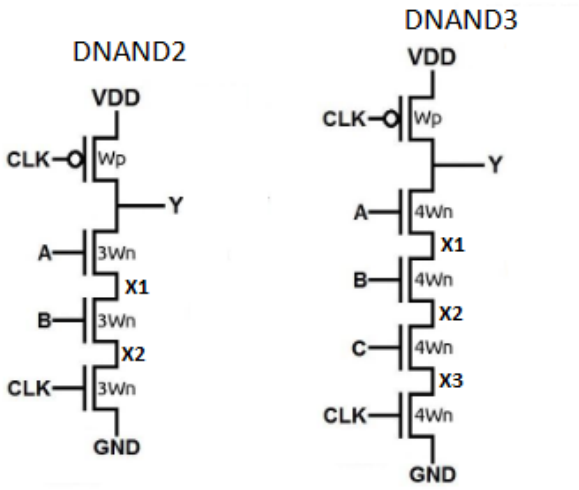

Figure 2.1: Dynamic schemes of NAND gates.

Since one of the aim of a report is to avoid redundancy, for all theoretical parts it has been done a reference to the dedicated chapter 1, and so below the results are just shown.

2.0.1 Static power estimation

The only assumption we took into account is that all the signals switch are immediate, in order to consider the gates into two static conditions, by starting from the NAND2 gate:

- **Precharge**:
  when the clock is at *zero*; the line is precharged at V_{DD} so the goes at *GND*.
  So considering all the structures:

$$I_{leakDNAND2}^{precharge} = I_{GATEp} W_P + I_{OFFn} 3W_N \quad [nA] \tag{2.1}$$

- **Evaluate**:
  when the clock is at *one*; the output is evaluated from the inputs.
  Every possible combination of the two inputs is considered and for each of those cases the different appearing leakages contribution are taken into account.

A	B	Y	LEAKEAGE CURRENT (logic)
0	0	1	$I_{OFFn} 3W_N + I_{GATEn} 3W_N$
0	1	1	$I_{OFFn} 3W_N + 2 \cdot I_{GATEn} 3W_N$
1	0	1	$I_{OFFn} 3W_N + I_{GATEn} 3W_N$
1	1	0	$I_{OFFp} W_P + 3 \cdot I_{GATEn} 3W_N$

Table 2.1: Leakage current contributes for each combination of inputs

By considering the probability for each input combination equal to 1/4, by adding all those terms we got:

$$I_{leakDNAND2}^{evaluate} = \frac{1}{4} \cdot (I_{OFFp} W_P + 9 \cdot I_{OFFn} W_N + 21 \cdot I_{GATEn} W_N) \quad [nA] \tag{2.2}$$

Assuming that those states occupy an half of the period each, is possible to say that half of the clock period is dedicated to precharge the system while the second half is used to evaluate the output. All this considerations can be synthesised in the following formula:

$$I_{leakDNAND2} = \frac{1}{2} \cdot I_{leakDNAND2}^{precharge} + \frac{1}{2} \cdot I_{leakDNAND2}^{evaluate} \tag{2.3}$$

and so:

$$I_{leakDNAND2} = \frac{1}{2} \cdot \frac{1}{4} \cdot (I_{OFFp} W_P + 4 \cdot I_{GATEp} W_P + 21 \cdot I_{OFFn} W_N + 21 \cdot I_{GATEn} W_N) \quad [nA] \tag{2.4}$$

Now, the same procedure has been done for the NAND3 dynamic gate, and so, in order to avoid redundancy, we have decided to shown directly the final results:

$$I_{leakDNAND3}^{precharge} = I_{GATEp} W_P + I_{OFFn} 4W_N \quad [nA] \tag{2.5}$$

exactly like in the case of the NAND2 since the precharge is the same. For the evaluation current, we have summarised the results inside a table:

C	B	A	Y	LEAKEAGE CURRENT (logic)
0	0	0	1	$I_{OFFn}4W_N + I_{GATEn}4W_N$
0	0	1	1	$I_{OFFn}4W_N + I_{GATEn}4W_N$
0	1	0	1	$I_{OFFn}4W_N + 2 \cdot I_{GATEn}4W_N$
0	1	1	1	$I_{OFFn}4W_N + I_{GATEn}4W_N$
1	0	0	1	$I_{OFFn}4W_N + 2 \cdot I_{GATEn}4W_N$
1	0	1	1	$I_{OFFn}4W_N + 2 \cdot I_{GATEn}4W_N$
1	1	0	1	$I_{OFFn}4W_N + 3 \cdot I_{GATEn}4W_N$
1	1	1	0	$I_{OFFp}W_P + 4 \cdot I_{GATEn}4W_N$

Table 2.2: Leakage current contributes for each combination of inputs

$$I_{leakDNAND3}^{evaluate} = \frac{1}{8} \cdot (I_{OFFp}W_P + 28 \cdot I_{OFFn}W_N + 64 \cdot I_{GATEn}W_N) \quad [nA] \tag{2.6}$$

All these considerations can be synthesise in the following formula:

$$I_{leakDNAND3} = \frac{1}{2} \cdot I_{leakDNAND3}^{precharge} + \frac{1}{2} \cdot I_{leakDNAND3}^{evaluate} \tag{2.7}$$

and so:

$$I_{leakDNAND3} = \frac{1}{2} \cdot \frac{1}{8} \cdot (I_{OFFp}W_P + 8 \cdot I_{GATEp}W_P + 60 \cdot I_{OFFn}W_N + 64 \cdot I_{GATEn}W_N) \quad [nA] \tag{2.8}$$

2.0.2 Delay estimation

By referencing again to the Elmore delay, specifically to the Nand2 gates, it is possible to establish the raise time (tr) and the fall time (tf) by looking at the following figure:

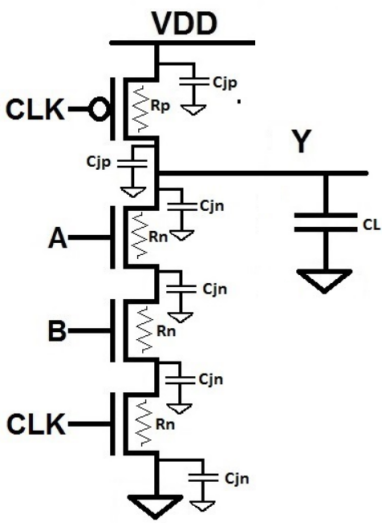

Figure 2.2: Dynamic NAND2 Elmore model

- **NAND2-Dynamic**

$$tr = R_p \cdot (C_{jp} + C_{jn} + C_L) \tag{2.9}$$

$$tf = R_n \cdot (C_{jn} + C_{jn} + C_{jn} + C_{jp} + C_L) + R_n \cdot (C_{jn} + C_{jn} + C_{jp} + C_L) + R_n \cdot (C_{jn} + C_{jp} + C_L) = \\ = R_n \cdot (6 \cdot C_{jn} + 3 \cdot C_{jp} + 3 \cdot C_L) \tag{2.10}$$

And by doing the same step for NAND3, the respective delays are:

- **NAND3-Dynamic**

$$tr_{DNAND3} = R_p \cdot (C_{jp} + C_{jn} + C_L) \tag{2.11}$$

$$tf_{DNAND3} = R_n \cdot (10 \cdot C_{jn} + 4 \cdot C_{jp} + 4 \cdot C_L) \tag{2.12}$$

2.0.3 Dynamic Power estimation

- **NAND2** : by starting from the NAND2 gates, what it has been evaluated is:

The expression to compute the dynamic power is:

$$C \cdot \alpha = C_{IN_{nmos}} \cdot (\alpha_A + \alpha_B) + C_X \cdot (\alpha_{X1} + \alpha_{X2}) + C_Y \cdot \alpha_Y + (C_{IN_{nmos}} + C_{IN_{pmos}}) \cdot \alpha_{CLK} \tag{2.13}$$

The considered capacitances are the following:

- $C_{IN_{nmos}}$ and $C_{IN_{pmos}}$ are the capacitances associated to the inputs for *n-MOS* and *p-MOS* respectively:

$$C_{IN_{nmos}} = C_{OX} \cdot 3W_N \cdot L_{eff} + 2C_{overlapN} = 3C_{OXN} + 2C_{overlapN} \quad [pF] \quad (2.14)$$

$$C_{IN_{pmos}} = C_{OX} \cdot W_P \cdot L_{eff} + 2C_{overlapP} = C_{OXP} + 2C_{overlapP} \quad [pF] \quad (2.15)$$

- C_{X1} and C_{X2} are the capacitances associated to the internal nodes, always supposing that source and drain are common for the two *n-MOS*:

$$C_{X1} = C_{X2} = C_{jN} \quad [pF] \quad (2.16)$$

- C_Y is the output capacitance:

$$C_Y = C_{jP} + C_{jN} + h \cdot C_L \quad [pF] \quad (2.17)$$

  Where C_L means load capacitance, and generally the standard output is the inverter, which has the following input capacitance:

$$C_{INV} = C_{OX} \cdot W_N \cdot L_{eff} + C_{OX} \cdot W_P \cdot L_{eff} + 2C_{overlapN} + 2C_{overlapP} \quad [pF] \quad (2.18)$$

and h is the parameter for the fanout that tells how many inverters are connected to the output of the gates.
Regarding the switching activity we have to do some considerations: α_{CLK} is the switching activity associated to the clock signal and can be considered equal to 2. This because for sure there are two commutations in a single clock period.
The switching activity associated to the input is the same seen for the CMOS static logic:

$$\alpha_A = \alpha_B = \frac{1}{2} \quad (2.19)$$

For the internal the switching activity can be computed as:

$$\alpha_{X,Y} = 2 \cdot (1 - P_{X,Y}) \quad (2.20)$$

This because, considering the worst case, each node commutes 2 times when in *pre-charge phase* is charged and then in *evaluation phase* is discharged, so in the case that the node goes to *zero*.
In this particular example we have:

$$P_{X1} = P_A \cdot (1 - P_B) \Rightarrow \alpha_{X1} = \frac{3}{2} \quad (2.21)$$

$$P_{X2} = P_A \cdot P_B \Rightarrow \alpha_{X2} = \frac{3}{2} \quad (2.22)$$

$$P_Y = (1 - P_A) \cdot (1 - P_B) \Rightarrow \alpha_Y = \frac{3}{2} \quad (2.23)$$

Summing up all the contribution, the final expression is the following:

$$\begin{aligned} C \cdot \alpha_{DAND2} &= 3C_{IN_{nmos}} + 3C_X + \frac{3}{2} \cdot C_Y + 2C_{IN_{pmos}} = \\ &= 9C_{OXN} + 6C_{overlapN} + 2C_{OXP} + 4C_{overlapP} + \frac{9}{2}C_{jN} + \frac{3}{2}C_{jP} + \frac{3}{2}hC_L \end{aligned} \tag{2.24}$$

Here are reported just the final expressions for the 3 inputs NAND cases:

- **NAND3**

$$C \cdot \alpha_{NAND3} = C_{IN_{nmos}} \cdot (\alpha_A + \alpha_B + \alpha_C) + C_X \cdot (\alpha_{X1} + \alpha_{X2} + \alpha_{X3}) + C_Y \cdot \alpha_Y + (C_{IN_{nmos}} + C_{IN_{pmos}}) \cdot \alpha_{CLK} = \tag{2.25}$$

$$C_{IN_{nmos}} + \frac{21}{4}C_X + \frac{7}{4}C_Y + 2(C_{IN_{nmos}} + C_{IN_{pmos}}) = \tag{2.26}$$

$$= 9C_{OXN} + 6C_{overlapN} + 2C_{OXP} + 4C_{overlapP} + 7C_{jN} + \frac{7}{4}C_{jP} + \frac{7}{4}hC_L \tag{2.27}$$

CHAPTER 3

NOR2/NOR3 realised in Dynamic Logic

Here we will follow the same steps that have been performed with the NAND gates, since the aims are the same: static power, delay estimation and dynamic power. First of all, it's better to show the circuits under study:

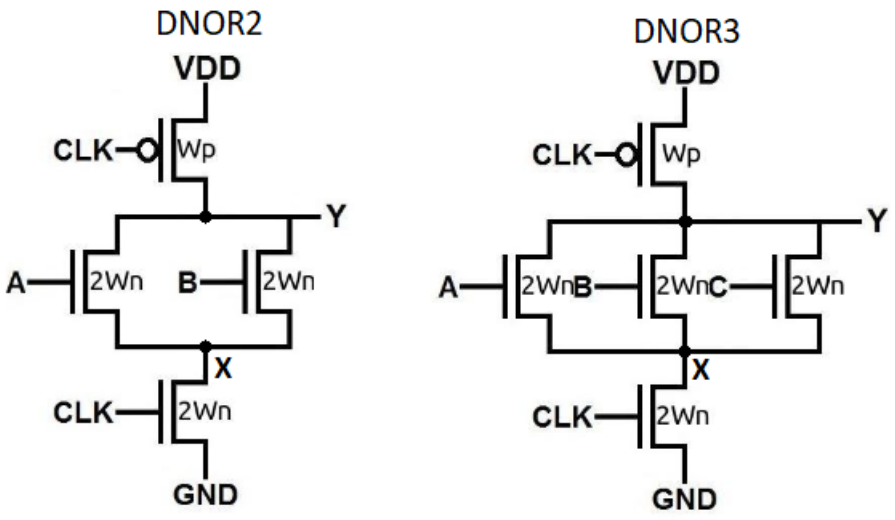

Figure 3.1: Dynamic schemes of NOR gates.

3.1 Static power estimation

The only assumption taken is that all the signals switch immediately in order to consider the gates into two static conditions, starting from the NOR2 gate:

- **Precharge**:
  when the clock is at *zero*; the line is precharged at V_{DD} so the goes at *GND*.

So considering all the structures:

$$I_{leakDNOR2}^{precharge} = I_{GATEp}W_P + 2 \cdot I_{OFFn}2W_N \quad [nA] \tag{3.1}$$

- **Evaluate**:
  when the clock is at *one*; the output is evaluated from the inputs.
  Every possible combination of the two inputs is considered and for each of those cases the different appearing leakage contributions are taken into account.

A	B	Y	LEAKEAGE CURRENT (logic)
0	0	1	$2 \cdot I_{OFFn}2W_N + I_{GATEn}2W_N$
0	1	0	$2 \cdot I_{GATEn}2W_N + I_{OFFp}W_P$
1	0	0	$2 \cdot I_{GATEn}2W_N + I_{OFFp}W_P$
1	1	0	$3 \cdot I_{GATEn}2W_N + I_{OFFp}W_P$

Table 3.1: Leakage current contributes for each combination of inputs

By considering the probability for each input combination equal to 1/4, by adding all those terms we got:

$$I_{leakDNOR2}^{evaluate} = \frac{1}{4} \cdot (3 \cdot I_{OFFp}W_P + 4 \cdot I_{OFFn}W_N + 16 \cdot I_{GATEn}W_N) \quad [nA] \tag{3.2}$$

Assuming that those states occupy an half of the period each, is possible to say that half of the clock period is dedicated to precharge the system while the second half is used to evaluate the output. All this consideration can be synthetized in the following formula:

$$I_{leakDNOR2} = \frac{1}{2} \cdot I_{leakDNOR2}^{precharge} + \frac{1}{2} \cdot I_{leakDNOR2}^{evaluate} \tag{3.3}$$

and so:

$$I_{leakDNOR2} = \frac{1}{2} \cdot \frac{1}{4} \cdot (3 \cdot I_{OFFp}W_P + 4 \cdot I_{GATEp}W_P + 20 \cdot I_{OFFn}W_N + 16 \cdot I_{GATEn}W_N) \quad [nA] \tag{3.4}$$

Now, the same reasoning has been done for the NOR3 dynamic gate, showing directly the final results:

$$I_{leakDNOR2}^{precharge} = I_{GATEp}W_P + 3 \cdot I_{OFFn}2W_N \quad [nA] \tag{3.5}$$

exactly like in the case of the NOR2 since the precharge is the same. For the evaluation current, we have summarised the result inside a table:

C	B	A	Y	LEAKEAGE CURRENT (logic)
0	0	0	1	$3 \cdot I_{OFFn} 2W_N + I_{GATEn} 2W_N$
0	0	1	0	$2 \cdot I_{GATEn} 2W_N + I_{OFFp} W_P$
0	1	0	0	$2 \cdot I_{GATEn} 2W_N + I_{OFFp} W_P$
0	1	1	0	$3 \cdot I_{GATEn} 2W_N + I_{OFFp} W_P$
1	0	0	0	$2 \cdot I_{GATEn} 2W_N + I_{OFFp} W_P$
1	0	1	0	$3 \cdot I_{GATEn} 2W_N + I_{OFFp} W_P$
1	1	0	0	$3 \cdot I_{GATEn} 2W_N + I_{OFFp} W_P$
1	1	1	0	$4 \cdot I_{GATEn} 2W_N + I_{OFFp} W_P$

Table 3.2: Leakage current contributes for each combination of inputs

$$I_{leakDNOR3}^{evaluate} = \frac{1}{8} \cdot (7 \cdot I_{OFFp} W_P + 6 \cdot I_{OFFn} W_N + 40 \cdot I_{GATEn} W_N) \quad [nA] \tag{3.6}$$

All these considerations can be synthetized in the following formula:

$$I_{leakDNOR3} = \frac{1}{2} \cdot I_{leakDNOR3}^{precharge} + \frac{1}{2} \cdot I_{leakDNOR3}^{evaluate} \tag{3.7}$$

and so:

$$I_{leakDNOR3} = \frac{1}{2} \cdot \frac{1}{8} \cdot (7 \cdot I_{OFFp} W_P + 8 \cdot I_{GATEp} W_P + 54 \cdot I_{OFFn} W_N + 40 \cdot I_{GATEn} W_N) \quad [nA] \tag{3.8}$$

3.1.1 Delay estimation

By doing again reference to the Elmore delay, it is possible to establish the raise time (tr) and the fall time (tf) by looking at the following figure:

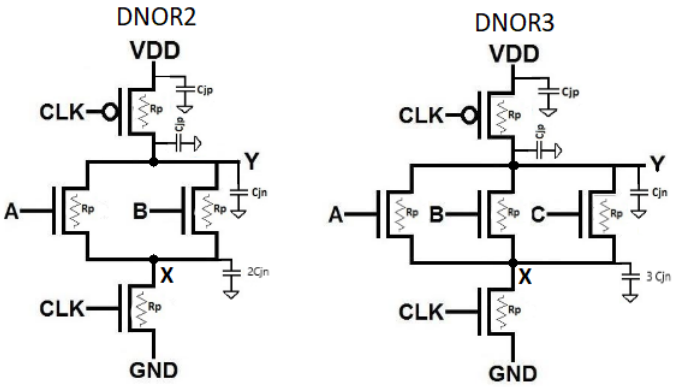

Figure 3.2: Dynamic NOR2 NOR3 Elmore model

- **NOR2-Dynamic**

$$tr = R_p \cdot (C_{jp} + C_{jn} + C_L) \tag{3.9}$$

$$\begin{aligned} tf = R_n \cdot (2C_{jn} + C_{jn} + C_{jp} + C_L) + R_n \cdot (C_{jn} + C_{jp} + C_L) = \\ = R_n \cdot (4 \cdot C_{jn} + 2 \cdot C_{jp} + 2 \cdot C_L) \end{aligned} \tag{3.10}$$

And by doing the same step for NOR3, the respective delays are:

- **NOR3-Dynamic**

$$tr = R_p \cdot (C_{jp} + C_{jn} + C_L) \tag{3.11}$$

$$tf = R_n \cdot (5 \cdot C_{jn} + 2 \cdot C_{jp} + 2 \cdot C_L) \tag{3.12}$$

This is a very pessimistic model, since of course, due to the parallel configuration of the Nmos, the capacitances can be discharged through the parallel of different R_N, but as always, we have to consider the worst case.

3.1.2 Dynamic Power estimation

- **NOR2** : by starting from the NOR2 gates, what it has been evaluated is:

The expression to compute the dynamic power is:

$$C \cdot \alpha = C_{IN_{nmos}} \cdot (\alpha_A + \alpha_B) + C_X \cdot \alpha_X + C_Y \cdot \alpha_Y + (C_{IN_{nmos}} + C_{IN_{pmos}}) \cdot \alpha_{CLK} \tag{3.13}$$

The considered capacitances are the following:

- $C_{IN_{nmos}}$ and $C_{IN_{pmos}}$ are the capacitances associated to the inputs for *n-MOS* and *p-MOS* respectively:

$$C_{IN_{nmos}} = C_{OX} \cdot 3W_N \cdot L_{eff} + 2C_{overlapN} = 3C_{OXN} + 2C_{overlapN} \quad [pF] \quad (3.14)$$

$$C_{IN_{pmos}} = C_{OX} \cdot W_P \cdot L_{eff} + 2C_{overlapP} = C_{OXP} + 2C_{overlapP} \quad [pF] \quad (3.15)$$

- C_X is the capacitance associated to the internal node, always supposing that source and drain are common for the two *n-MOS*:

$$C_X = 2 \cdot C_{jN} \quad [pF] \quad (3.16)$$

- C_Y is the output capacitance:

$$C_Y = C_{jP} + C_{jN} + h \cdot C_L \quad [pF] \quad (3.17)$$

  Where C_L means load capacitance, and generally the standard output is the inverter, which has the following input capacitance:

$$C_{INV} = C_{OX} \cdot W_N \cdot L_{eff} + C_{OX} \cdot W_P \cdot L_{eff} + 2C_{overlapN} + 2C_{overlapP} \quad [pF] \quad (3.18)$$

and h is the parameter for the fanout that tells how many inverters are connected to the output of the gates.
Regarding the switching activity we have to do some considerations: α_{CLK} is the switching activity associated to the clock signal and can be considered equal to 2: for sure there are two commutations in a single clock period.
The switching activity associated to the input is the same seen for the CMOS static logic:

$$\alpha_A = \alpha_B = \frac{1}{2} \quad (3.19)$$

For the internal the switching activity can be computed as:

$$\alpha_{X,Y} = 2 \cdot (1 - P_{X,Y}) \quad (3.20)$$

This because, considering the worst case, each node commutes 2 times when in *pre-charge phase* is charged and then in *evaluation phase* is discharged, so in the case that the node goes to *zero*.
In this particular example we have:

$$P_X = P_A \cdot P_B \Rightarrow \alpha_X = \frac{3}{2} \quad (3.21)$$

$$P_Y = 1 - P_A \cdot P_B \Rightarrow \alpha_Y = \frac{1}{2} \quad (3.22)$$

Summing up all the contributions, the final expression is the following:

$$\begin{aligned} C \cdot \alpha_{DNOR2} &= 3C_{IN_{nmos}} + \frac{3}{2}C_X + \frac{1}{2} \cdot C_Y + 2C_{IN_{pmos}} = \\ &= 9C_{OXN} + 6C_{overlapN} + 2C_{OXP} + 4C_{overlapP} + \frac{7}{2}C_{jN} + \frac{1}{2}C_{jP} + \frac{h}{2}C_L \end{aligned} \tag{3.23}$$

Here are reported just the final expressions for the 3 inputs NOR case:

- **Dynamic NOR3**

$$C \cdot \alpha_{NOR3} = C_{IN_{nmos}} \cdot (\alpha_A + \alpha_B + \alpha_C) + C_X \cdot \alpha_X + C_Y \cdot \alpha_Y + (C_{IN_{nmos}} + C_{IN_{pmos}}) \cdot \alpha_{CLK} = \tag{3.24}$$

$$C_{IN_{nmos}} + \frac{7}{4}C_X + \frac{1}{4}C_Y + 2(C_{IN_{nmos}} + C_{IN_{pmos}}) = \tag{3.25}$$

$$= 9C_{OXN} + 6C_{overlapN} + 2C_{OXP} + 4C_{overlapP} + \frac{11}{2}C_{jN} + \frac{1}{4}C_{jP} + \frac{h}{4}C_L \tag{3.26}$$

CHAPTER 4

MATLAB implementation and results

In table 4.2 the variables used into the modules are reported. Then, grafical results about dynamic power and delay are shown. Static power evaluation is reported:

Gate	Static power $[nW]$
NAND2	722.7
NAND3	1050.3
NOR2	430.9
NOR3	538.2

Table 4.1: Static Power of different gates.

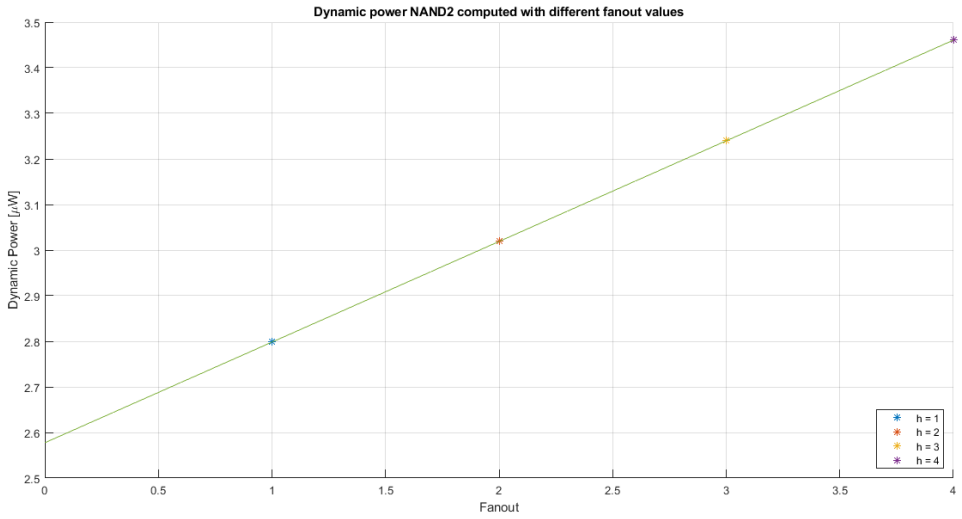

Figure 4.1: Dynamic power NAND2

Code variable	Source file	Physical quantity
Lgate	Technology file	nm
Wgate	Technology file	nm
Vdd	Technology file	V
Xj	Technology file	nm
Cox	Technology file	F/cm^2
Cj0n	Technology file	$pF/\mu m^2$
Cjswn	Technology file	$pF/\mu m^2$
Cj0p	Technology file	$pF/\mu m^2$
Cjswp	Technology file	$pF/\mu m^2$
Cgd0n	Technology file	F/m
Cgd0p	Technology file	F/m
Gamma	Technology file	$-$
Mjn	Technology file	%
Mjp	Technology file	%
Mswn	Technology file	%
Mswp	Technology file	%
Pbn	Technology file	V
Pbp	Technology file	V
Pbswn	Technology file	V
Pbswp	Technology file	V
mueff_n	Mobility module	cm^2/Vs
mueff_p	Mobility module	cm^2/Vs
Vth_n	Vth module	V
Vth_p	Vth module	V
Ioff_n	Ioff module	$nA/\mu m$
Ioff_p	Ioff module	$nA/\mu m$
Igate_n	Igate module	$nA/\mu m$
Igate_p	Igate module	$nA/\mu m$

Table 4.2: Variables required and used by the module

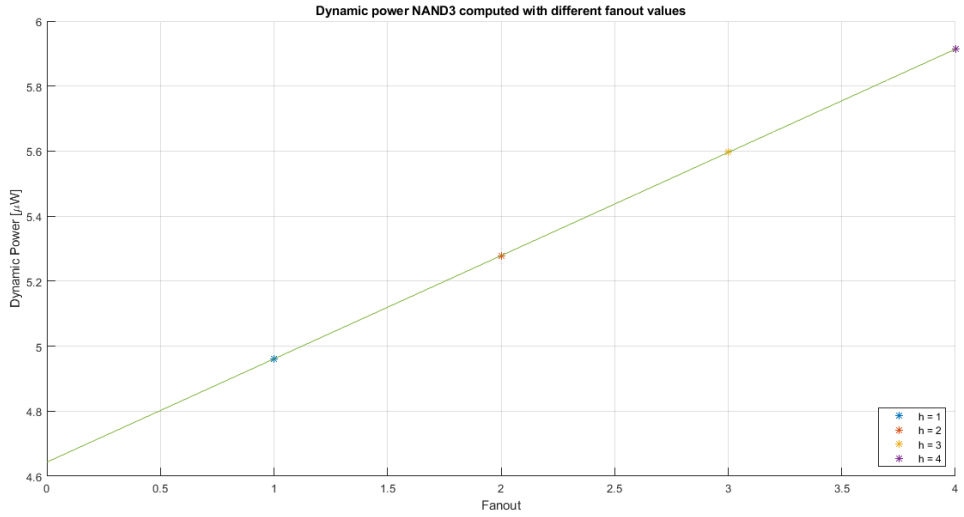

Figure 4.2: Dynamic power NAND3

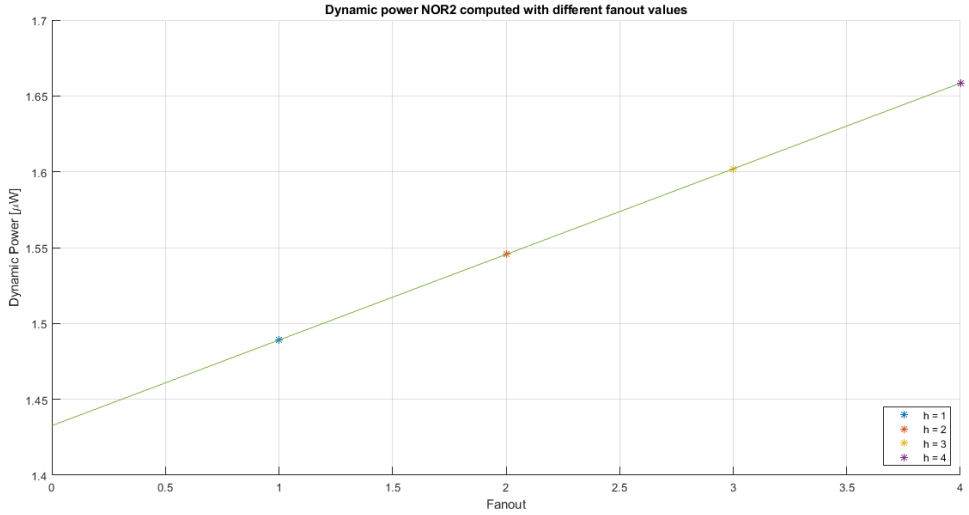

Figure 4.3: Dynamic power NOR2

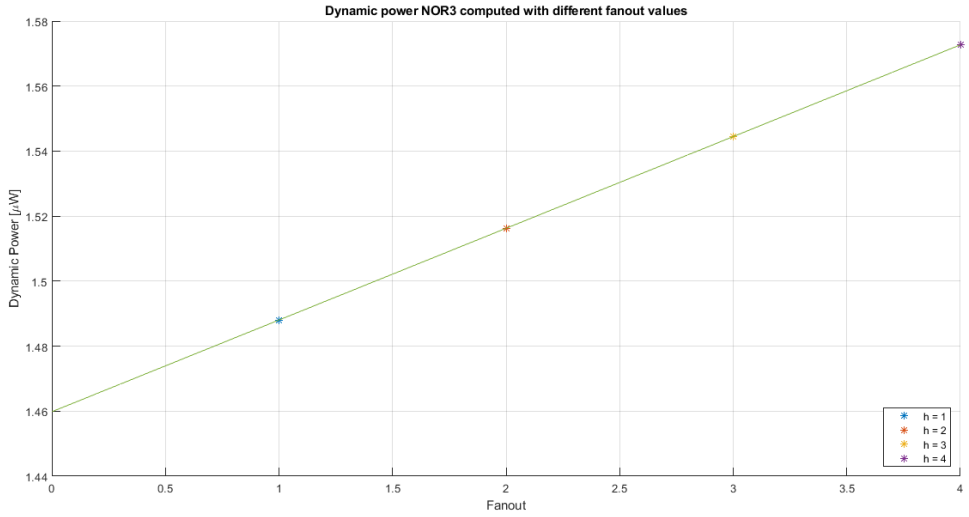

Figure 4.4: Dynamic power NOR3

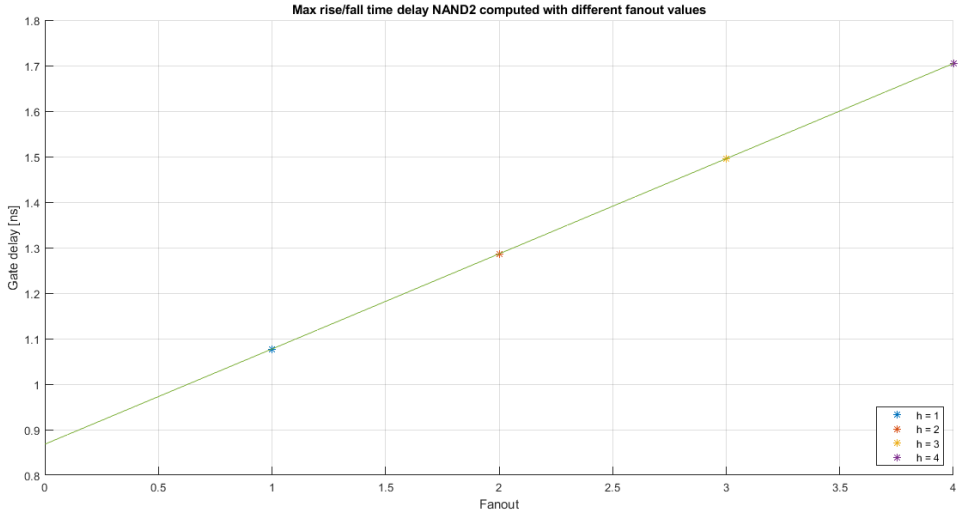

Figure 4.5: Delay NAND2

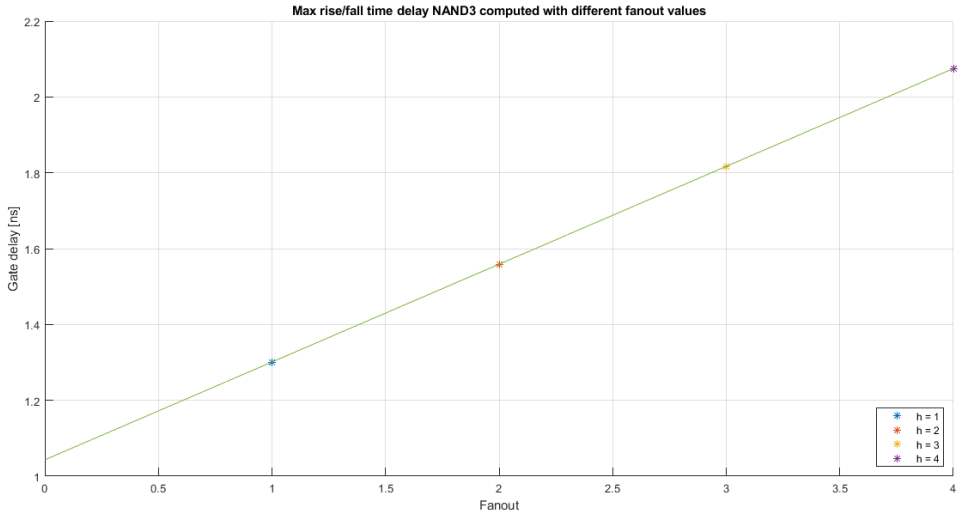

Figure 4.6: Delay NAND3

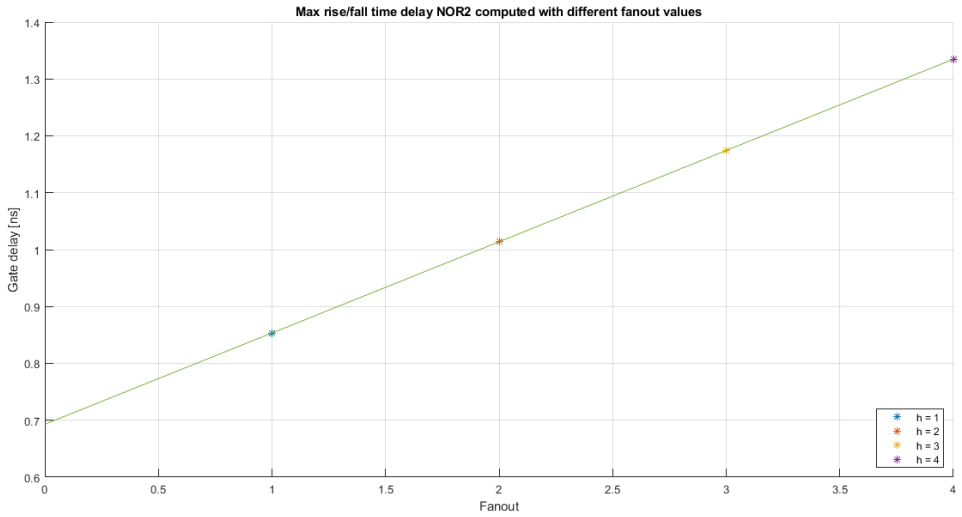

Figure 4.7: Delay NOR2

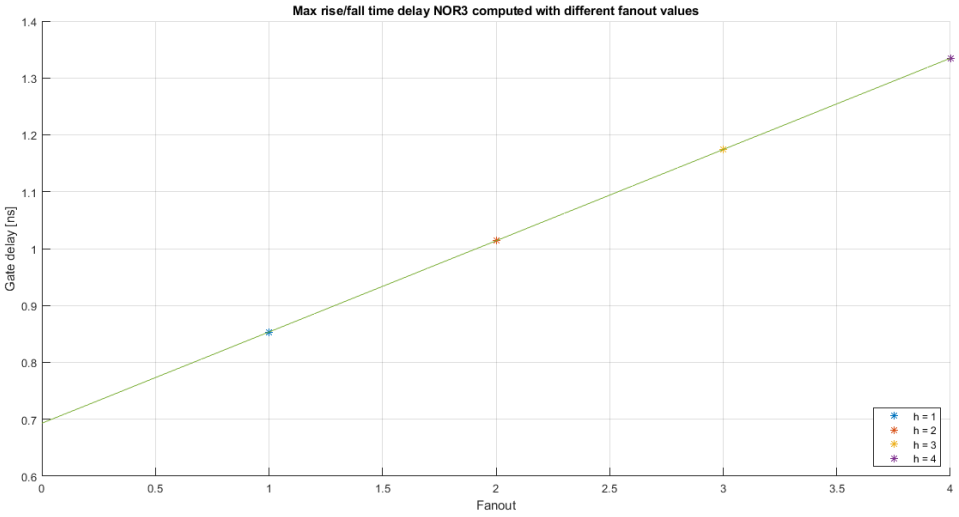

Figure 4.8: Delay NOR3

4.0.1 Conclusion

About the static power, like it is possible to appreciate in the table 4.1, the lowest value is for the NOR2 gate while the biggest is for the NAND3 gate. This is due to the dimensions since in the NOR2 we have $W_N = 2 \cdot W_{GATE}$ while for the NAND3 $W_N = 4 \cdot W_{GATE}$. This is true also for the delays and dynamic power.
Of course these figures of merit depends strongly on which parameters of the table 4.2 have been considered but after the considerations regarding the dimensions, we can conclude that the result that we have got are reasonable.