A Low-Power Circuit Technique for Domino CMOS Logic

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***Abstract*-- Dynamic logic style is used in high performance circuit design because of its fast speed and less transistors requirement as compared to CMOS logic style. But it is not widely accepted for all types of circuit implementations due to its less noise tolerance and charge sharing problems. Domino logic uses one static CMOS inverter at the output of dynamic node which is more noise immune and has less capacitance at the output node. In this paper we have proposed a novel circuit for domino logic which less noise at the output node and has very less power-delay product (PDP) as compared to previous reported articles. The proposed circuit is being compared with previous reported domino logic and the basic domino logic structures in different ways and found to be having least PDP from others.**

***Keywords*-- Domino logic; dynamic logic; power consumption; leakage tolerance; robustness.**

I. INTRODUCTION

Dynamic logic is used in the implementation of logic circuit for high speed designs such as data path in microprocessor [1]. However, it is not widely used because of its disadvantages like less noise robust and more power consuming compared to static logic style [2]. Domino logic is made by adding one inverter at the output of the dynamic gate. Domino gate has got advantage over the dynamic gate because fan-out of former is driven by inverter which has low output impedance and thus increases the noise immunity of the gate along with decreasing the output capacitance [3]. Fig. 1 shows the standard domino logic style. Keeper transistor is used to maintain the logic one in the evaluation phase (CLK goes high) when there is charge leakage from the dynamic node through the pull down network (PDN). When PDN is ON in the evaluation phase dynamic node is discharged to zero through the PDN and evaluation transistor. Output inverter starts switching from zero to one and the keeper transistor starts turning OFF from ON. During this period there is static power dissipation from Vdd to Gnd.

During the evaluation phase small noise-signal at the input(s) of dynamic gate can change the desired output because of discharge of dynamic node. In worst case the circuit becomes very less noise-tolerant in case of high-fan in OR gate implementations.

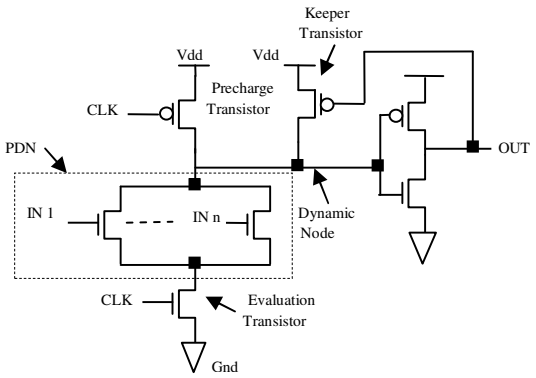

Fig.1. Standard Domino OR gate.

Noise robustness can be improved by upsizing the keeper transistor (making wider) which makes keeper (PMOS) more conducting and thus maintains the charge at the dynamic node [4]. But this comes at the cost of static power dissipation which flows from Vdd to Gnd through keeper transistor when noise signal arrives at one of the inputs. To make dynamic circuit more noise robust different circuit styles have been proposed [4-9].

In this paper we have presented a novel circuit scheme for the domino logic. When compared with the recent proposals, the proposed circuit scheme has better power-delay product and very fast circuit operation.

The rest of the sections are organized as follows. Some related works for noise robustness in domino logic are described

in section II. Section III presents the novel domino circuit approach and simulation results and comparisons are discussed in section IV. Conclusions are presented in Section V.

II. PROBLEM STATEMENT

Fig. 2 is an example of footless domino gate. During the precharge phase when the clock is LOW, the pre-charging PMOS gets ON and the dynamic node is connected to the VDD and gets precharge to VDD. When clock goes high, the evaluation phase starts and the output gets evaluated with the pull-down network and conditionally gets discharged if any one of the input is at logic 1. At the evaluation period when all the inputs are at logic 0, the dynamic node should be at logic 1. But the wide fan-in NMOS pull-down leaks the charge stored in the capacitance at the dynamic node due to the subthreshold leakage. This is again compensated by the PMOS keeper, which aims to restore the voltage of the dynamic node. When a noise voltage impulse occurs at ant gate input, the keeper may not be able to restore the voltage level of the dynamic node. The subthreshold leakage current is exponentially dependent upon V_{GS}. So in the presence of noise impulse the gate voltage increases, which leads to increase in V_{GS} and the dynamic node gets wrongly discharged.

As noise of domino gates is now more important than the area, energy dissipation and delay issues, so recently several techniques have been proposed [6,7] to reduce the noise of dynamic circuits. All the techniques have reduced the noise sensitivity but there are many drawbacks with area, power dissipation and delay.

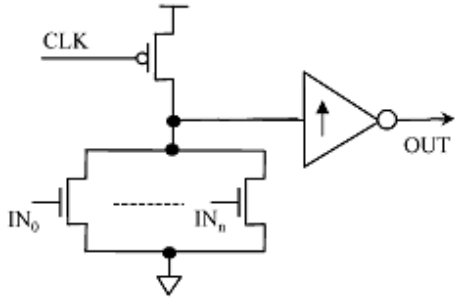

Fig. 2. A typical footless Domino OR gate

III. BACKGROUND AND RELATED WORKS

To compensate the leakage current at the dynamic node a week transistor called keeper transistor is used. Keeper transistor prevents the charge loss and keeps the dynamic node at strong high when PDN is OFF. In the first domino proposal [3] the gate of the keeper transistor is tied to ground, therefore the keeper is always on. If at the beginning of evaluation the pull-down network (PDN) turns on, the dynamic node tends to discharge through the PDN. However, the keeper is injecting charge to the dynamic node as it is always on. This is called contention. Furthermore, a potential DC power consumption problem is generated. To alleviate the potential DC power consumption problem a feedback keeper was proposed in Fig. 2a [4, 5].

Domino circuit to improve noise tolerance proposed in [5] is shown in Fig. 4. At the beginning of the evaluation phase node C is at 0 V. Noise glitches at the input temporarily increases the gate-to-source voltage of the corresponding NMOS in PDN. Increase in the subthreshold current increases the charging of node C. During this process, gate-to-source voltage of the active NMOS decreases and the subthreshold leakage current is exponentially reduced.

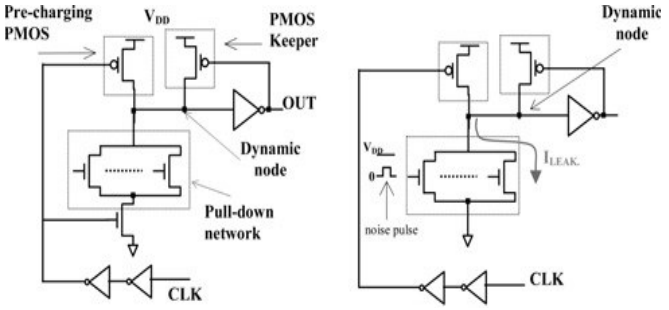

Fig. 3. Standard domino OR gate
a Footed scheme
b Footless scheme

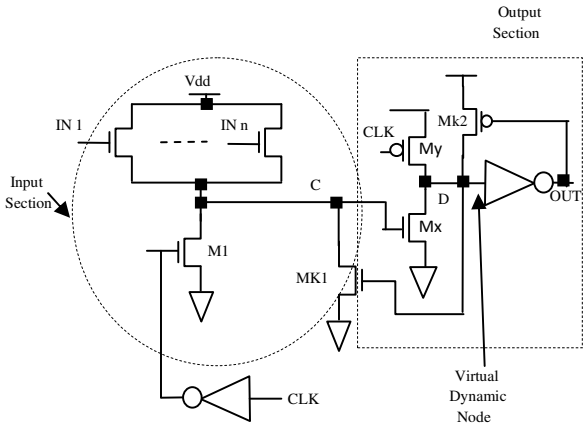

Fig. 4. Domino style proposed in [7]

IV. PROPOSED DOMINO CIRCUIT SCHEME

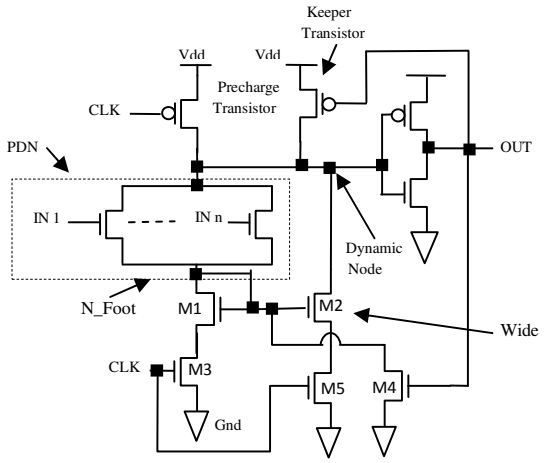

Fig. 5. Proposed domino circuit scheme

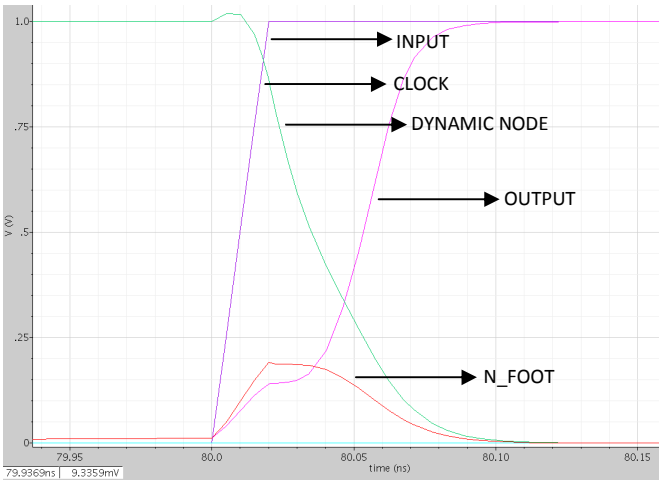

Fig. 6. Simulated waveform of proposed scheme

The proposed novel domino circuit scheme is shown in Fig. 5. Transistor M1 is used as diode. Due to voltage drop across M_1, gate-to-source voltage of the NMOS transistor in the PDN decreases (stacking effect [10]). The proposed circuit differs from [4] as it has additional evaluation transistor M5 with gate connected to the CLK. In [4], when M_1 has voltage drop due to presence of noise-signals, M_2 starts leaking that causes the circuit to dissipate power and also makes it less noise robust. The purpose of M_5 in proposed scheme causes the stacking effect and makes gate-to-source voltage of M_2 smaller (M_2 less conducting).

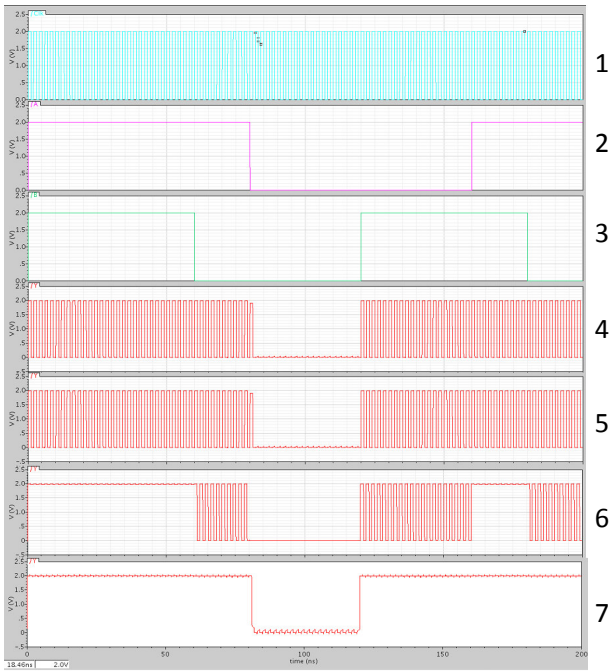

Fig. 7. Waveform simulated for the OR gate
1. Clock Input
2. Input A
3. Input B
4. Output for basic circuit
5. Output for [6]
6. Output for [7]
7. Output for Proposed circuit

Hence circuit becomes more noise robust and less leakage power consuming. But for performance degrades because of stacking effect in mirror current path. This can be increased by widening the M2 (high W/L) to make it more conducting. Due to the stacking effect of the diode footer the subthreshold leakage also decreases [4]. Due to the presence of the diode footer there is a voltage drop across the diode footer in evaluation phase. Due to the voltage drop V_{GS} becomes negative which cause exponential reduction in the threshold voltage.

Fig. 6 shows the simulated waveform of the proposed circuit. This waveform shows the characteristic of the output node, the dynamic node and the N_Foot with the input waveform. This wave form has been taken at the evaluation phase of the clock, when the dynamic node evaluates the input waveform.

Fig. 7 shows the output simulation result of the proposed circuit with the other reference circuits. The proposed circuit output is containing very less noise as compared to the other domino circuits, which can be shown in the waveform. The proposed circuit output waveform does not have more number of charging and discharging which minimises the power dissipation of the circuit and also makes the circuit fast from expected. This reduction in power and delay reduces the power-delay product (PDP) of the circuit.

Also the power can be reduced due to the voltage drop across the diode footer, which makes the VGS of the OFF evaluation network negative, causing exponential reduction in subthreshold leakage. This phenomenon reduces the power consumption of the circuit.

V. SIMULATION RESULTS, COMPARISONS AND DISCUSSIONS

Circuits are simulated using Cadence specter simulator at temperature of 27 degree Celsius with in 90 nm CMOS technology for bulk CMOS [11]. The simulation was being done in different voltages of V_{GS} and the power dissipation and delay was measured. That delay and power of the proposed circuit were compared with the basic CMOS footed and footless domino circuits, the keepered and keeperless circuits and previous proposed circuits. It can be shown from the tables that power-delay product can be reduced up to 100% from the latest proposed schemes. This can be a better circuit for high speed embedded circuits.

TABLE I. POWER DELAY COMPARISON OF THE PROPOSED CIRCUIT WITH PREVIOUS REPORTED ARTICLES SIMULATED WITH 2 INPUT OR GATE

Supply Voltage in Volt	Parameters	Basic Domino Footless and Keeperless	Basic Domino Footless and with Keeper	Basic Domino Footed and with Keeper	Scheme on Paper [4]	Scheme on paper [5]	Proposed Scheme
1	Delay	1.57 E-11	2.40 E-11	4.109 E-8	1.23 E-9	1.04 E-9	3.2 E-10
	Power	3.33 E-5	3.32 E-5	5.6 E-6	4.58 E-5	5.6 E-8	1.33 E-8
0.9	Delay	1.78 E-11	2.69 E-11	4.10 E-8	1.28 E-9	1.05 E-9	2.76 E-10
	Power	2.39 E-5	2.39 E-5	9.6 E-6	3.20 E-5	8.58 E-8	3.26 E-8
0.8	Delay	2.08 E-11	3.13 E-11	4.11 E-8	1.32 E-9	1.06 E-9	3.67 E-10
	Power	1.62 E-5	1.62 E-5	2.80 E-5	2.20 E-5	1.49 E-8	3.70 E-8
0.7	Delay	2.52 E-11	3.82 E-11	4.00 E-8	1.35 E-9	1.09 E-9	4.24 E-10
	Power	1.01 E-5	1.01 E-5	1.14 E-5	1.39 E-5	1.39 E-8	3.10 E-8
0.6	Delay	3.29 E-11	5.04 E-11	4.01 E-8	1.42 E-9	1.15 E-9	6.54 E-10
	Power	5.56 E-6	5.56 E-5	1.4 E-5	7.81 E-5	1.44 E-8	2.02 E-8
0.5	Delay	4.90 E-11	7.73 E-11	4.16 E-8	1.58 E-9	1.31 E-9	7.20 E-10
	Power	2.44 E-6	2.46 E-5	1.4 E-5	3.50 E-5	3.1 E-8	5.50 E-8

TABLE II. COMPARISON OF OR GATE FOR PROPOSED DOMINO LOGIC WITH OR GATE DESIGNED WITH BASIC CIRCUIT AND OTHER REFERENCE CIRCUITS

OR-Gate fan-in	Parameters	Basic Domino Footless and Keeperless	Basic Domino Footless and with Keeper	Basic Domino Footed and with Keeper	Scheme on Paper [4]	Scheme on paper [5]	Proposed scheme
1-Bit	Delay	2.52E-11	4.22E-11	4.20E-08	1.54E-09	1.32E-09	5.71E-10
	Power	2.88E-05	2.87E-05	4.60E-06	4.28E-05	5.22E-08	2.33E-08
2-Bit	Delay	3.96E-11	6.86E-11	5.10E-08	1.98E-09	1.95E-09	6.56E-10
	Power	2.29E-05	2.29E-05	7.80E-06	5.30E-05	7.32E-08	2.26E-08
4-Bit	Delay	4.58E-11	6.99E-11	7.45E-08	3.12E-09	2.56E-09	7.47E-10
	Power	3.92E-05	3.92E-05	7.98E-06	5.25E-05	1.29E-07	3.10E-08
8-Bit	Delay	5.59E-11	7.79E-11	8.70E-08	5.46E-09	4.09E-09	8.32E-10
	Power	5.84E-05	5.84E-05	9.12E-06	7.42E-05	1.59E-07	3.42E-08
16-Bit	Delay	6.53E-11	8.23E-11	9.51E-08	7.52E-09	7.15E-09	9.74E-10
	Power	6.85E-05	6.83E-05	1.40E-05	8.81E-05	3.44E-07	3.76E-08
32-Bit	Delay	9.95E-11	1.95E-10	1.35E-07	1.58E-08	1.56E-08	1.20E-09
	Power	7.44E-05	7.43E-05	4.42E-05	9.72E-05	7.10E-07	5.47E-08

Fig. 8 compares the proposed circuit's power-delay product with the basic keeper, keeperless and footed footless schemes. Also it compares the PDP with recent proposed articles. The lowest line shows the proposed circuit's PDP at different V_{DC}. This can conclude that the proposed circuit shows least PDP then others.

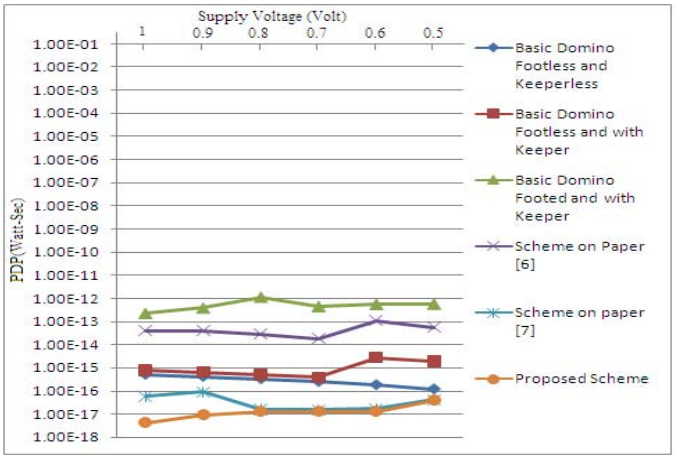

Fig. 8. Comparison of the PDP of the proposed circuit with other reference circuits and the basic circuits for different supply voltages

The circuit was being simulated for a fan-in of 1 bit to 32 bit OR gate and compared with the conventional basic CMOS domino logics i.e. footed and footless logics and also the keepered and keeperless logics. The OR-gate with different fan-in of the proposed circuit also compared to the previous reported domino logics and found to be having least PDP from others. Table 2 shows the delay and power dissipation comparison of the proposed logic with others. Fig. 9 shows the PDP comparison of all the logics and it can be seen that the proposed logic possesses lowest PDP.

TABLE III. UNG AND PERFORMANCE MEASUREMENT WITH DIFFERENT WIDTH OF M_2 FOR THE PROPOSED CIRCUIT AT 90 NM TECHNOLOGY FOR AN INPUT OF 2

Width of M2	UNG (normalized to VDD=1V)	Power	Delay
0.12 um	782	1.33 E-8	3.20 E-10
0.18 um	775	2.45 E-8	2.67 E-10
0.24 um	756	2.56 E-8	1.74 E-10
0.30 um	731	2.91 E-8	1.50 E-10
0.36 um	724	3.20 E-8	1.42 E-10
0.42 um	731	3.25 E-8	1.20 E-10

Transistor M_2 plays a crucial role in terms of leakage and performance of gate in the proposed scheme. Its high width improves the performance by making the speed more but penalty paid is less noise robustness and slightly more power consumption. Table 3 shows the UNG, power and delay measurements for various widths of M_2 which was simulated with 1 V and 90 nm technology.

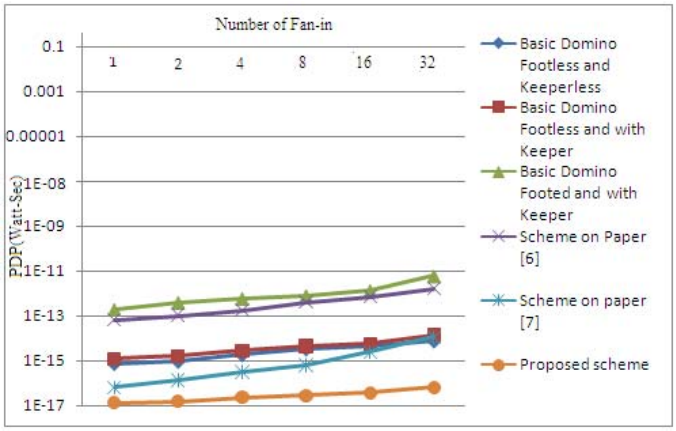

Fig. 9. Comparison of the PDP of the proposed circuit with other reference circuits and the basic circuits for different numbers of fan-in

VI. CONCLUSION

A new circuit scheme for the domino logic is proposed in this paper. The proposed circuit style is simulated nm CMOS technology for bulk CMOS model. Proposed scheme when compared with the recent proposals shows high power savings as well as less power-delay product with almost same noise immunity. With this circuit PDP can be increased by 100% of the recent proposed schemes. The proposed circuit can be used in design of high-speed embedded processors where low power consumption is an essential requirement.

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