Impact of Technology Scaling on the Minimum Energy Point for FinFET Based Flip-Flops

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***Abstract*—Analysis of FinFET based transmission gate (TG), sense amplifier (SA), and semi dynamic (SD) Flip-flops metrics are evaluated with technology scaling from 20nm down to 7nm technology node. The impact of supply voltage variation on delay, power, and energy is reported. The power delay product of Flip-flops is enhanced with technology scaling. The optimum supply voltage value at each technology node from minimum energy perspective is evaluated which is used by the industry to optimize logic and memory circuitry designs. For instance, considering the 7nm TG Flip-flop, the optimum supply voltage from energy saving point of view occurs at 0.65V. The work also characterizes each Flip-flop according to the obtained simulation results. SD Flip-flop has the best performance, however it exhibits high power consumption. TG Flip-flop is the best choice from power dissipation perspective, but it has high clock load. SA Flip-flop has a very useful feature of monotonous transitions at the outputs, which drives fast domino logic, however it might have glitches and it is the most vulnerable to soft errors**.

I. INTRODUCTION

Short channel effects (SCEs) and process variations are great challenges facing CMOS technology that leads to searching for emerging devices like FinFET and CNFET [1]. FinFET has a promising future to keep on the technology scaling trend for future generations of beyond 22 nm technologies [2]. FinFET devices offer superior scalability [3], lower gate leakage current [4], excellent control of short-channel effects [5], and relatively immunization to gate line-edge roughness [6]. The tri-gate FinFET provides a symmetric device architecture where the channel is controlled by gate from three sides of the Si film. Since the gate control is increased, the requirements on the Si film thickness are relaxed as compared to single gate or double gate MOSFET. Compared to FDSOI MOSFET or double gate FinFET, Tri-gate FinFETs are better due to the increased electrostatics controllability [7]. So we can efficiently control the short channel effects and also further scaling is possible to meet the ITRS [8] trends.

Flip-flops and latches are used as data storage elements, they are the basic building blocks of sequential logic circuits and digital circuits [9]. Flip-flop is an essential part of programmable logic devices (PLD), field programmable gate array (FPGA), and system on chip (SoC). Flip-flops also can be used for synchronization purposes.

Some studies have discussed analysis of predictive technology models (PTM) circuits with technology scaling [10-13]. For instance, a simulation study for PTM ring oscillator and basic logic gates is discussed [10]. Other studies have discussed analysis of process variations impact on Flip-flops. For instance, analysis of process variation impact on CMOS Flip-flops soft error rate is discussed [14]. In this work, we report supply voltage impact on four FinFET based Flip-flops topologies performance and power at different technology nodes starting from 20 nm down to 7 nm, and we determine the optimum supply voltage from energy consumption point of view at each technology node as the optimum supply voltage is used by the industry to optimize logic and memory circuitry designs.

This paper is organized as follows. Simulation setup is presented in Section II. Tri-gate FinFET based Flip-flops simulation results and discussions are presented in Section III. Evaluation of FinFET Flip-flops performance is presented in section IV. Some conclusions are drawn in Section V.

II. SIMULATION SETUP

In this paper, Low-standby power devices (LSTP) predictive technology models (PTM-MG) [15] based on BSIM-CMG for Multi-gate devices (Tri-gate FinFET) are used from 20 nm down to 7 nm technology node. A scaling strategy is adopted according to the PTM models which involves: scaling of the channel length (L), scaling of the supply voltage (V_{DD}), fin thickness (T_{fin}), and fin height (H_{fin}). For tri-gate FinFET devices the effective channel width is given by:

$$W = N_{fin}(2H_{fin} + T_{fin}) \quad (1)$$

We studied the performance and the power consumption of the Flip-flops topologies at room temperature within a supply voltage range from 0.5V to 1V with 0.05V step at technology nodes from 20nm down to 7nm. Pseudo-random sequence with equal probability of all transitions (data

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activity rate = 0.5) is considered in power consumption calculation to reflect average internal power consumption given the uniform data distribution.

PTM-MG used the published results from foundries such as Intel, TSMC, and IBM [16-19] to extract the fitting PTM parameters such as DIBL, sub-threshold slope by fine-tuning both primary parameters (Gate length, Fin thickness, Fin height, and Fin pitch) and secondary parameters (Gate work function, channel doping, source-drain channel coupling, and DIBL coefficient) [11] to match on-current and off-current of the published results.

For future technologies (Beyond 14nm) PTM-MG model cards are developed using ITRS as a reference. The off-current for 14nm technology node and below is expected to be (I_{off}=0.01nA/um for LSTP and 100nA/um for HP) according to ITRS trends [8]. The difference between ITRS off-current and PTM off-current impact on transmission gate flip-flop (TG-FF) metrics is evaluated and plotted in figures 1-2.

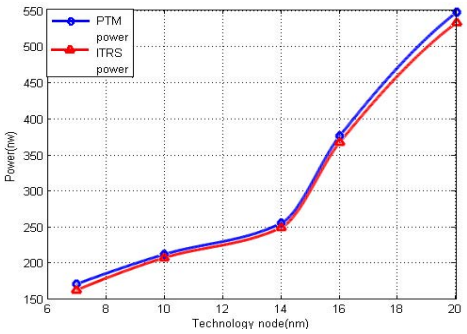

Fig 1. ITRS off-current and PTM off-current impact on TG-FF power.

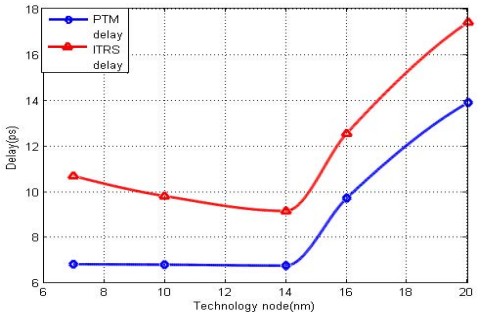

Fig 2. ITRS off-current and PTM off-current impact on TG-FF delay.

This means that simulation results using nominal PTM-MG parameters have slight deviation from fabricated devices with ITRS off-current. For instance, 7nm PTM TG-FF has power with 5% deviation from similar device with ITRS off-current.

III. TRI-GATE FINFET BASED FLIP-FLOPS SIMULATION RESULTS AND DISCUSSIONS

A. *Transmission gate Flip-flop (TG-FF)*

Transmission gate Flip-flop in Fig. 3 is simulated using device parameters listed in Table 1. Power delay product of transmission gate Flip-flop versus supply voltage at each technology node is drawn in Fig. 4.

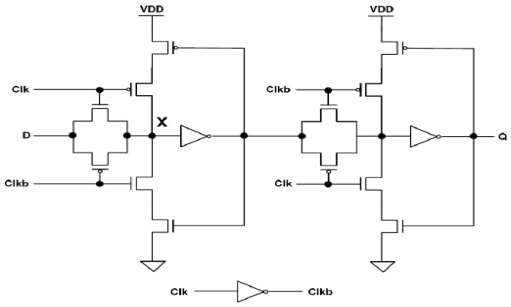

Fig. 3. Transmission gate Flip-Flop

Table 1: The simulated device parameters of TG-FF

Device	**TG-FinFET**				
L(nm)	20	16	14	10	7
T_{fin}	15	12	10	8	6.5
H_{fin}	28	26	23	21	18
N_{fin}	1	1	1	1	1

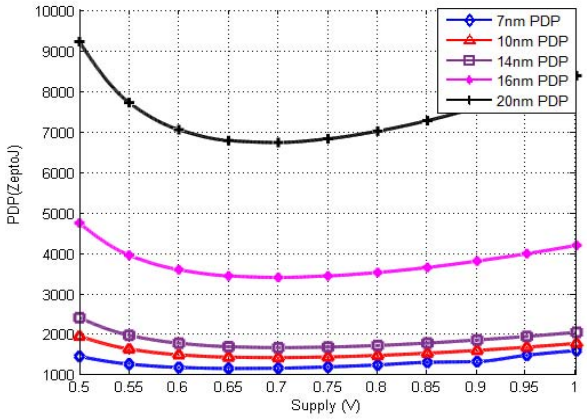

Fig. 4. TG-FF power delay product versus supply voltage with technology scaling from 20nm to 7nm node

From Fig. 4, the transmission gate Flip-flop optimum (minimum) power delay product (PDP) value at different technology nodes from 20nm down to 10nm occurs at 0.7V supply voltage. However, for the 7nm technology node at 0.65V supply voltage optimum power delay product is achieved. Figure (4) also shows that PDP trends of TG FF are improved with technology scaling.

B. *Sense Amplifier Flip-flop (SA-FF)*

Sense Amplifier Flip-flop shown in Fig. 5 is simulated using device parameters in Table 1 (with Nfin = 2 for pmos). Power delay product of SA Flip-flop versus supply voltage at each technology node is illustrated in Fig. 6.

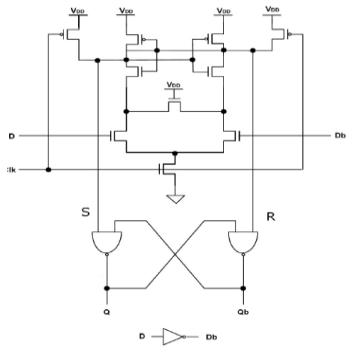

Fig.5. Sense Amplifier Flip-Flop

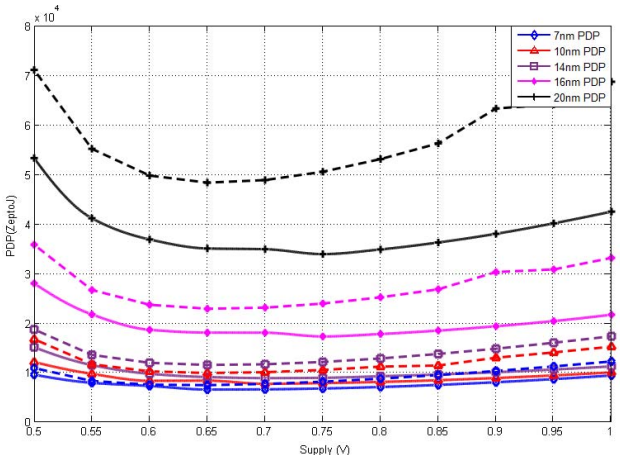

Fig. 6. SA-FF and SD-FF power delay product versus supply voltage with technology scaling from 20nm to 7nm node (the solid lines are for SA-FF, and the dotted lines are for SD)

From Fig. 6, sense amplifier Flip-flop optimum power delay product for technology nodes from 20nm to 16nm occurs at 0.75V supply voltage, however for technology nodes 14nm and 10nm it occurs at 0.7V supply, and for 7nm technology node it occurs at 0.65V supply. From the Figure we also can obtain that PDP trends of SA FF are enhanced with technology scaling.

C. Semi Dynamic Flip-flop (SD-FF)

Semi Dynamic Flip-flop shown in Fig. 7 is simulated using device parameters in Table 2. Power delay product of SD Flip-flop versus supply voltage at each technology node is illustrated in Fig. 6.

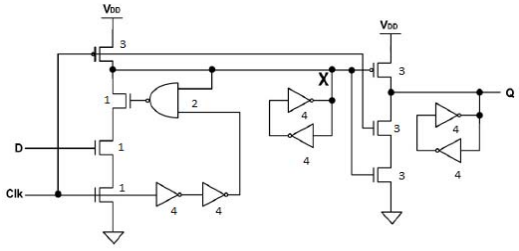

Fig. 7. Semi Dynamic Flip-Flop

Table 2: The simulated device parameters of SD-FF

Device	**TG-FinFET**				
L(nm)	20	16	14	10	7
H_{fin}	28	26	23	21	18
N_{fin} (1)	25	22	22	18	15
N_{fin} (2)	7	6	6	5	4
N_{fin} (3)	5	4	4	3	3
N_{fin} (4)	1	1	1	1	1

Observing SD Flip-flop energy, semi dynamic Flip-flop optimum (minimum) supply voltage from power delay product (energy) perspective for technology nodes from 20nm and 7nm occurs at 0.65V. SD Flip-flop PDP trends also decrease with technology scaling.

IV. EVALUATION OF FINFET FLIP-FLOPS PERFORMANCE

We evaluated Tri-gate FinFET based Flip-flops performance according to many factors and metrics such as:

1. Soft Errors Rate

This minimum value of the charge collected (Qcollected), is called a critical charge (Qcritical) which can be used as a measure of memory element vulnerability to soft errors. Qcritical can be modeled as a measure of the SER for different flip-flops topologies. The recombination of the collected charges results in a very short duration current pulse which might cause soft error [14].

The critical charge is calculated at all nodes of each flip-flop for the 1-to-0 flip and the 0-to-1 flip at the output node. Then, the node that has the smallest critical charge is selected as the most susceptible node to soft errors (Node X in Fig. 3, and Fig. 7, and S in Fig. 5). Soft Errors Rate (SER) of the different four Flip-flops types at the nominal supply voltage of each technology node is reported in Table 3.

Table 3. Soft errors rate in different Topology (In coulombs)

Tech. node	20nm	16nm	14nm	10nm	7nm
Nominal supply	0.9V	0.85V	0.8V	0.75V	0.7V
TG	1.25f	1.25f	1.25f	1f	0.75f
SA	0.25f	0.25f	0.25f	0.25f	0.25f
SD	2.5f	2f	2f	1.75f	1.25f

From Table 3, the sense amplifier (SA) Flip-flop is the most vulnerable Fip-flop to soft errors, while semi dynamic (SD) Flip-flop is the least vulnerable Flip-flop to soft errors. Also technology scaling impact on SER of FinFET exhibits a similar trend to CMOS technology (SER is decreased with technology scaling in both of CMOS and FinFET).

1. Operations Delay

Delay (Clk-Q) is an essential parameter in evaluating the performance of Flip-flops. Our study shows that Flip-flops performance is enhanced with increasing the supply voltage,

for 7nm TG Flip-flop increasing the supply voltage from 0.5V to 1V the performance is enhanced by a factor of 3.14 of its value at 0.5V.

2. *Power consumption*

The power is continuously decreasing with scaling down the technology as a result of shrinking the channel length and the scaling of the supply voltage.

The study also shows that Flip-flops power dissipation is increased with increasing the supply voltage, for 7nm TG Flip-flop the supply voltage from 0.5V to 1V the power dissipation at 1V supply voltage is 4.55 times its value at 0.5V.

3. *Power Delay Product*

By observing power delay product trends with technology scaling, we can get the optimum supply voltage for each Flip-flop topology with technology scaling from 20nm to 7nm. The study also shows that PDP of each Flip-flop topology is enhanced with technology scaling.

4. *Design Insights*

In this section we recommend each Flip-flop for a specific application according to the obtained simulation results (Not listed) such as:

Semi dynamic (SD) Flip-flop is the fastest one of the four types, also it has negative setup time, so it is very good choice for high performance systems (within available power budget), however it is the most power consuming and has hold time.

Transmission gate (TG) Flip-flop is the least power consuming compared to the other Flip-flops, it has positive setup time and small clock to output delay and it has the minimum number of transistors compared to other two types, however its Clock load is high.

Sense Amplifier (SA) Flip-flop has a very useful feature of monotonous transitions at the outputs, which drives fast domino logic; however its rise and fall times not only degrade speed but also cause glitches in succeeding logic stages, which increases total power consumption. SA-FF is the most vulnerable Flip-flop to soft errors. The reason for that is due to its small flipping time [14]. The least vulnerable Flip-flop to soft errors is SD-FF.

V. CONCLUSION

The performance of FinFET Flip-flops is evaluated with technology scaling. The impact of supply voltage on basic performance metrics is reported. The results show that, TG, SA, and SD Flip-flops have better performance and power with technology scaling, also the optimum supply voltage from energy saving perspective for each technology node is reported. The study also shows SER values for each Flip-flop topology with technology scaling.

Some design insights and Flip-flop choice recommendation are obtained and reported. For instance, SD FF is the best choice for high performance designs. From power consumption point of view, TG-FF is the best choice since it is the least power consuming Flip-flop among the three discussed topologies.

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