Multiphase Pipelining in Domino Logic ALU

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***Abstract*— Background/Objectives: Domino Logic is extensively used in high performance microprocessor designs. The conventional pipelining of domino logic designs are more prone to timing overhead due to the factors, namely, clock skew, delay caused by the latches, and its inability to borrow time.**

Methods/Statistical analysis: The cascaded pipelined domino stages utilizes two and four phase clocks for sequencing the operation.The pipelined stages are sensitive to clock edges, and are incapable of borrowing time. Hence, latches are included between the consecutive stages to facilitate the pipeline. Considering the required computation time of the circuit, the speed enhancement in a domino logic pipelined circuit could be achieved by reducing the precharge and evaluation period.

Findings: In this paper, four phase self-timed clocking scheme is implemented on a pipelined domino logic ALU. In addition to the maximum computation time of an individual stage, the setup and hold time are also considered for defining the clock evaluation time in the four phase scheme. Furthermore, it is ensured that the precharge operation happens only after the previous output is passed on to the next stage. The analysis and comparison of the conventional pipelined domino circuit design,the skew tolerant self timed pipeline design of an inverter chain and the ALU, using two phase and four phase overlapping clocks are done using Cadence® Virtuoso Spectre employing 180nm technology library and analyzed in the ADE-L environment.

Improvements/Applications: The skew tolerant self-timed design of the domino logic pipelined ALU demonstrates an increased speed of 60% and reduction in power of 30% as compared to the single phase pipelined ALU design.

Keywords: Domino Logic Arithmetic Logic Unit (ALU), Clock Skew in Domino Logic, Pipelined ALU, precharge, Pipelined Domino, Self-Timed Domino

1. INTRODUCTION

The increasing demand for high performance processor had led to the design of high speed Arithmetic logic unit (ALU). The instruction level parallelism is one factor which facilitates to achieve faster throughput. The instruction execution is broken into series of operations, and performed in a sequential manner. This enables more number of instructions to be executing various operations. This results in parallel processing of multiple instructions.

Domino logic designs are a good choice to obtain high speed with less transistor count. The domino logic comprises the pull-up network (PUN) consisting of single precharge PMOS transistor and the pull-down network (PDN) consisting of the evaluation block and a footer transistor. The precharge transistor and the footer transistor are driven by the clock signal. In general, the cascading of domino logic structures is implemented using a single phase clock. The clock is made available for the consecutive stages after the computation time of the previous stages. This is accomplished by providing delay using buffers in the clock path. Hence, the clock arrives to the subsequent stage after the computation is completed in the previous stage. This leads to increased delay and increased area owing to the delay circuitry. To overcome this drawback, pipelining is implemented using two and four phase clocks. Considering a microprocessor design, the entire sequential operation hinges on the clock pulses used to control and streamline the operation. Hence, to obtain a faster response, various clocking schemes are devised with different domino logic circuit designs in a microprocessor[1, 2, 3]. Fast computation of a processor can be achieved by deploying the clock signals in an overlapped manner. Thus, the performance is improved by carefully choosing the clocking schemes and clocking parameters such as the period, pulse width and overlap time. Various constraints on precharge and evaluation period of the clock due to clock skew, clock jitters and delay in clock also are needed to be ensured.

In this paper, the design of a pipelined ALU using single rail domino logic style is performed and analyzed under various clocking schemes. The overlapping clock phases are utilized to enable the pipelined architecture. The clock distribution network of a pipelined architecture takes the benefit of clock skew by utilizing the clock in an overlapped manner.

Section 2 details a conventional pipelined domino circuits using latches between consecutive stages, utilizing two and four phase clocking schemes. Section 3 details the domino circuits utilizing overlapping clock phases and the skew tolerant design of domino logic. Section 4 details the constraints to be imposed during precharge and evaluation period of the clock, while designing the skew tolerant design. Section 5 represents the skew tolerant mechanism implemented in a pipelined ALU. Section 6 analyzes the performance benefits of skew tolerant pipelined domino design with respect to the traditional pipelined domino using various clocking schemes. Section 7 summarizes the timing results of pipelined domino ALU structure.

978-1-5090-5913-3/17/$31.00

2. Conventional Pipelined Domino Logic Design

The pipelining technique accelerates the computation of data in the digital processors. The minimum clock period (**Tmin**) required to ensure accurate evaluation is given as in Eq.1

$$\mathbf{Tmin} = \mathbf{tcq} + \mathbf{tpd,logic} + \mathbf{tsu} - \mathbf{tskew} \quad (1)$$

where **tcq** is the propagation delay of latch (clock to output), **tsu** is the setup time of the pipelined stage , **tskew** is the clock skew and **tpd,logic** is the worst case combinational logic delay. The clock skew is caused by mismatches in the arrival time of the clock and affects the functionality of the sequential circuits[4]. The setup time is the minimum amount of time that the data should be steady before the clock occurs. This ensures that only the reliable data is sampled by the clock which will be used in the next stage. The hold time (**thold**) is the minimum amount of time during which the data must be held stable after the arrival of clock, and this ensures valid transfer of data to the next stage. Hence, for accurate computation, the constraint stated in Eq.2 needs to be satisfied to ensure correct data transfer to the next stage.

$$\mathbf{tskew} < \mathbf{tcq} + \mathbf{tpd,logic} - \mathbf{thold} \quad (2)$$

In the conventional domino clocking scheme with ideal clock, the evaluated output is held in a latch before the precharge of the consecutive stage. [Figure.1] depicts the timing diagram of an ideal two phase clocking scheme where the circuit is triggered with two clock signals.

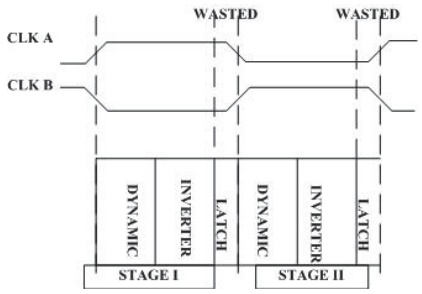

Figure 1. Timing diagram of Pipelined domino logic with ideal clock

Each stage of the domino circuit comprises of the dynamic circuit for computation of the functionality followed by an inverting circuit. The evaluated output is then retained in a latch to make it available for the next stage. As the clock signal is prone to skew, irregular clock distribution network, clock loading and cross die process variation as shown in [Figure.2], an increased clock time period needs to be defined in reality[5]. This necessitates having longer clock period and hinders the operating speed.

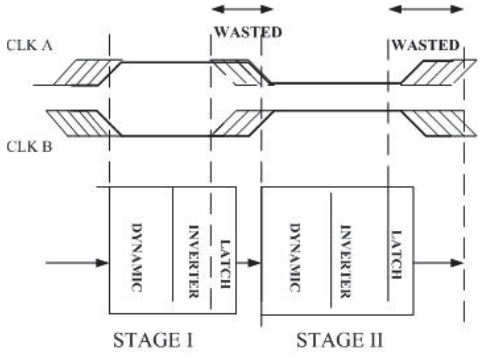

Figure 2. Timing diagram of Pipelined domino logic with clock skew

The first stage starts the evaluation at the rising edge of the clock A (evaluation phase) and it is needed to complete the execution before the setup time of the next stage. The subsequent domino stage starts computing during the evaluation phase of the second clock signal B. The previous stage output must be ensured for stability before clock B arrives at the subsequent stage. This imposes certain conditions on the evaluation period for reliable operation. The evaluation period (**Teval**) is decreased by clock skew, since clocks of different phases may arrive early or late. To be precise, the time available for the logical evaluation is $\mathbf{Teval - 2\ X\ tskew}$ where T is the time period of clock[6].

2.1 Two Phase Conventional Pipelining

[Figure 3] depicts the timing of a two stage pipelined conventional domino circuit using two phase clock. During the HIGH of the first clock (CLK A) i.e., during the evaluation phase, the stage 1 evaluates. The output is stored in a latch at the end of the evaluation period. Subsequently, while the second clock B arrives, the stage 2 evaluates considering the output of the first stage. The stage 1 is also precharged by the CLK A during the same time. This makes the stage 1 ready for the next evaluation. Thus, the two stages are continuously busy and the waiting duration for the previous stage output is eliminated.

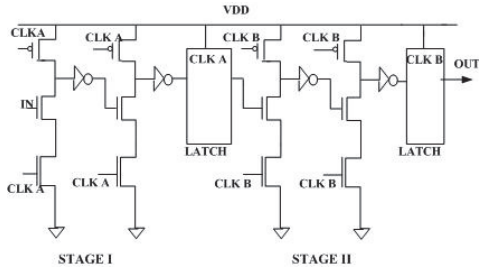

Figure 3. Structure of conventional pipelining using two phase clock in Domino buffer chain

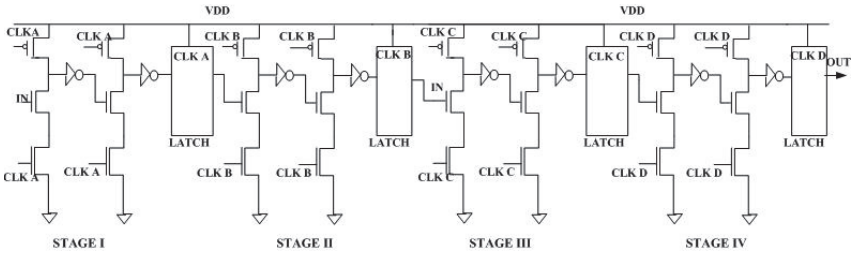

Figure 4. Structure of conventional pipelining using four phase clock in Domino buffer chain

2.2 Four Phase Conventional Pipelining

In the four stage conventional pipelining method, four instructions are available in the pipeline stall at all times as shown in [Figure 4]. Thus, all the stages perform their task simultaneously without relying on the input from the other stages and store the result in the corresponding pipelined latch, and again proceed to precharge. The major drawback in the conventional pipelining is that more time is elapsed in storing the output in the latch of the respective stage rather than utilizing the time in logical evaluation. Thus, the self-timed skew tolerant pipeline has become a better alternative solution in alleviating this problem.

3. Self-Timed Pipelining

In the skew tolerant self-timed pipelining, the clocking is scheduled in such a way that the domino logic stages are ready with the data for evaluation. The clock constraints are taken into consideration while determining the minimum time required for the evaluation. In this, the precharge of a stage is hindered, till the output is fed to the next stage. Thus, the two and four phase overlapping clocks with clock constraints enable the reliable evaluation of the functionality of the design as shown in [Figure 5] and [Figure 6].

At the interface of two stages of different clock phases, the subsequent stage will start its evaluation only when the previous stage output becomes stable. This necessitates defining skew at the interface, in case of delayed arrival of the output from the previous stage. By deploying the clock in an overlapping manner, the problem of sequencing overhead is eliminated in the self-timed pipeline[7].

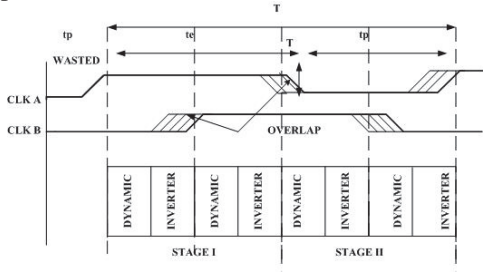

Figure 5. Timing diagram of two-phase overlapped clock for domino circuit

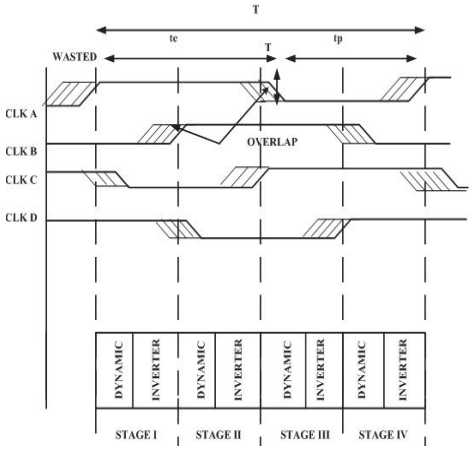

Figure 6. Timing diagram of four-phase overlapped clock for domino circuit

3.1 Two Phase Self Timed Pipelining

A two stage self-timed pipelining is as shown in [Figure 7]. In this, the first stage starts evaluating as the HIGH pulse of clock A arrives. Before the completion of evaluation of the stage 1, the HIGH clock for the next stage arrives enabling the evaluation of the stage 2. Thus, there is an overlapping of evaluation phases for two consecutive stages. This avoids the necessity for latches between the two stages, and makes the data available for the subsequent stage. The overlapping time is considered as the time borrowed from the previous stage clock period and also it includes the skew of the clock.

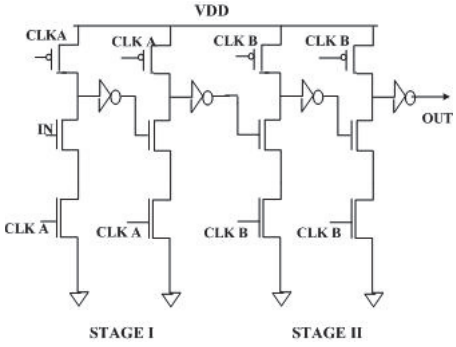

Figure 7. Two phase self-timed pipeline in domino logic buffer circuits

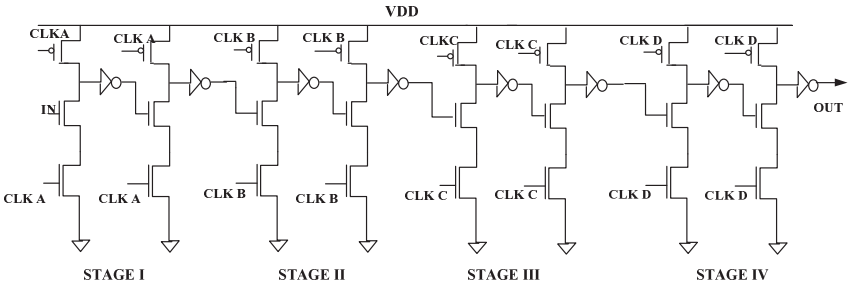

Figure 8. Four phase self-timed pipeline in domino buffer circuits

3.2 Four Phase Self Timed Pipelining

The four phase self-timed pipelining is implemented by deploying overlapped four clock signals as shown in [Figure 8]. The pipelined stages operate by borrowing time from the previous stage. Therefore, the critical path does not include the latches and leads to faster computation. Due to the clock skew, the clock loading effect and cross-die process variations, various constraints are needed to be imposed as elaborated in the following section.

4. Clock Constraints:

In a synchronous design, the clock pulses are fed to millions of devices to harmonize the events. While configuring the clock schemes, it is also mandatory to evaluate the extent to which a circuit cannot be synchronized. To synchronize the clocks and obtain correct output, clock tolerance is to be calculated before deploying. In the four phase clock schemes, four clock signals of same duty cycle but of different phases are deployed.

4.1 Precharge Constraints

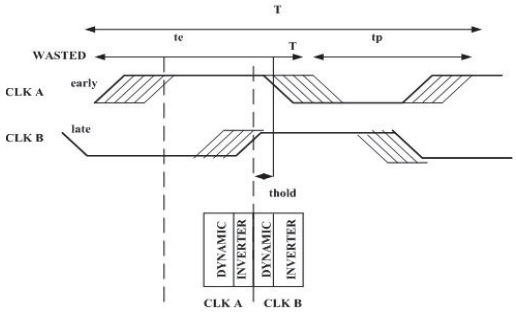

Figure 9. Precharge time constraint

In a four phase clocked circuit, the next phase of the clock signal rises after T/4 of the previous clock phase. The **tp** (precharge period) is limited by the rate at which the stages precharge to a HIGH logic. The consecutive stages of the pipeline design needs to be considered while determining the precharge period. A particular stage must be fully pre-charged before it enters into the evaluation phase. In a pipelined design, the clock CLK A may arrive late and CLK B may arrive early. Therefore, to guarantee a complete precharge of the circuit

$$\mathbf{tp} \geq \mathbf{tprech} + \mathbf{tskew} \tag{3}$$

Precharge time constraint is represented as in [Figure 9].

4.2 Evaluation Constraints

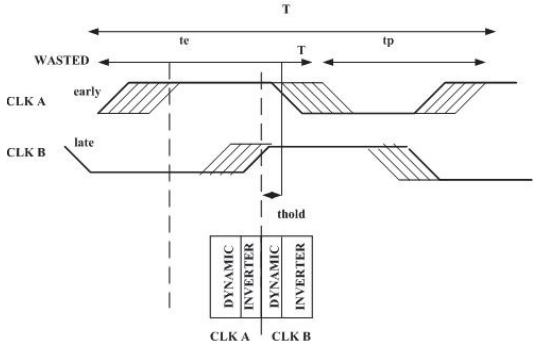

Figure 10. Evaluation time constraints

For reliable operation, the overlap in two consecutive stages is incorporated during the **te** (evaluation period) of the clock. The evaluation time is dictated by the time till the subsequent stage takes the output of the previous stage and the overlap time between two phases i.e.(**thold** + **tskew**)[5]. Hence the evaluation time is defined as in [Figure 10] and is given by Eq. 4.

$$\mathbf{te} \geq \frac{\mathbf{T}}{\mathbf{N}} + \mathbf{tskew} + \mathbf{thold} \tag{4}$$

Where N is the number of overlapping clock period, **thold** is the hold time of the clock, **tskew** is the clock skew, T is the period of clock. Irrespective of the design and the number of stages in the pipeline, the maximum tolerable skew needs to be calculated[5]. Hence, combining the constraints of precharge and evaluation time in Eq (3)

and Eq.(4) the maximum allowable skew is defined as in Eq.(5).

$$t_{skew} - max = (\frac{N-1}{N} - t_{hold} - t_{prech})/2 \qquad (5)$$

For large period (T) and N, the maximum tolerable skew can approach to T/2. If the valid skew between two phases exceeds the maximum skew, the pipelining operation fails to operate in the particular frequency, irrespective of the speed of the gates employed within the pipeline stage.

5. Pipelining In ALU by Strategic Time Borrowing

The arithmetic logic unit (ALU) is the basic building block of any microprocessor for performing arithmetic and logical operation. The ALU comprises of instruction unit, decoding unit and arithmetic unit and logic unit as shown in Figure 11. The instruction unit fetches the instruction and enables the computation and register selection depending on the opcode. The second unit decoder identifies the operand location and the operation to be performed. Thus, the computation of the specified data gets executed and the result is written back into register.

In a single cycle data path microprocessor design, the flow of the data through the various stages happens with in a cycle and gets completed as shown in **[Figure 11].** However, higher clock rate operation may not be possible as few instructions may require more computation time. Hence, the clock period is determined by considering the maximum computation time of the block among the entire circuitry in the ALU. The major drawback of the single cycle processor is the poor resource utilization, and there are some instructions which are impossible to implement.

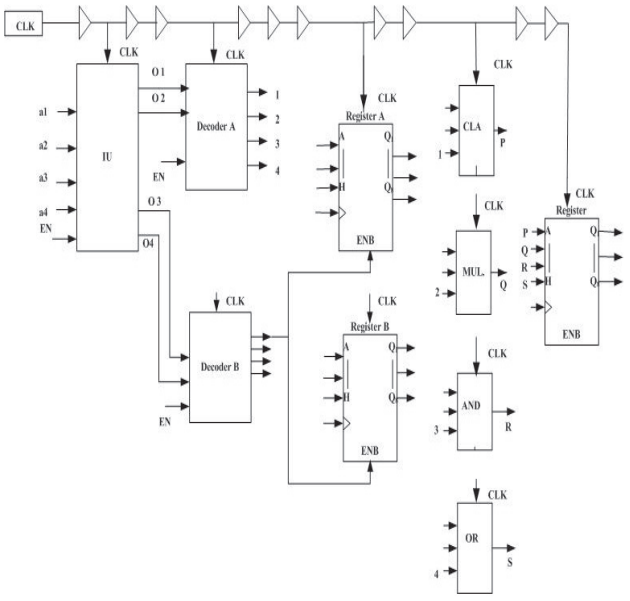

Figure 11. Single phase execution of ALU

To get rid of this problem, the four phase self-timed ALU is proposed in the paper. The units of ALU such as the instruction register, the instructor decoder, the operational block and the output registers are governed by four different phases of clock. The four phase pipelined design supports increased clock frequency rate. This is achieved as it is specific to each micro operation of a particular stage. The hardware and timing is also reduced to a greater extent. In the conventional four phase pipelining, the latches are inserted between the stages to store the result. The consecutive stages are evaluated on the arrival of clock phases, and the result is stored in pipelined latches.

More time is wasted in the pipelined latches during the evaluation of the four phases pipelined circuit design. Hence the latches can be removed from the critical path with the help of overlapping clocks. The overlapping of clock is one methodology of the self-timed pipeline where the timing of the clocks is appropriately fixed. It needs to be ensured that the next stage should start evaluating before the precharge of the previous stage. The self-timed four phases pipelined ALU is as shown in [Figure 12].

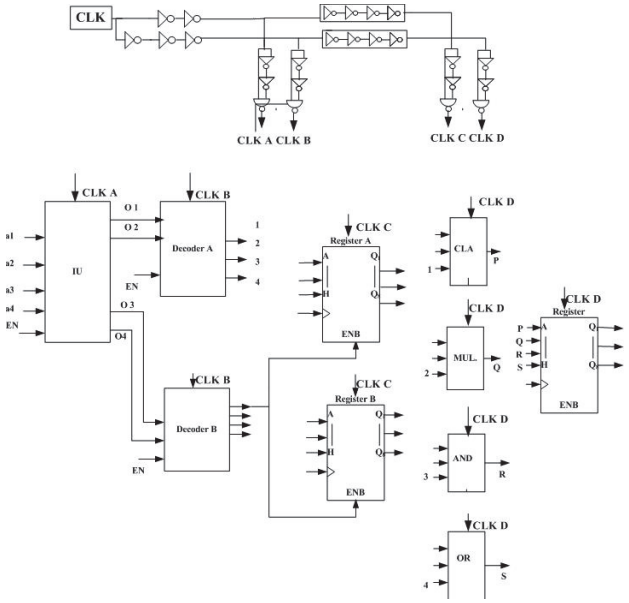

Figure 12. Four phase pipelining in execution unit of ALU

A skew tolerant pipelined ALU is designed and a comparative study has been done between single cycle and multi cycle pipelining. The static timing analysis is done to configure the phase of the clocks of the pipelined ALU. Initially, the computation delay of each stage is calculated. Furthermore, the analysis of the set up time and hold time of each block of the ALU is used to configure the period and phase of the clock[8]. The slack available in each clock phase is used as the borrowed time

between the stages and to limit the clock skew between the two clock phases. The positive slack is ensured at all stages, so that the circuit can operate at much higher frequency[9].

6. Analysis of four phase pipelined ALU Design:

The simulation of all sub blocks of ALU design is carried out using EDA tool Cadence® Virtuoso-64 using gpdk 180nm technology library and analysis is carried out using Spectre. The ALU design contains instruction register, instructor decoder, arithmetic and logical units, and registers to store the result. The four bit instruction is fed to the instruction register. The two units of the decoder unit are used to identify the operand location and the operation to be performed by the instruction. The decoder activates the registers containing the operands, and the corresponding arithmetic or logical unit. The ALU design contains a two bit array multiplier. Array multiplier is less complex, easily scalable, easy to place and route and easy to pipeline. The four bit adder unit is a carry-look-ahead (CLA) adder. It improves the speed by reducing the amount of time required to determine carry bits. The logical units of the ALU design comprise of the four input NAND and OR gate. The computation of the specified data gets executed in respective ALU unit and the result is written back into register.

Table 1. Conventional Vs. Skew Tolerant Pipeline of Cascaded Domino Logic Gates

Pipelined circuits	Conventional Vs. Skew Tolerant Pipeline in domino buffer circuits		
	Computation Time	*Avg.Power*	*PDP (Power Delay Product)*
Single phase pipelining	127ps	23.51uw	2.921E-15
Two stage conventional pipelining	343ps	89.05uw	30.544E-15
Two stage overlap pipelining	87.02ps	367.4uw	31.971E-15
Four stage conventional pipelining	795ps	2.9mw	2.31E-12
Four stage overlap pipelining	443ps	1.38mw	611.34E-15

The computation time and the average power dissipation of single, two phase and four phase pipelined domino logic stages is tabulated in **[Table 1].** The pipelined circuits show better performance in terms of speed and power consumption. Therefore, the power delay product (PDP) is minimal indicating the efficiency of the design. **[Table 2]** depicts the precharge constraints to be imposed with N number of clock overlap to determine the minimum time period required for right operation of the design.

Table 2. Precharge Constraints

N (overlap)	Precharge Constraints
	T_{prech}
2	246Ps
3	244ps
4	242ps

To determine the minimum time required for each unit to execute the operation, the computation time and the average power dissipated of each block of the ALU design is computed as given in [**Table 3]**. Furthermore, the set up time and hold time of each block of ALU is used in determining the period and phase of clock. Initially, the ALU design is simulated using a single phase clock. The time period of the clock is based on the maximum computation time as required by sub blocks of the ALU design. The ALU design is also triggered using four phase clock in an overlapped manner. The performance of the four phase self-timed pipelined ALU design is compared with the single phase ALU design. The total computation time and the average power of the four phase self-timed pipelined ALU design and single phase ALU design is shown in **[Table 4]**.

Table 3. Computation Time Of Different Blocks Of ALU Execution Unit

Stages	ALU Units	Computation time	Average Power
Stage I	Instruction Register	217ps	4.99mw
Stage II	Decoder	49ps	6.41uw
Stage III	4 I/P NAND	189.1ps	2.84uw
Stage III	4 I/P OR	132.4ps	124.69uw
Stage III	4 bit Carry look ahead Adder	200.4ps	164.6uw
Stage III	Two Bit Multiplier	107ps	19.87uw
Stage IV	Storage Register	217 ps	4.99mw

Table 4. Computation Time and Average power dissipation ff ALU design in single phase and four phase pipelined circuits

S.No.	ALU Design	Computation Time	Average Power
1	Single Phase ALU	6.50ns	4.98mw
2	Four Phase ALU	1.569n	2.56mw

7. CONCLUSION

A domino logic four stage buffer circuit is pipelined in two and four phase clock in a conventional method and self-timed skew tolerant method. The computation time is reduced by 70% in the case of two stages overlapping pipelining and it realizes a reduction of 44% in case of four stages overlapping pipelining as compared to conventional pipelining. The performance of the four phase self timed domino logic ALU demonstrates 60% increase in the speed and power is reduced by 30% in comparison with the single phase pipelined ALU execution unit. The various units of ALU are designed using domino logic and the maximum computation time of the individual unit, the setup and hold time are considered in defining the clock evaluation time for the four phase clocks.

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