Design and Simulation of Low Power Dynamic Logic Circuit Using Footed Diode Domino Logic

Sujeet Kumar, Sanchit Singhal, Amit Kumar Pandey and R. K. Nagaria

Abstract— **In this paper, we proposed a new technique to reduce power dissipation for domino logic circuits. In this proposed circuit we put a diode on the foot of domino logic circuit which results in power reduction as compared to reported and conventional domino logic. We are using NMOS as a diode and due to this extra diode (NMOS), in precharge period leakage current reduce due to stacking effect. For simulation we are using cadence spectre tool at 180nm CMOS technology and comparison between conventional, reported & proposed logic styles has been done. The result of simulation shows an improvement of 72% and 41% power as compared to the standard conventional domino logic & pseudo dynamic buffer based domino logic.**

Index Terms— **Dynamic logic, Low power domino logic, Footed diode, CAD tool.**

I. INTRODUCTION

Low power and high speed logic design circuits[1-3] continue to get more attention in consideration of product manufacturing. So now a day's power saving has more importance than any other thing. Dynamic logic circuits came into the picture because of power efficient circuitry. Domino logic circuits are more power efficient and cooperatively faster, so these circuits have almost half the transistor count with respect to complementary static circuits. Domino logic is basically a dynamic logic circuit followed by a static inverter and having a capacitor as a load. The clock signal is used to control the operation of domino logic circuit [4]. The output of the dynamic logic circuit is stored in the parasitic capacitance which is located just before the static inverter [5]. The parasitic capacitance just stores the output voltage and passes it to the next state which is the output stage of the domino circuit and stored in the load capacitor [4]. The dynamic logic circuit requires two phases. The first phase, when Clock is low, is called the precharge phase and the second phase, when Clock is high, is called the evaluation phase [5]. In the setup phase, the output is driven high unconditionally (no matter the values of the inputs). The capacitor, which represents the load capacitance, becomes charged. Because the transistor at the bottom is turned off, it is impossible for the output to be driven low during this phase. During the evaluation phase, Clock is high. In the precharge phase also extra noise introduced to the dynamic circuit [6].

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978-1-4673-5630-5//13/$31.00 ©2013 IEEE

To avoid the introduced noise TSPC based dynamic logic circuits [7] are used which disabled the buffer during the precharge phase, but an extra clock transistor used in the output stage static inverter [9]. Due to this extra transistor load capacitance also increases by which more power dissipated during the precharge phase. A reported work dynamic logic design using pseudo dynamic buffer [8] has been done, in their circuit when the circuit is in the precharge phase, precharge pulse is blocked at input of the buffer and stopped from being passed to the domino gate, and as a result power is saved during the precharge pulse [11-14]. To reduce more power subsequently in the precharge phase we proposed a diode footed dynamic clock controlled circuit. Using this diode footed dynamic structure; precharge pulse is blocked & prevented to pass through the buffer. So, during the precharge phase more power saved as compared with reported work, as a result our proposed circuit is more power efficient in comparison with reported and TSPC based dynamic logic design.

II. DIODE FOOTED BASED DOMINO LOGIC

A. Conventional domino logic

Conventional domino logic consists of a dynamic gate followed by a static inverter. Generally, the dynamic gate used is of n-type and called pull down network. The logic gate operated under two conditional phases called precharge phase & evaluation phase respectively. Clock signals are used to control the operation of domino logic circuit, when the clock pulse goes high the logic circuit is operating under the evaluation phase and when the clock pulse goes low then it operates under precharge phase.

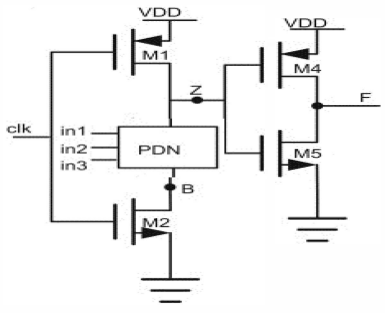

Fig. 1. A conventional domino buffer.

Under precharge phase when clock is low, PMOS M1 is on and a dynamic node named as Z is charged up to V_{DD}. During evaluation phase clock NMOS transistor M2 is on and PMOS M1 is off. So it is up to input combination whether the node Z is isolated from ground or not. In evaluation phase when input combination is high then dynamic node Z is directly connected

to ground so it will discharge to zero [10]. Fig.2. shows the timing diagram of conventional domino logic. In the timing diagram precharge pulse propagation from dynamic node Z to output node shown, the precharge phase when clock pulse is at low level.

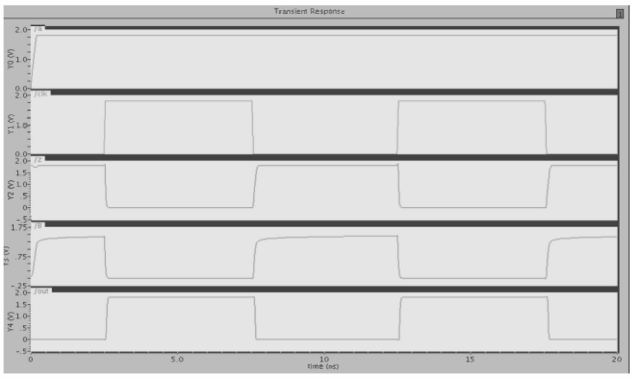

Fig. 2. Timing diagram of conventional domino buffer when input A= '1'.

B. *TSPC based dynamic logic circuit*

Fig.3. shows the schematic structure of TSPC based dynamic logic circuit [7]. This circuit uses three clock transistors to operate so the load capacitance is increased due to this. In this circuit a node Z is denoted which is referred as the dynamic node, during precharge phase when clock goes low M6 transistor in fig,3 turned off so, at the output node no change experience by the circuit.

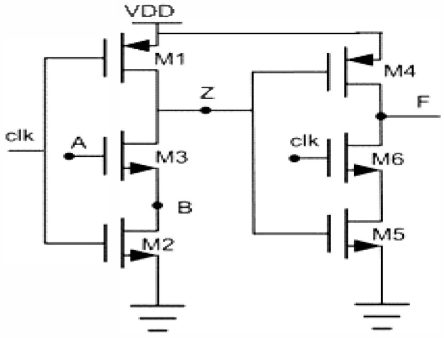

Fig. 3. A TSPC based dynamic logic buffer.

In TSPC based dynamic circuit we avoid the precharge pulse propagation during precharge phase at the cost of one extra clock transistor due to which this circuit suffers from larger power consumption[9].

C. *PDB based domino logic*

In TSPC based dynamic logic during precharge phase more power is consumed, so to avoid this extra power consumption a reported work dynamic logic design using pseudo dynamic buffer has been done. We have taken an example of PDB based buffer [8] shown in the fig.4.

In the fig.4. source of NMOS transistor M5 is connect to node B instead of GND. So, during the precharge phase when clock pulse is kept low, the value of dynamic node Z cannot propagate to the output node because the NMOS clock transistor m2 is disabled. In the circuit when input A is low then dynamic node Z is always high and output is kept low regardless of operating phase. When input A is high then circuit will efficiently operated under two phases namely precharge and evaluation [9].

- Evaluation phase- in this phase when clock pulse is kept high then the PMOS transistor M1 is turned off and NMOS transistor turned on so, the dynamic node Z discharge through node B that's why output node became high.
- Precharge phase- in this phase when clock pulse is kept low then PMOS clock transistor m5 is turned on and dynamic node Z is charged to V_{DD}. The output is still high because the clock pulse turns off the transistor M2 so output node is not able to discharge.

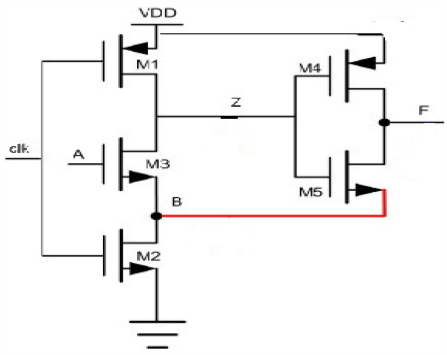

Fig. 4. A domino buffer using pseudo dynamic buffer.

In fig.5. We have shown the timing response of PDB based buffer at 25fF load capacitance.

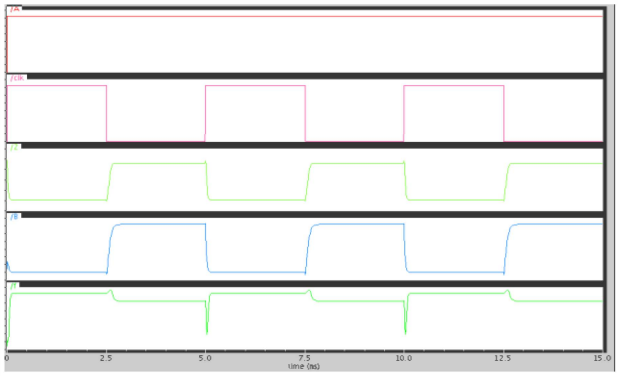

Fig. 5. Timing diagram of conventional domino buffer when input A= '1'.

D. *Proposed diode footed based domino logic*

In the previous section we monitored the performance degradation of circuit due to propagation of precharge pulse from dynamic node to the output node. The PDB based design [8] for domino logic compensates this problem up to some extent but there is always a room for improvement. In our proposed circuit we put an NMOS transistor which is working as a diode in between GND and M2 clock transistor. Let us take an example of a diode footed buffer shown in the fig6. In the circuit shown in the fig.6 the source of the NMOS

transistor m5 is connected to the node B instead of the GND. An NMOS transistor is introduced in the circuit whose gate is shorted with its drain and connected to the source of the NMOS clock transistor M2, the source of NMOS transistor M6 is connected to ground. In the circuit when input A is low then dynamic node Z is always high and output is kept low regardless of operating phase.

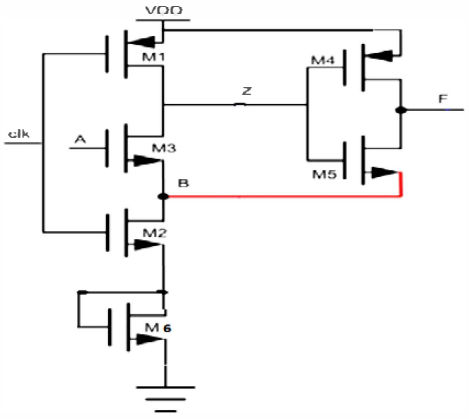

Fig. 6. A proposed domino logic buffer using footed diode.

When input A is high then circuit will efficiently operate under two phases namely precharge and evaluation [9].

- Evaluation phase- in this phase when clock pulse is kept high then the PMOS transistor M1 is turned off and NMOS transistor is turned on so, the dynamic node Z discharges through node B and therefore output node became high.
- Precharge phase- in this phase when clock pulse is kept low then poms clock transistor M5 is turned on and dynamic node Z is charged to V_{DD}. The output is still high because the clock pulse turns off the transistor M2 so, M6 is also off and therefore output node is not able to discharge. Due to stacking effect power is compensated.

In the Fig.7. We have shown the transient analysis of proposed buffer at 500 MHz clock frequency and 1fF load capacitance.

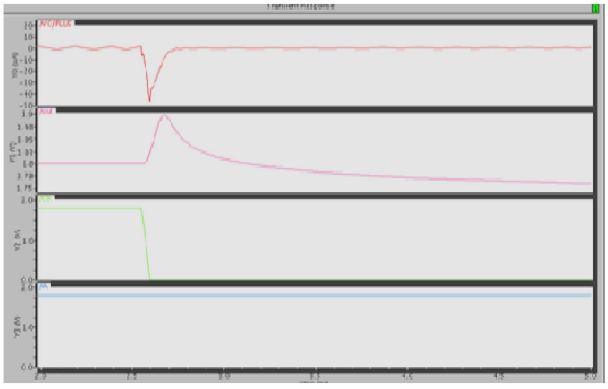

Fig. 7. Transient analysis of proposed buffer.

Fig.8. shows the schematic of 1 bit proposed full adder.

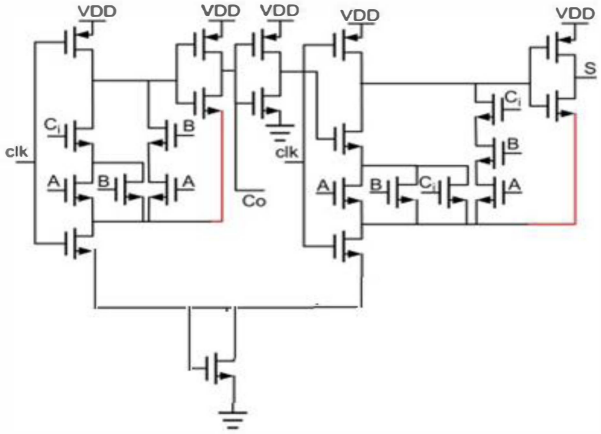

Fig. 8. Schematic of proposed 1 bit full adder.

III. SIMULATION RESULTS

To evaluate the performance of proposed technique we are using 180nm standard CMOS technology. In order to show the power saving of our proposed circuit design, simulation was performed using cadence spectre simulator for 180nm standard CMOS technology. In table I we have performed different type of logic design simulation with a 1:1 clock duty cycle at 500 MHz frequency and 25fF load capacitance.

Table I

Logic function	Power (conv.) (µW)	Power (PDB) (µW)	Power (Pro.) (µW)	Power Saving (PDB) (µW)	Power Saving (Pro.) (µW)
Z=AB	11	6.8	4.73	38	57
Z=A+B	19.7	10.94	7.5	44.5	62
Z=ABC	22	12.3	8.23	44.1	62.6
Z=A+B+C	24.6	11.6	7.65	53	68.9
Z=A+B+C+D	27.7	13	11	53	60.3
Z=ABC+D	20.2	9.89	5.64	51	72
Z=AB+CD	20.9	12.75	6.73	39	67.8

Table II shows the power delay comparison of proposed logic style & reported logic style for different logic at 500 MHz clock frequency and 25fF load capacitance.

Table II

Logic Func.	Power (PDB) (µW)	Power (Pro.) (µW)	Delay (PDB) (ns)	Delay (Pro.) (ns)	PDP (PDB) $\times 10^{-15}$ (W-s)	PDP (Pro.) $\times 10^{-15}$ (W-s)
AB	6.8	4.73	0.32	0.38	2.18	1.79
A+B	10.94	7.5	0.2	0.24	2.19	1.8
A+B+C	11.6	7.65	0.2	0.23	2.32	1.76
A+B+ C+D	13	11	0.17	0.14	2.21	1.54
ABC+D	9.89	5.64	0.29	0.36	2.87	2.03
AB+CD	12.75	6.73	0.26	0.35	3.32	2.35

In Fig.9. We have shown the power consumption comparison of 1bit full adder between different logic styles in 180nm technology. (Vdd=1.8v, 500 MHz)

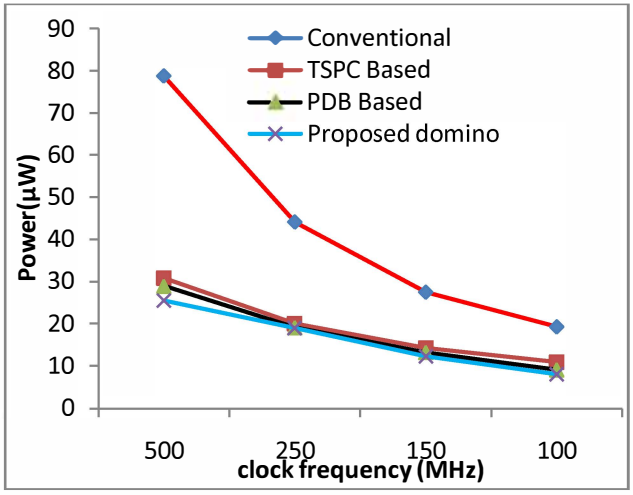

Fig. 9. Power consumption comparison between proposed logic styles, PDB based logic style, TSPC-based logic style & conventional logic style at 25fF load capacitance for different clock frequency.

So, as a result we observed that if we increase the operating clock frequency power consumption increases. In Fig.10. We have shown the power consumption comparison of 1bit full adder between different logic styles in 180nm technology. (Vdd=1.8v, 500 MHz) at different load capacitance.

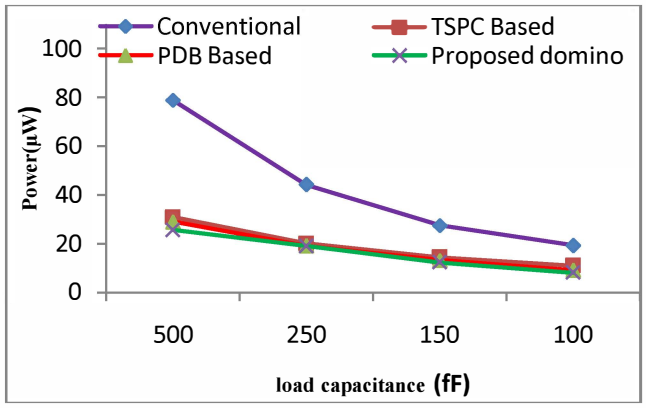

Fig. 10. Power consumption comparison between proposed logic styles, PDB based logic style, TSPC-based logic style & conventional logic style at 500 MHz clock frequency for different load capacitance.

IV. CONCLUSION

Due to propagation of the precharge pulse to the output node in conventional domino logic increased the power dissipation by the circuit. This paper proposes a footed diode domino logic style design which can eliminates the precharge pulse propagation to output node and more power has been saved as compared to other logic style. We have shown the power consumption comparison between our proposed logic styles with different logic design techniques at 180nm standard CMOS technology. Simulation results shows that power can be saved upto 72% as compared to convention logic for different dynamic logic gates and upto 41% as compared with PDB based logic style.

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