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Comparative analysis of various Domino logic circuits for better performance

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***Abstract* - In this paper, basically the delay and the noise margin parameter associated in the circuit has been analyzed. The paper gives a better approach for the reduction in delay variation and compares the result with different-different types of domino logic circuits. The other domino logic circuits used to discriminate the result of proposed circuit are footed domino logic circuit, footless domino logic circuit, high speed domino logic circuit and conditional keeper domino logic circuit. The simulation process here has been done in 65nm CMOS technology using Cadence Virtuoso at 27^0C operating temperature and 0.8 V supply voltage. In this paper the parameters like delay, average power, no. of transistors and UNG has been calculated and after simulation it is found that the proposed paper gives better output if it is compared with the other circuits.**

Keywords- Noise immunity; Domino logic circuit; High speed integrated circuit; dynamic logic circuit; Unity noise gain (UNG);Digital Signal Processing (DSP).

I. INTRODUCTION

Dynamic logic circuits have a very important role in the modern digital circuits. The dynamic logic circuit provides higher speed, less power consumption and less area [8]. These are some advantages which makes the dynamic logic circuits more preferable instead of a static logic circuit [10]. Domino logic circuit is also a kind of dynamic logic circuit which is used for the high speed and high performance applications [5]. Also the domino logic circuit plays a vital role where fan in are high in any circuit [6]. Domino circuits are widely used in high performance microprocessors [9] and DSP circuits, such as high fan-in multiplexer or comparator circuits.

This paper contains several sections in which section I gives a brief introduction about domino logic circuits. The literature review and various types of domino logic circuits such as footed domino logic circuit, footless domino logic circuit, high speed domino logic circuit, and conditional keeper domino logic circuit has been highlighted in section II. Section III illustrates the proposed work and section IV deals with the results obtained after the simulation. Section V gives brief detail about the conclusion and future scope of the proposed work.

II LITERATURE REVIEW

The literature shows various proposed domino logic circuits like footed domino logic, footless domino logic circuit [1], High speed domino logic [4] and conditional keeper domino logic circuits [7].

The main advantage of footer domino logic circuits over footless domino logic circuit is that, the reduction in leakage current due to stacking effect provides better noise immunity to footer domino logic circuit. Fig. 1 and Fig. 2 show the conventional circuit diagram for footed and footless domino logic circuit respectively.

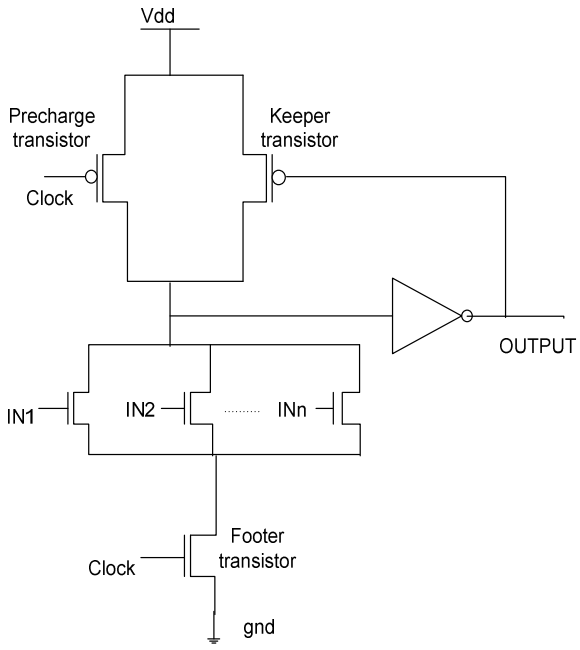

Fig. 1: Footed domino logic

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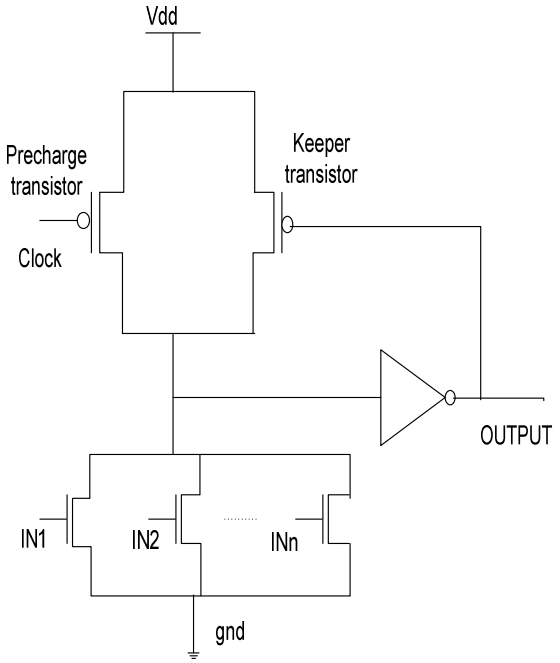

Fig. 2: Footless domino logic

II (A) HIGH SPEED DOMINO

High speed domino is another domino logic circuit. In domino logic circuit current drawn through the keeper transistor and pull down network NMOS transistors at the beginning of the evaluation phase, can be reduced by applying a clock delay in the circuit. That does not affect the leakage current in the circuit. But apart from this the extra clock delay consumes extra area and power, which is a big drawback of the circuit [4].

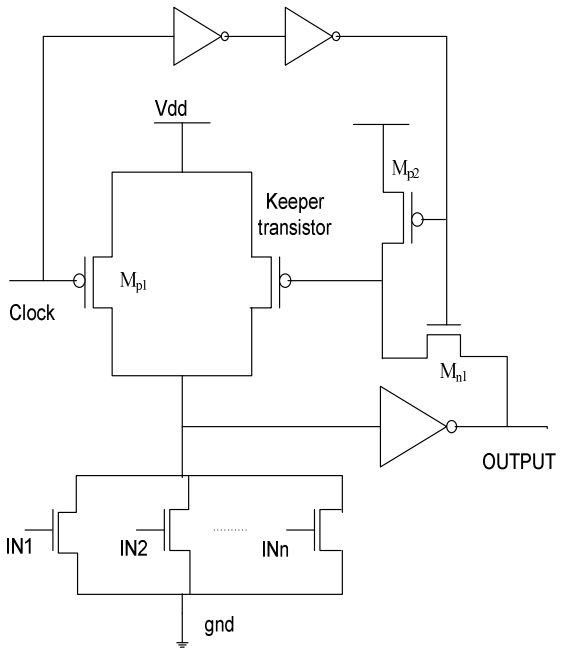

Fig. 3: High speed domino logic

In High speed domino logic circuit when clock becomes high, M_{n1} is still off and M_{p2} is still on. Therefore M_{p2} turns off the keeper transistor. After some delay of inverter M_{p2} becomes off. Now if dynamic node remains high during the evaluation phase, NMOS is turn on which turns on the keeper transistor. Hence at the beginning of evaluation phase dynamic node is afloat, so in the absence of keeper transistor, evaluation node may be discharged for any noise at the input section. Also the voltage at the gate of the keeper transistor would be $V_{DD} - V_{t,Mn1}$. This would provide a dc current flow through the PMOS keeper transistor and the NMOS network.

II (B) CONDITIONAL KEEPER DOMINO LOGIC

The conditional keeper domino logic contains two PMOS transistor keeper circuit in which one is of smaller strength and other is of higher strength [1], [7]. Now when the dynamic node is at high voltage M_{kp1} gets turn on to avoid voltage drop at the dynamic node. If the dynamic node is still high, then after a certain amount of delay, during the evaluation phase output of NAND gate becomes low this makes M_{kp2} to turn on. For maintaining the state of dynamic node, M_{kp1} is responsible during the beginning of evaluation phase and M_{kp2} is responsible for the rest of the evaluation phase.

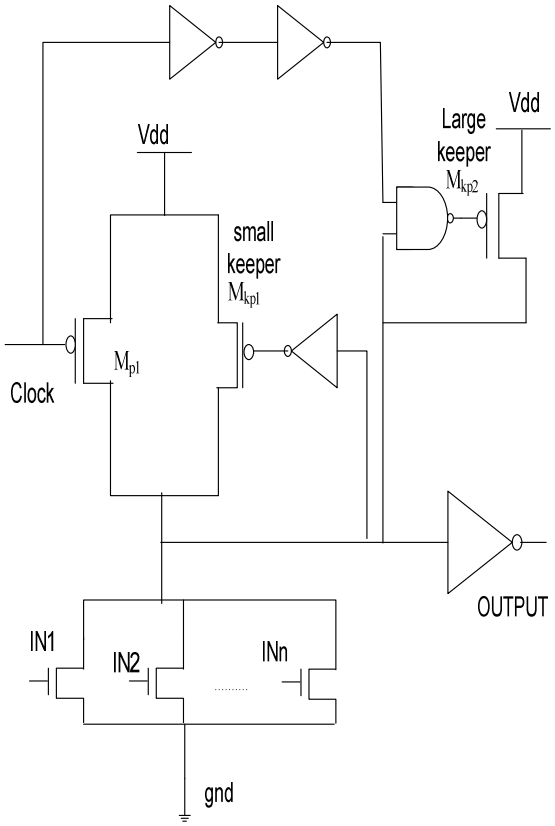

Fig. 4: Conditional keeper domino logic

III PROPOSED CIRCUIT

The proposed circuit here is implemented in 65 nm Cadence Virtuoso CMOS technology with the power supply of 0.8 V. This circuit is based on footed domino logic circuit and based on this the proposed circuit is given which is having better leakage tolerance and improved noise immunity. In the proposed circuit, the two keeper terminology is used. The delay variability problem occurs in various high performance applications [1], [2] and hence domino logic circuit basically deals with high performance application so it very much important to make remedy for these kind of problems. The delay variability issue can be overcome by using two transistor keeper technology illustrated in [3]. That approach gives improvement in reducing delay variability without any increment in silicon chip area. By doing some modification in the two keeper technology domino a new proposed circuit is implemented which gives better improvement in noise immunity and a marginal improvement in delay associated in the circuit. The circuit diagram for the proposed approach can be given as shown in Fig. 5.

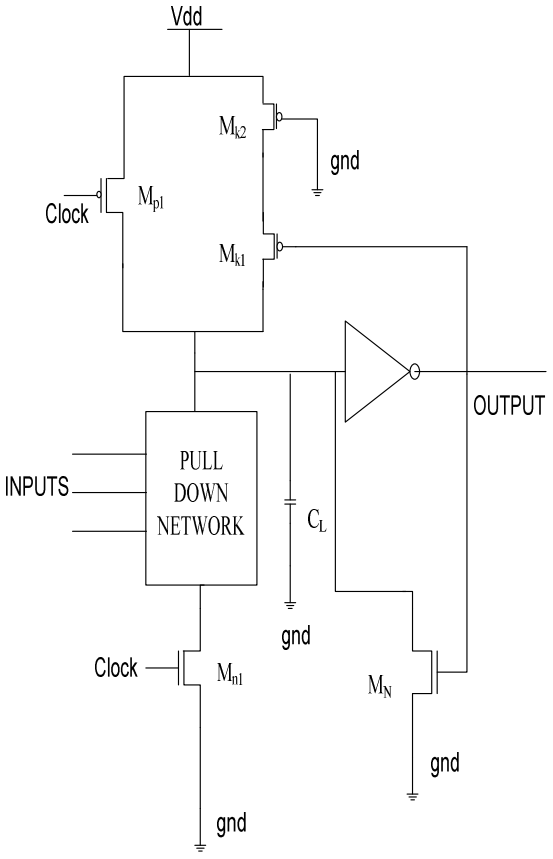

Fig. 5: Proposed noise tolerant domino logic circuit

To operate the circuit basically there are two modes of operation, namely pre-charge mode and evaluation mode. During pre-charge phase, the dynamic node of all the gates are charged to V_{DD}, which also causes the inverter output to go to 0 V. Now during the evaluation phase, the logic signal associated with the pull down network is evaluated and the inverter output perhaps changes from 0 to V_{DD} or some inverter output may remain at ground depending upon the logic signal provided to the pull down network.

In the proposed circuit an NMOS is added as shown in Fig. 5. The main function of this transistor is to draw the contention current of the PMOS keeper and also it helps to speed up the discharging process of the capacitor at the dynamic node. At the beginning of the pre-charge mode the pre-charge device is in active mode. Therefore the voltage at the dynamic node will be at 0 V and hence that will pass through an inverter so the output at the inverter will be V_{DD}. In consequence the extra added transistor will turn on and at the beginning of the pre-charge phase there will be contention of current between the two current derived from the extra added transistor and the keeper transistor because the pre-charge device tries to charge the capacitor C_L and the current due to the added NMOS tries to discharge the capacitor C_L.

During the evaluation phase the pre-charge device gets OFF because at this time the clock switches from logic '0' to logic '1'. Now the cases where inputs are such that the capacitor C_L must retain the charge, then the output will be zero. Also if the inputs are such that the pull down network must discharge the capacitor C_L, then the dynamic node voltage will start decreasing. At the beginning of discharging process the inverter output will be at zero, which will cause the extra added NMOS to stay inactive. The extra added NMOS compensates the keeper current and speed up discharging of capacitor C_L.

IV SIMULATION AND RESULT

The simulation process here is done by using Cadence Virtuoso Tool 65 nm technology using Analog Design Environment (ADE). In the proposed circuit all the parameters given here is calculated in 65nm technology only. Here all above mentioned circuits such as footed domino, footless domino, and conditional keeper domino logic circuit has been designed and all its parameters such as delay, power, UNG has been calculated. These parameters are calculated here for 2, 4 and 8 inputs respectively. The comparative analysis of various domino logic circuits is illustrated in table given below. The parameters calculated here is obtained by applying supply voltage V_{DD} as 0.8 V and operating temperature as 27^0 C. The tables which show the comparison are as given next.

TABLE I. Comparison table for 2 input

Parameters	Footed domino	Footless Domino	High speed Domino	Conditional keeper Domino	Proposed circuit
Delay (ps)	23.67	24.08	23.12	24.11	22.98
Avg. Power (µW)	0.3908	0.3748	79.1	60.8	0.4018
No. of transistors	7	6	12	19	9
UNG	0.218	0.211	0.239	0.287	0.279

TABLE II. Comparison table for 4 input

Parameters	Footed domino	Footless Domino	High speed Domino	Conditional keeper Domino	Proposed circuit
Delay (ps)	24.32	24.37	23.68	27.32	23.43
Avg. Power (µW)	0.4745	0.4238	116.4	120.15	0.5625
No. of transistors	9	8	14	21	11
UNG	0.196	0.189	0.217	0.263	0.311

TABLE III. Comparison table for 8 input

Parameters	Footed domino	Footless Domino	High speed Domino	Conditional keeper Domino	Proposed circuit
Delay (ps)	36.15	37.3	34.29	36.09	32.87
Avg. Power (µW)	0.594	0.542	158	205.34	0.636
No. of transistors	13	12	18	25	15
UNG	0.171	0.169	0.186	0.242	0.340

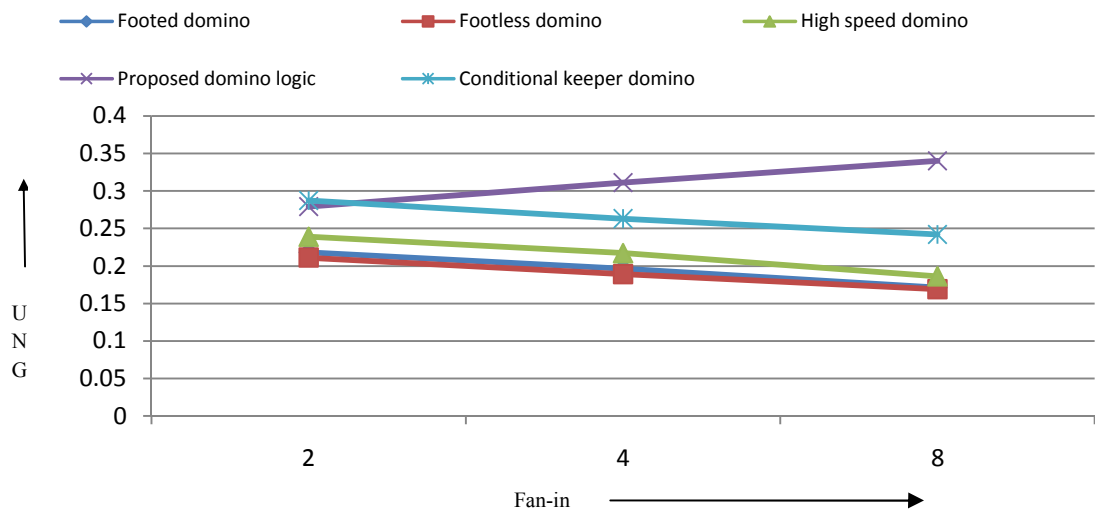

Fig. 6: Comparison of UNG of different Domino logic

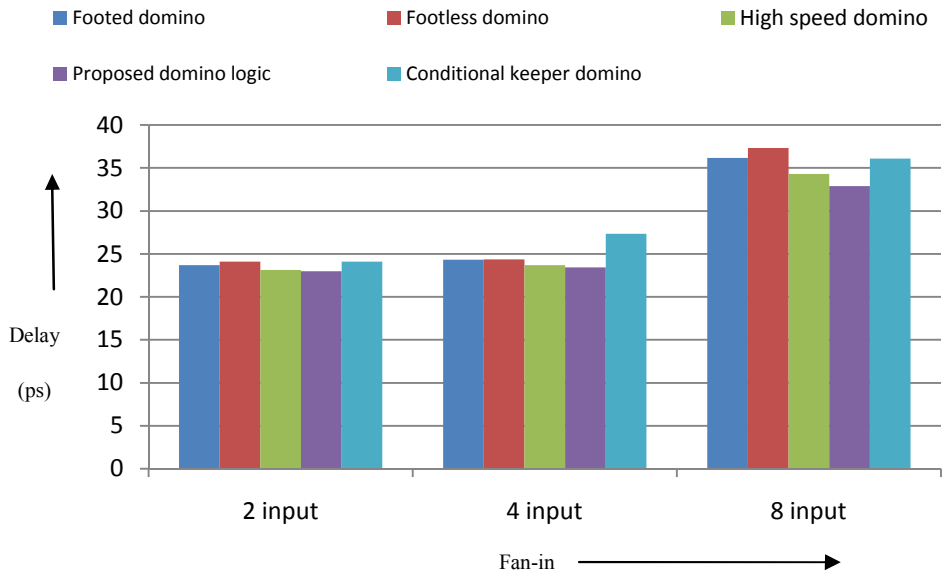

Fig. 7: Comparison of delay of different Domino logic

V CONCLUSION AND FUTURE SCOPE

In this paper the main objective is to compare all previous domino logic circuit with the proposed domino logic circuit. Hence in modern VLSI field a bit of improvement in any parameter plays an important role. So this paper can proves to be useful because it gives a remarkable improvement in the field of Delay, power, noise immunity and area when the proposed circuit is compared with the previously mentioned circuits. For more improvement in the proposed circuit, future scope would be to make it better for high fan-in circuits. The whole comparison is based upon 65 nm CMOS technology using Cadence Virtuoso tool.

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