# Comparative Performance Analysis of Dual-Rail Domino Logic and CMOS Logic Under Near-Threshold Operation

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***Abstract*—The designs of an asynchronous dual-rail domino logic (DRDL) and the conventional CMOS logic under near-threshold operation are compared. The delay time and energy consumption of an 8-bit full adder pipeline are simulated using HSPICE with 180-nm CMOS technology. The results show that, considering process variations, DRDL is faster than CMOS below 1.1 V. The delay performance of DRDL at 0.25 V is equivalent to that of CMOS at 0.4 V, while the energy-delay product of DRDL is 40% smaller than that of CMOS.**

***Keywords—Asynchronous circuit, dual-rail domino logic, full adder, energy-delay product***

## I. INTRODUCTION

In accordance with Moore's law [1], transistor performance has been improved by shrinking the transistor size. However, our ability to follow the law is approaching its limit. At this point, one critical problem is that of power. Near-threshold computing (NTC) [2] is expected to be a solution to this problem. NTC is a technique that reduces energy by lowering the power-supply voltage to a near threshold voltage to reduce the product of delay and the required energy to a minimum. However, if we lower the supply voltage, we will face a new problem: an increase in performance variations due to process, voltage, and temperature (PVT) variations.

Synchronous circuits have a clock in their registers, and the circuit cycle has to be larger than the maximum delay of the combinational circuit in between the resistors. The maximum delay becomes large under near-threshold operation with PVT variations. Therefore, synchronous circuits are not suited for NTC.

Asynchronous circuits are clockless and event-driven; therefore, they are delay-insensitive. Asynchronous circuits will not cause malfunction even with large performance variations caused by PVT variations. Null convention logic (NCL) [3] is one major type of asynchronous circuit that utilizes threshold gates to remain delay-insensitive. Threshold gates have improved their speed in [4]. However, it still need many transistors to make threshold gates, so the total number of transistors in NCL is still large.

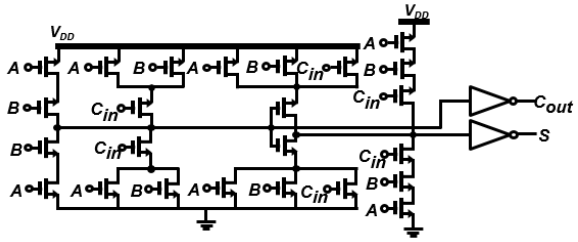


Fig. 1. Conventional CMOS full adder [9]

Recently, dual-rail domino logic (DRDL) [5, 6] was proposed as a new asynchronous circuit. Transistor counts of DRDL are lower than those of NCL, so DRDL is expected to be a good alternative to NCL. Previous studies [7, 8] show that DRDL performs well at low supply voltages, considering variations. However, there is no direct comparison with conventional CMOS logic.

Here, we compare DRDL with the conventional CMOS logic by using an 8-bit full adder pipeline under near-threshold operation. PVT variations are taken into account in order to conduct fair comparisons.

## II. SYNCHRONOUS LOGIC

### A. Synchronous CMOS logic

Fig. 1 shows a conventional CMOS full adder, which combines PMOS pull-up and NMOS pull-down networks to produce outputs. The advantage of the circuit is its small transistor count (specifically, 28), small delay, and thus, low amount of energy required for computation. However, we cannot determine when computation is complete by observing the circuit's outputs. We need clocking circuits to make a pipeline for computation, as described in the next section.

### B. Synchronous pipeline

Fig. 2 shows a synchronous pipeline of an 8-bit full adder. It has 17 inputs and 9 outputs. The clock cycle is determined by the maximum delay of the 8-bit full adder because the completion of the computation cannot be confirmed by simply observing its outputs. Outputs (S1–S8, $C_{out}$)

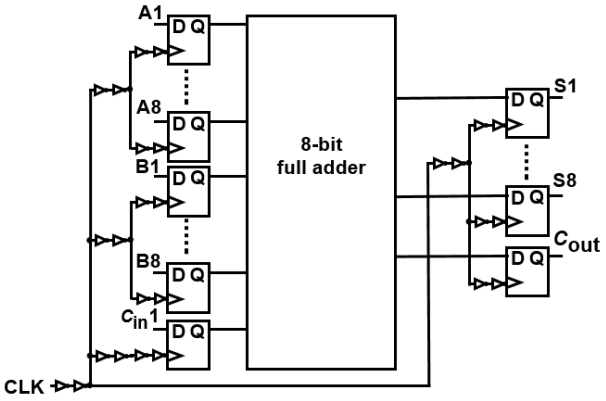


Fig. 2. Synchronous pipeline [10]

may remain the same or toggle depending on the circuit's inputs (A1–A8, B1–B8, $C_{in1}$). In short, the performance of the circuit is determined by its performance with the worst inputs, taking PVT variations and input signal combinations into account.

## III. Asynchronous Logic

### A. Null Convention Logic (NCL)

NCL is one of the major asynchronous logic styles. It has "set" and "reset" logic networks. In the set phase, data changes from spacer (NULL) to code-word (DATA), and in the reset phase, data changes from DATA to NULL. A dual-rail signal, D, consists of two wires, $\overline{D}$ and D. When $\overline{D}$=0 and D=1, D is logic 1(DATA1). When $\overline{D}$=1 and D=0, D is logic 0(DATA0). When $\overline{D}$=0 and D=0, D is NULL. $\overline{D}$ and D are mutually exclusive, so $\overline{D}$=1 and D=1 is an illegal code-word. NCL

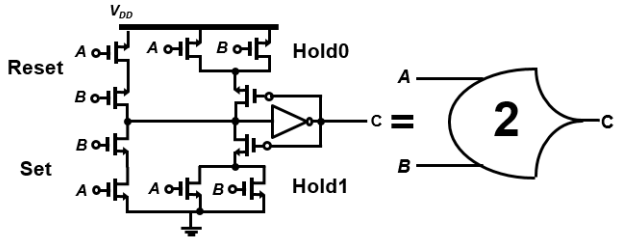


Fig. 3. TH22 gate

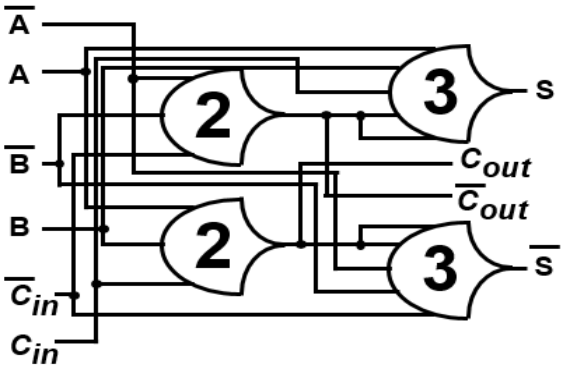


Fig. 4. NCL full adder [3]

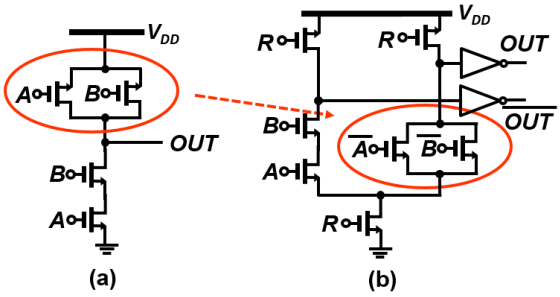


Fig 5. (a) CMOS NAND, (b) DRDL NAND [6]

circuits are made of threshold gates. Each gate is demonstrated as $THmnW_{W1W2...Wn}$, wherein "m" is the threshold of the gate, "n" is the number of inputs, and "$_{W1W2...Wn}$" are the weights of the inputs when the input is bigger than 1. Fig. 3 shows the TH22 gate. The output data asserts DATA when both inputs are asserted. NCL has a hold function, so once the threshold gate opens, it will not close until all the input sends 0. Therefore, NCL is delay-insensitive [4].

Fig. 4 shows an NCL full adder. NCL is a dual-rail logic, so its outputs always change NULL to DATA when completing computation. Therefore, we can obtain the completion signal by observing its output, leading to a clockless design. The problem, however, is that it needs 82 transistors for a 1-bit full adder. This is about three times as many transistors as a conventional CMOS circuit. Even with its clockless nature, it is difficult to make a system more energy-efficient with NCL for this reason.

### B. Dual-Rail Domino Logic(DRDL)

Fig. 5 (a) shows a CMOS NAND, and Fig. 5 (b) shows a DRDL NAND, which combines an NMOS pull-down network and a PMOS pair, driven by reset, which brings the gate in the precharge and evaluation modes. By converting the PMOS

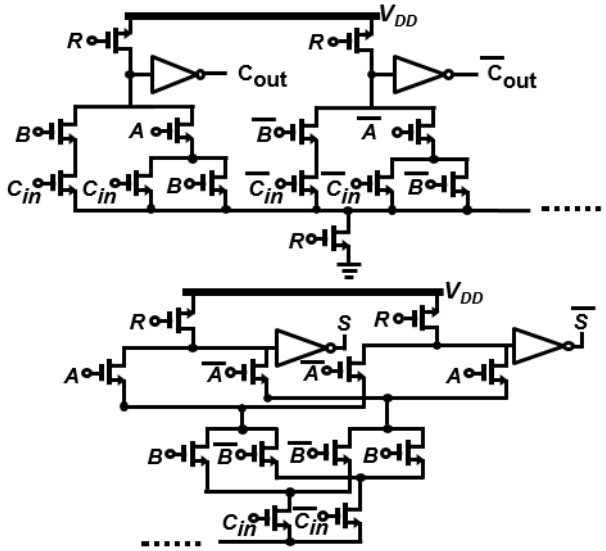


Fig. 6. DRDL full adder [5]

TABLE I. TRANSISTORS OF FULL ADDER

| | CMOS | NCL | DRDL |
|---|---|---|---|
| Transistors | 28 | 82 | 33 |

pull-up network in the CMOS NAND to the NMOS pull-down network in DRDL NAND, DRDL achieves dual-rail logic. Therefore, the number of transistors for DRDL will be almost the same as for CMOS and much smaller than for NCL.

Fig. 6 shows a DRDL 1-bit full adder. DRDL enables a dual-rail 1-bit full adder with 33 transistors.

Table I shows the transistor number of 1-bit full adders. The number for DRDL is 33 while that for NCL is 82. Therefore, DRDL has higher area-efficiency than NCL. Further, DRDL can achieve dual-rail logic using only 5 more transistors than CMOS does.

### C. Asynchronous pipeline

Fig. 7 shows an asynchronous pipeline of an 8-bit full adder. It has 34 inputs and 18 outputs. Fifty-two TH22 gates are required as register gates. Each of them receives one wire with a data meaning and one wire with a control meaning. Four TH33 gates and a TH22 gate following eight TH33 gates form the completion watcher gates. The operation of the pipeline is as follows.

1. At the initial state, all of the inputs and outputs of the full adder are NULL.

2. Both watcher gates send 1 to the register gates.

3. After sending input data (A1–A8, B1–B8, $C_{in1}$), the input register gates send DATA to the full adder.

4. Then, the input watcher gates send 0 to the registers in the preceding stage.

5. The full adder completes the computation, and the output register gates send DATA to the output (S1–S8,$C_{out}$).

6. The output watcher gates send 0 to the input registers.

7. The input register gates send NULL to the full adder because the input data (A1–A8, B1–B8, $C_{in1}$) returns to NULL.

8. Finally, all output registers send NULL when they receive 0 from the watcher gates in the next stage, and the watcher gates returns to 1.

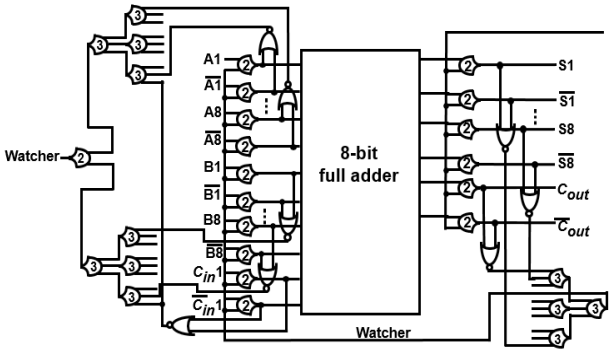


Fig. 7. Asynchronous pipeline [3]

As described above, the pipeline operates without clocking.

## IV. SIMULATION RESULTS AND DISCUSSION

### A. DRDL vs NCL

We simulated DRDL and NCL 8-bit full adder pipelines with HSPICE using a 180-nm process at 0.4 V. Fig. 8 shows the simulation results. A1 and $\overline{A1}$ are inputs of registers; S8 and $\overline{S8}$ are outputs of registers. Table II gives a performance comparison of DRDL and NCL. The delay is defined in Fig. 8. Monte Carlo simulations with process variations and randomized input signal were conducted 1000 times, and the average delay and energy were calculated. DRDL uses 1460 transistors while NCL uses 1824. The delay time of DRDL is 1.91 µs while that of NCL is 2.80 µs. The energy required for DRDL is 2.31 pJ while that for NCL is 2.83 pJ.

The energy delay product is normalized with respect to NCL. The results show that DRDL's energy delay product is 44% smaller than that of NCL. Therefore, DRDL has higher energy- and area-efficiency than NCL.

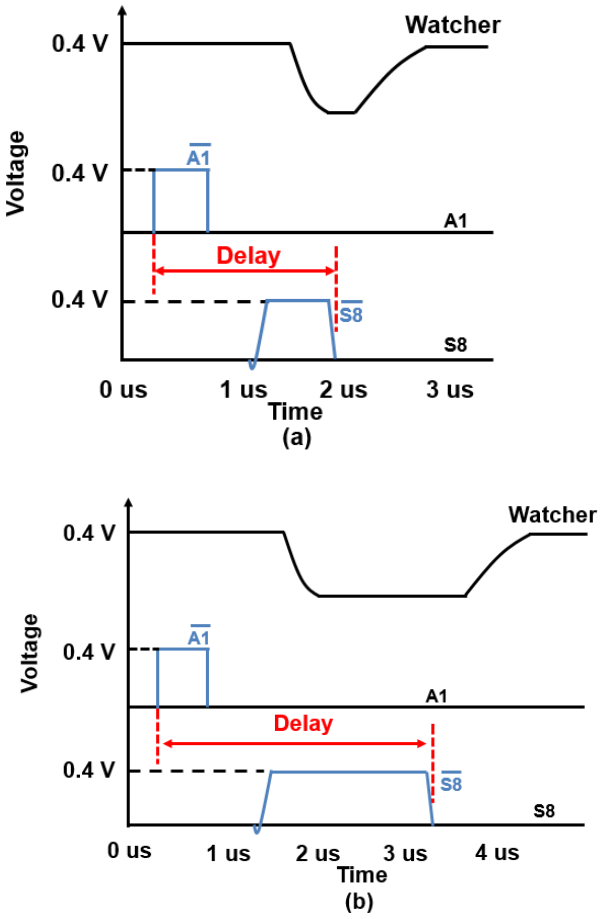


Fig. 8. Simulation results for (a) DRDL and (b) NCL

TABLE II. PERFORMANCE COMPARISON OF DRDL AND NCL

| | Transistors | Delay (µs) | Energy (pJ) | Energy× Delay |
|---|---|---|---|---|
| DRDL | 1460 | 1.91 | 2.31 | 0.56 |
| NCL | 1824 | 2.80 | 2.83 | 1.00 |

TABLE III. PERFORMANCE COMPARED WITH DRDL AND CMOS

| | Transistors | Delay (µs) | Energy (fJ) | Energy× Delay |
|---|---|---|---|---|
| DRDL | 1460 | 62.6 | 499 | 0.60 |
| CMOS | 764 | 59.3 | 871 | 1.00 |

### B. *DRDL vs CMOS*

Next, we compare DRDL and the conventional CMOS logic. Fig. 9 shows the delay vs. supply voltage of the 8-bit full adder pipeline shown in Figs. 2 and 7. For CMOS, we have two curves, one of which is a typical delay and the other of which is the maximum delay. The typical delay is the average delay with typical process conditions and random inputs. The maximum delay is the critical path delay of 1000 Monte Carlo simulations with Vt variations (local(random) + global(+0.1V)), which corresponds to 4σ process corner.

When comparing the average delay, CMOS is faster than DRDL over the voltage range of 0.4 to 1.8 V. However, CMOS has to be considered with the maximum delay time because it is a synchronous system. Comparing the maximum delay of CMOS and the average delay of DRDL, DRDL gets faster when the supply voltage is below 1.1 V.

As shown in Fig. 9, the delay of DRDL at 0.25 V is about the same as that of CMOS at 0.4 V. We compare the energy delay product, shown in Table III. The energy delay product is normalized with respect to CMOS. CMOS has 764 transistors while DRDL has 1460. The maximum delay time for CMOS at 0.4 V is 59.2 µs, and the average delay time for DRDL at 0.25 V is 62.6 µs. The energy required for DRDL is 499 fJ while that for CMOS is 871 fJ, which are the average of random input simulation results.

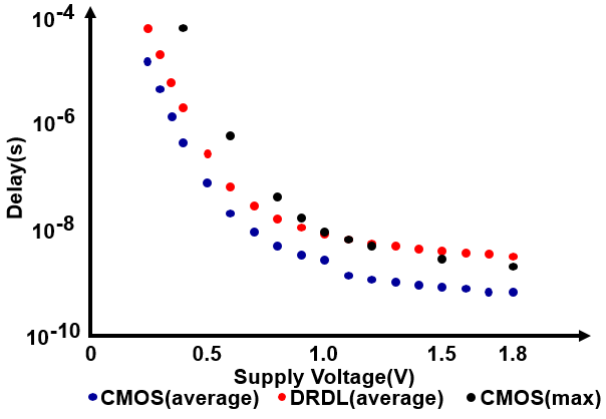


Fig. 9. Voltage vs. delay for CMOS and DRDL

Considering transistor counts, CMOS has a higher area-efficiency than DRDL. However, the energy delay products of DRDL are 40% smaller than those of CMOS. Therefore, DRDL has a higher energy-efficiency than CMOS under near-threshold operation.

## V. CONCLUSION

We employed DRDL in an asynchronous pipeline and compared its performance with that of the conventional CMOS synchronous pipeline. We showed that DRDL has a 40% smaller energy delay product than CMOS under near-threshold operation, considering process variations.


## ACKNOWLEGEMENT

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