Politecnico di Torino

TAMTAMS Web

Integrated System Technology

NAND/AND MODULES:

Delay_Pow_and2_dyn, Delay_Pow_and3_dyn, Delay_Pow_and4_dyn

Delay_Pow_or2_dyn, Delay_Pow_or3_dyn, Delay_Pow_or4_dyn

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Contents

1 Introduction

Analysis and parameters estimation in terms of power and delay of different single logic gates. To do that *AND2, AND3, AND4* and *OR2, OR3, OR4* logic gates implemented in *Dynamic-logic* are analysed.
This *OCTAVE* files are implemented for *TAMTAMS*:

- **Delay_Pow_and2_dyn.m**: Dynamic-logic 2-inputs AND;
- **Delay_Pow_and3_dyn.m**: Dynamic-logic 3-inputs AND;
- **Delay_Pow_and4_dyn.m**: Dynamic-logic 4-inputs AND;
- **Delay_Pow_or2_dyn.m**: Dynamic-logic 2-inputs OR;
- **Delay_Pow_or3_dyn.m**: Dynamic-logic 3-inputs OR;
- **Delay_Pow_or4_dyn.m**: Dynamic-logic 4-inputs OR;

where the following parameters are estimated:

- **Delay_nand_and**: input to output delay;
- **Pnand_and_dyn**: dynamic power;
- **Pnand_and**: static power;

2 Logic Implementation

The different logic gates involved into the analysis are represented in form of schematic.
The dimension of the transistor are forced in order to have a resistance (and an I_{on}) equal to the inverter of minimal dimension.
The figure 1 shows the *Dynamic* structures taken in account.
The *n-MOS* and the *p-MOS* connected to *CLK* are the header and the footer used to disclaim between the two dynamic phase. Then a pull-down network is used to evaluate the output. A *CMOS* inverter must be added because of the sharing of charge that could appears between one gate and the next one. For that reason the inverter is added as a part of the gates itself and must be taken into account in all analysis; it is a fundamental part of the structure.
Note that those gates are *non-inverting* where a *CMOS* logic is *inverting*; moreover this fact does not afflict the comparison between the two structure because if the *NAND2* is the fundamental block of *CMOS* logic, the *AND2* is the fundamental one for the *Dynamic* logic.

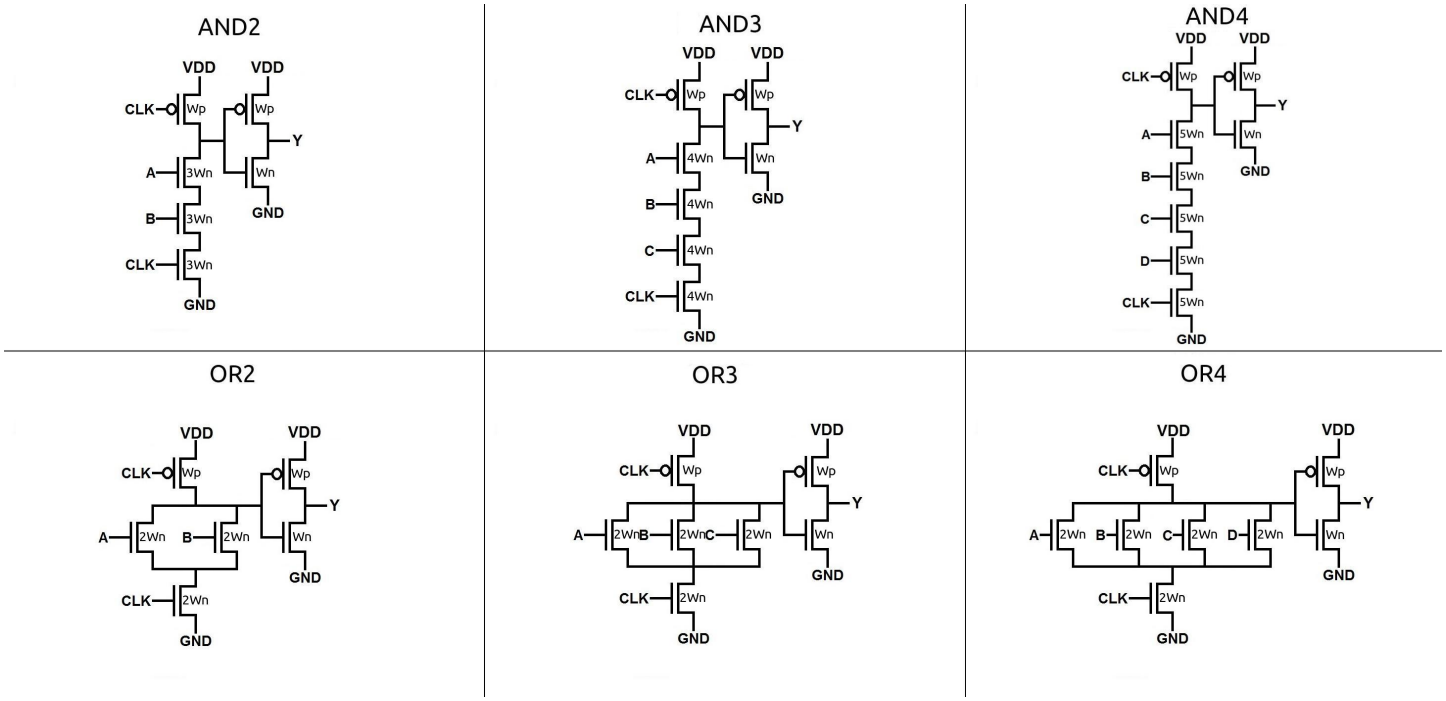

Figure 1: Dynamic schemes

3 Delay

3.1 Theoretical Analysis

The delay analysis of the different gates is implemented exploiting the *Elmore* Delay model, taking into account that it is an optimistic model. Moreover it could be used to easily compare different technological implementation.
Necessary technological parameters in order to evaluate the delay are reported below.
The analysis is done on gate with a load made of a minimum inverter or multiple of it. Is possible compute input capacitance of *n-MOS* and *p-MOS* transistors per unit length:

$$C_{in_N} = C_{OX} + C_{overlapN} \quad [pF/\mu m] \tag{1}$$
$$C_{in_P} = C_{OX} + C_{overlapP} \quad [pF/\mu m] \tag{2}$$

where the two overlap capacitances are due to the overlap size between the gate and drain/source areas:

$$C_{overlapN} = 10^6 \cdot C_{GDOn} \quad [pF/\mu m] \tag{3}$$
$$C_{overlapP} = 10^6 \cdot C_{GDOp} \quad [pF/\mu m] \tag{4}$$

The junction capacitances between source and drain are:

$$C_{jN} = C_{bottomN} + C_{sidewallN} \quad [pF/\mu m] \tag{5}$$
$$C_{jP} = C_{bottomP} + C_{sidewallP} \quad [pF/\mu m] \tag{6}$$

C_{bottom} is the capacitance due to the area of the pool of the source/drain and $C_{sidewall}$ is the one due to the edge of the same pool.

$$C_{bottomN} = C_{j0_N} \cdot \left(1 + \frac{V_{DD}}{2 \cdot P_{bN}}\right)^{-M_{jN}} \cdot 2.5 \cdot L_{drawn} \quad [pF/\mu m] \tag{7}$$
$$C_{bottomP} = C_{j0_P} \cdot \left(1 + \frac{V_{DD}}{2 \cdot P_{bP}}\right)^{-M_{jP}} \cdot 2.5 \cdot L_{drawn} \quad [pF/\mu m] \tag{8}$$
$$C_{sidewallN} = 10^6 \cdot C_{sw_N} \cdot \left(1 + \frac{V_{DD}}{2 \cdot P_{bswN}}\right)^{-M_{jswN}} \quad [pF/\mu m] \tag{9}$$
$$C_{sidewallP} = 10^6 \cdot C_{sw_P} \cdot \left(1 + \frac{V_{DD}}{2 \cdot P_{bswP}}\right)^{-M_{jswP}} \quad [pF/\mu m] \tag{10}$$

Moreover for the estimation of parasitic capacitances C_{jN} and C_{jP}, it is necessary to evaluate the perimeter.

$$\text{perim}_N = 2 \cdot \text{lungh\_diff} + W_N[\mu m] \tag{11}$$
$$\text{perim}_P = 2 \cdot \text{lungh\_diff} + W_P[\mu m] \tag{12}$$

We consider only one side for the W, because the internal one does not touch a conductor, but just a spatial charge.
Therefore C_{jN} and C_{jP} are:

$$C_{jN} = C_{bottomN} \cdot W_N + C_{sidewallN} \cdot \text{perim}_N \quad [pF] \tag{13}$$
$$C_{jP} = C_{bottomP} \cdot W_P + C_{sidewallP} \cdot \text{perim}_P \quad [pF] \tag{14}$$

Now we have to evaluate the equivalent resistance of the *MOS* that contributes in the delay calculation:

$$R_n = \frac{1}{\mu_n \cdot C_{OX} \cdot \frac{W_N}{L_{eff}} \cdot (V_{DD} - V_{tn})} \quad [\Omega] \tag{15}$$

$$R_p = \frac{1}{\mu_p \cdot C_{OX} \cdot \frac{W_P}{L_{eff}} \cdot (V_{DD} - V_{tp})} \quad [\Omega] \tag{16}$$

Another parameters used in our analysis is h. It's simply the multiplier of the number of inverter linked in output, the parametrized fan-out.

3.2 Delay calculation

In figure 2 the *Elmore* model of *AND2-Dynamic* gate is shown.
The total delay it's the combination of two contributes: the delay of the *pull-down dynamic* structure plus the delay of the inverter. In this architecture we have to consider also the *pre-charge* time that in the case of the fall time will be summed up with the other two contributes. Note that the first stage has to charge the inverter input capacitance too.

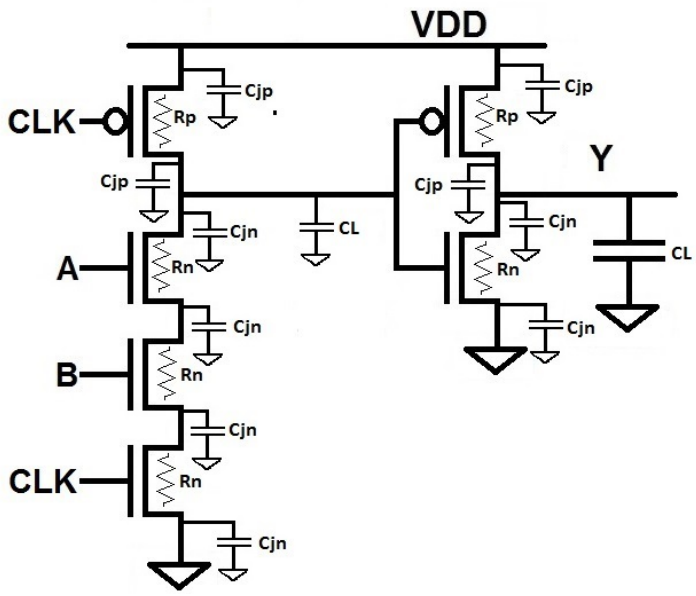

Figure 2: Dynamic-AND2 Elmore Model

So in general we can represent the two delays (for both OR and AND) as :

$$\begin{aligned} t_r &= t_{precharge} + t_{fall-gate} + t_{rise-inverter} \\ t_f &= t_{precharge} + t_{fall-inverter} \end{aligned} \tag{17}$$

Where the rise and fall time of the inverter are :

$$\begin{aligned} t_{rise-inverter} &= R_p \cdot (C_{jp} + C_{jn} + h \cdot C_L) \\ t_{fall-inverter} &= R_n \cdot (C_{jn} + C_{jp} + h \cdot C_L) \end{aligned} \tag{18}$$

From here on out it will be showed only the contribute depending from the first part of the gate because the *inverter* contribute it's always the same.

- **AND2-Dynamic**

$$tr_{dand2} = R_p \cdot (C_{jp} + C_{jn} + C_L) \tag{19}$$

$$\begin{aligned} tf_{dand2} = R_n \cdot (C_{jn} + C_{jn} + C_{jn} + C_{jp} + C_L) + R_n \cdot (C_{jn} + C_{jn} + C_{jp} + C_L) + R_n \cdot (C_{jn} + C_{jp} + C_L) = \\ = R_n \cdot (6 \cdot C_{jn} + 3 \cdot C_{jp} + 3 \cdot C_L) \end{aligned} \tag{20}$$

- **AND3-Dynamic**

$$tr_{dand3} = R_p \cdot (C_{jp} + C_{jn} + C_L) \tag{21}$$

$$tf_{dand3} = R_n \cdot (10 \cdot C_{jn} + 4 \cdot C_{jp} + 4 \cdot C_L) \tag{22}$$

- **AND4-Dynamic**

$$tr_{dand4} = R_p \cdot (C_{jp} + C_{jn} + C_L) \tag{23}$$

$$tf_{dand4} = R_n \cdot (15 \cdot C_{jn} + 5 \cdot C_{jp} + 5 \cdot C_L) \tag{24}$$

- **OR2-Dynamic**

$$tr_{dor2} = R_p \cdot (C_{jp} + 2 \cdot C_{jn} + C_L) \tag{25}$$

$$tf_{dor2} = R_n \cdot (C_{jn} + C_{jn} + C_{jn} + C_{jp} + C_L) + R_n \cdot (C_{jn} + C_{jn} + C_{jp} + C_L) = R_p \cdot (7 \cdot C_{jn} + 2 \cdot C_{jp} + 2 \cdot C_L) \tag{26}$$

- **OR3-Dynamic**

$$tr_{dor3} = R_p \cdot (C_{jp} + 3 \cdot C_{jn} + C_L) \tag{27}$$

$$tf_{dor3} = R_n \cdot (10 \cdot C_{jn} + 2 \cdot C_{jp} + 2 \cdot C_L) \tag{28}$$

- **OR4-Dynamic**

$$tr_{dor4} = R_p \cdot (C_{jp} + 4 \cdot C_{jn} + C_L) \tag{29}$$

$$tf_{dor4} = R_n \cdot (13 \cdot C_{jn} + 2 \cdot C_{jp} + 2 \cdot C_L) \tag{30}$$

4 Dynamic Power

4.1 Theoretical Analysis

The dynamic power can be evaluated through the following:

$$P_{dynamic} = \frac{1}{2} \cdot f \cdot C \cdot \alpha \cdot V_{DD}^2 \quad [W] \tag{31}$$

Where α is the switching activity, f the frequency and C the total capacitance.
This analysis was made imposing two assumption in order to get simplified expression to easily make consideration on the technological behaviour of described gates:

- The input probability is always considered as $\frac{1}{2}$;
- The computation of the switching activity for every single node is based on a *probabilistic model* (shown in detail later).

All the necessary technological parameters involved into this analysis are detailed in 3.1.

4.2 Dynamic power calculation

In this section is reported a detailed analysis of *NAND2* gate implemented exploiting *dynamic* logic. In Figure 3 can be seen the scheme of the analysed gate. The expression to compute the dynamic power is:

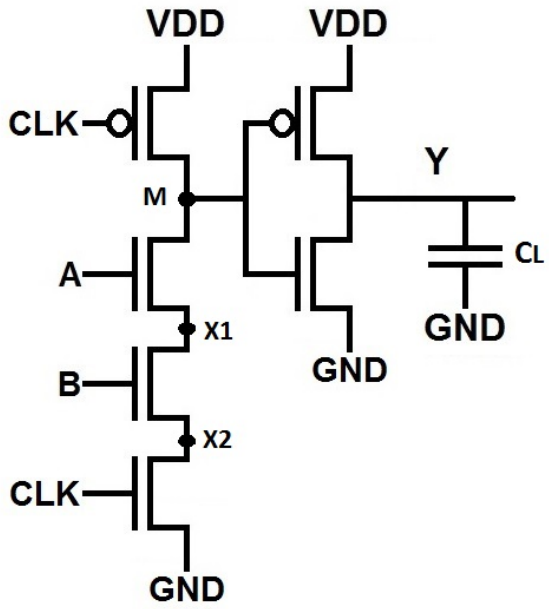

Figure 3: Dynamic 2-input AND architecture

$$C \cdot \alpha = C_{IN_{nmos}} \cdot (\alpha_A + \alpha_B) + C_M \cdot \alpha_M + C_X \cdot (\alpha_{X1} + \alpha_{X2}) + C_Y \cdot \alpha_Y + (C_{IN_{nmos}} + C_{IN_{pmos}}) \cdot \alpha_{CLK} \quad (32)$$

The considered capacitances are the following:

- $C_{IN_{nmos}}$ and $C_{IN_{pmos}}$ are the capacitances associated to the inputs for *n-MOS* and *p-MOS* respectively:

$$C_{IN_{nmos}} = C_{OX} \cdot 3W_N \cdot L_{eff} + 2C_{overlapN} = 3C_{OXN} + 2C_{overlapN} \quad [pF] \quad (33)$$

$$C_{IN_{pmos}} = C_{OX} \cdot W_P \cdot L_{eff} + 2C_{overlapP} = C_{OXP} + 2C_{overlapP} \quad [pF] \quad (34)$$

- C_{X1} and C_{X2} are the capacitances associated to the internal nodes, always supposing that source and drain are common for the two *n-MOS*:

$$C_{X1} = C_{X2} = 3C_{jN} \quad [pF] \quad (35)$$

- C_M is obviously the capacitance of the middle node M:

$$C_M = C_{jP} + 3C_{jN} + C_{INV} \quad [pF] \quad (36)$$

  To note that C_{INV} is simply the input capacitance for the inverter:

$$C_{INV} = C_{OX} \cdot W_N \cdot L_{eff} + C_{OX} \cdot W_P \cdot L_{eff} + 2C_{overlapN} + 2C_{overlapP} \quad [pF] \quad (37)$$

- C_Y is the output capacitance:

$$C_Y = C_{jP} + C_{jN} + C_L \quad [pF] \quad (38)$$

Regarding the switching activity we have to do some consideration: α_{CLK} is the switching activity associated to the clock signal and can be considered equal to 2. This because for sure there are two commutations in a single clock period.
The switching activity associated to the input is the same seen for the CMOS static logic:

$$\alpha_A = \alpha_B = \frac{1}{2} \quad (39)$$

For the internal and the M nodes the switching activity can be computed as:

$$\alpha_{X,M} = 2 \cdot (1 - P_{X,M}) \quad (40)$$

This because, considering the worst case, each node commutes 2 times when in *pre-charge phase* is charged and then in *evaluation phase* is discharged, so in the case that the node goes to *zero*.
In this particular example we have:

$$P_{X1} = P_A \cdot (1 - P_B) \quad (41)$$

$$P_{X2} = P_A \cdot P_B \quad (42)$$

$$P_M = (1 - P_A) \cdot (1 - P_B) \quad (43)$$

Regarding the node Y we can say that $\alpha_M = \alpha_Y$.This due to the presence of the inverter, it's easy to see that if the there's a commutation on the M node there will be also on the node Y. Summing up all the contribution, the final expression is the following:

$$\begin{aligned} C \cdot \alpha_{DAND2} &= 3C_{IN_{nmos}} + \frac{3}{2} \cdot C_M + 3C_X + \frac{3}{2} \cdot C_Y + 2C_{IN_{pmos}} = \\ &= \frac{21}{2}C_{OXN} + 9C_{overlapN} + \frac{7}{2}C_{OXP} + 7C_{overlapP} + 15C_{jN} + 3C_{jP} + C_L \end{aligned} \tag{44}$$

The other logic gates are analysed in similar way.
Here are reported just the final expression for $C \cdot \alpha$ in those cases:

- **AND3-Dynamic**:

$$C{\cdot}\alpha_{DAND3} = C_{IN_{nmos}}{\cdot}(\alpha_A{+}\alpha_B{+}\alpha_C){+}C_M{\cdot}\alpha_M{+}C_X{\cdot}(\alpha_{X1}{+}\alpha_{X2}{+}\alpha_{X3}){+}C_Y{\cdot}\alpha_Y{+}(C_{IN_{nmos}}{+}C_{IN_{pmos}}){\cdot}\alpha_{CLK} \tag{45}$$

$$\frac{3}{2} \cdot C_{IN_{nmos}} + \frac{7}{4} \cdot C_M + \frac{15}{2} \cdot C_X + \frac{7}{4} \cdot C_Y + 2 \cdot (C_{IN_{nmos}} + C_{IN_{pmos}}) \tag{46}$$

$$= \frac{63}{4}C_{OXN} + \frac{21}{2}C_{overlapN} + \frac{15}{2}C_{OXP} + \frac{15}{2}C_{overlapP} + \frac{155}{4}C_{jN} + \frac{7}{2}C_{jP} + C_L \tag{47}$$

- **AND4-Dynamic**:

$$\begin{aligned} C \cdot \alpha_{DAND4} &= C_{IN_{nmos}} \cdot (\alpha_A + \alpha_B + \alpha_C + \alpha_D) + C_M \cdot \alpha_M + \\ &+ C_X \cdot (\alpha_{X1} + \alpha_{X2} + \alpha_{X3} + \alpha_{X4}) + C_Y \cdot \alpha_Y + (C_{IN_{nmos}} + C_{IN_{pmos}}) \cdot \alpha_{CLK} = \end{aligned} \tag{48}$$

$$= 2 \cdot C_{IN_{nmos}} + \frac{15}{8} \cdot C_M + 7 \cdot C_X + \frac{15}{8} \cdot C_Y + 2 \cdot (C_{IN_{nmos}} + C_{IN_{pmos}}) = \tag{49}$$

$$= \frac{175}{8}C_{OXN} + \frac{47}{4}C_{overlapN} + \frac{31}{8}C_{OXP} + \frac{31}{4}C_{overlapP} + \frac{185}{4}C_{jN} + \frac{15}{4}C_{jP} + C_L \tag{50}$$

- **OR2-Dynamic**:

$$C \cdot \alpha_{DOR2} = C_{IN_{nmos}} \cdot (\alpha_A + \alpha_B) + C_M \cdot \alpha_M + C_X \cdot \alpha_{X1} + C_Y \cdot \alpha_Y + (C_{IN_{nmos}} + C_{IN_{pmos}}) \cdot \alpha_{CLK} = \tag{51}$$

$$= C_{IN_{nmos}} + \frac{3}{2} \cdot C_M + \frac{1}{2} \cdot C_X + \frac{3}{2} \cdot C_Y + 2 \cdot (C_{IN_{nmos}} + C_{IN_{pmos}}) = \tag{52}$$

$$= \frac{15}{2}C_{OXN} + 9C_{overlapN} + \frac{7}{2}C_{OXP} + \frac{7}{C_{\,overlapP}} + \frac{21}{2}C_{jN} + 3C_{jP} + C_L \tag{53}$$

- **OR3-Dynamic**:

$$C{\cdot}\alpha_{COR3} = C_{IN_{nmos}}{\cdot}(\alpha_A{+}\alpha_B{+}\alpha_C){+}C_M{\cdot}\alpha_M{+}C_X{\cdot}\alpha_{X1}{+}C_Y{\cdot}\alpha_Y{+}(C_{IN_{nmos}}{+}C_{IN_{pmos}}){\cdot}\alpha_{CLK} = \tag{54}$$

$$= \frac{3}{2} \cdot C_{IN_{nmos}} + \frac{7}{4} \cdot C_M + \frac{1}{4} \cdot C_X + \frac{7}{4} \cdot C_Y + 2 \cdot (C_{IN_{nmos}} + C_{IN_{pmos}}) = \tag{55}$$

$$= \frac{35}{4}C_{OXN} + \frac{21}{2}C_{overlapN} + \frac{15}{4}C_{OXP} + \frac{15}{2}C_{overlapP} + \frac{57}{4}C_{jN} + \frac{7}{2}C_{jP} + C_L \tag{56}$$

- **OR4-Dynamic**::

$$C \cdot \alpha_{COR4} = C_{IN_{nmos}} \cdot (\alpha_A + \alpha_B + \alpha_C + \alpha_D) + C_M \cdot \alpha_M + C_X \cdot \alpha_{X1} + C_Y \cdot \alpha_Y + (C_{IN_{nmos}} + C_{IN_{pmos}}) \cdot \alpha_{CLK} = \tag{57}$$

$$= 2 \cdot C_{IN_{nmos}} + \frac{15}{8} \cdot C_M + \frac{1}{8} \cdot C_X + \frac{15}{8} \cdot C_Y + 2 \cdot (C_{IN_{nmos}} + C_{IN_{pmos}}) = \tag{58}$$

$$= \frac{79}{8} C_{OXN} + \frac{47}{4} C_{overlapN} + \frac{31}{8} C_{OXP} + \frac{31}{4} C_{overlapP} + \frac{145}{8} C_{jN} + \frac{15}{4} C_{jP} + C_L \tag{59}$$

5 Static Power

5.1 Theoretical Analysis

The static power can be evaluated as shown below:

$$P_{static} = V_{DD} \cdot I_{leak} \quad [W] \tag{60}$$

where I_{leak} is the total leakage current and V_{DD} is the supply voltage. For the leakage current we consider two factors:

- **I_{OFF} - Subthreshold current**: is the leakage current that flows drain-source when $V_{GS} = 0$ and $|V_{DS}| = V_{DD}$ as shown in figure 4.

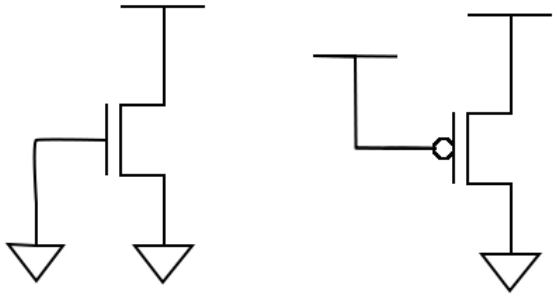

Figure 4: Leakage drain/source current when MOS are off

- **I_{GATE} - Gate Current**: is the leakage current that flows from drain and source to gate or vice versa when $|V_{GS}| = V_{DD}$ and $V_{DS} = 0$ as can be seen in fig 5. Also in other condition a small gate current could appear but is possible to say that in those other cases the contribution is negligible.

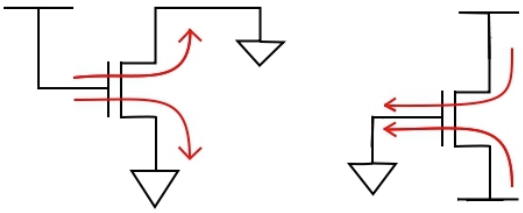

Figure 5: Leakage gate current

5.2 Static power calculation

As example the detailed procedure used to estimate the static power of the *AND2* is fully explained. Assuming that all the signal switches are immediate is possible to consider the gates into two static condition:

- **Precharge**:
  when the clock is at *zero*; the line is precharged at V_{DD} so the goes at *GND*.
  So considering all the structure:

$$I_{leakDAND2}^{precharge} = I_{OFFp}W_P + I_{GATEp}W_P + I_{OFFn}3W_N + I_{GATEn}W_N \quad [nA] \tag{61}$$

- **Evaluate**:
  when the clock is at *one*; the output is evaluated from the inputs.
  Every possible combination of the two inputs are considered and for each of those cases the different appearing leakages contribution are taken into account.
  To simplify the leakage current due by the dynamic structure is separated from the one due by the inverter. Notice that this contribution must be added because as told in the section 2 is an essential part of the gate. The table 1 shows as before this analysis.

A	B	Y	LEAKEAGE CURRENT (logic)	LEAKEAGE CURRENT (inverter)
0	0	0	$I_{OFFn}3W_N + I_{GATEn}3W_N$	$I_{OFFp}W_P + I_{GATEn}W_N$
0	1	0	$I_{OFFn}3W_N + 2 \cdot I_{GATEn}3W_N$	$I_{OFFp}W_P + I_{GATEn}W_N$
1	0	0	$I_{OFFn}3W_N + I_{GATEn}3W_N$	$I_{OFFp}W_P + I_{GATEn}W_N$
1	1	1	$I_{OFFp}W_P + 3 \cdot I_{GATEn}3W_N$	$I_{OFFn}W_N + I_{GATEp}W_P$

Table 1: Leakage current contributes for each combination of inputs

  Adding all those terms and exploiting the mean value:

$$I_{leakDAND2}^{evaluate} = \frac{1}{4} \cdot (4 \cdot I_{OFFp}W_P + I_{GATEp}W_P + 10 \cdot I_{OFFn}W_N + 24 \cdot I_{GATEn}W_N) \quad [nA] \tag{62}$$

Assuming that those states occupy an half of the period each, is possible to say that half of the time the logic is in one condition, half in the other, so the to total static current is:

$$I_{leakDAND2} = \frac{1}{2} \cdot I_{leakDAND2}^{precharge} + \frac{1}{2} \cdot I_{leakDAND2}^{evaluate} \tag{63}$$

and so:

$$I_{leakDAND2} = \frac{1}{2} \cdot \frac{1}{4} \cdot (5 \cdot I_{OFFp}W_P + 2 \cdot I_{GATEp}W_P + 13 \cdot I_{OFFn}W_N + 25 \cdot I_{GATEn}W_N) \quad [nA] \tag{64}$$

Exploiting the same analysis is possible to found an expression for the static current for all the other gates. Only the final expression are reported below.

- **AND3-Dynamic**:
  $I_{leakDAND3} = \frac{1}{2} \cdot \frac{1}{8} \cdot (9 \cdot I_{OFFp} W_P + 2 \cdot I_{GATEp} W_P + 33 \cdot I_{OFFn} W_N + 68 \cdot I_{GATEn} W_N) \quad [nA]$
- **AND4-Dynamic**:
  $I_{leakDAND4} = \frac{1}{2} \cdot \frac{1}{16} \cdot (17 \cdot I_{OFFp} W_P + 2 \cdot I_{GATEp} W_P + 81 \cdot I_{OFFn} W_N + 161 \cdot I_{GATEn} W_N) \quad [nA]$
- **OR2-Dynamic**:
  $I_{leakDOR2} = \frac{1}{2} \cdot \frac{1}{4} \cdot (5 \cdot I_{OFFp} W_P + 4 \cdot I_{GATEp} W_P + 7 \cdot I_{OFFn} W_N + 18 \cdot I_{GATEn} W_N) \quad [nA]$
- **OR3-Dynamic**:
  $I_{leakDOR3} = \frac{1}{2} \cdot \frac{1}{8} \cdot (9 \cdot I_{OFFp} W_P + 8 \cdot I_{GATEp} W_P + 11 \cdot I_{OFFn} W_N + 42 \cdot I_{GATEn} W_N) \quad [nA]$
- **OR4-Dynamic**:
  $I_{leakDOR4} = \frac{1}{2} \cdot \frac{1}{16} \cdot (17 \cdot I_{OFFp} W_P + 16 \cdot I_{GATEp} W_P + 18 \cdot I_{OFFn} W_N + 98 \cdot I_{GATEn} W_N) \quad [nA]$

6 Octave Implementation

In table 2 the variables used into the modules are reported and in table 3 there are the output parameters estimates.

Code variable	Source file	Physical quantity
Lgate	Technology file	nm
Wgate	Technology file	μm
Vdd	Technology file	V
Xj	Technology file	nm
Cox	Technology file	F/cm^2
Cj0n	Technology file	$pF/\mu m^2$
Cjswn	Technology file	$pF/\mu m^2$
Cj0p	Technology file	$pF/\mu m^2$
Cjswp	Technology file	$pF/\mu m^2$
Cgd0n	Technology file	F/m
Cgd0p	Technology file	F/m
Gamma	Technology file	–
Mjn	Technology file	%
Mjp	Technology file	%
Mswn	Technology file	%
Mswp	Technology file	%
Pbn	Technology file	V
Pbp	Technology file	V
Pbswn	Technology file	V
Pbswp	Technology file	V
mueff_n	Mobility module	cm^2/Vs
mueff_p	Mobility module	cm^2/Vs
Vth_n	Vth module	V
Vth_p	Vth module	V
Ioff_n	Ioff module	$\mu A/\mu m$
Ioff_p	Ioff module	$\mu A/\mu m$
Igate_n	Igate module	$\mu A/\mu m$
Igate_p	Igate module	$\mu A/\mu m$

Table 2: Variables required and used by the module

Code variable	Physical quantity	Meaning
Delay_nand_and	ns	input to output delay of selected module
Pnand_and_dyn	W	Dynamic power of selected module
Pnand_and	W	Static power of selected module

Table 3: Variables provided in output of selected module

6.1 Text Results

An example of the output provided by the TAMTAMS analysis using the *Print text results* is provided below. The computed values of delay, dynamic and static power are reported for four possible value of *Fan Out* where this quantity just means the number of inverter considered as output load for the gate.

```
Technology: bulk/HP_2005

System Setup: 2016-04-17 13:37:08
Cox =  2.8776e-06
Vtlong =  0.61691
SCE =  0.18990
DIBL =  0.24118
mueff_n =  252.01
mueff_p =  61.319
Ecrit_n =  7.9360e+04
Ecrit_p =  3.2616e+05
Vdsat_n =  0.15325
Vdsat_p =  0.41401
Cdep =  5.0656e-07
m =  1.2831

Module 0 : Delay_Pow_and2_dyn

Fan Out = 1:
I/ODelay[ns]  DynPower[W]  StaticPower[W]
  1.2092e+01   3.0145e-06   4.4364e-09

Fan Out = 2:
I/ODelay[ns]  DynPower[W]  StaticPower[W]
  1.2971e+01   3.2121e-06   4.4364e-09

Fan Out = 3:
I/ODelay[ns]  DynPower[W]  StaticPower[W]
  1.3851e+01   3.4096e-06   4.4364e-09

Fan Out = 4:
I/ODelay[ns]  DynPower[W]  StaticPower[W]
  1.4730e+01   3.6072e-06   4.4364e-09
```

6.2 Graphical Results

Using the *Show graphical results* three different graph are provided as output. The first one represents the delay; an example is reported in fig. 6. There are four different lines, one for each value of *Fan Out*.
The figure 7 shows the second graph provided and it represent the dynamic power.
The last graph shows the static power (fig. 8). This value does not depends on output load so all the lines are overlapped.

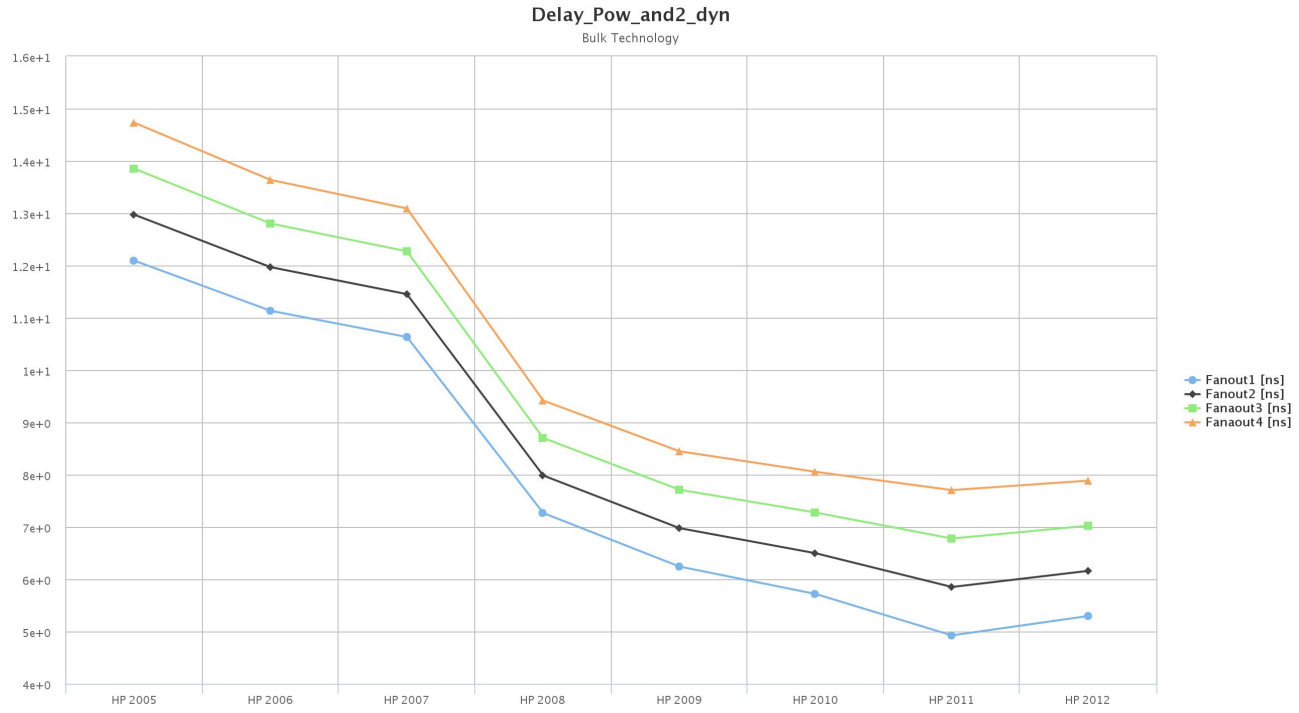

Figure 6: Delay graphical output

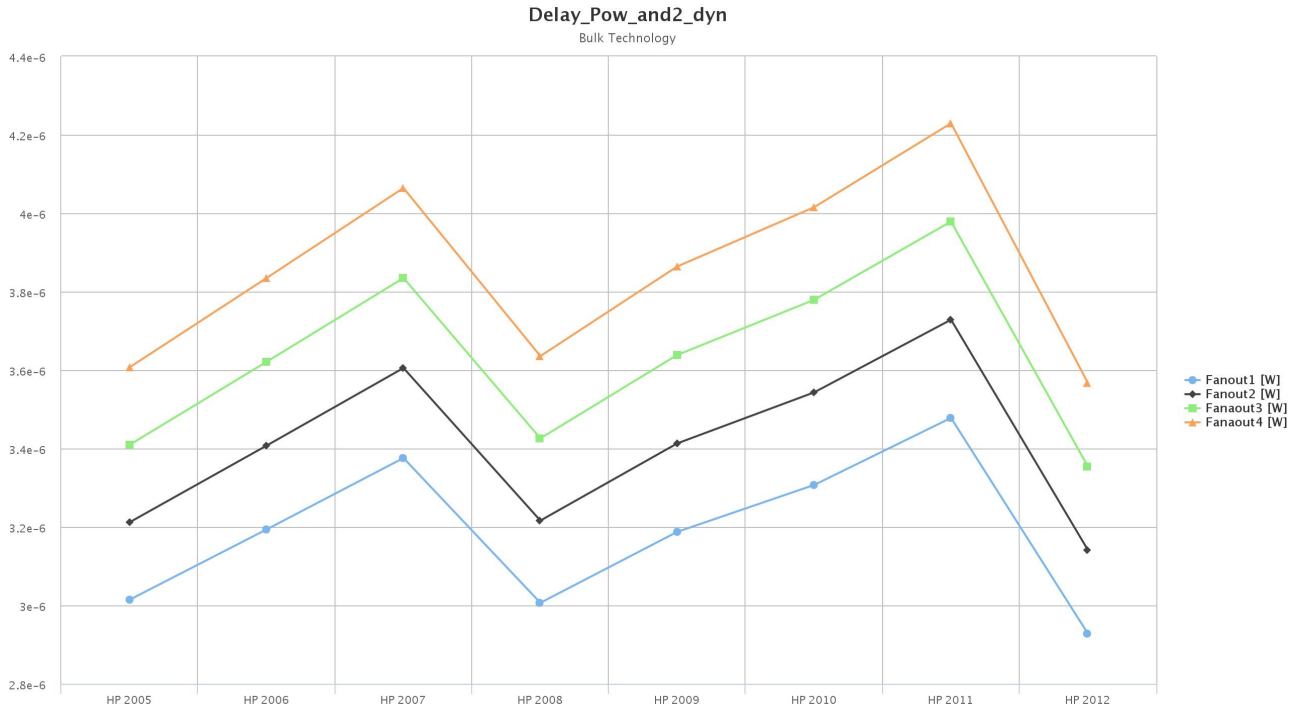

Figure 7: Dynamic power graphical output

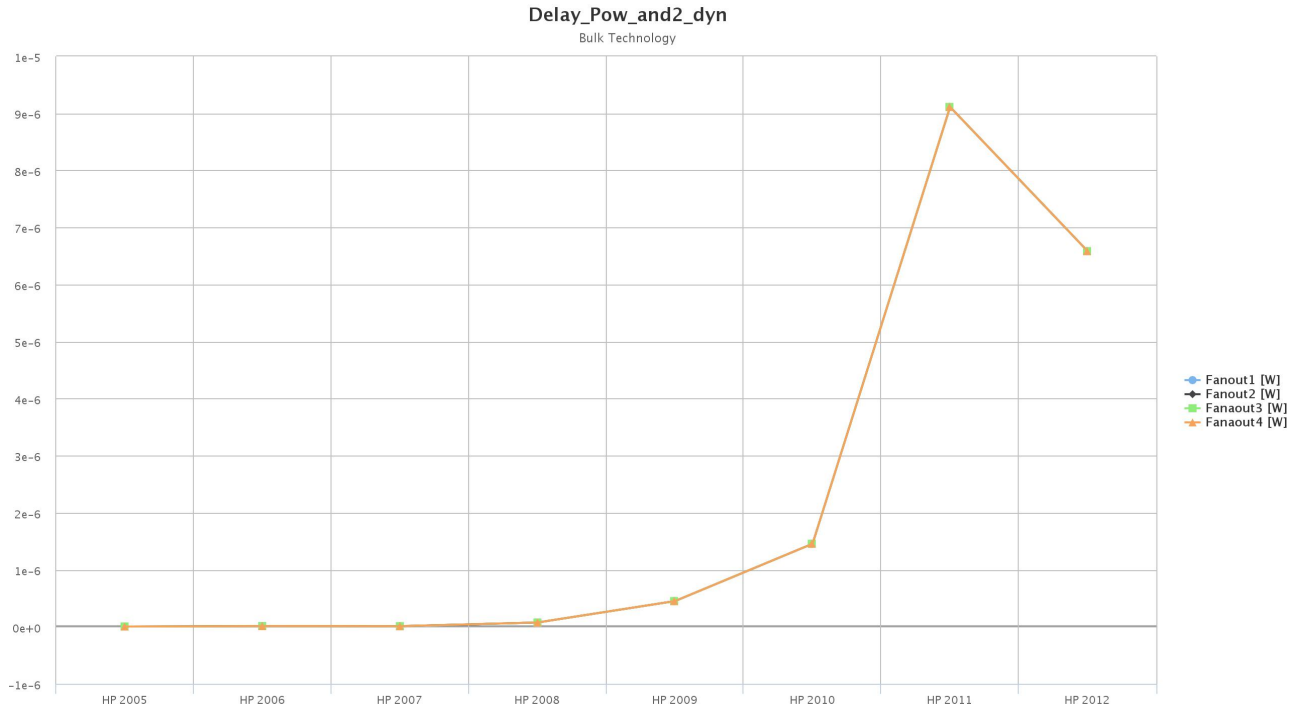

Figure 8: Static power graphical output