A Novel Leakage Reduction DOIND Approach For Nanoscale Domino Logic Circuits

Ambika Prasad Shah[1], Vaibhav Neema[2], Shreeniwas Daulatabad[3]
[1,2,3] Electronics & Telecommunication Engineering Department
IET- Devi Ahilya University, Indore- 452017, INDIA
ambika_shah@rediffmail.com[1], vaibhav.neema@gmail.com[2], shreedaulty@gmail.com[3]

***Abstract*— Dynamic CMOS logic circuits are used in modern VLSI circuits because of its high system performance and its performance is high due to higher speed over static CMOS circuit. However dynamic logic circuit has less noise immunity and increased leakage power dissipation. Increase in leakage current combine with reduced noise margin results in performance degradation of dynamic circuits.**

In this paper DOIND logic approach is proposed for domino logic which reduces the leakage current with minimum delay penalty. Simulation is performed at 70 nm technology node for a domino logic and DOIND logic buffer using tanner EDA tool. Simulation results shows that proposed DOIND approach decreases the leakage current 93.3%, static power 93.3% and static energy 86.66% at supply voltage 1.15V. Proposed circuit also improves dynamic power 60.78%, dynamic energy delay product (EDP) 62.18% and dynamic power delay product (PDP) 62.07% at 1.15V supply voltage.

Keywords*— Domino logic, subthreshold leakage, Deep Submicron, Transistor staking, PDP, EDP, Precharge, Evaluation

I. INTRODUCTION

Dynamic logic circuits are widely used in modern digital VLSI circuits because of supreme speed and area characteristics of dynamic CMOS logic circuits as compare to static CMOS logic circuits. However dynamic CMOS logic circuits have less immune to noise and increased power dissipation than static CMOS logic circuit. The lower value of noise margin makes dynamic CMOS logic circuits more sensitive to noise as compare to static CMOS logic circuit. With the increasing rigorous noise requirement and leakage current due to hostile technology scaling, the noise tolerance and less leakage dynamic circuits has to be improved the reliable operation of VLSI system designed using very deep submicron process technology. As technology scales down the leakage current increases therefore as continue scaling of transistor dimensions in nanoscale regime, it is required to design the circuit which mitigate leakage current.

In this paper domino logic and DOIND logic based buffer is used to analyze different parameters. Proposed DOIND logic technique has less leakage current as compare to domino logic CMOS buffer. Organization of this paper is as follows: Section II describes the previous work related to leakage reduction in domino logic circuit. Section III describes the DOIND logic and its characteristics. Section IV presents the simulation results followed by the conclusion in section V.

II. RELATED WORK

There are several techniques to control leakage current at transistor level design in domino logic circuits. Body biasing is one of the techniques to reduce leakage current of circuit.

INDEP approach [1] is the technique which mitigates the leakage current in nanoscale circuit. This technique has two extra inserted transistors between pull up and pull down networks which are input logic dependent.

Sleepy keeper approach [2] uses two weak keeper transistors which are connected parallel to the sleep transistors and gate of both sleepy keepers is controlled by output voltage.

Dual threshold voltage domino logic [3] has low threshold voltage transistors and high threshold voltage transistors. Low threshold voltage transistors are connected in critical path which improve the performance and high threshold voltage transistors are connected in non critical path to mitigate le leakage current.

Dual threshold voltage with sleep switch domino logic [4] has same configuration as dual threshold voltage domino logic except an extra high threshold voltage transistor is connected between dynamic node and ground.

Variable threshold voltage keeper [5] is another leakage reduction technique in domino logic circuits.

Leakage biased domino circuit [6] maintains high speed of circuit with fine grain leakage reduction.

III. DOIND LOGIC

For high performance integrated circuits the critical paths are often implemented with domino logic circuits. The operating principles of domino logic circuits are reviewed in this section. To reduce leakage current in domino logic circuit proposed DOIND logic is also reviewed.

A. Domino Logic Circuit

A standard domino logic circuit is shown in fig. 1. The operation of domino circuits is in the following manner. When the clock signal is low, the domino logic circuit is in precharge phase. During precharge phase, the node N1 is charged to Vdd through MP1. Vout of the circuit is low which turn on the keeper transistor (MP2). When the clock signal is high, the circuit enters into the evaluation phase. In this phase according to the input combination of pull down network dynamic node N1 is discharged to ground or remain high. During the

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evaluation phase, output voltage of inverter can make at most one transition from 0 to 1.

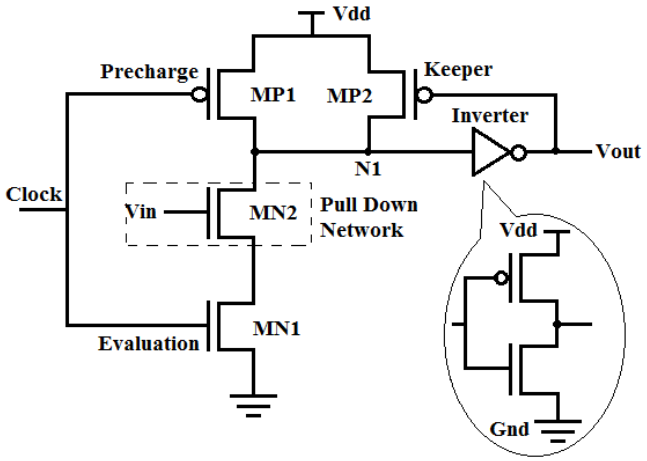

Fig. 1: Domino Logic circuit based buffer

To avoid cascading and charge sharing problem, inverter and week keeper transistor are respectively used. Performance degrades by adding keeper transistor. Upsizing the keeper transistor improves robustness at the cost of delay and power dissipation and small sized keeper is desired for high speed application. Means there is trade off between delay and power to improved noise and leakage immunity.

B. DOIND Logic Circuit

A proposed DOIND (**DO**mino logic with Clock and **IN**put **D**ependent transistors) logic circuit is shown in fig. 2. It has two DOIND transistors MP3 (PMOS) and MN3 (NMOS) connected between A and B. Gate terminal of DOIND transistors (MP3 and MN3) are V0 and V1 which are clock and input logic dependent respectively. Body terminal of all PMOS transistors are connected to Vdd and Body terminal of all NMOS transistors are connected to Gnd.

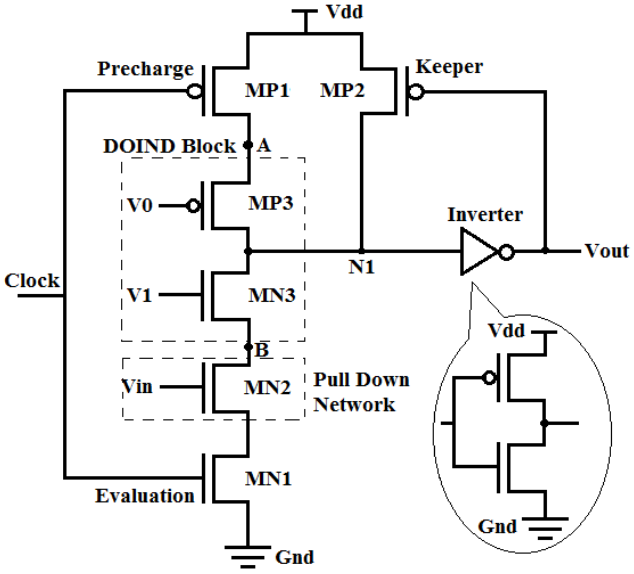

Fig. 2: DOIND Logic circuit based buffer

When the clock signal is low, then V0 should be 0 (low) so that MP1 and MP3 is turn on and the DOIND logic circuit comes in precharge phase. During precharge phase, the node N1 is charged to Vdd through MP1and MP3. Vout of the circuit is low which turn on the keeper transistor (MP2). When the clock signal is high, the circuit enters into the evaluation phase. In evaluation phase, when input Vin = 1 (high) then V1 should be 1 so that dynamic node N1 becomes 0 and when input Vin = 0 (low) then V1 should be 0 so that dynamic node N1 becomes 1. Operating status of each transistor is given in table I.

TABLE I. OPERATING STATUS OF THE TRANSISTORS IN THE DOIND LOGIC BUFFER

Clock	MN1	MP1	Input(Vin)	MN2	MP2	MN3	MP3
Logic 0	OFF	ON	Logic 0	OFF	ON	OFF	ON
Logic 0	OFF	ON	Logic 1	ON	ON	OFF	ON
Logic 1	ON	OFF	Logic 0	OFF	ON	OFF	OFF
Logic 1	ON	OFF	Logic 1	ON	OFF	ON	OFF

Fig. 3 shows DC characteristics of domino logic and DOIND logic based CMOS buffer in which the graph clearly shows that DOIND logic based circuit has better response than domino logic based circuit.

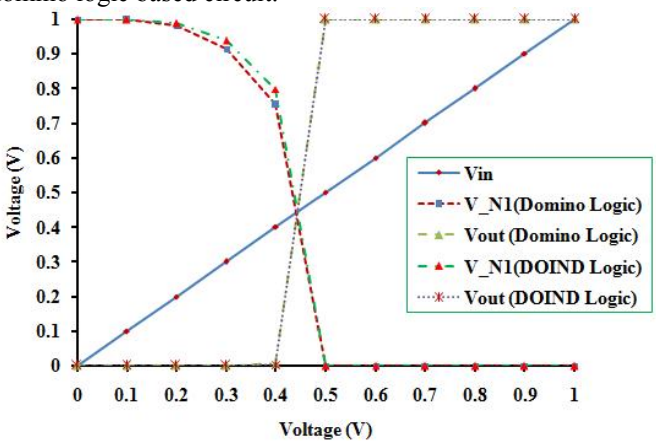

Fig. 3: DC characteristics of Domino logic and DOIND logic based buffer.

IV. SIMULATION RESULTS

The TSPICE simulator is used for study of domino logic and DOIND logic with different supply voltage. All the experimental data were obtained at 70 nm technology node. Channel width and channel length are same for NMOS transistors which is equal to technology node and channel width of all PMOS is 2X of channel length except keeper transistor. Channel length of keeper transistor is 5X and width is 2X of technology node. 20 MHz clock frequency (*f*) has been taken for the simulation.

As delay and leakage current of the circuit is a function of supply voltage. We have taken ±30% variation of supply voltage from its nominal value. All the parameters are given in table- II and III

A. *Effect on Leakage current*

As Supply voltage (Vdd) scaling threshold voltage (Vth) also scale which cause performance degradation with some leakage current penalty. The relation between leakage current and threshold voltage is given by[7][8]:

$$I_{Leakage} = I_0 \frac{(V_{gs} - V_{th})}{\eta V_t}\left(1 - exp\frac{-V_{ds}}{V_t}\right)$$

Where $I_0$is saturation current, Vgs is gate to source voltage, Vt is thermal equivalent voltage, Vds is drain to source voltage and η is sub-threshold slope factor.

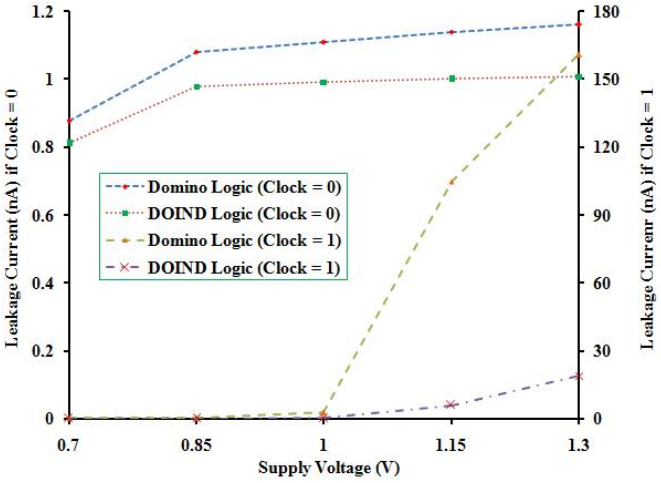

Fig. 4: Leakage current for Clock = 0 and Clock = 1.

Fig. 4 shows that DOIND logic circuit has less leakage current as compare to domino logic circuit for different supply voltage with both Clock = 0 and Clock = 1.

B. *Effect on static power*

Fig. 5 shows DOIND logic circuit has better in static power control with different supply voltage as compare to domino logic circuit for both Clock = 0 and Clock = 1. Static power for domino logic with Clock = 1 increases rapidly if supply voltage is greater than 1V.

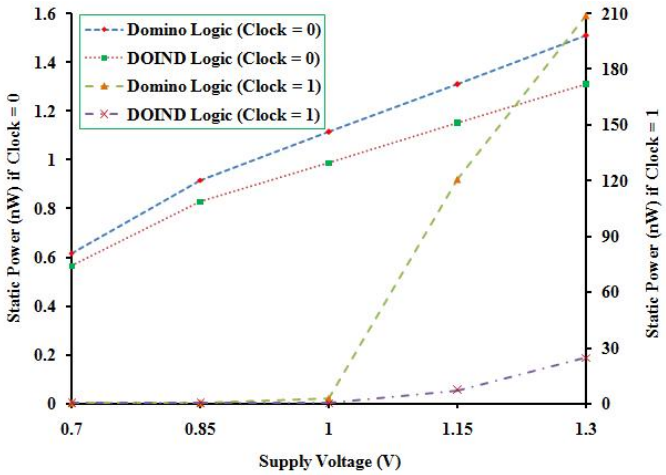

Fig. 5: Static power for Clock = 0 and Clock = 1.

C. *Effect on static energy*

Static energy component is proportional to Vdd whereas dynamic energy component is proportional to square of Vdd. Static and dynamic energy component is given by:

$$E_{dynamic} = \propto C_L V_{dd}^2$$
$$E_{static} = I_{leakage} V_{dd} T_{delay}$$

where α is transition activity, C_L is load capacitance, $I_{leakage}$ is leakage current, T_{delay} is circuit delay

Fig. 6 shows that static energy is less for DOIND logic circuit for Clock = 0 and Clock = 1 as compare to domino logic circuit.

TABLE II. DIFFERENT PERFORMANCE METRICS FOR DOMINO LOGIC AND DOIND LOGIC CIRCUITS

Technique →		**Domino Logic**					**DOIND Logic**				
Supply Voltage (V)→		**0.7**	**0.85**	**1**	**1.15**	**1.3**	**0.7**	**0.85**	**1**	**1.15**	**1.3**
Leakage Current (nA)	**Clock = 0**	0.88	1.08	1.11	1.14	1.16	0.81	0.98	0.99	1.00	1.01
	Clock = 1	0.36	0.40	2.83	104.89	160.79	0.17	0.18	0.29	6.09	18.96
Static Power (nW)	**Clock = 0**	0.61	0.92	1.12	1.31	1.51	0.57	0.83	0.99	1.15	1.31
	Clock = 1	0.26	0.34	2.83	120.60	209.04	0.12	0.15	0.29	7.00	24.65
Static Energy (aJ)	**Clock = 0**	2.66	3.95	4.83	5.88	6.65	2.43	3.56	4.24	4.98	5.61
	Clock = 1	1.10	1.47	12.28	54.08	91.88	0.52	0.64	1.25	3.03	10.55
Dynamic Power (nW)		47.44	81.47	116.40	452.26	1105.81	61.50	85.05	131.76	177.36	601.25
Dynamic EDP (yJ×sec)		10.27	17.54	25.22	101.39	243.04	13.20	18.24	28.16	38.34	128.62
Dynamic PDP (fJ)		0.21	0.35	0.50	2.03	4.86	0.26	0.36	0.56	0.77	2.57

TABLE III. COMPARISION OF PERFORMANCE METRICS FOR DOMINO LOGIC AND DOIND LOGIC CIRCUITS

Performance metric ↓	Supply Voltage (V) →	0.7	0.85	1	1.15	1.3
Average Leakage Current (nA)	Domino Logic	0.62	0.74	1.97	53.02	80.98
	DOIND Logic	0.49	0.58	0.64	3.55	9.98
	% Improve	**20.97%**	**21.62%**	**67.5%**	**93.3%**	**87.68%**
Average Static Power (nW)	Domino Logic	0.43	0.63	1.97	60.96	105.28
	DOIND Logic	0.34	0.49	0.64	4.08	12.98
	% Improve	**20.93%**	**22.22%**	**67.51%**	**93.3%**	**87.67%**
Average Static Energy (aJ)	Domino Logic	1.88	2.71	8.56	29.98	49.27
	DOIND Logic	1.47	2.1	2.74	4	8.08
	% Improve	**21.8%**	**22.5%**	**67.99%**	**86.66%**	**83.6%**
Dynamic Power (nW)	Domino Logic	47.44	81.47	116.4	452.26	1105.81
	DOIND Logic	61.5	85.05	131.76	177.36	601.25
	% Improve	**-29.63%**	**-4.39%**	**-13.2%**	**60.78%**	**45.63%**
Dynamic EDP (yJ×sec)	Domino Logic	10.27	17.54	25.22	101.39	243.04
	DOIND Logic	13.2	18.24	28.16	38.34	128.62
	% Improve	**-28.53%**	**-3.99%**	**-11.66%**	**62.18%**	**47.08%**
Dynamic PDP (fJ)	Domino Logic	0.21	0.35	0.5	2.03	4.86
	DOIND Logic	0.26	0.36	0.56	0.77	2.57
	% Improve	**-23.8%**	**-2.86%**	**-12%**	**62.07%**	**47.12%**

$$\%\ \boldsymbol{Improve} = \frac{\boldsymbol{Domino\ logic\ value - DOIND\ Logic\ value}}{\boldsymbol{Domino\ logic\ value}} \times \mathbf{100}\%$$

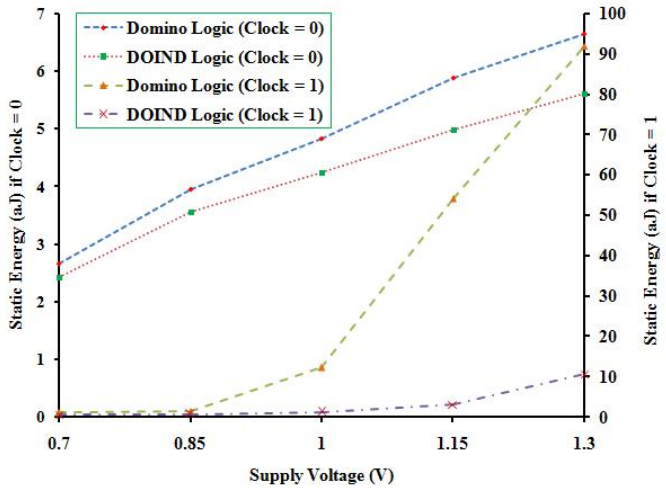

Fig. 6: Static energy for Clock = 0 and Clock = 1.

D. Effect on dynamic power

Dynamic power is proportional to square of Vdd. dynamic power component is given by:

$$P_{dynamic} = \propto C_L f V_{dd}^2$$

Fig. 7 shows that dynamic power is less for DOIND logic circuit as compare to domino logic circuit.

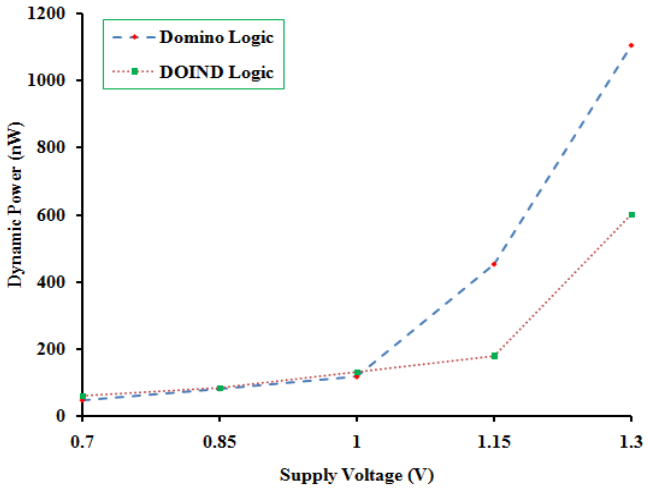

Fig. 7: Dynamic power with different supply voltage.

E. Effect on dynamic EDP and dynamic PDP

To design energy efficient circuit in low power application energy delay product and power delay product are important parameters. EDP and PDP of any circuit should be as small as possible for low power circuit design.

Dynamic energy delay product (EDP) and dynamic power delay product (PDP) is given by:

$$EDP_{dynamic} = E_{dynamic} \times T_{delay}$$

$$PDP_{dynamic} = E_{dynamic} \times Clock\ Frequency \times T_{delay}$$

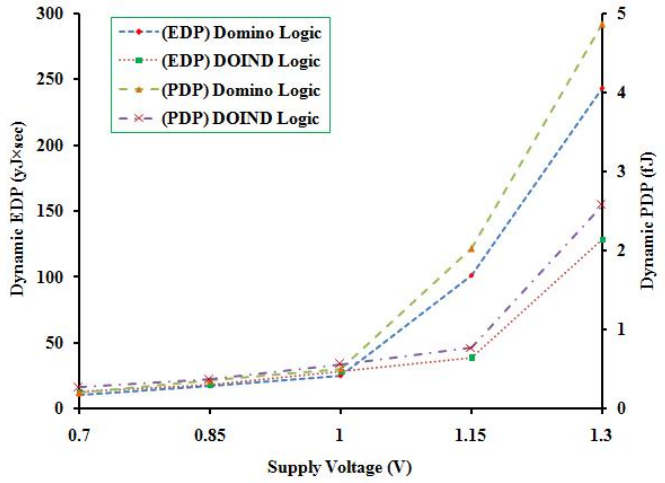

Fig. 8: Dynamic EDP and dynamic PDP with different supply voltage.

Fig. 8 shows that dynamic EDP and dynamic PDP for DOIND logic circuit and domino logic circuit are approximately equal upto supply voltage 1V and they increases rapidly above supply voltage 1.15V. It can also observe that rate of change in EDP and PDP is more for domino logic as compare to DOIND logic circuit.

V. CONCLUSION

This paper presents the comparative analysis of different parameters for domino logic and DOIND logic based buffer circuit. DOIND logic circuit has reduction in average leakage current 93.3%, average static power 93.3% and average static energy 86.66% for the supply voltage 1.15V. DOIND logic circuit gives better control on dynamic power, dynamic EDP and dynamic PDP. Dynamic power of domino logic increase 60.78% at 1.15V of supply voltage.

We can also observe that EDP and PDP increase rapidly for domino logic above supply voltage 1V. Dynamic EDP and PDP are in control up to 62.18% and 62.07% respectively for DOIND logic at supply voltage 1.15V.

Dynamic power, dynamic EDP and dynamic PDP are less for domino logic if supply voltage is less than or equal to 1V. Reason for increase in EDP and PDP is delay offered by DOIND logic. As these parameters are function of delay and it dominates up to supply voltage 1V

Simulation results also shows that DOIND logic has better performance and less effect of supply voltage variations on different parameters as compare to domino logic circuit.

REFERENCES

[1] V.K. Sharma, M. Pattanaik and B.Raj, "INDEP approach for leakage reduction in nanoscale CMOS circuits," International Journal of Electronics, vol. 102,no. 2, 2015, pp. 200-215.

[2] S.H. Kim and V.J. Mooney, "Sleepy keeper: A New approach to low leakage power VLSI Design," IFIP International Conference on very Large Scale Integration; 2006. pp. 367-372.

[3] J. Kao, "Dual Threshold Voltage Domino Logic," Procedings of 25th European Conference on Solid State Circuits , 1999, pp. 118-121.

[4] V. Kursun and E.G. Friedman, "Sleep Switch Dual Threshold Voltage Domino Logic With reduced Standby leakage Current," IEEE Trans VLSI System, vol. 12, no. 5, May 2004, pp. 485–496.

[5] V. Kursun and E.G. Friedman, "Domino logic with variable threshold Voltage Keeper," IEEE Trans VLSI System, vol. 11, no. 6, Dec 2003, pp. 1080–1093.

[6] S. Heo and K. Asanovic, "Leakage Biased Domino Circuits for Dynamic Fine- Grain leakage reduction," The 2002 Symposium on VLSI Circuits, Honolulu, HI, 2002, pp.316-319.

[7] H. Al-hertani, D. Al-Khalili and C. Rozon, "UDSM Subthreshold Leakage Model for NMOS Transistor Stacks," Microelectronics Journals, Vol 39, no. 12, 2008, pp. 1809-1816.

[8] B. S. Deepaksubramanyam and A. Nunez, "analysis of subthreshold leakage reduction in cmos digital circuits" Proceding of 50th Midwest Symposium on Circuits and Systems (MWSCAS 2007), Aug. 2004, pp. 1400- 1404.