1 A Dynamic CMOS Survey

Along with the work of the two adder designs, a brief survey about dynamic logic is made. The main issue is to find whether there are new dynamic logic technologies that can be used in adders, instead of the standard static MOS structure. The main characteristics of dynamic logic are introduced and discussed, in order to understand the positive and negative aspects of this design technique. For further general information [1] can be seen.

1.1 General aspects

Dynamic logic is an alternative design approach of Pseudo NMOS and static CMOS and presents several advantages similar to these ones. Figure 1 shows the general schematic of a dynamic logic topology. In this case a pull down network is used, just like the static CMOS logic, but the dual pull up network can be used instead.

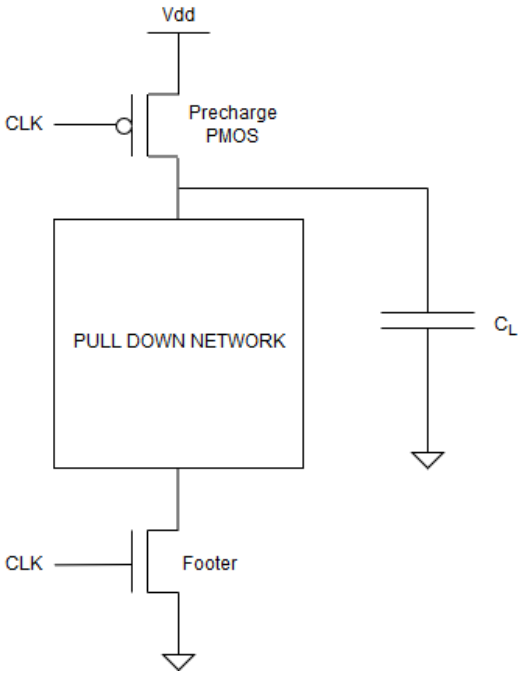

Figure 1: Dynamic logic general schematic.

The first positive feature is the less area occupation: the number of transistors increases linearly with the number of inputs. A generic dynamic N port gate has N+2 transistors, which is close to the pseudo NMOS design, and less than the static CMOS logic, which is 2N. The first N transistors are needed to implement the Pull Down (or Up) Network, while a PMOS and NMOS are used for the clock signal. The clock signal is needed to define the two working phases of the circuit, the pre-charge and the evaluation phases.

Another important aspect is the absence of static power consumption, unlike pseudo NMOS but similar to the static CMOS logic. The static power is the generated power due to short path between supply voltage and ground.

Furthermore, the circuit presents a lower fan-in with respect to the static CMOS implementation, and this aspect leads dynamic logic to better performance. These features together makes dynamic logic suitable for high performance and low cost implementation.

The dynamic logic presents several drawbacks, though. The need of a clock signal affects negatively power consumption, since at least two transistors are charged and discharged in each clock cycle. Power consumption is also affected by an activity factor $\alpha_{1\to 0}$ higher than the static CMOS. For example, if all the inputs of a NOR gate have a uniform statistic distribution, the activity factor of the dynamic logic and static logic implementations are, respectively the (1) and (2):

$$\alpha_{dynamic} = 75\% \tag{1}$$

$$\alpha_{static} = 18,75\% \tag{2}$$

The dynamic power consumption is given by the (3):

$$P_{dyn} = \alpha \cdot C_L V_{dd}^2 f_{clk} \tag{3}$$

which is proportional to the activity factor. Leakage currents are to be considered also, since they can discharge the output node, and determine the minimum period between two pre-charge phases, which is the minimum clock frequency accepted. This value is about some KHz. Leakage currents tend to discharge the output node, since this one is an high impedance node. This problem can be resolved by using a *bleeder* transistor [1].

Another aspect to be considered is the charge sharing with other output and with the clock signal (*clock feedthrough*) which affects dramatically reliability. The latter can forward bias the drain-bulk junction of the pre-charge MOS which can switch the high impedance node voltage from '1' to '0' or, worse, cause *latch-up*.

1.2 Domino design techniques

An evolution of dynamic logic is the Domino one, which was first described by [2]. Figure 2 shows the schematic of a single stage Domino circuit.

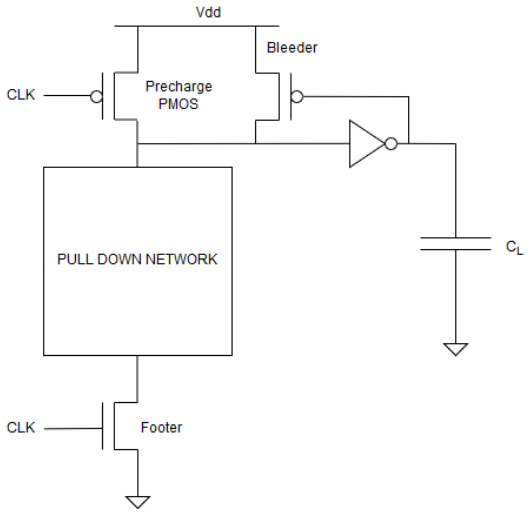

Figure 2: General schematic of domino logic circuit. The bleeder transistor is optional but highly recommended, in order to avoid information loss due to leakage currents.

The main advantage is that Domino circuits can be placed in multiple stages with the same topology and can be pipelined with multiphase clocking system [3] instead of using latches. At architectural level, the adoption of multiphase clocking prevent the use High performance are reached at the expense of higher power consumption due to the more clock lines needed.

1.3 Dual Rail Domino Logic

A particularly and interisting case of Domino logic is the Dual Rail Domino Logic (DRDL) implementation in order to make low power adders [4]. An example of Dual rail Domino circuit is reported in figure 3.

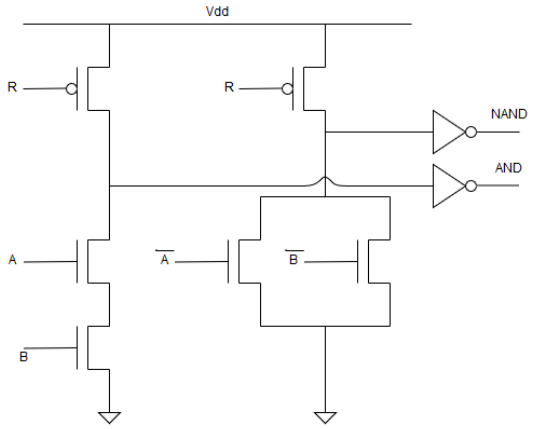

Figure 3: Dual Rail Domino logic implementation of a NAND circuit. The main advantage is to have inverting and non inverting function, at the expense of more area occupation.

In this implementation, circuit works in near threshold in order to reduce power consumption and uses an asynchronous pipeline. This approach reduces the energy-delay product, defined as:

$$EDP = E_{op} \times \tau_{delay} \tag{4}$$

where E_{op} is the energy drained by the device during the SPICE simulation and τ_{delay}. Although there is an improvement in energy consumption, performance and area become worse than a synchronous pipelined static CMOS implementation. Energy consumption, number of transistors and delay of [4] are reported in table 1. The worst case is used for synchronous adder and average case for the dual rail Domino logic one.

	Transistors	Delay μs	Energy fJ
DRDL	1460	62.6	499
CMOS	764	59.3	871

Table 1: Comparison between DRDL and static CMOS 8-bit adder.

As it can be seen, energy consumption is improved with respect to CMOS at the cost of almost double area and a little worse delay.

1.4 Technology scaling comparison

An important issue is to find whether technology scaling improve significantly the Domino circuits power consumption with respect to static CMOS logic. Two interesting works are found are compared in table .

	Power	Pwr diff. with the previous gate
32 nm FinFET static NAND2 in [5]	440 nW	0 %
25 nm FinFET Domino AND2 in [6]	1.6 μW	+264 %
32 nm FinFET static NOR2 [5]	440 nW	0 %
25 nm FinFET Domino OR2 [6]	4 μW	+810 %

Despite of the use of a better technology, the Domino logic suffers for higher power consumption, compared with the static CMOS logic.

1.5 Final Considerations

Dynamic logic based circuits are a good alternative if area and performance are required. Multistage Domino circuits can be also pipelined with a multiphase clock approach, so no more latches are needed and there is more area saving. These aspects are balanced by a higher power consumption, which can be far higher than the static logic. Scaling does not improve the power consumption issue, so dynamic logic is generally not suitable for low power implementations, which is the current tendency. The Dual Rail Domino logic can be an interesting choice in case of asynchronous pipeline designs, since energy consumption is better than synchronous static implementations, although they occupy more area and have a performance similar to the static logic.

References

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