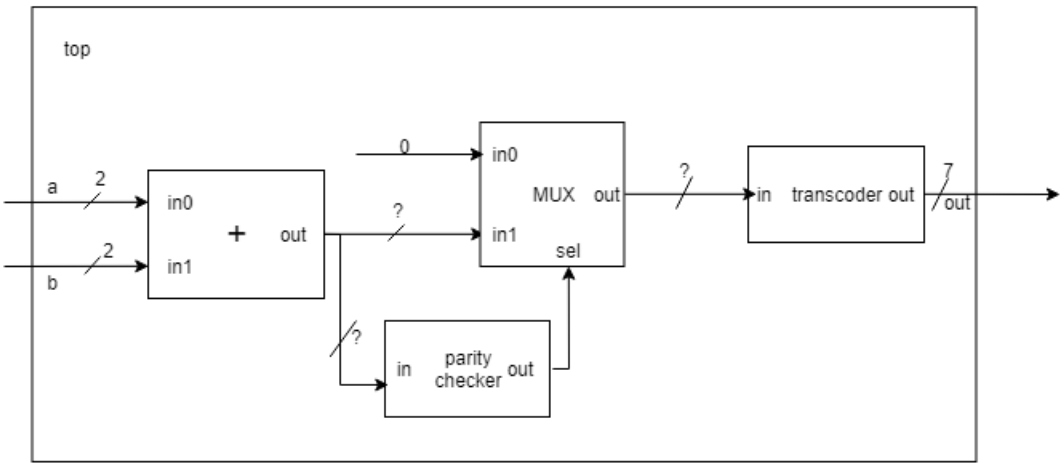
Subject:

Work time: 50m

Task:

Implement the following design in Verilog, check correct functionality using simulations and synthesize and program the design on the FPGA board.

Schema bloc:



Schematic description + particular tasks:

Ths circuit sums the 2 in puts and in the case of even result will select to display this result. If the result is odd, it will display 0 on the 7seg display.

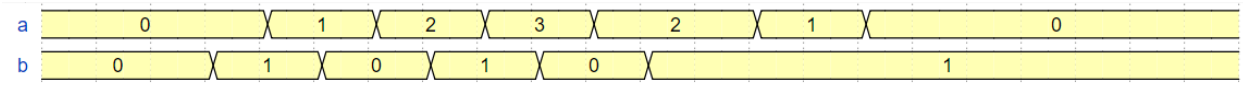
Parity checker - returns 1 if the input number is even or 0 if the number is odd.

Transcoder - transforms binary numbers into their corresponding representation on the 7segment display.

"?" - replace the question mark with the correct size for the wires. If you do not know how to obtain the size, make all sizes 10b long (you will receive reduced scoring for using this default but will at least have a compilable design).

For simulation:

Waveforms should correspond to the below diagram:



The space between the vertical dotted lines represents 5ns.

For board programming:

a - switch [1,0]

b - switch [3,2]

out - 7seg_0

Points:

Total - 20p

design - 11p

- top - 3p - interface 0.5p + instantiation 1.5p + wires + conexions 1p
- adder - 2p
- mux - 2p
- parity_checker - 2p
- transcoder - 2p

simulare - 5p

- testbench 3p - 1p instantiation + 2p correct signal generation
- simulation demonstration (show me) - 2p

board programming - 4p

- constraint file (pin planner) - 2p
- functional demonstration (show me) - 2p