ESE 370: CIRCUIT-LEVEL OPTIMIZATION FOR DIGITAL SYSTEMS

Project 2 Milestone: FIFO Queue

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Design Schematics

Top-Level Design

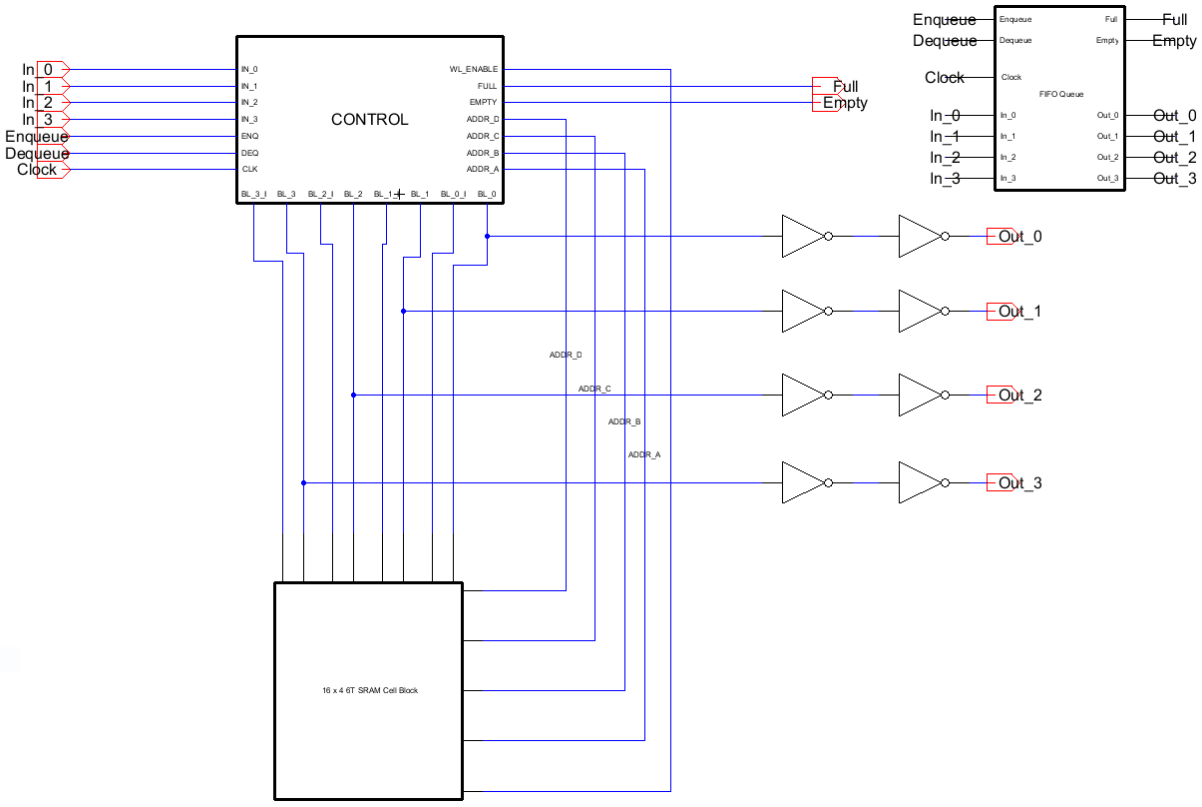

Figure 1: Queue top-level schematic

Memory Cell Block

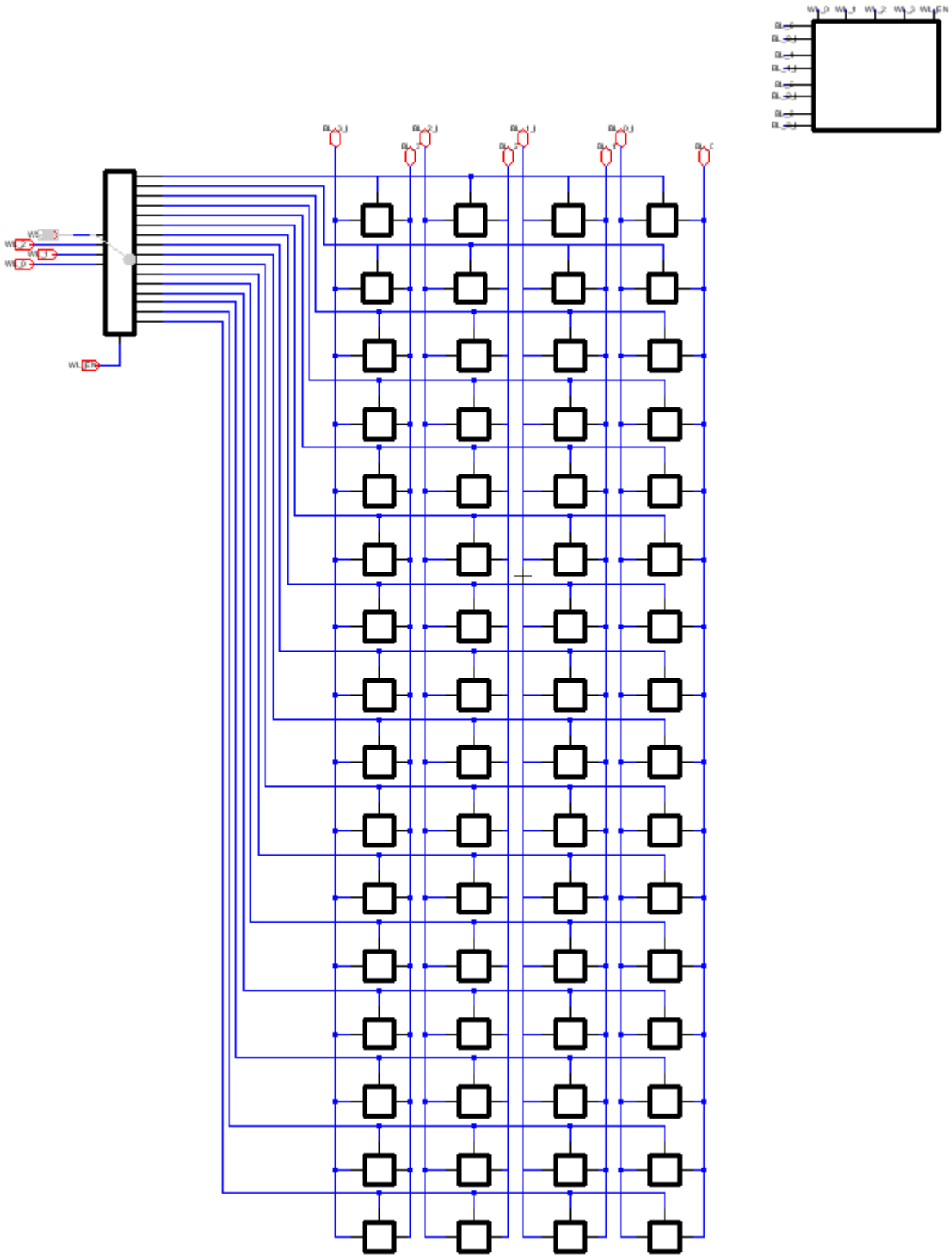

Figure 2: Memory block toplevel schematic

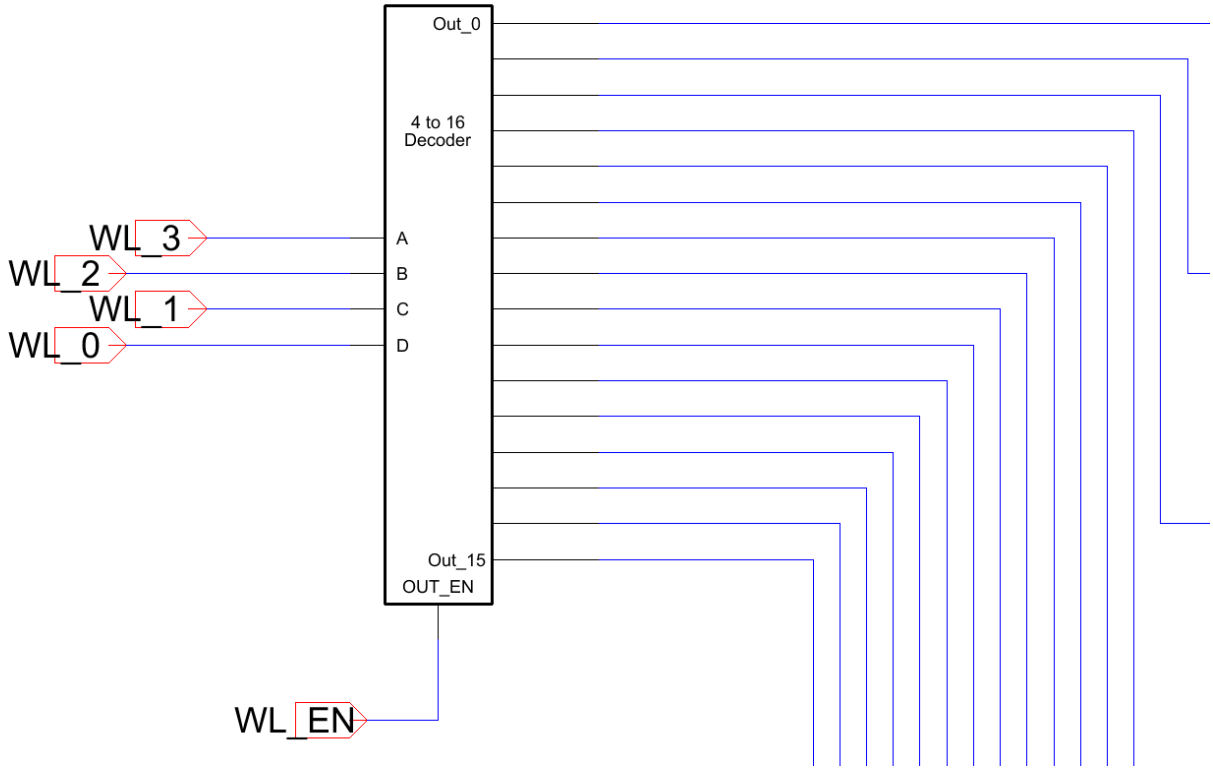

Figure 3: Memory block schematic in detail, decoder

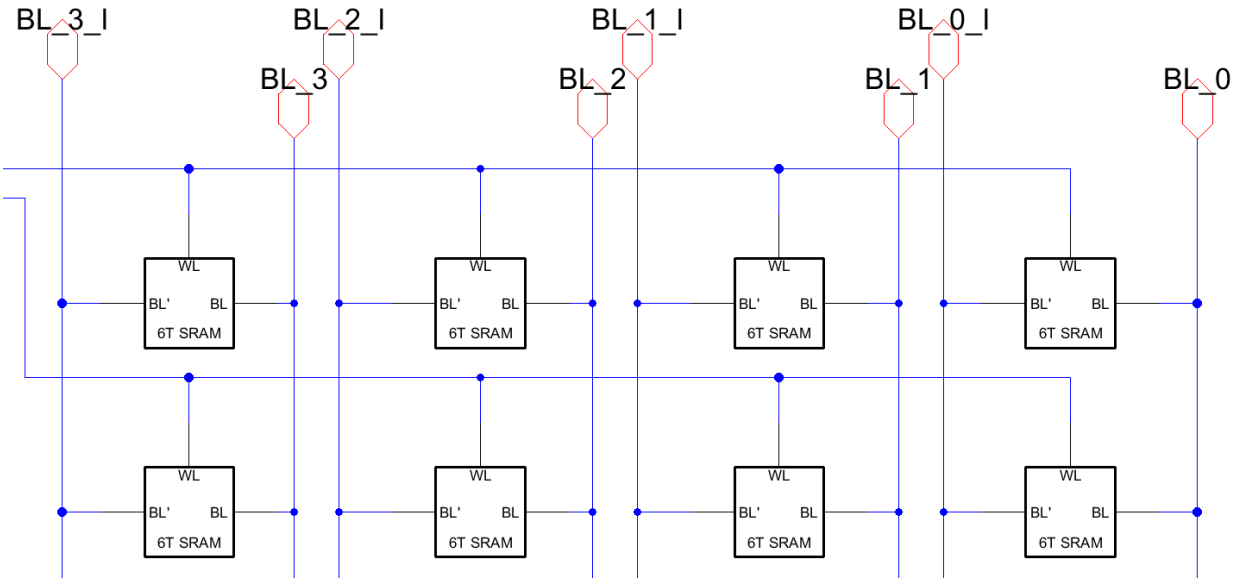

Figure 4: Memory block schematic in detail, word slice

6T SRAM Cell

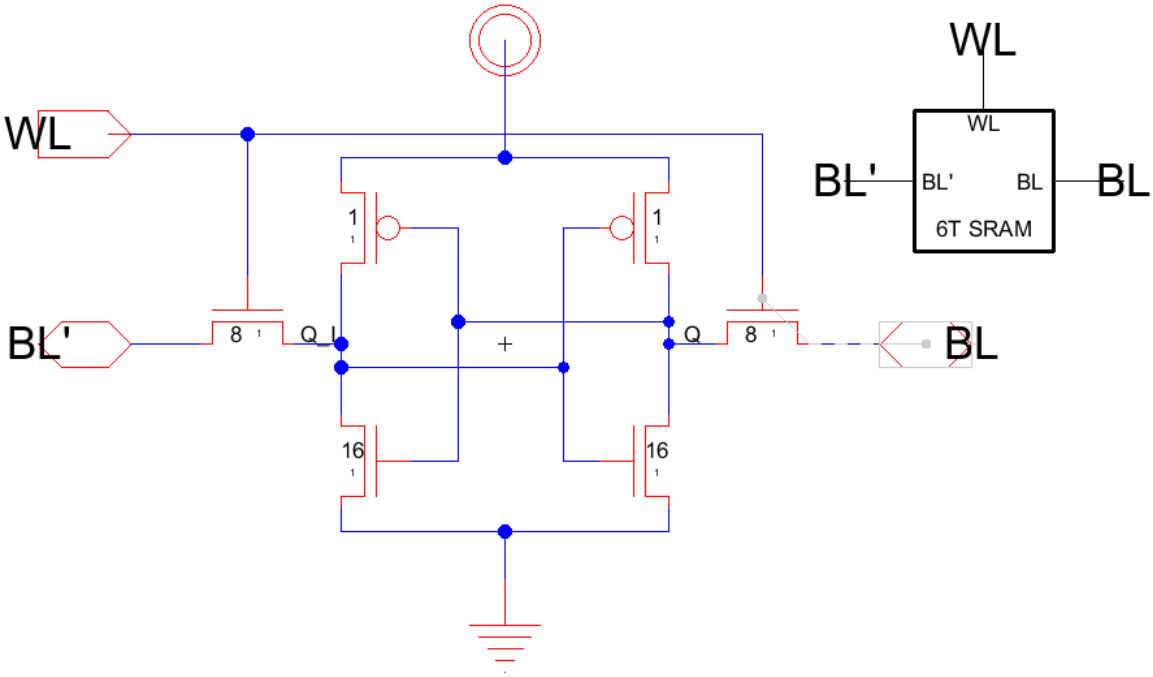

Figure 5: SRAM cell schematic

Control Block

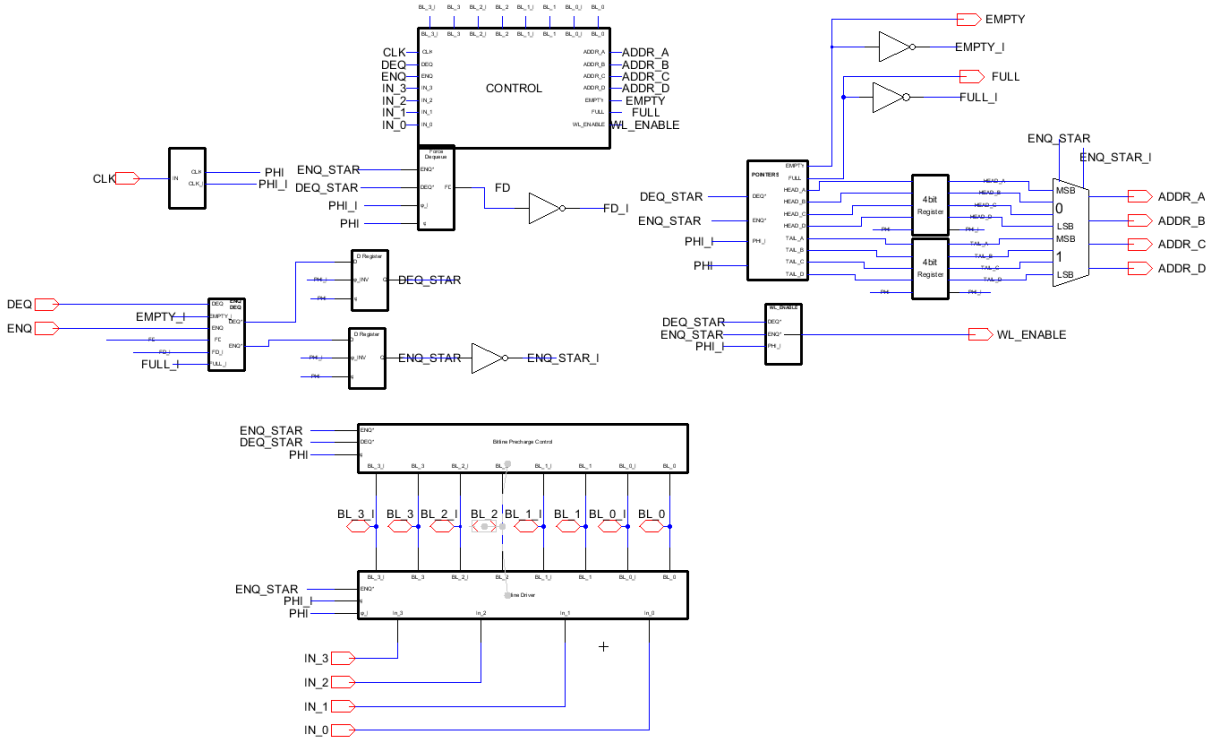

Figure 6: Control block toplevel schematic

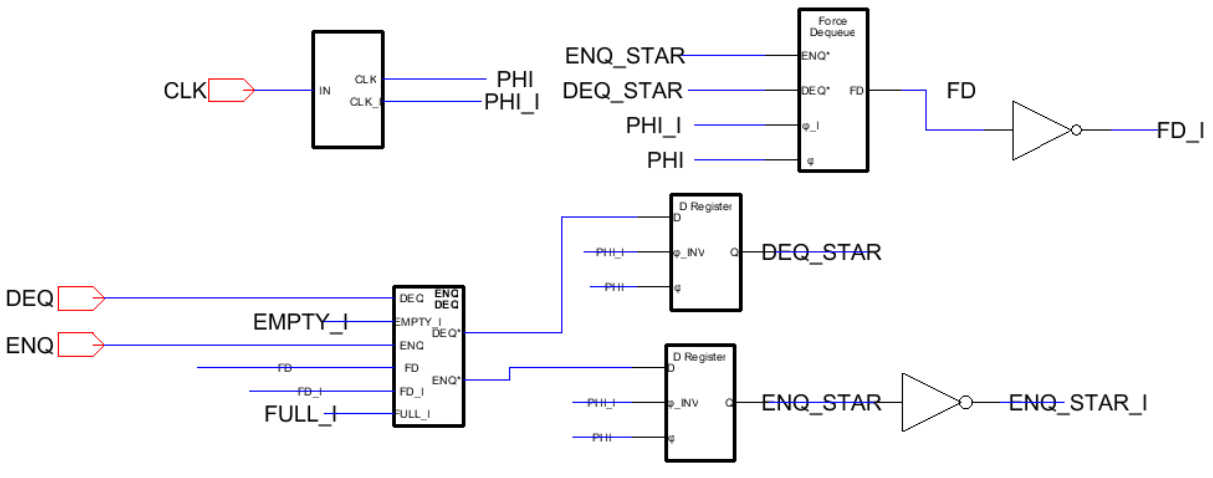

Figure 7: Control block schematic in detail, FD, clock generator, and ENQ*/DEQ* generation

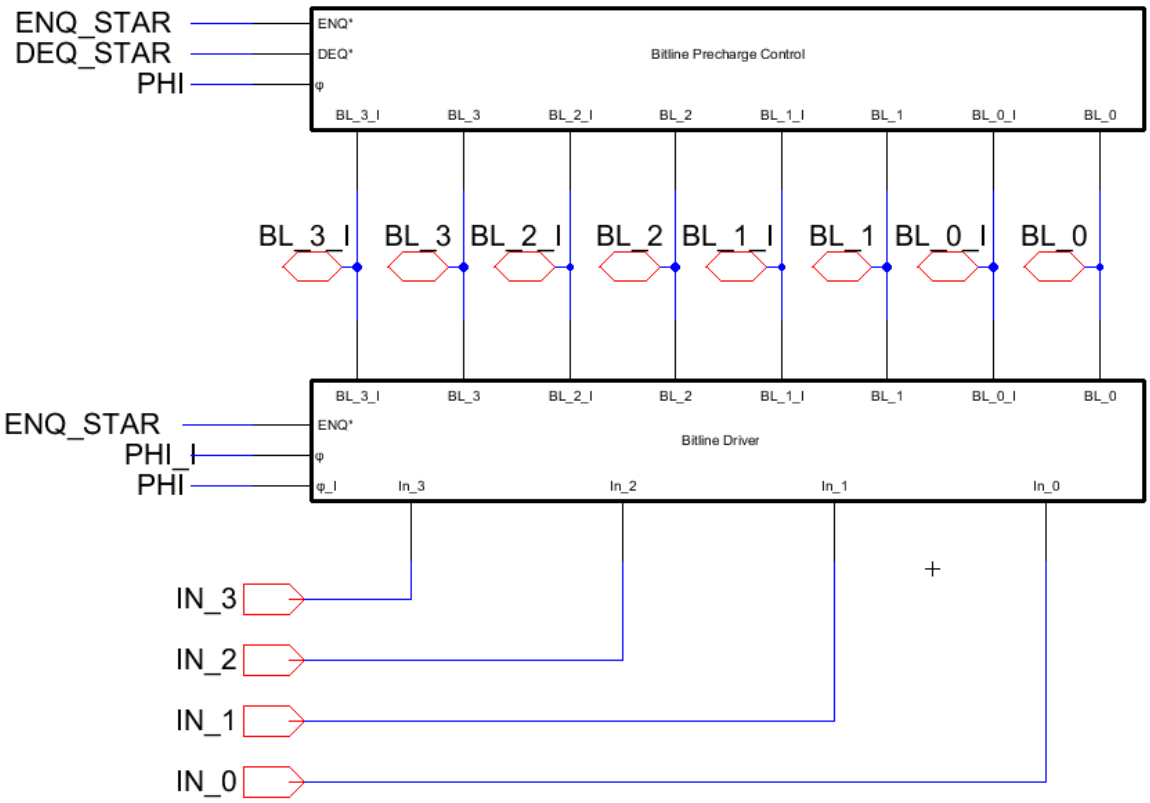

Figure 8: Control block schematic in detail, bitline driver and precharger

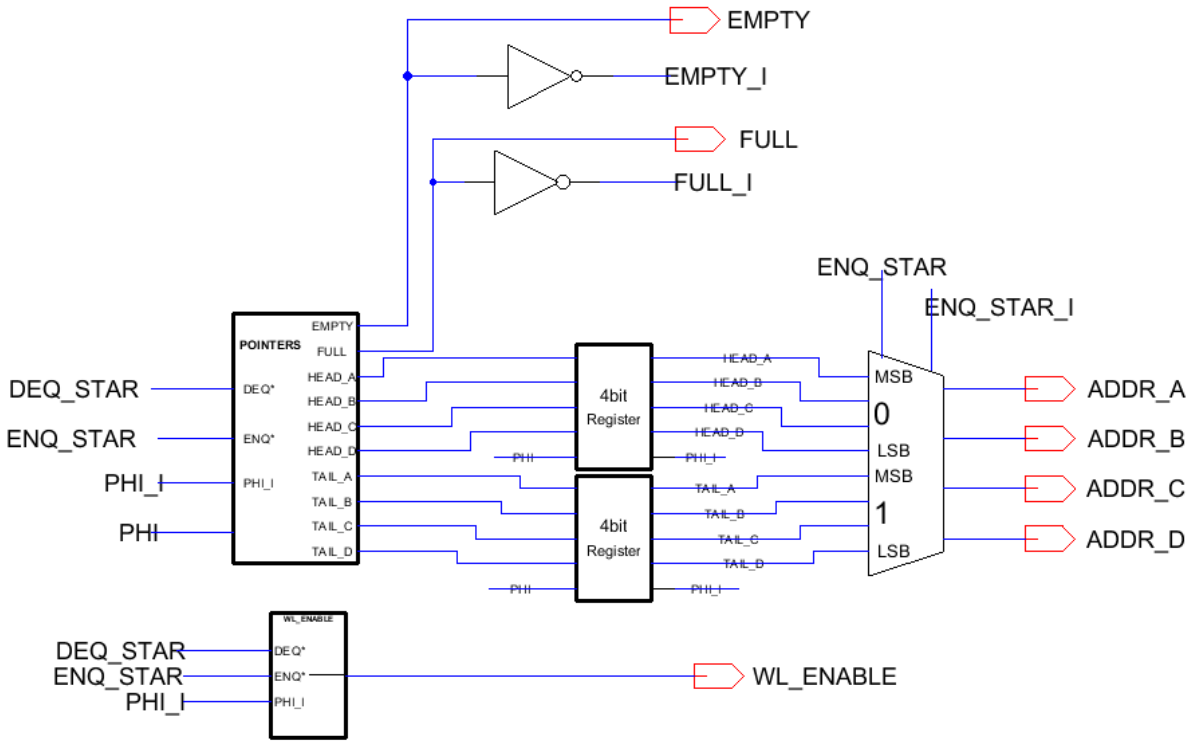

Figure 9: Control block schematic in detail, pointers, WL_EN, and EMPTY/FULL generation

Clock Generator

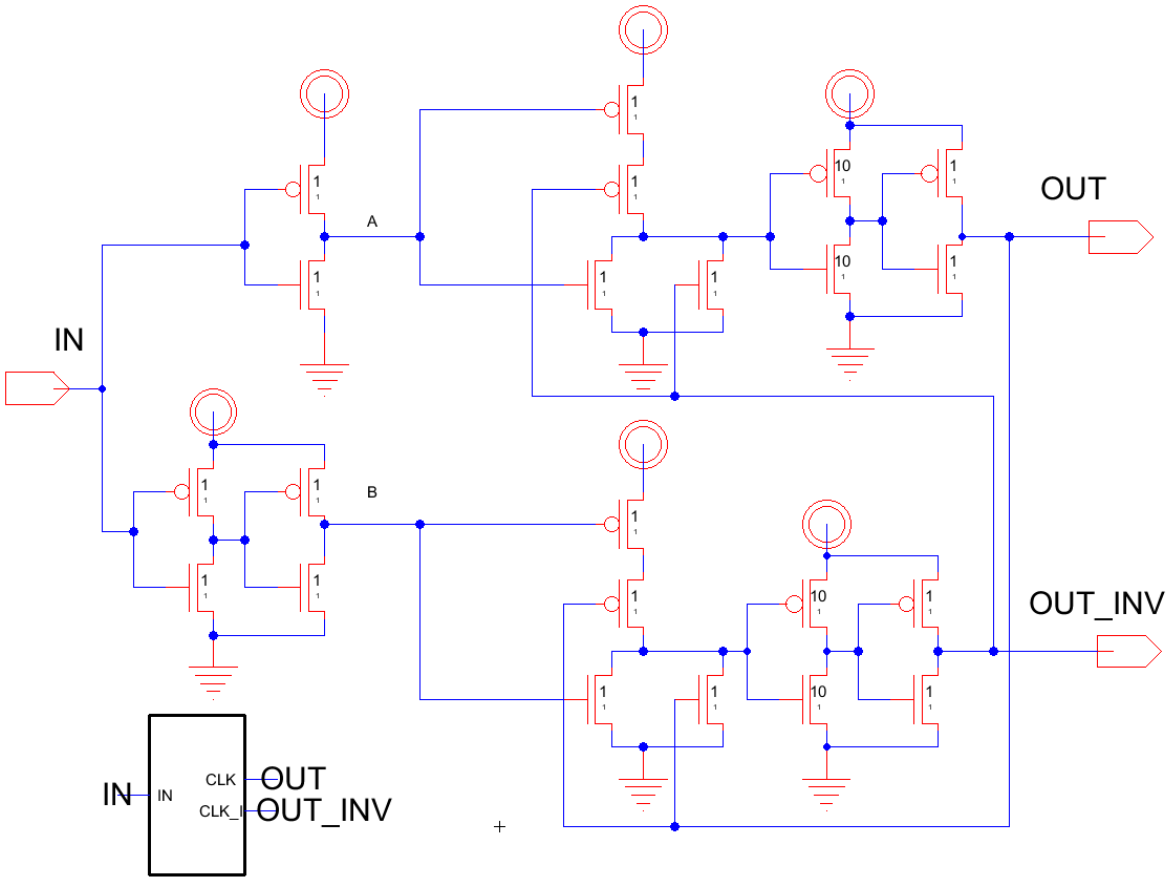

Figure 10: Clock generator schematic

Force Dequeue (FD)

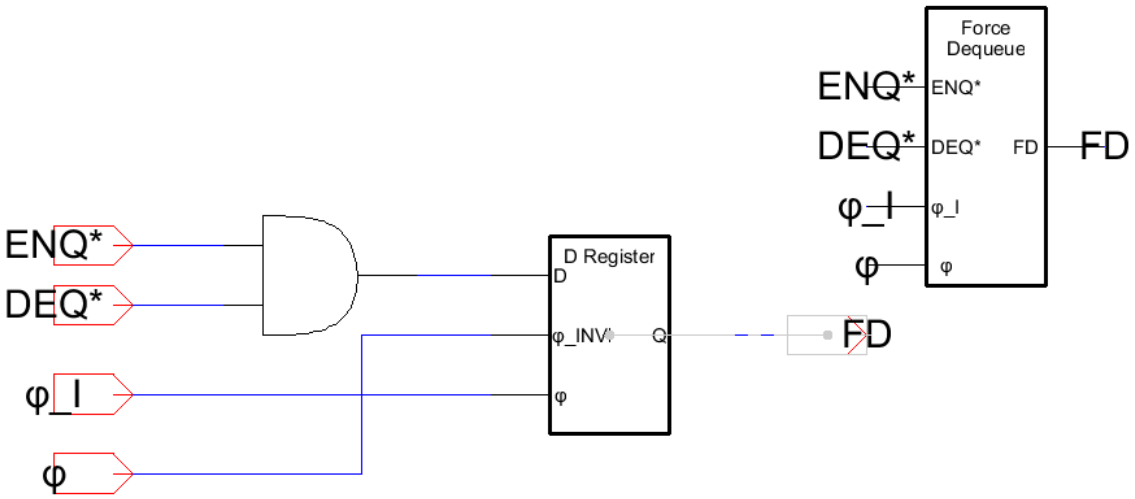

Figure 11: Force dequeue generation schematic

Pointers

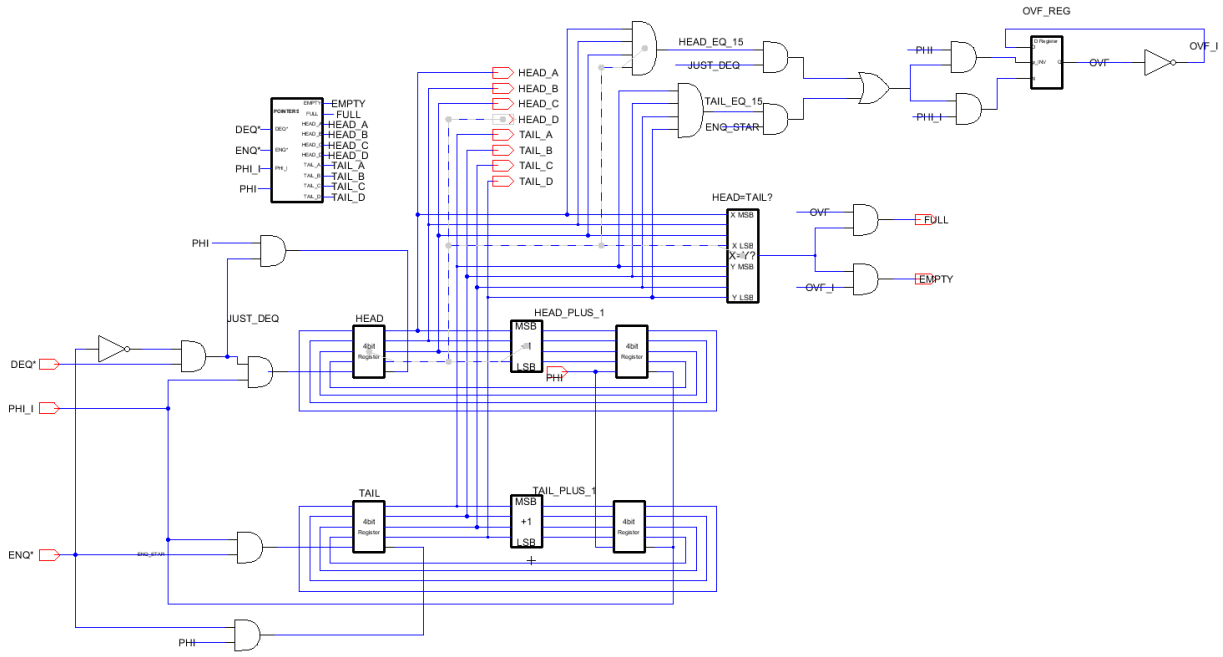

Figure 12: Pointers toplevel schematic

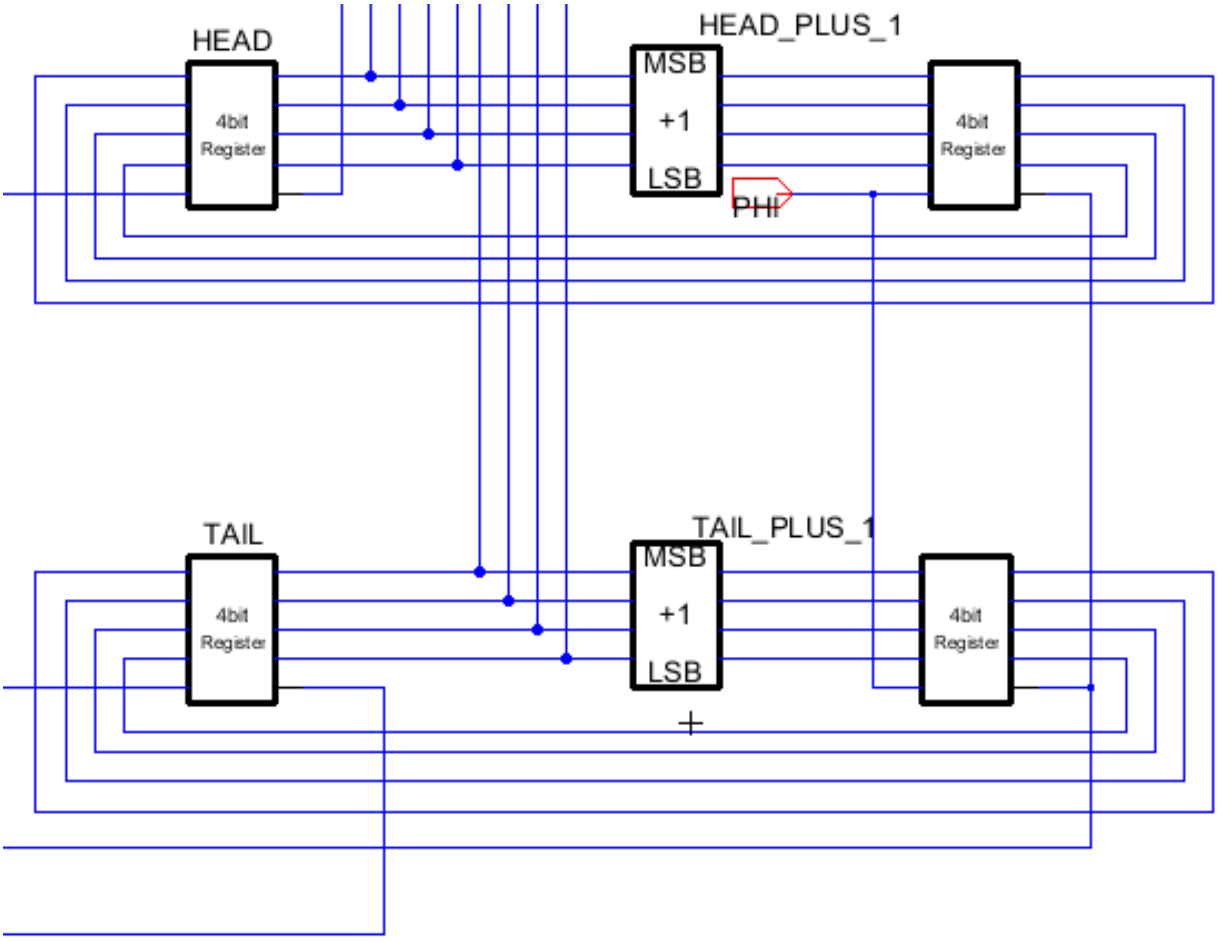

Figure 13: Pointers schematic in detail, head/tail state

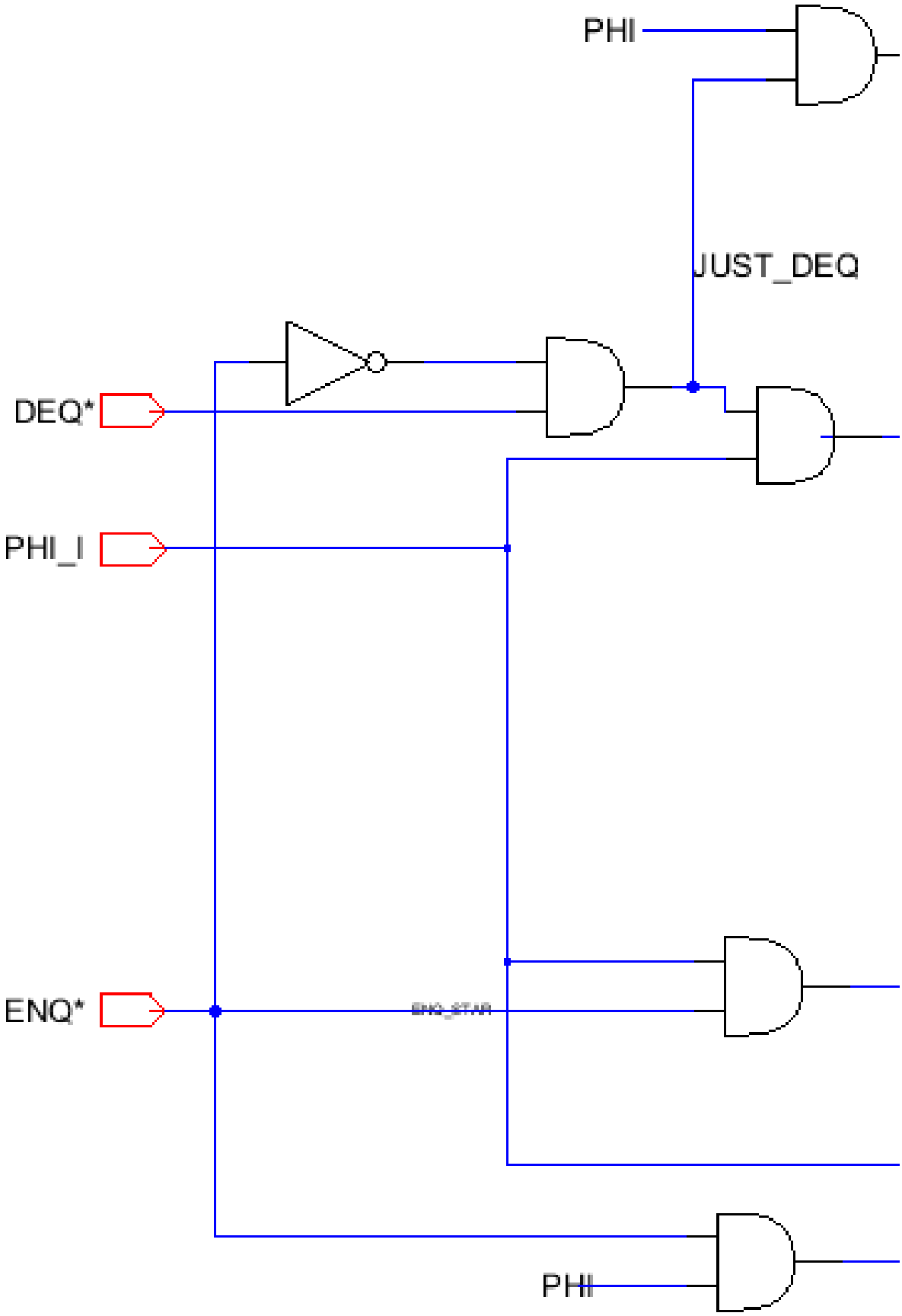

Figure 14: Pointers schematic in detail, inputs

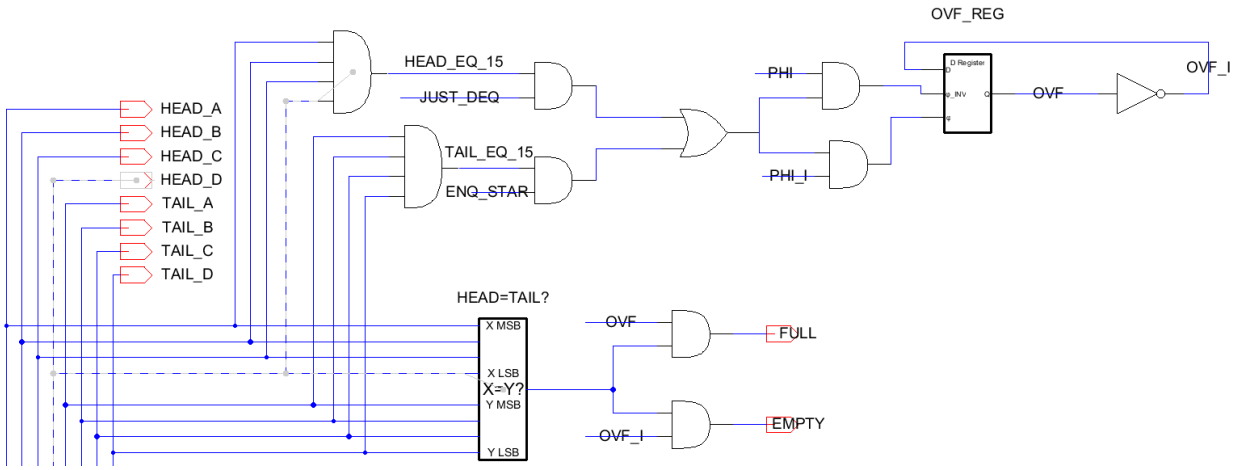

Figure 15: Pointers schematic in detail, overflow handler

D Latch

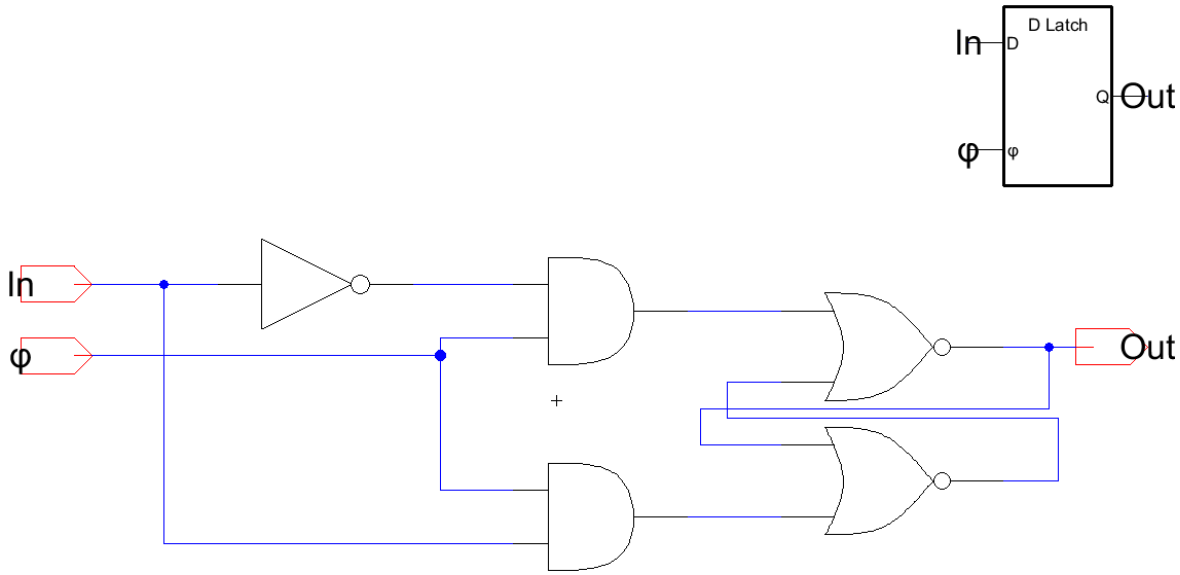

Figure 16: D latch schematic

D Register

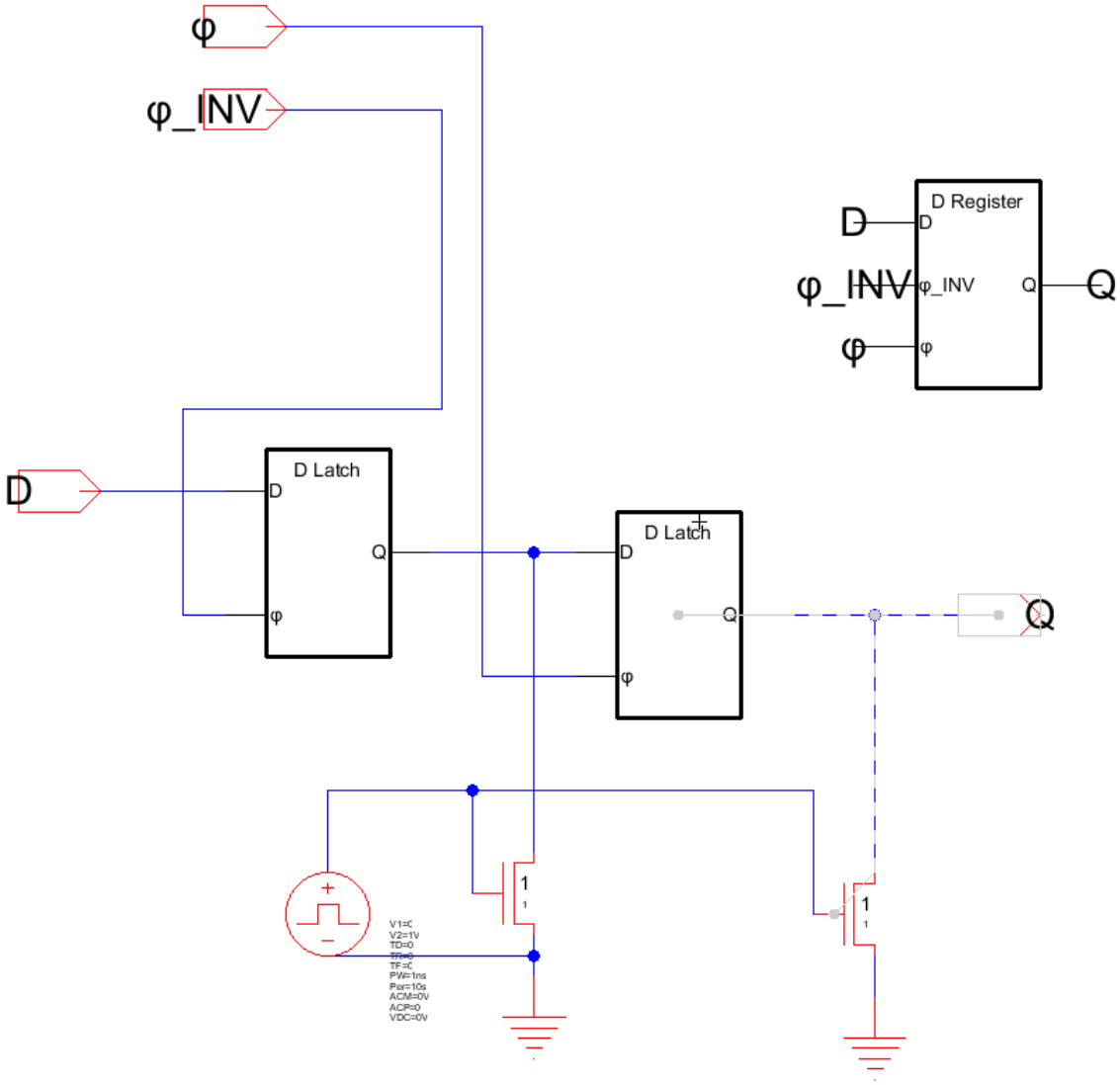

Figure 17: D register schematic

4-bit Register

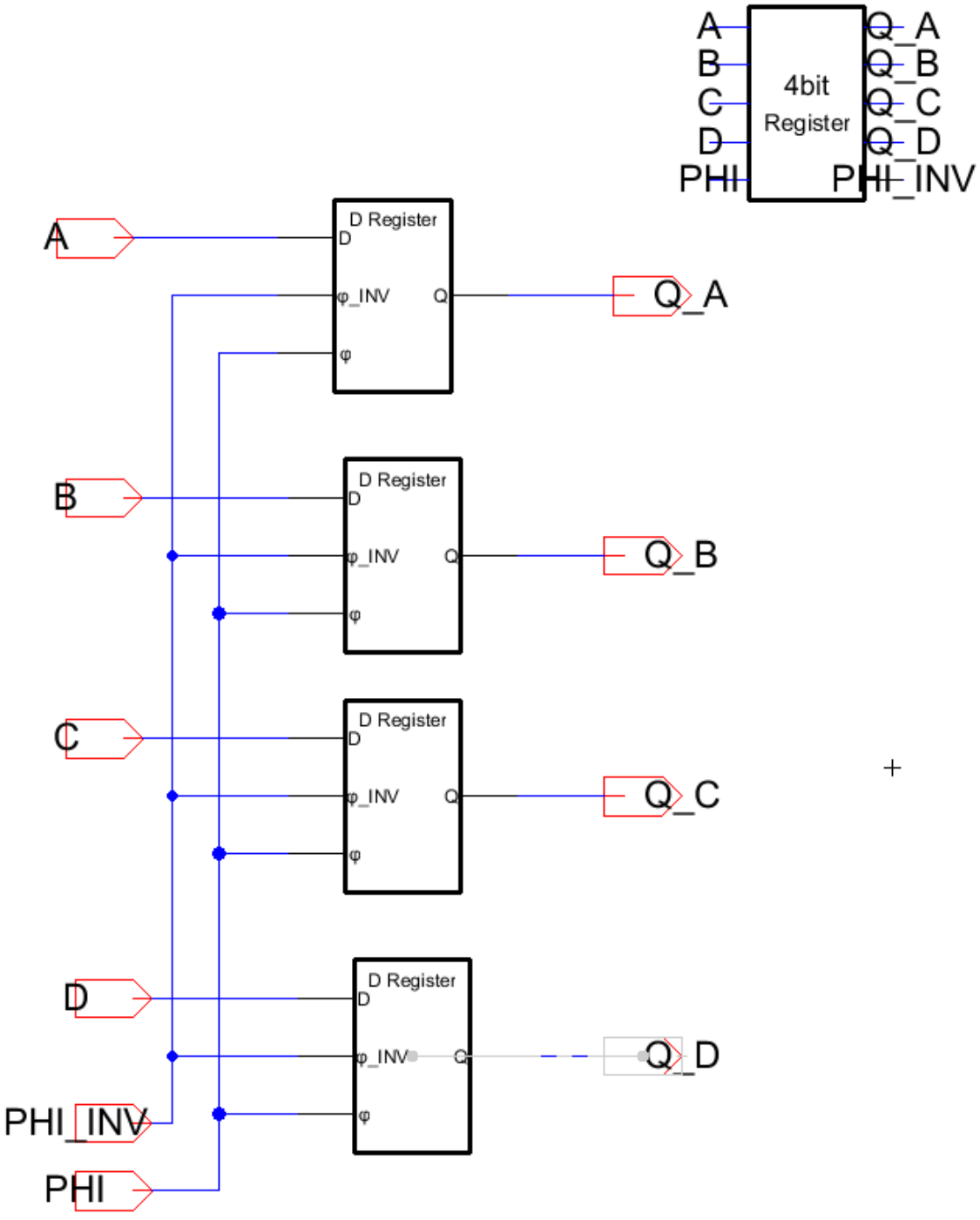

Figure 18: 4-bit register schematic

Incrementer

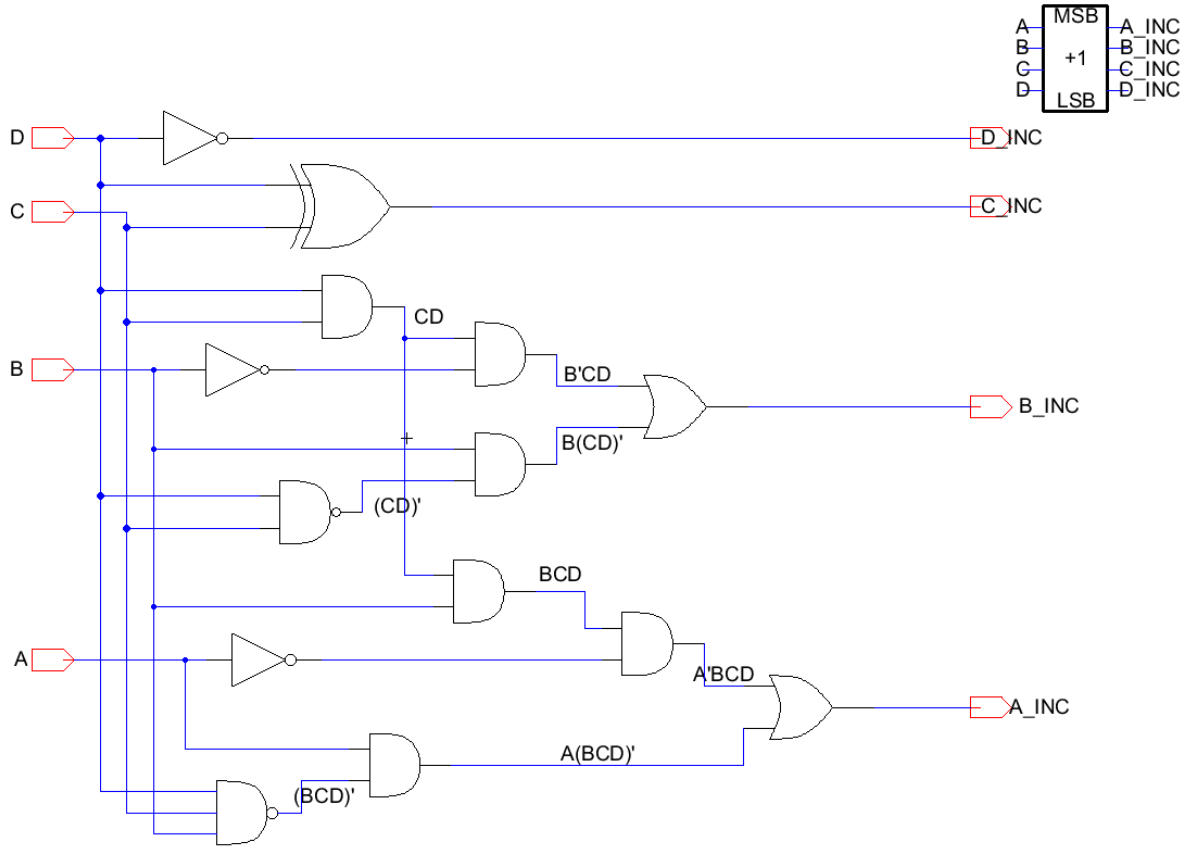

Figure 19: Incrementer schematic

Comparator

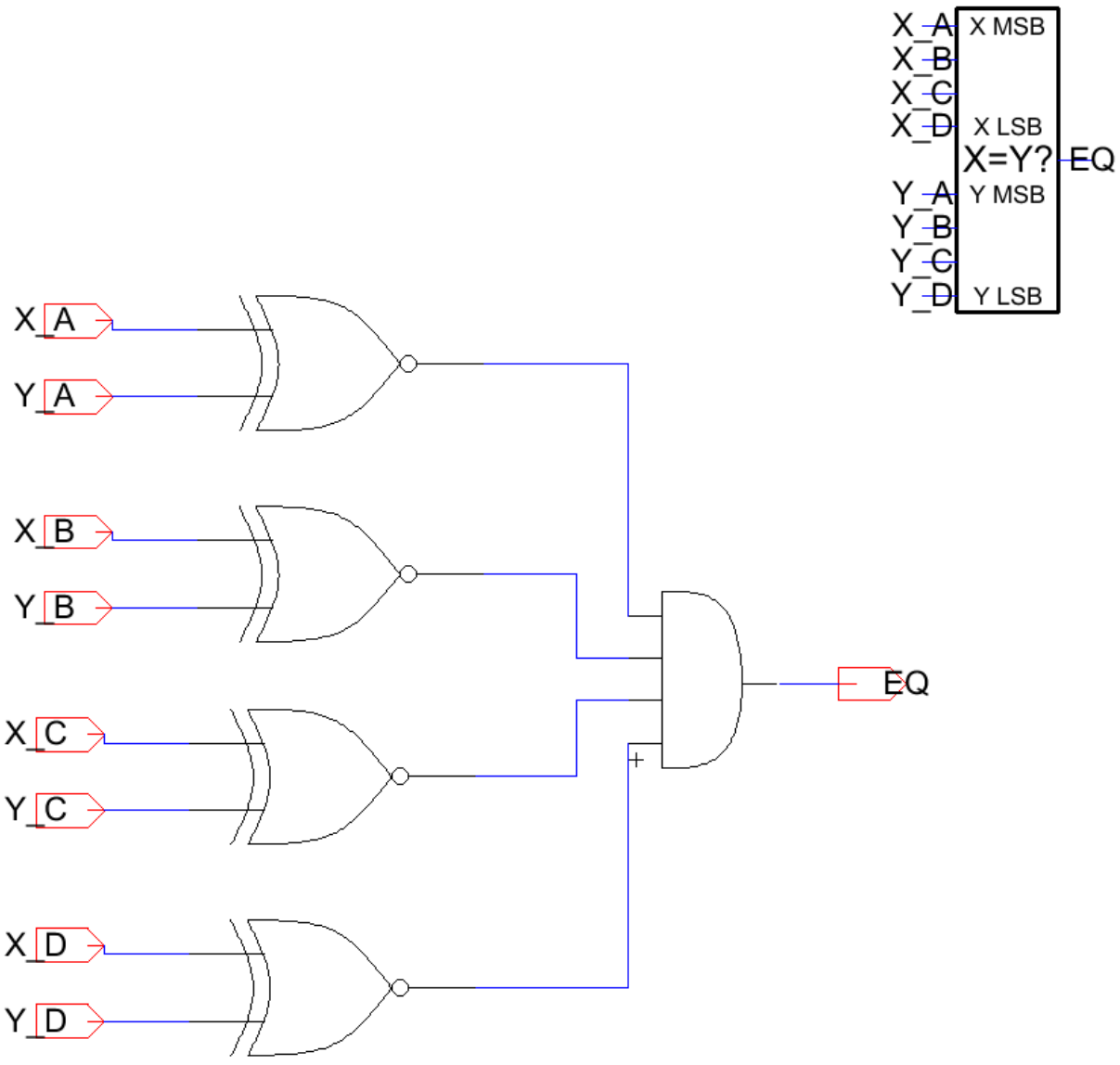

Figure 20: Equality comparator schematic

Mux

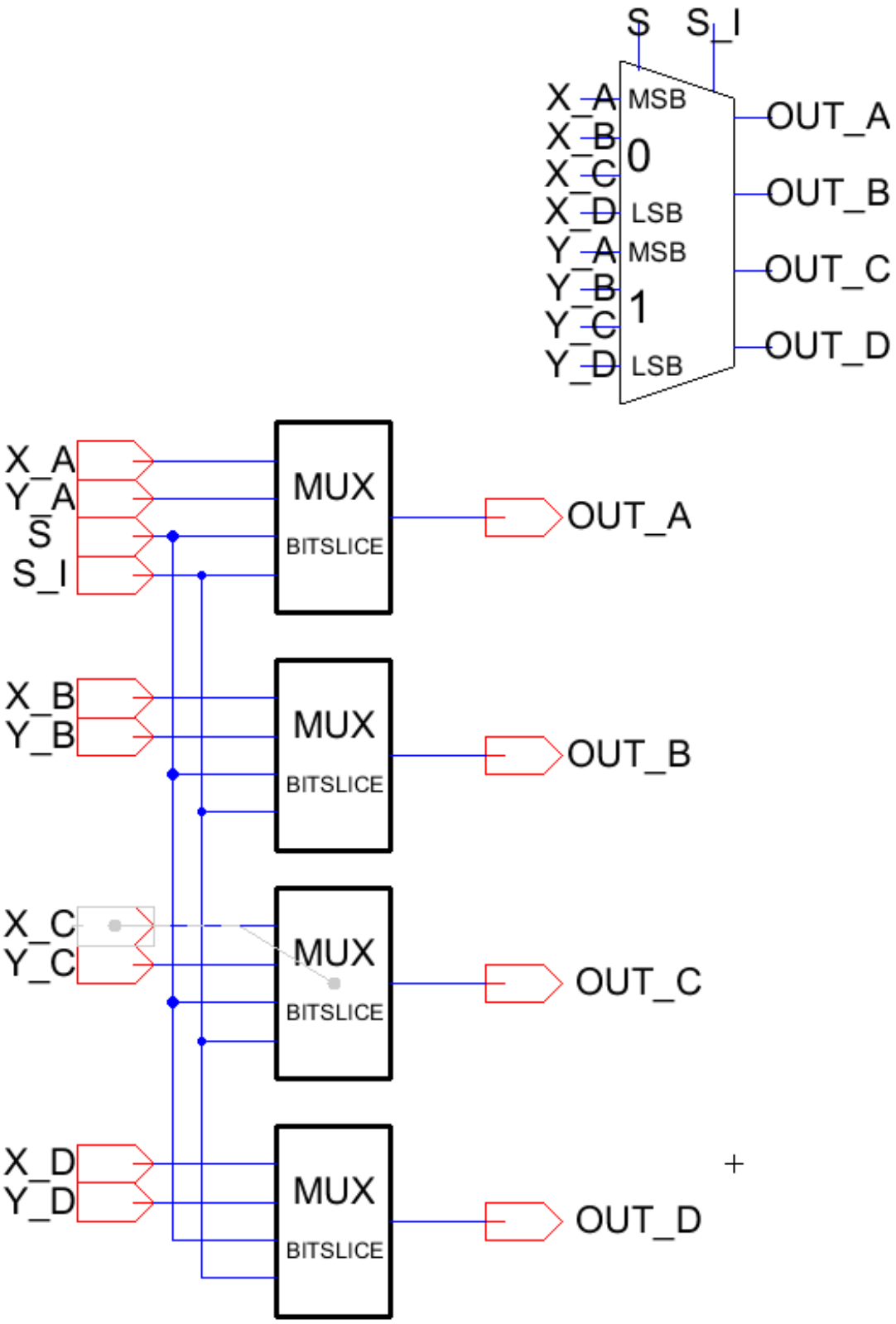

Figure 21: Mux schematic

Mux Bitslice

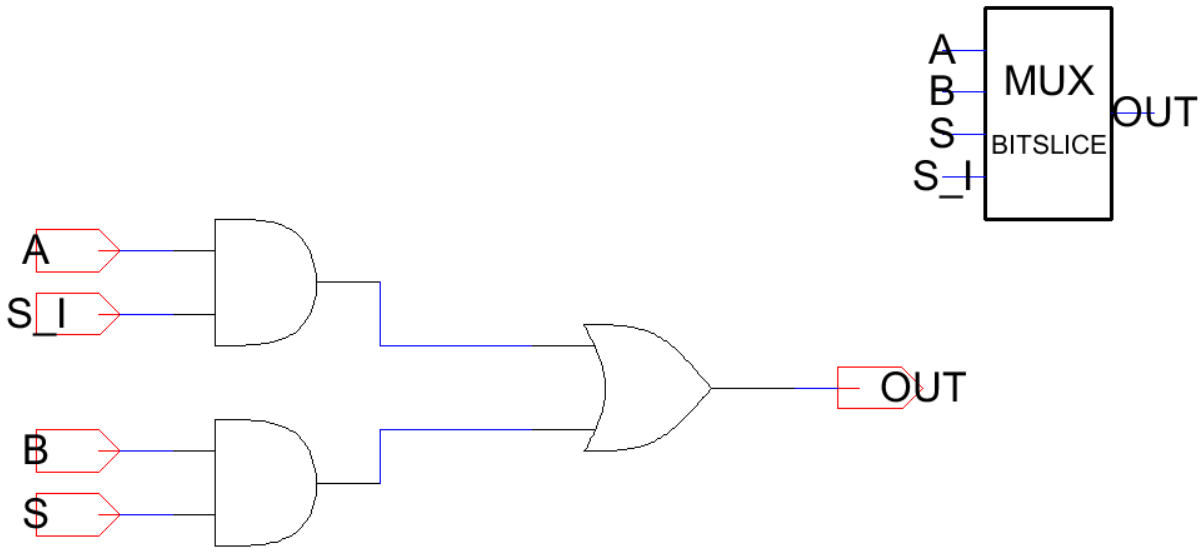

Figure 22: Mux bitslice schematic

Wordline Enable (WL_EN)

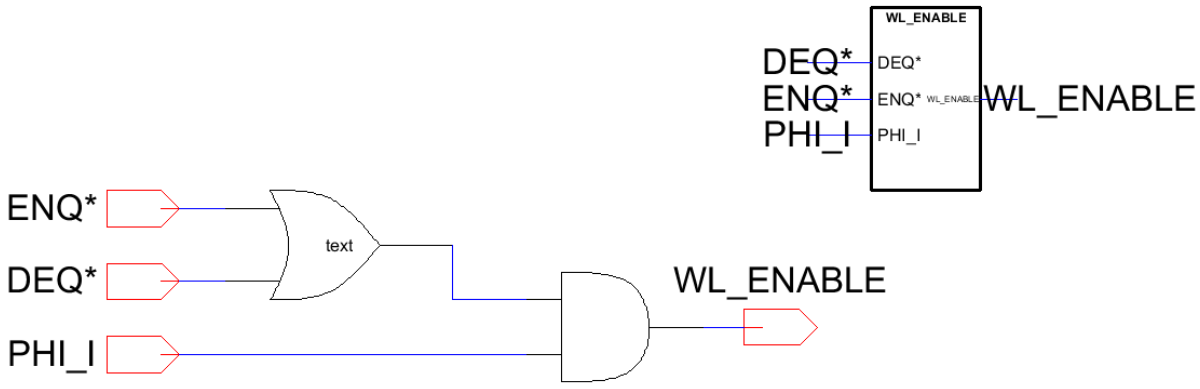

Figure 23: Word line enable generator schematic

ENQ*/DEQ* Generator

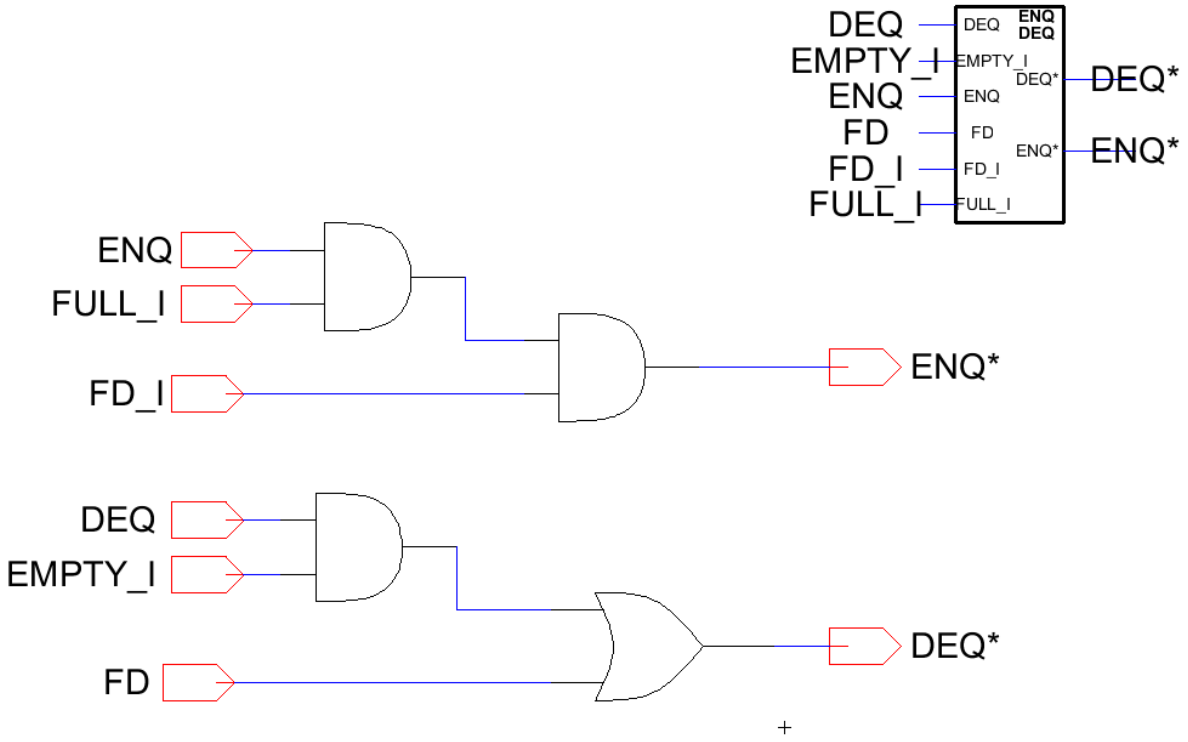

Figure 24: ENQ*/DEQ* generator schematic

4-bit Bitline Precharger

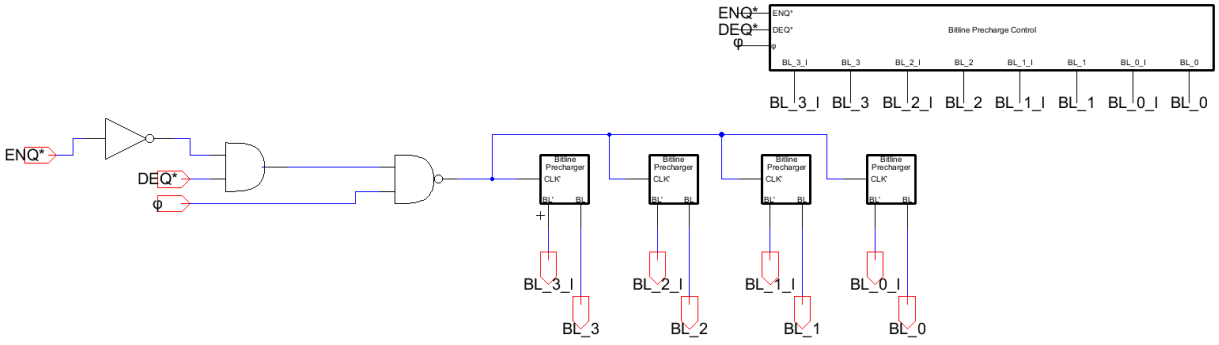

Figure 25: 4-bit bitline precharger schematic

1-bit Bitline Precharger

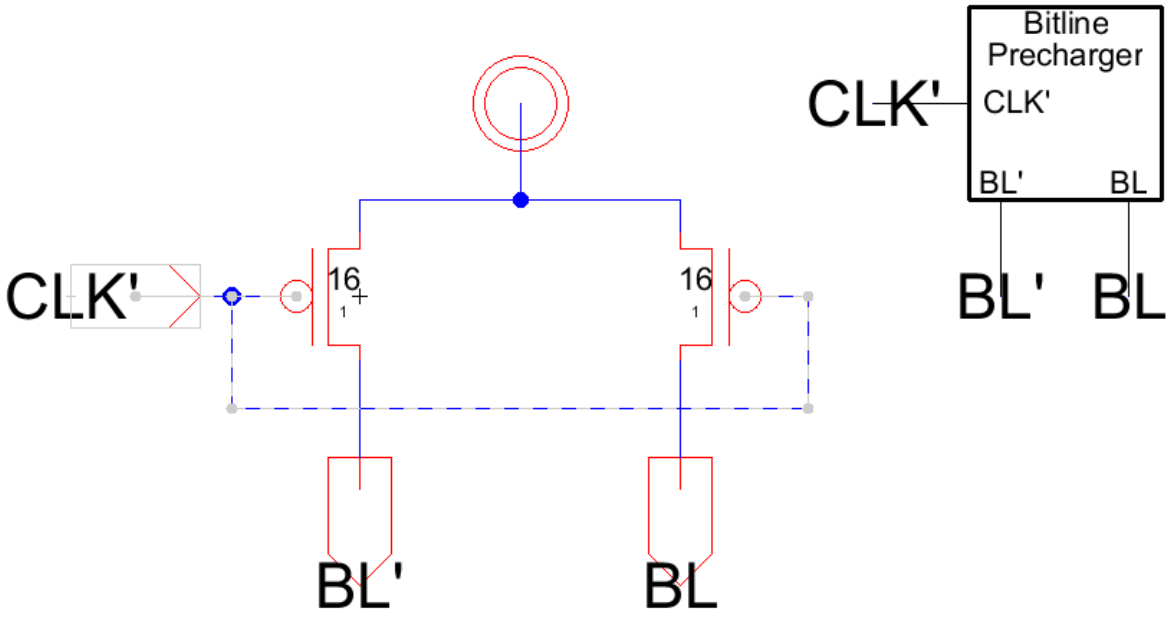

Figure 26: 1-bit bitline precharger schematic

Bitline Driver

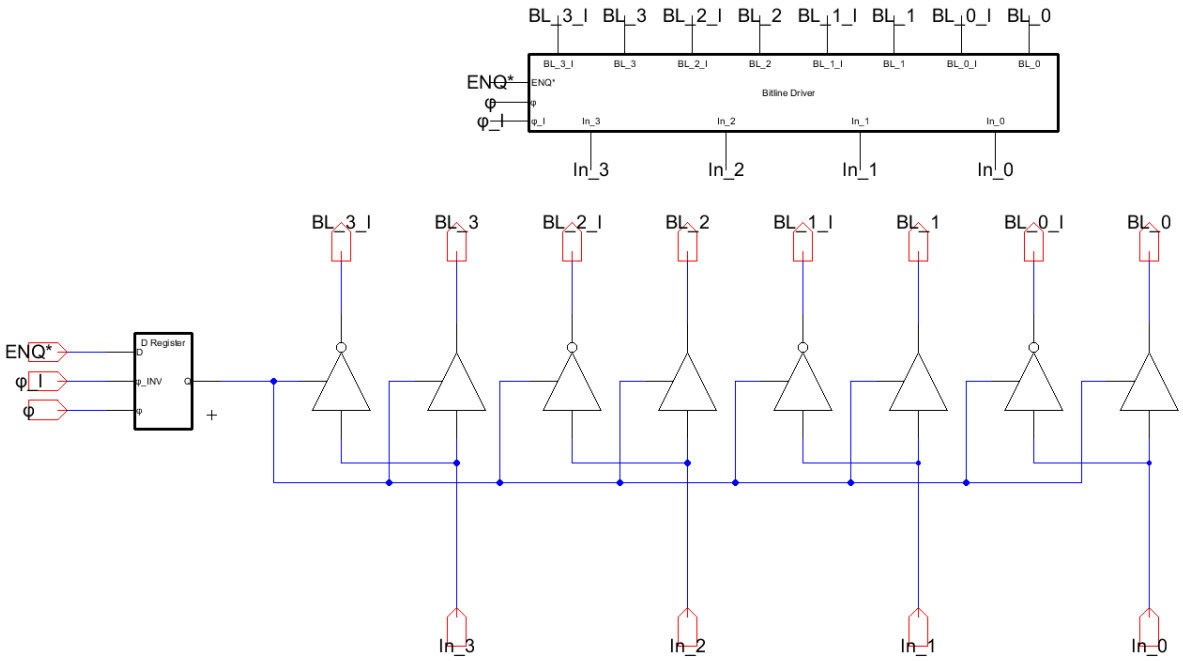

Figure 27: Bitline driver schematic

Inverter

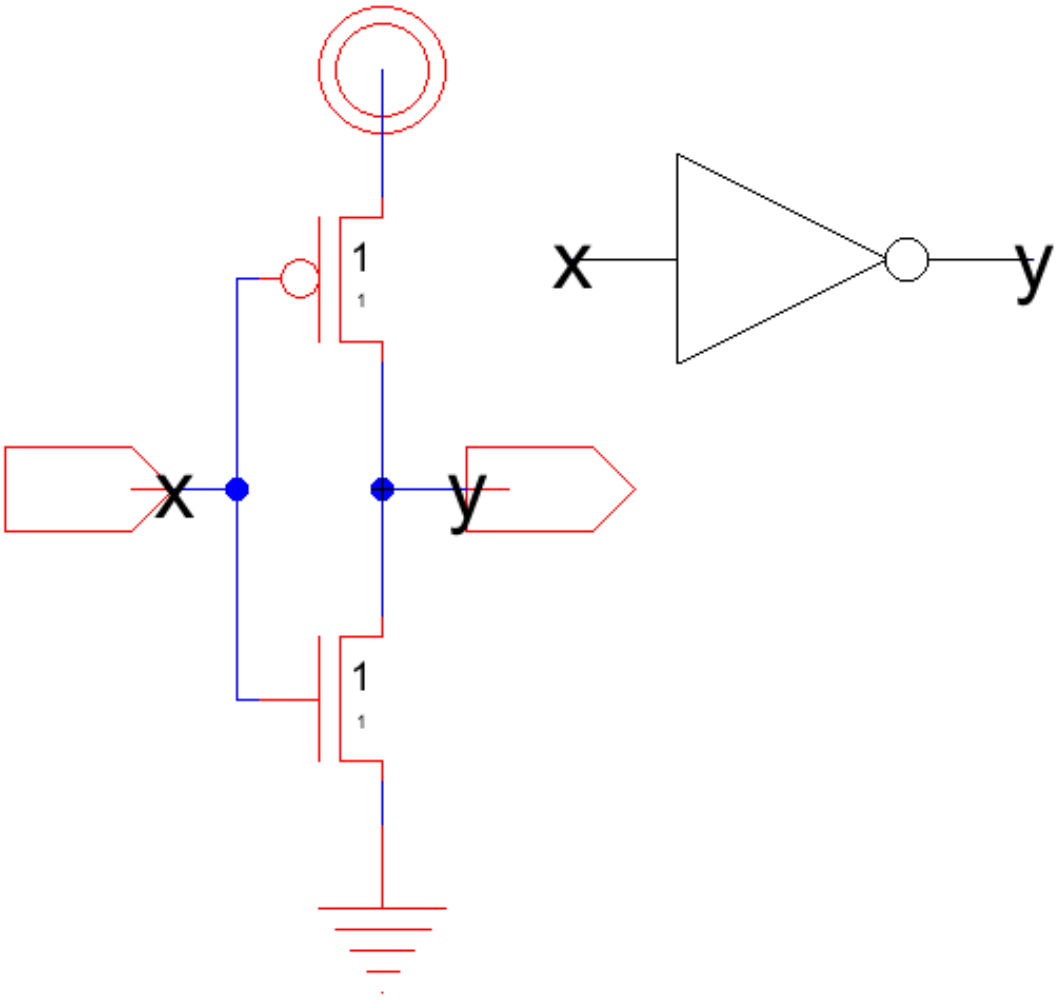

Figure 28: Inverter schematic

NAND2

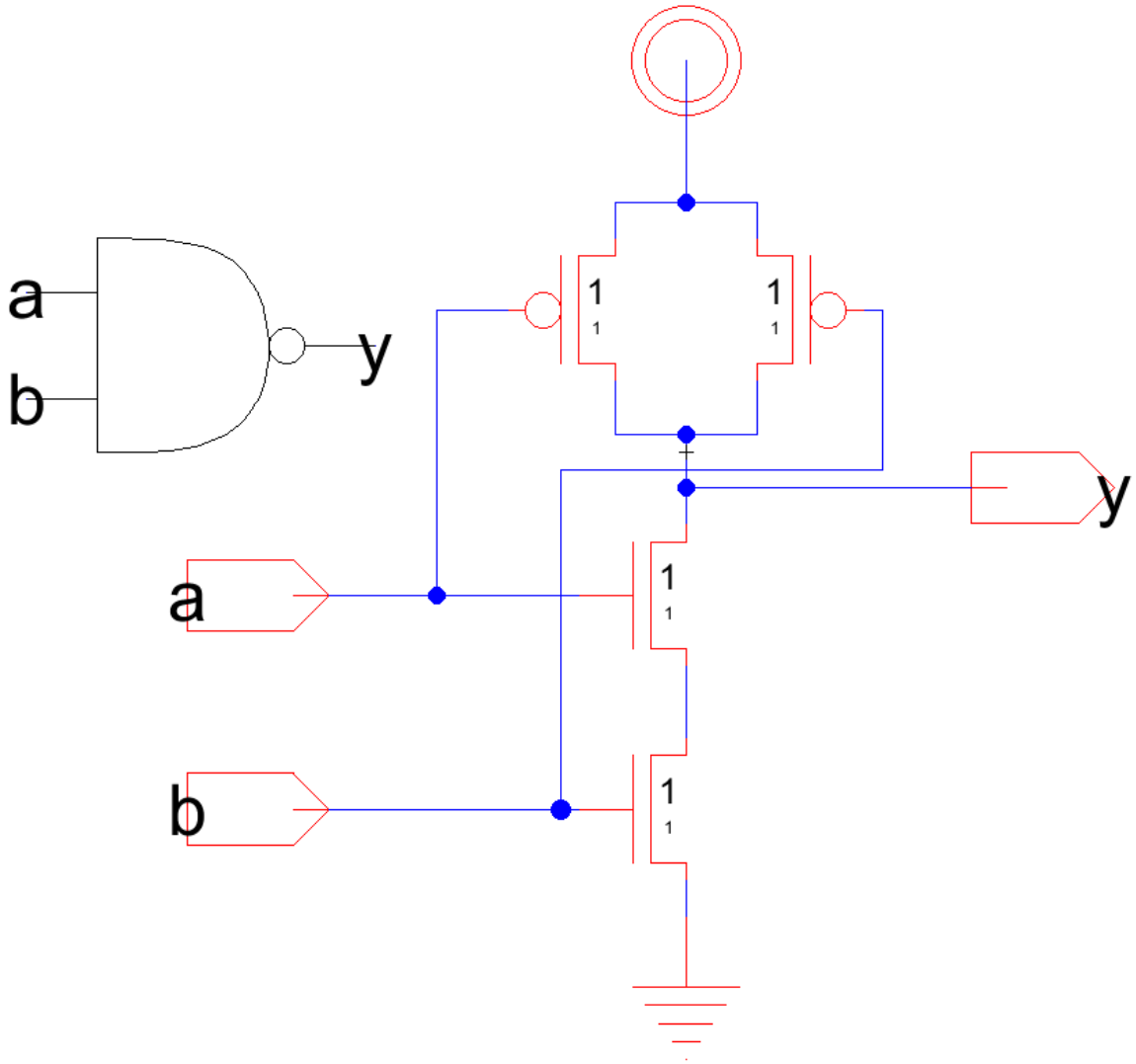

Figure 29: NAND2 gate schematic

AND2

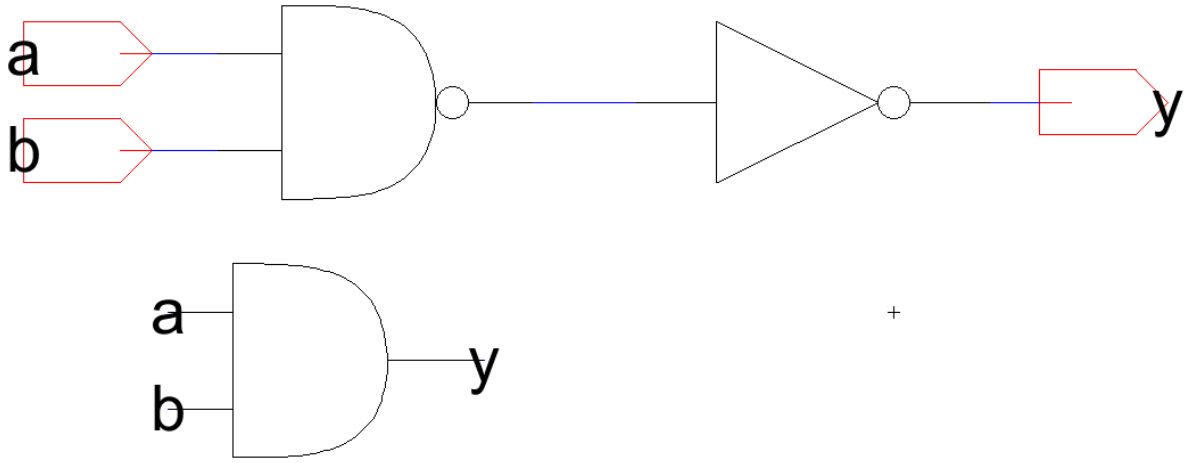

Figure 30: AND2 gate schematic

AND4

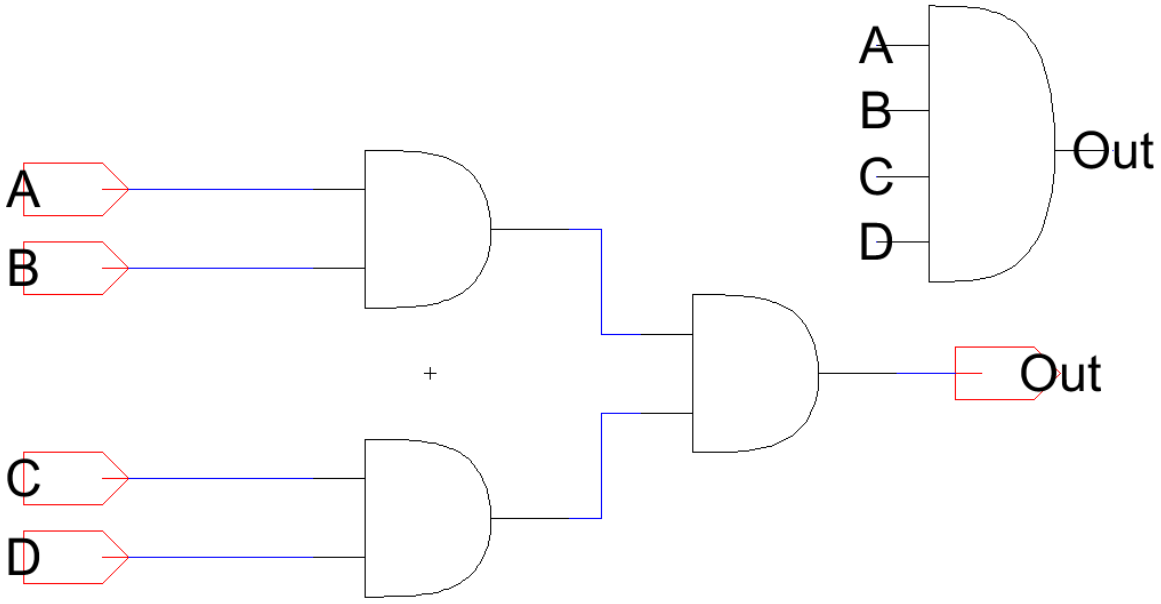

Figure 31: AND4 gate schematic

NOR2

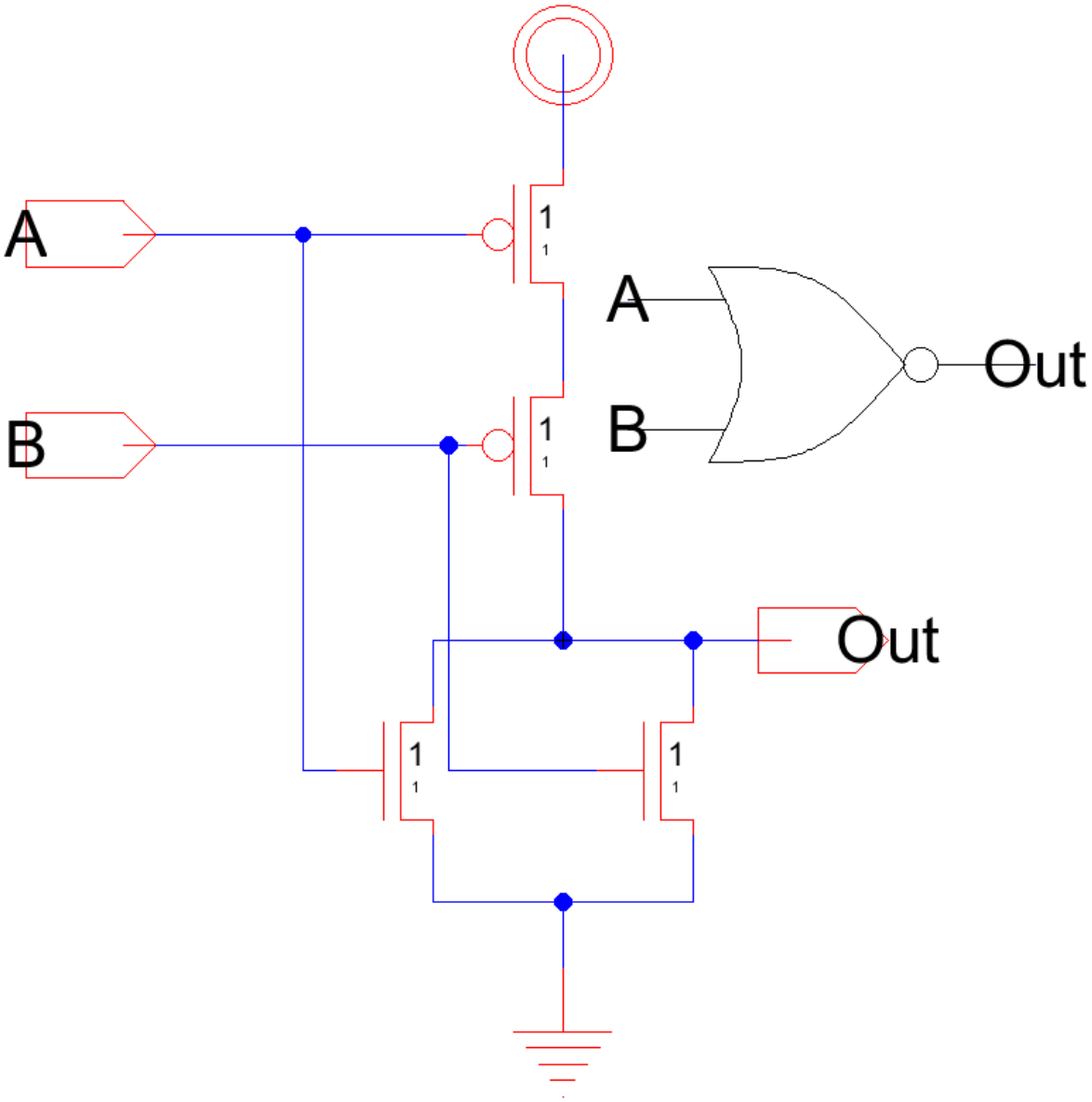

Figure 32: NOR2 gate schematic

Decoder

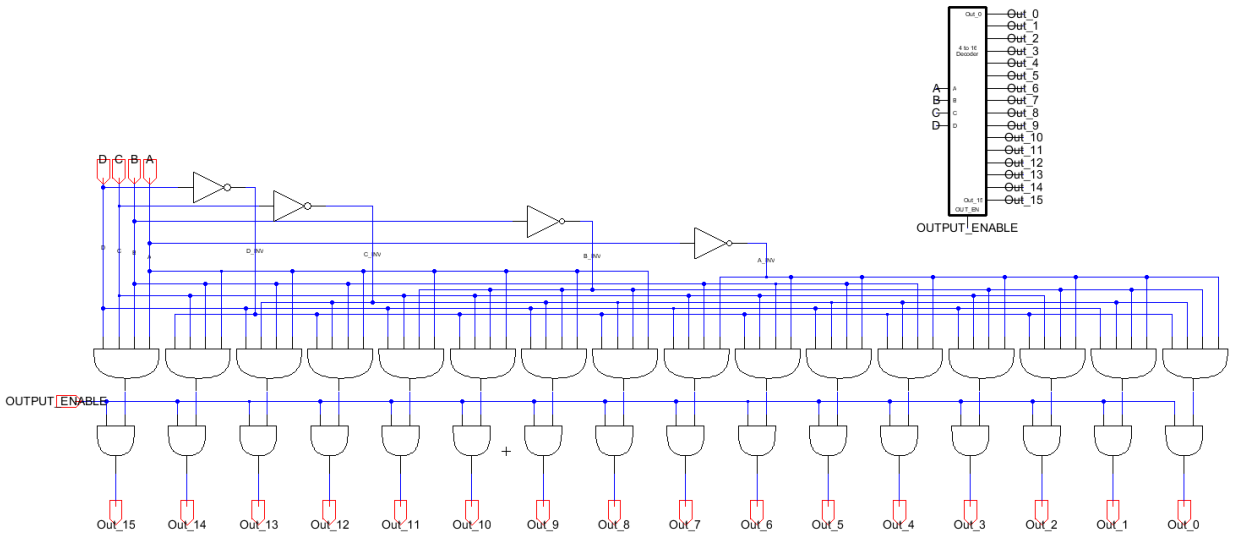

Figure 33: 4-to-16 decoder schematic

Tri-State Buffer

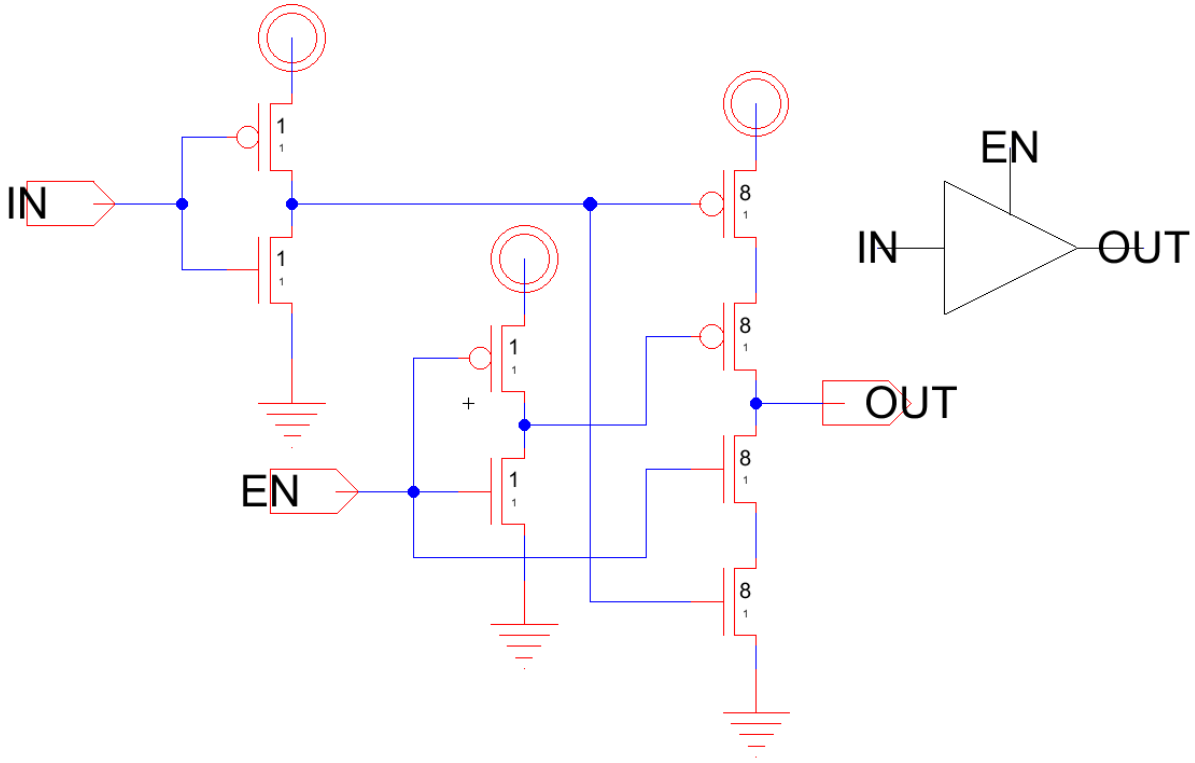

Figure 34: Tri-state buffer schematic

Tri-State Inverter

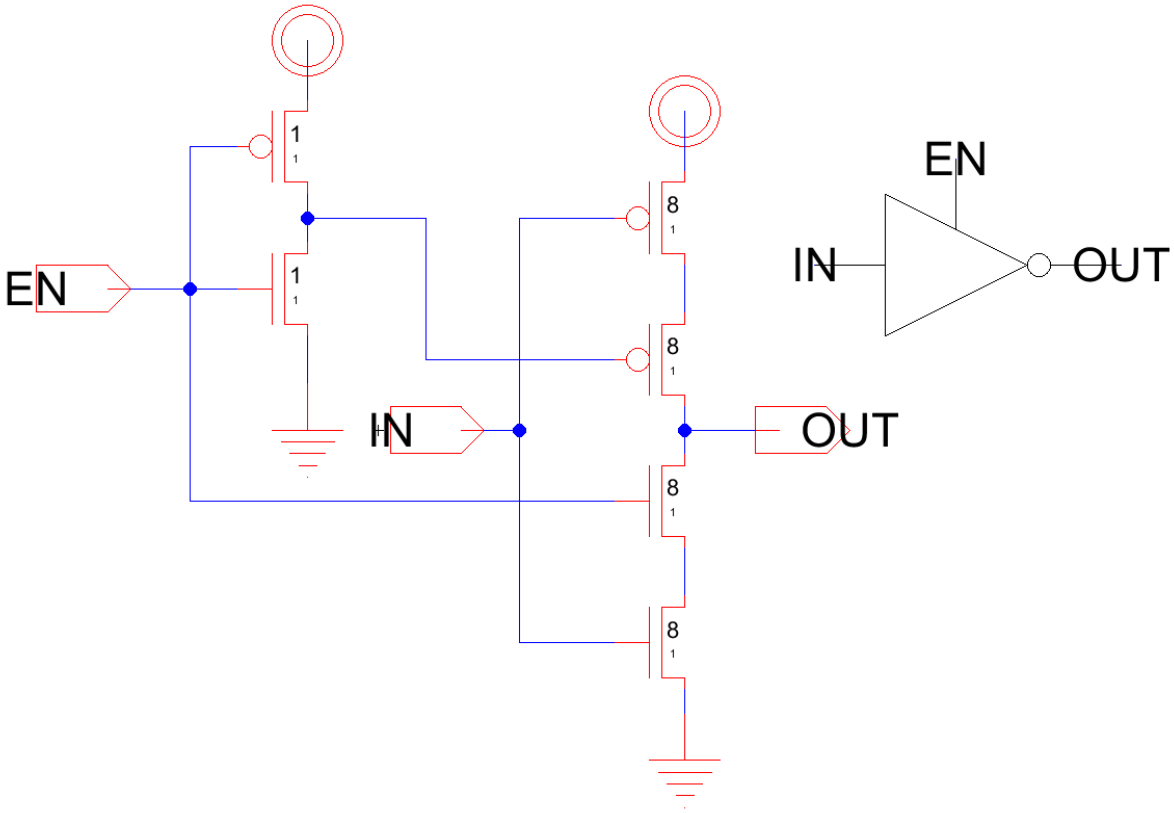

Figure 35: Tri-state inverter schematic

Timing of Key Signals

Memory Operation and Design Choices

Breakdown of Energy Contributions

Optimization of Energy

Validation of Correctness

Summary of Design Metrics

Honor Pledge

We, Jack Harkins and Mauricio Mutai, certify that we have complied with the University of
Pennsylvania's Code of Academic Integrity in completing this project.