

ESE 370: CIRCUIT-LEVEL OPTIMIZATION FOR DIGITAL
SYSTEMS

Project 2 Milestone: FIFO Queue

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Bitline Capacitance

TODO

Circuit Schematics

TODO

Memory Column Driver Schematic

Sized Memory Cell Schematic

Tri-State Buffer Schematic

Tri-State Inverter Schematic

Reading and Writing (Cell)

TODO

Test Cases to Consider

Writing 0 and Reading 0

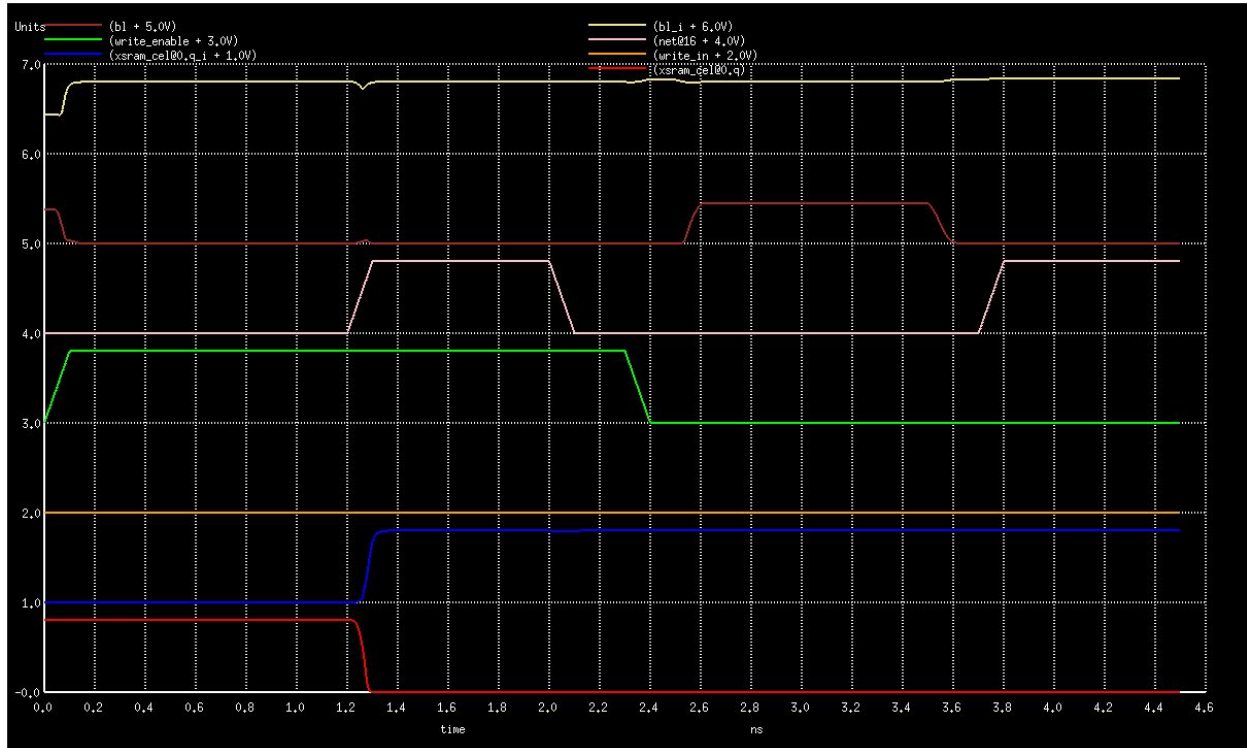


Figure 1: Writing 0 and then reading 0

Writing 1 and Reading 1

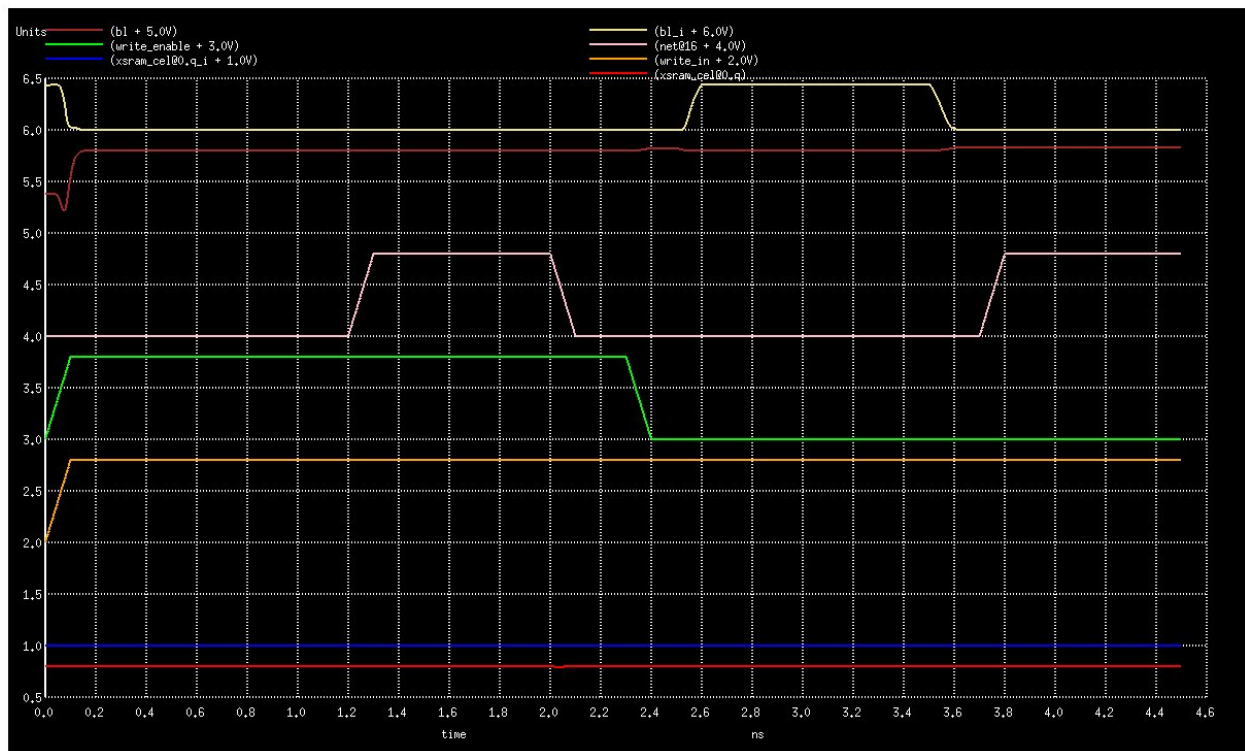


Figure 2: Writing 1 and then reading 1

Writing 0

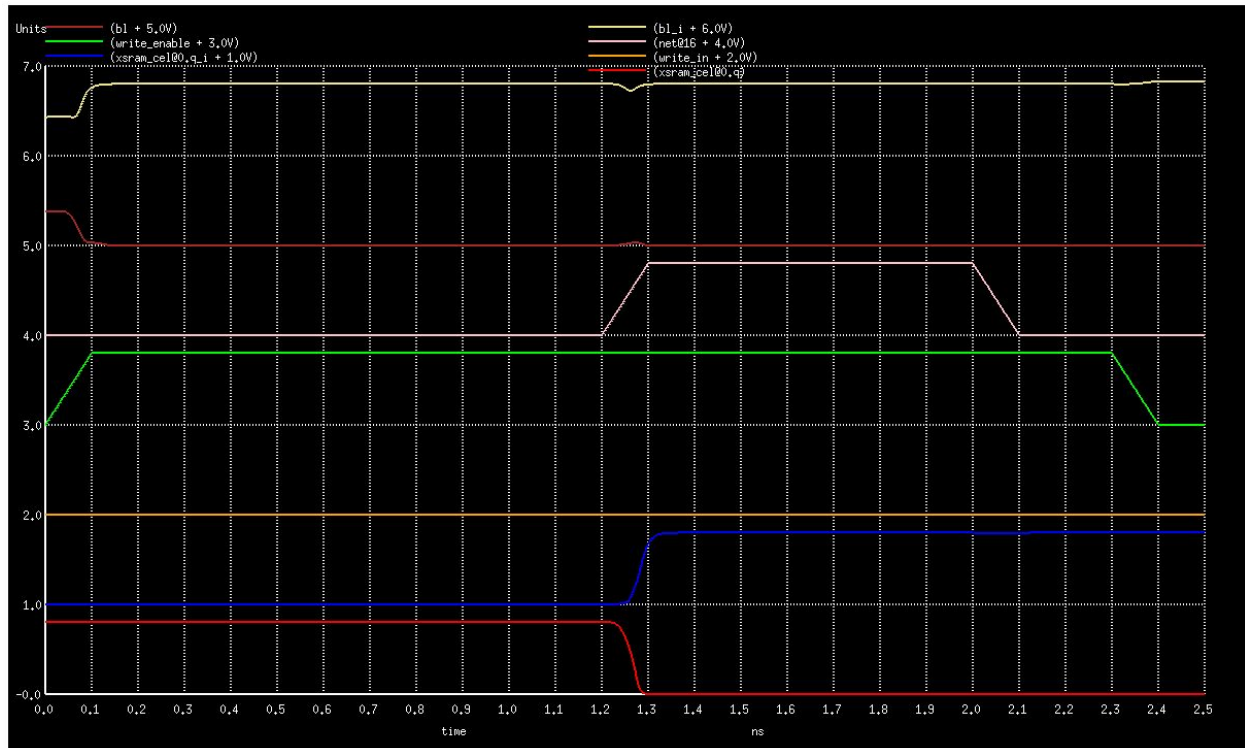


Figure 3: Writing 0

Writing 1

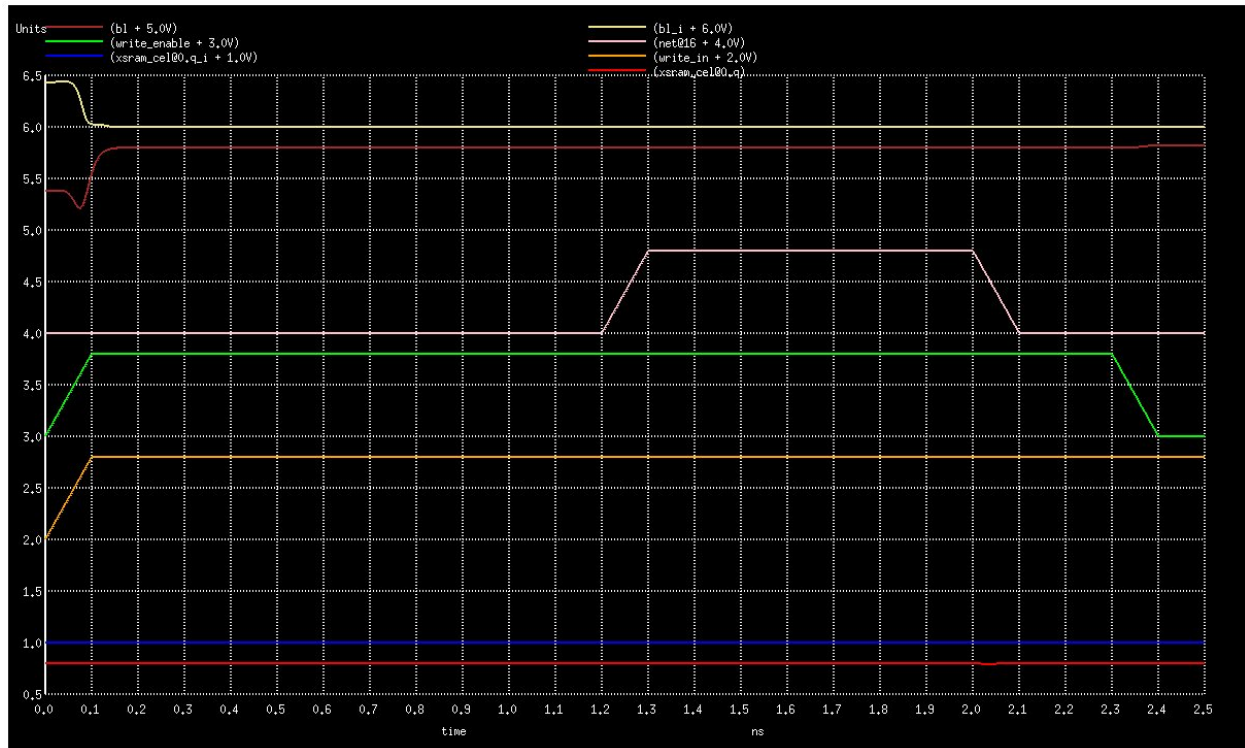


Figure 4: Writing 1

Writing 0 and Writing 1

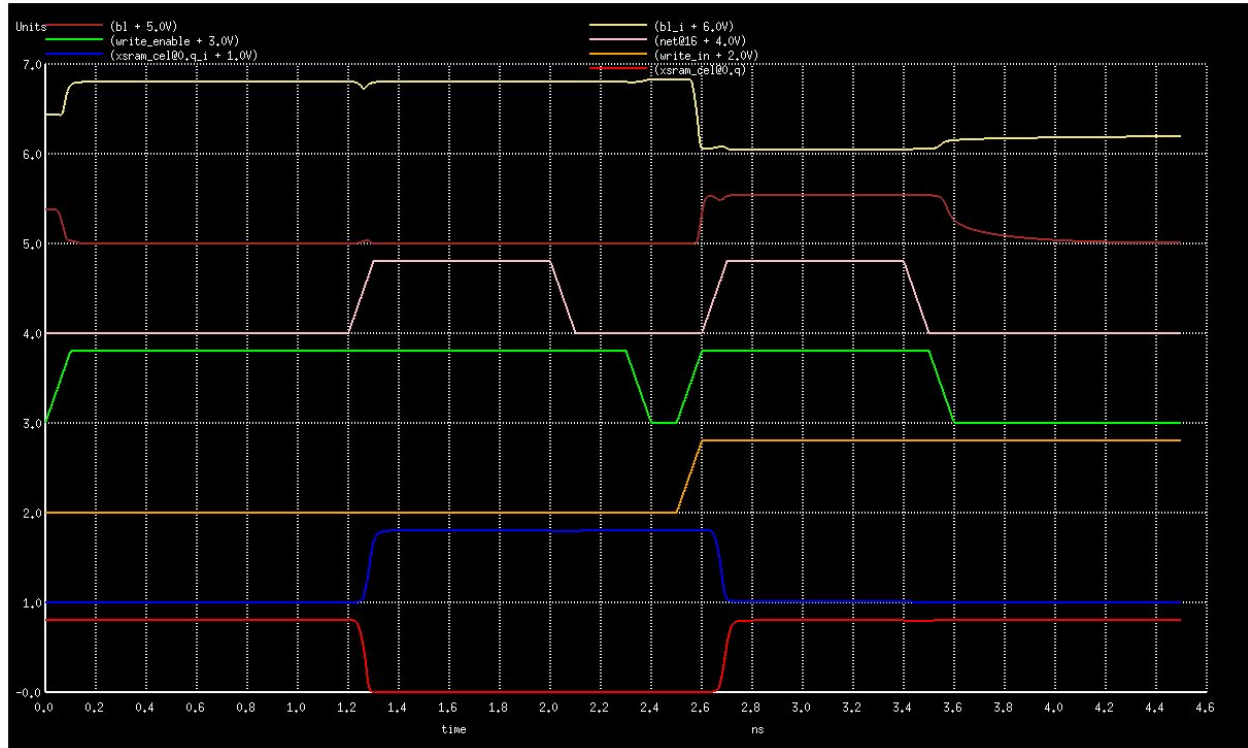


Figure 5: Writing 0, then writing 1

Writing 0 and Writing 0

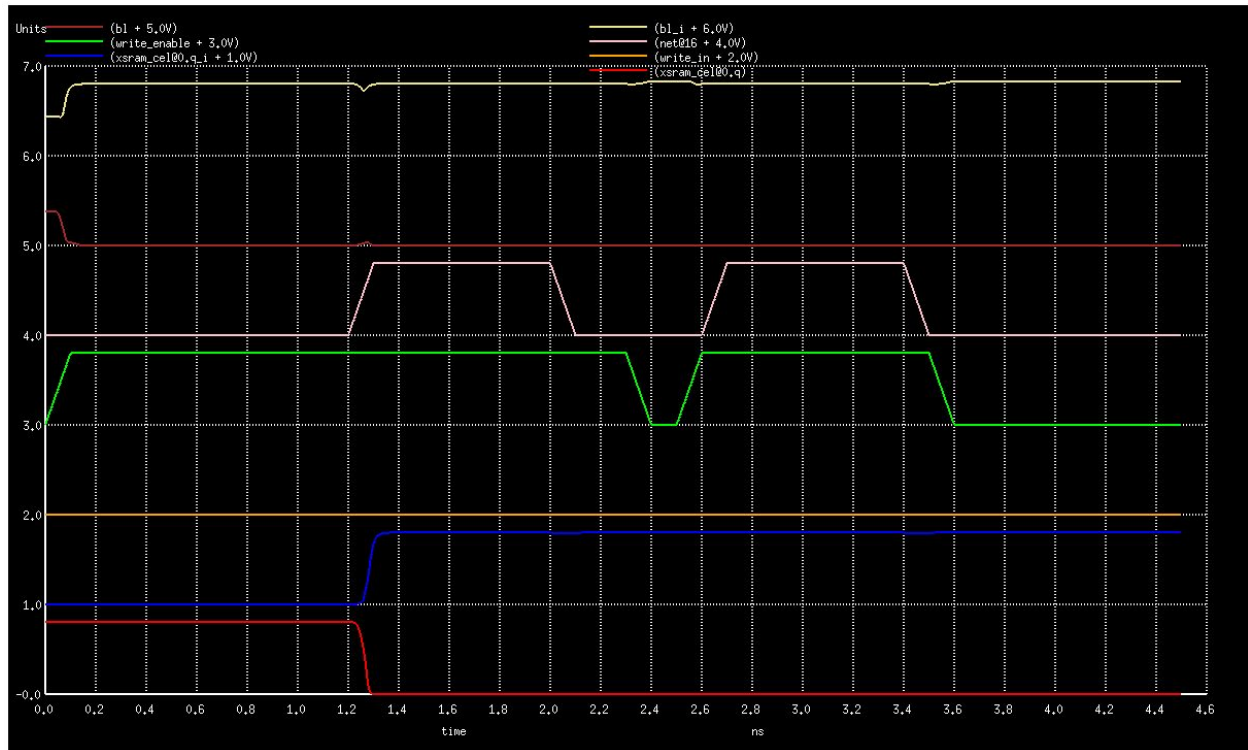


Figure 6: Writing 0, then writing 0

Constraints on Write Timing, Full FIFO Design

TODO