5. Übung IBN

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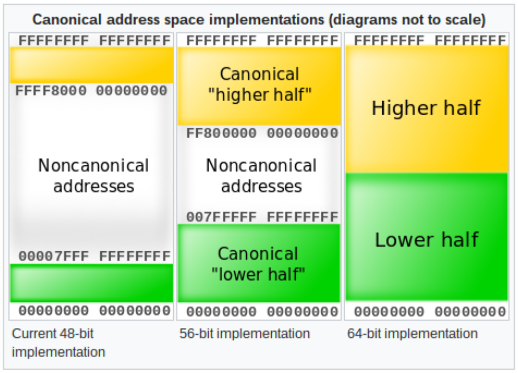
Augabe 1

a. In Intels *System programming guide* for their 64 and IA-32 Architectures , all the necessary information about paging can be found: `https://software.intel.com/sites/default/files/managed/a4/60/325384-sdm-vol-3abcd.pdf`
The supported page sizes for the 4-Level-Paging used on the 64-Bit Architecture are 4KiB, 2MiB, and 1GiB.

b. The canonical address design ensures, that there are effectively two halves of virtual addresses. Some systems use these memory halves to implement a *user* and a *kernal space*. This feature eases later scalability into true 64-Bit addressing, because there is still a large unused non-canonical region in memory. Because it lies in the ”center” of the virtual address space, both the lower and upper memory half can easily be extended by increasing/decreasing the addresses of each region, respectively.



Aufgabe 2

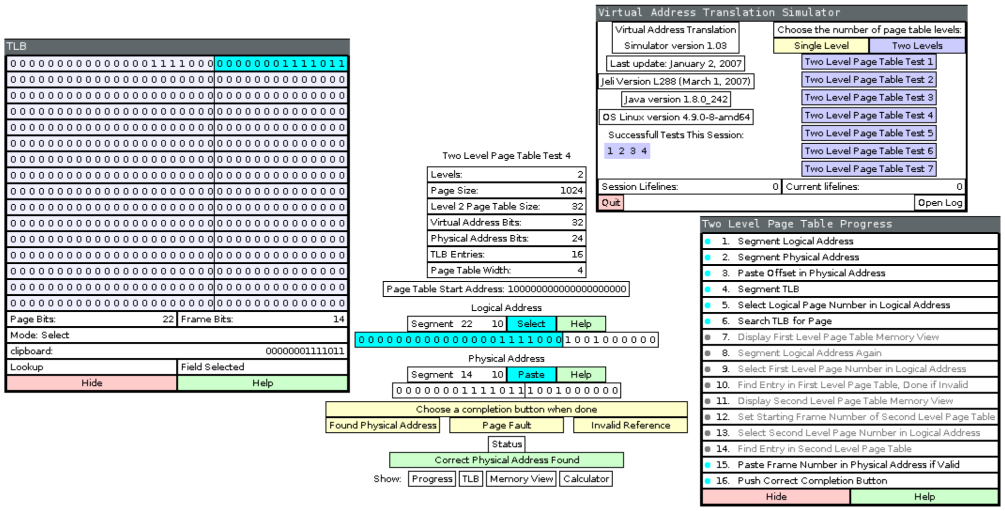
The benefit of supersections is an effectively lower amount of required accesses. This can e.g. be benificial for operating systems, where large regions of memory have to be loaded at all times. This doesnt come without a trade-off though, as the chance for internal fragmentation rises exponentially with the pagesize.

Aufgabe 4

For a pagesize of 4 kB, the offset is 12 bits. This leaves 20 bits for the page index. That means there are $2^{20} = 1$ MB entries in the direct page table. To address 512 MB physical memory, we need 512 MB / 4 kB pages, which means 2^{17} entries in the inverted page table. Since each entry of these tables has 4 bytes, the sizes of each tables are 8 MB (1.5%) of memory, and 512 kB (0.1% of memory), respectively.

Aufgabe 5

The virtual address $\overset{\text{page index}}{0000000000000001111000}\ \overset{\text{offset}}{1001000000}$ translates to $\overset{\text{frame index}}{00000001111011}\ \overset{\text{offset}}{1001000000}$ in the physical address space.
Its location can be found in the TLB, so a further lookup of the level 1 and 2 page tables in the memory is not necessary. See below for the result.



TLB

0000000000000001111000	00000001111011
0000000000000000000000	00000000000000
0000000000000000000000	00000000000000
0000000000000000000000	00000000000000
0000000000000000000000	00000000000000
0000000000000000000000	00000000000000
0000000000000000000000	00000000000000
0000000000000000000000	00000000000000
0000000000000000000000	00000000000000
0000000000000000000000	00000000000000
0000000000000000000000	00000000000000
0000000000000000000000	00000000000000
0000000000000000000000	00000000000000
0000000000000000000000	00000000000000
0000000000000000000000	00000000000000
0000000000000000000000	00000000000000
Page Bits: 22	Frame Bits: 14

Mode: Select
clipboard: 00000001111011
Lookup | Field Selected

Two Level Page Table Test 4

Levels:	2
Page Size:	1024
Level 2 Page Table Size:	32
Virtual Address Bits:	32
Physical Address Bits:	24
TLB Entries:	16
Page Table Width:	4

Page Table Start Address: 100000000000000000000

Logical Address
Segment 22 10
0000000000000001111000 | 1001000000

Physical Address
Segment 14 10
00000001111011 | 1001000000

Choose a completion button when done
Status: Correct Physical Address Found

Virtual Address Translation Simulator
Virtual Address Translation Simulator version 1.03
Last update: January 2, 2007
Jeli Version L288 (March 1, 2007)
Java version 1.8.0_242
OS Linux version 4.9.0-8-amd64
Successfull Tests This Session: 1 2 3 4
Session Lifelines: 0
Current lifelines: 0

Two Level Page Table Progress
1. Segment Logical Address
2. Segment Physical Address
3. Paste Offset in Physical Address
4. Segment TLB
5. Select Logical Page Number in Logical Address
6. Search TLB for Page
7. Display First Level Page Table Memory View
8. Segment Logical Address Again
9. Select First Level Page Number in Logical Address
10. Find Entry in First Level Page Table, Done if Invalid
11. Display Second Level Page Table Memory View
12. Set Starting Frame Number of Second Level Page Table
13. Select Second Level Page Number in Logical Address
14. Find Entry in Second Level Page Table
15. Paste Frame Number in Physical Address if Valid
16. Push Correct Completion Button

Select
Help
Paste
Found Physical Address
Page Fault
Invalid Reference
Show: Progress TLB Memory View Calculator
Choose the number of page table levels:
Single Level
Two Levels
Two Level Page Table Test 1
Two Level Page Table Test 2
Two Level Page Table Test 3
Two Level Page Table Test 4
Two Level Page Table Test 5
Two Level Page Table Test 6
Two Level Page Table Test 7
Quit
Open Log
Hide
Help