

P65_1233

I/O PAD Library Datasheet

Process: 65nm 1.2V/3.3V

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Library Description

The P65_1233_1P5M is a library that offers designers a wide range of functional and performance options for I/O circuits. Using this library, a design can obtain the optimum electrical solution with minimal effort. The library includes circuitry such as:

TABLE 1 I/O application table

I/O Type	Option and possible Combination
Standard I/O interface pads	1.2V core 3.3V input and output Schmitt trigger/CMOS input buffer Pull-up Tr. resistor range: 50k (Ohm) Pull-down Tr. resistor range: 50k (Ohm) Output frequency: 100MHz Output buffer with programmable driver strength 2mA,8mA, 10mA, and 16mA

Library Attributes

Physical description

This databook for the P65_1233 describes each cell in the library. This section discusses certain attributes that are general to all cells in the library. As it is implemented, a design should incorporate these general attributes as well as the data for specific cells.

The cells in the P65_1233 are constructed to have the following dimensions:

TABLE 2 Digital I/O Physical Specification

<i>ITEMS</i>	<i>CONTENTS</i>
Process	P65_1233 Salicide 1.2V/3.3V
Metal Layers	Suitable for 4,5,6,7 or 8 layers application
Cell Size (Width * height)	65 um * 130 um including pads
Pad opening window size (Width * height)	55 um * 55 um
Pad opening window center Coordinate	(X, Y): (32.5, 34)

TABLE 3 Analog I/O Physical Specification

<i>ITEMS</i>	<i>CONTENTS</i>
Process	P65_1233Salicide 1.2V/3.3V
Metal Layers	Suitable for 4,5,6,7 or 8 layers application
Cell Size (Width * height)	65 um * 130 um including pads
Pad opening window size (Width * height)	55 um * 55 um
Pad opening window center Coordinate	(X, Y): (32.5, 34)

Recommended Operating Conditions

Table 4 shows recommended operating conditions for integrated circuits developed with this library.

TABLE 4 Recommended Operating Conditions

<i>Symbol</i>	<i>Parameter</i>	<i>Min.</i>	<i>Norm.</i>	<i>Max.</i>
VDDIO	Post-driver supply voltage	2.97V	3.3V	3.63V
VDD	Pre-driver supply voltage	1.08V	1.2V	1.3V
VIH	Input High Voltage	2.0V		
VIL	Input Low Voltage			0.8V
VT+	Schmitt trig Low to High threshold point	1.88V	1.94V	2.0V
VT-	Schmitt trig. High to Low threshold point	1.36V	1.42V	1.55V
RPU	Pull-up resistor		50Kohm	
RPD	Pull-down resistor		50Kohm	
TJ	Junction Temperature	-40°C	25°C	125°C
II	Input leakage current @VI=3.3V or 0V			±100nA
VOL	Output low voltage			0.4V
VOH	Output high voltage	2.4V		
Output pad operating frequency @C_{Load}=10p		100MHz		

These estimates are not valid for designs that fall outside of these typical conditions.

See *Estimating Cell Delay* on page 5 for information and equations to use when making estimates for designs.

Metal Layer Support

The P65_1233 supports all metal layers supported by foundry. With foundry's approval, you may restrict the number of metal layers that you will use in your implementations. The I/O library properly implements designs using five, six, seven, or eight layers of metal. Foundry requires that the top-level metal uses a greater minimum spacing than lower-level metal layers.

Synopsys Timing Considerations

The timing models included with this library are based on the Synopsys table-driven look-up model. To improve accuracy, the library timing models use input slews and output loads that minimize error due to nonlinear behavior. The library specifies Max Slew and Max Capacitance attributes that correspond with the technology the library supports. The power characteristics of circuits with pull-up or pull-down options are extracted from worst case scenarios. In these scenarios, the device is constantly supplying the maximum current possible under the appropriate environmental conditions.

Design Considerations

To use the I/O library most effectively, a design must take into account many physical, electrical, and functional considerations. This library includes a set of application notes that discusses these considerations, including the following types of information about the library circuitry:

- Physical and electrical characteristics
- Implementation guidelines
- Recommendations for power/ground pin placement

Estimating Cell Performance

The values that appear in the databook for power and cell delay apply only to the typical operating conditions, as follows:

- $V_{dd} = 1.2V$
- Junction temperature = $25^{\circ}C$
- Typical process parameters for both thin and thick (high voltage) gate oxide devices.

Estimating Cell Delay

Output driver loading conditions and interface I/O cell floor planning can vary to a great extent. As a result, calculating the delay of an output is often difficult. The databook provides delay values for simple capacitive loading under ideal power supply conditions. From this data, it is possible to estimate the amount of delay that the output driver incurs. However, such an estimate must take into account the drive level for the given load condition. For information about impedance characteristics, see the Application Notes. The delay of a signal through an interface connection consists of four parts:

- Intrinsic delay
- Output slew rate
- Driver impedance vs load
- I/O cell floor planning

Intrinsic Delay

Intrinsic delay is the amount of time it takes a signal to propagate through an output driver under no-load condition. To obtain a first order approximation for the intrinsic delay, simply use the delay for the lightly loaded condition (i.e., nearest to $0pF$).

Output slew Rate

Output slew rate is the rate at which the output signal voltage changes during transition. The slew rate is dependent upon the amount of current that can be sourced into or sunk from the load, as well as dependent upon the transient characteristics of the current. An estimate for the slew rate of the output depends on the particular loading condition such as physical line configuration or impedance. In most simple cases where the output impedance of the driver matches that of the load, the slew data for a $10pF - 15pF$ load range is sufficient.

Driver Impedance vs Load

The relationship between the driver and load impedances (R_s vs Z_o) determines the characteristics of the signal that propagates through the interconnect load. The resulting signal can be over damped, under damped, or critically damped. In critically damped and under damped cases, the time that it takes a signal to propagate through the interconnect load is represented by the time of flight. For over damped cases, the propagation time can be multiples of the time of flight. (See the Application Notes for more information about impedance matching.) The total delay introduced by the output driver and the interconnect can then be represented by: *Intrinsic delay* + $(0.5) (VDDIO/SR)$ + $(m) (Interconnect\ time\ of\ flight)$ where m is greater than 1 if the signal is over damped.

In many cases, using the $10pF$ - $15pF$ delay data given in the databook is sufficient. Thus the total delay for the $10pF$ case can be:

$$(Delay@10pF) + (m) (Interconnect\ time\ of\ flight)$$

I/O Cell Floor planning

I/O cell floor planning refers to the order in which I/O signals and power/ground pins are distributed around a device. Floor planning can affect the propagation delay. This effect is highly dependent upon the type of circuit used, package characteristics, loading conditions, and the signal environment. The worst performance degradation occurs when many I/O signals switch logic states at the same time and in the same direction. This is known as simultaneously switching outputs (SSOs). See the Application Notes for more information. The Application Notes also show how to approximate the effect a particular floor plan can have on time delay.

Reading the Library Datasheet

Each datasheet in the databook contains a standard set of information. This chapter describes the information contained in each element of the datasheet.

Note: This chapter shows various examples of datasheet elements. Do not assume that the data in these examples corresponds to the data for any specific library technology. The examples in this chapter are intended to illustrate the types of data each datasheet element contains.

I/O Cell Datasheet Elements

An I/O cell datasheet includes the following elements:

- Cell Name
- Pin Descriptions
- Cell Attributes
- Cell Delays

Cell Name

This databook uses naming conventions to identify cells by their function, voltage interface, standard, output drive, and relative performance level. A representative cell name is P65_1233_PBMUX. The name of the cell is built from fields indicating required or optional information about the cells. For example, the cell name P65_1233_PBMUX indicates a Bi-directional I/O cell with analog pin.

The table below lists the fields used to derive cell names the table below lists the fields used to derive cell names. The cell description is effectively an expanded version of the cell name.

TABLE 5 Cell Name Description

<i>Field Number</i>	<i>Characters</i>	<i>Description</i>
P	P	PAD
6	65-1233	65nm 1.2/3.3V
P	P	Pad Limited
	C	Core Limited
A	S	Schmitt
	N	Normal
B	B	Bi-directional
	I	Input Only
	O	Output Only
	A	Analog
C	C	N-Channel
	O	P-Channel
	DS1	Programmable driver strength
D	U	Pull Up
	D	Pull Down
E	1.2V	1.2V input
	3.3V	3.3V input
F	2	2mA
	8	8mA
	10	10mA
	16	16mA

Cell Attributes and Operating Conditions

The following table shows a representative set of cell attributes and operating conditions. Area is in square microns, VDD is in volts, VDDIO is in volts, temperature is in degrees C, and process used is typical, unless otherwise stated.

Cell Attributes and Operating Conditions

<i>Area</i>	<i>VDD</i>	<i>VDDIO</i>	<i>Temp</i>	<i>Process</i>
16900	1.2V	3.3V	25°C	Typical

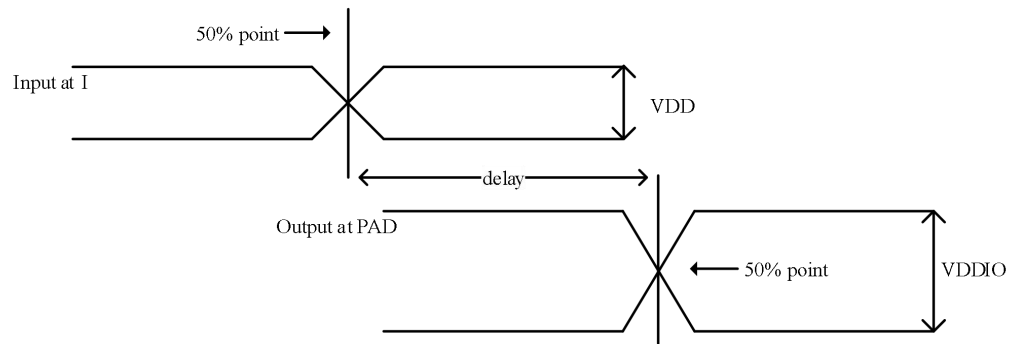
The values in the cell delay and power dissipation tables that appear in the datasheet for a given cell are based on characterizations that use these cell attributes.

Cell Delays

The following table shows how the datasheet expresses cell delays. Values for cell delay express the input-to-output delays for both rising and falling transitions on the output. The delay values are based on:
Load: the capacitive load (in pF) for signals that drive external circuitry.

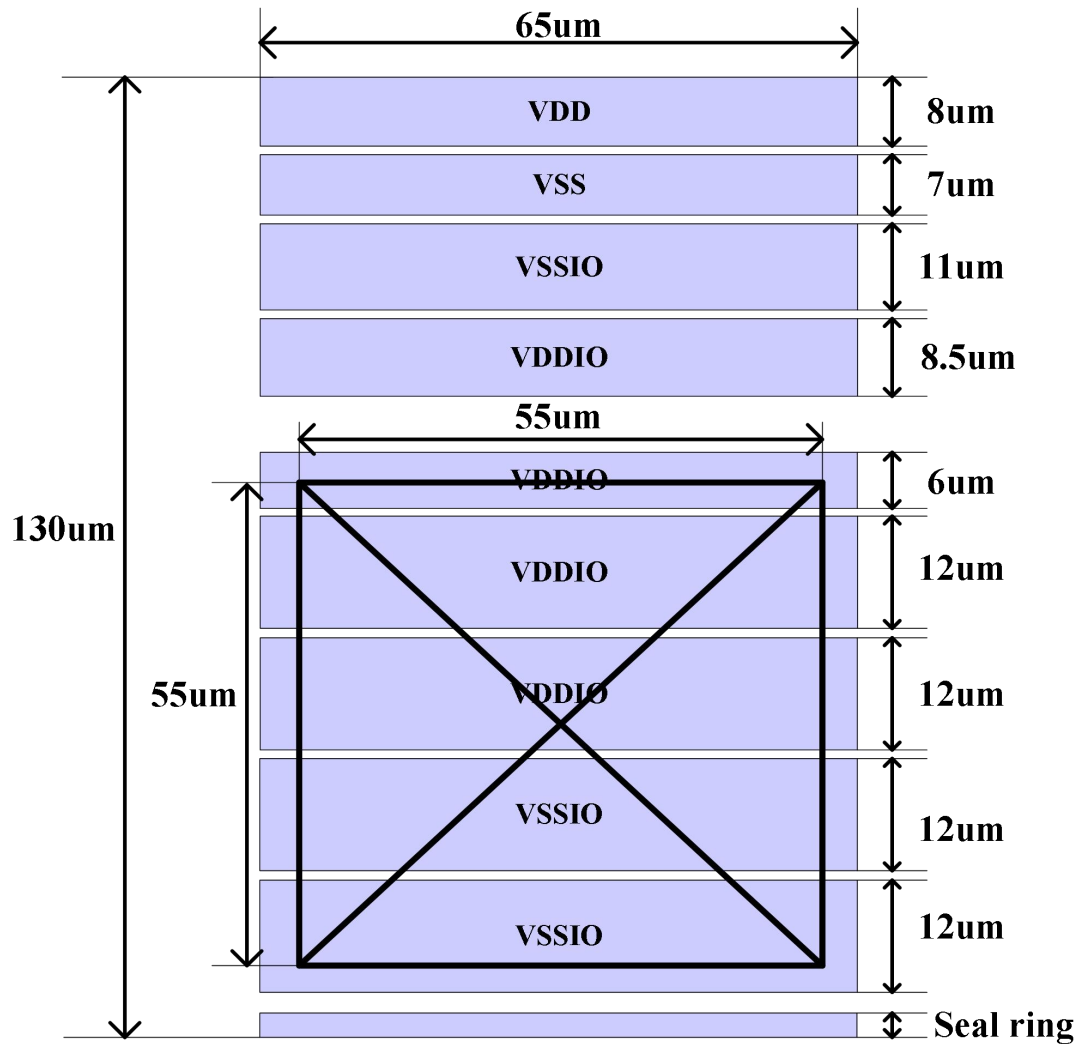
Delay Time

The time delay of a signal simply represents the amount of time it takes a signal to propagate through any given circuit. Be aware that most signals are shifted in voltage scale as they pass from one side of the interface to another. For example, Figure 1 illustrates an input signal of VDD that is shifted in scale to an output signal of $VDDIO$.



Power bus Scheme

Preliminary Power Bus scheme used for the pad limited IO in line pad of 65um * 130 um.



Special Cells

The standard library includes a number of cells that satisfy special circuitry needs. This section discusses the types of special cells included in the library.

Filler Cells

Filler cells provide a connection between power and ground rails in an area where cells are not present; for instance, between the cells. Filler cells are used during place and route. The library contains several filler cells. The filler cell number specifies the width of the cell in microns (except for 0, which is 0.1mm). For more information on the characteristics and use of filler cells, see the Application Notes.

Please refer to the Application Notes for further information on special cells and their usage.

Table of Physical Cells

The library contains Digital and analog I/O cells. Table6 and Table7 lists cell names and types, and the number of cells the library provides for each type of cell.

1 Digital I/O Cell Category

TABLE 6 Digital I/O Cell categories

<i>Cells Name</i>	<i>Function Description of Digital I/O Cells</i>	<i>Cell Size (um * um)</i>
P65_1233_PBMUX	Bi-directional I/O cell with analog pin	65*130
P65_1233_PWE	Crystal Oscillator, with High Enable, Low Frequency (~20MHz)	130*130
P65_1233_VDD1	1.2V VDD power pad for core	65*130
P65_1233_VDD3	1.2V VDD power pad for I/O pre-driver & core	65*130
P65_1233_VDDIO3	3.3V VDDIO power pad for I/O post-driver & core	65*130
P65_1233_VSS1	VSS ground pad for core	65*130
P65_1233_VSS3	VSS ground pad for I/O pre-driver & core	65*130
P65_1233_VSSIO3	VSSIO ground pad for I/O post-driver & core	65*130
P65_1233_FILLER0005	Digital Filler cell 0.005um	0.005*130
P65_1233_FILLER001	Digital Filler cell 0.01um	0.01*130
P65_1233_FILLER01	Digital Filler cell 0.1um	0.1*130
P65_1233_FILLER1	Digital Filler cell 1um	1*130
P65_1233_FILLER2	Digital Filler cell 2um	2*130
P65_1233_FILLER5	Digital Filler cell 5um	5*130
P65_1233_FILLER10	Digital Filler cell 10um	10*130
P65_1233_FILLER20	Digital Filler cell 20um	20*130
P65_1233_FILLER50	Digital Filler cell 50um	50*130
P65_1233_CORNER	Digital corner cell	130*130

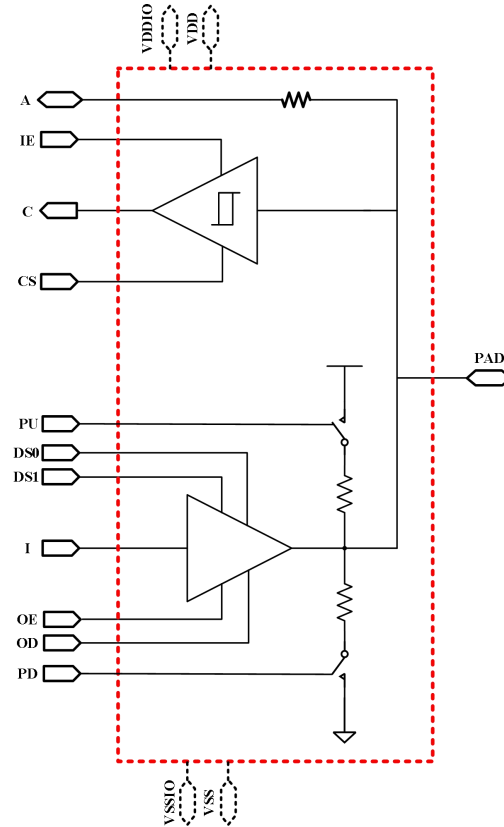
Symbol used in Truth Table

<i>Symbol</i>	<i>Description</i>
0	Logic low
1	Logic high
W	Whatever 0 or 1 input, no impact to output result
-	No input signal
L	Weak logic low
H	Weak logic high
Z	High impedance
X	Unknown state

1.1 P65_1233_PBMUX

Description:

Bi-directional I/O cell with analog pin (pull up/down resistor 50Kohm)



Pin Description:

Name	Type	Voltage	Description	Edge Active
PAD	In/Out	3.3	PAD	-
C	Out	1.2	Input buffer output	-
A	In/Out	3.3	Analog signal pin	-
IE	In	1.2	Input buffer enable	High True
CS	In	1.2	Schmitter trigger input buffer	0
	In	1.2	CMOS input buffer	1
I	In	1.2	Output buffer input	-
OE	In	1.2	Output mode enable	High True
OD	In	1.2	Open drain output mode enable	High True
PU	In	1.2	Weak pull-up resistor mode	High True
PD	In	1.2	Weak pull-down resistor enable	High True
DS0	In	1.2	4bit different driving strength	-
DS1	In	1.2		-

Cell Attributes and Operating Conditions

Area	VDD	VDDIO	Temp	Process
8450	1.2V	3.3V	25°C	Typical

Output AC Specification (from pin 'I' to pin 'PAD')

Conditions			Rise time (ns)			Fall time (ns)		
Supply Voltage(V)	Frequency (MHz)	CL (pf)	Min.	Typ.	Max.	Min.	Typ.	Max.
3.3	10	50	2.866	3.981	5.821	2.561	3.565	5.787
	40	20	1.254	1.719	2.529	1.124	1.567	2.487
	100	10	0.706	0.988	1.454	0.661	0.909	1.441
Conditions			Delay ↑(ns)			Delay ↓(ns)		
Supply Voltage(V)	Frequency (MHz)	CL (pf)	Min.	Typ.	Max.	Min.	Typ.	Max.
3.3	10	50	1.863	2.631	4.157	1.931	2.706	4.349
	40	20	1.14	1.624	2.641	1.153	1.646	2.668
	100	10	0.896	1.289	2.141	0.916	1.315	2.152

Truth Table

Mode	Input Pins								Output Pins	
	OE	IE	CS	PU/PD	I	OD	DS0/DS1	PAD/A	PAD/A	C
Input Mode	0	1	W	W	W	W	W	1	1	1
	0	1	W	W	W	W	W	0	0	0
	0	1	W	1	W	W	W	-	H(PU)/L(PD)	1(PU)/0(PD)
	0	1	W	0	W	W	W	-	Z	X
	0	0	W	W	W	W	W	1	1	0
	0	0	W	W	W	W	W	0	0	0
	0	0	W	1	W	W	W	-	H(PU)/L(PD)	0
	0	0	W	0	W	W	W	-	Z	0
Output Mode	1	1	W	W	1	0	W	-	1	1
	1	1	W	W	0	0	W	-	0	0
	1	1	W	W	0	1	W	-	0	0
	1	1	W	1	1	1	W	-	H(PU)/L(PD)	1(PU)/0(PD)
	1	1	W	0	1	1	W		Z	X
	1	0	W	W	1	0	W		1	0
	1	0	W	W	0	0	W		0	0
	1	0	W	W	0	1	W		0	0
	1	0	W	1	1	1	W		H(PU)/L(PD)	0
	1	0	W	0	1	1	W	-	Z	0

Attention: PU and PD cannot be high at the same time.

<i>DS1</i>	<i>DS0</i>	<i>Driver Strength</i>
0	0	16mA
0	1	10mA
1	0	8mA
1	1	2mA

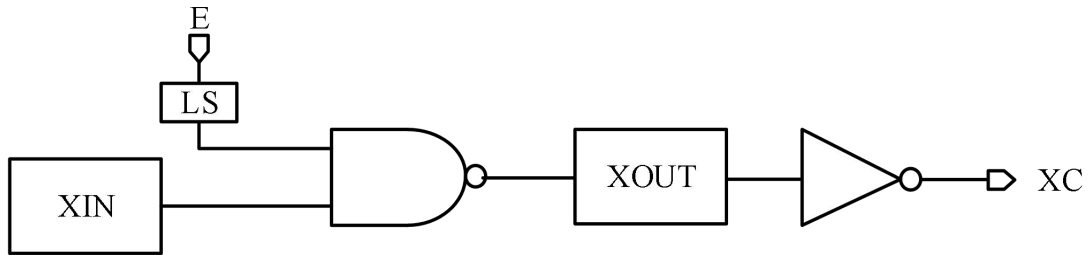
Important: Customer making use of the above pad please notes there is difference from other bidirectional pad in that:

- 1) The DS0 and DS1 are low active;*
- 2) The Output enable is Positive Enable.*

1.2 P65_1233_PWE

Description:

Crystal Oscillator, with High Enable, Low Frequency (~20MHz)



Pin Description:

Name	Type	Voltage	Description	Edge Active
XIN	In	3.3	Oscillator input pad	-
E	In	1.2	Oscillator enable	High True
XOUT	Out	3.3	Oscillator output pad	-
XC	Out	1.2	Clock output to core	-

Cell Attributes and Operating Conditions

Area	VDD	VDDIO	Temp	Process
16900	1.2V	3.3V	25°C	Typical

Output AC Specification (from pin 'XIN' to pin 'XOUT')

Conditions			Delay ↑(ns)			Delay ↓(ns)		
Supply Voltage(V)	Frequency (MHz)	CL (pf)	Min.	Typ.	Max.	Min.	Typ.	Max.
3.3	20	10	1.765	2.095	2.541	2.162	2.193	2.23

Output AC Specification (from pin 'XIN' to pin 'XC')

Conditions			Delay ↑(ns)			Delay ↓(ns)		
Supply Voltage(V)	Frequency (MHz)	CL (pf)	Min.	Typ.	Max.	Min.	Typ.	Max.
3.3	20	0.05	2.981	3.47	4.203	2.089	2.39	2.643

Output AC Specification (from pin 'E' to pin 'XOUT')

Conditions			Delay ↑(ns)			Delay ↓(ns)		
Supply Voltage(V)	Frequency (MHz)	CL (pf)	Min.	Typ.	Max.	Min.	Typ.	Max.
3.3	20	10	3.281	4.205	5.701	3.292	4.177	5.715

Output AC Specification (from pin 'E' to pin 'XC')

<i>Conditions</i>			<i>Delay ↑(ns)</i>			<i>Delay ↓(ns)</i>		
<i>Supply Voltage(V)</i>	<i>Frequency (MHz)</i>	<i>CL (pf)</i>	<i>Min.</i>	<i>Typ.</i>	<i>Max.</i>	<i>Min.</i>	<i>Typ.</i>	<i>Max.</i>
3.3	20	0.05	4.235	5.426	7.36	3.429	4.51	6.338

Truth Table

<i>Input Pins</i>		<i>Output Pins</i>	
E	XIN	XOUT	XC
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

2 Analog I/O Cell Categories

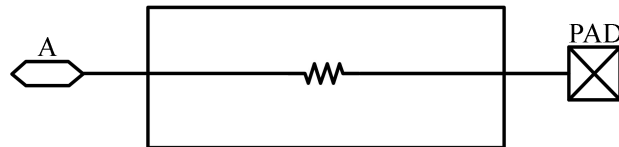
TABLE 7 Analog I/O Cell Categories

<i>Cells Name</i>	<i>Function Description of Analog I/O Cells</i>	<i>Target Cell Size (um*um) (Width*height)</i>
P65_1233_PAR	Analog pad with series resistor (resistor 300ohm)	65*130
P65_1233_PAR_5	Analog pad with series resistor (resistor 5ohm)	65*130
P65_1233_VDD1A	3.3V analog VDD1A power pad for core	65*130
P65_1233_VSS1A	3.3V analog VSSA ground pad for I/O ground ring & core	65*130
P65_1233_CUT	Power-cut cell for same voltage level between digital and analog	65*130

2.1 P65_1233_PAR

Description:

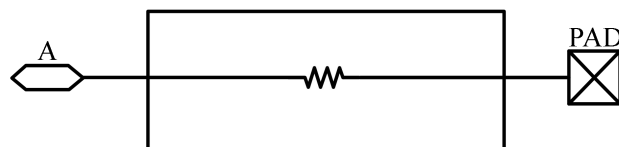
Analog pad with series resistor 300ohm, metal width is 22um and maximum allowable current 10mA.



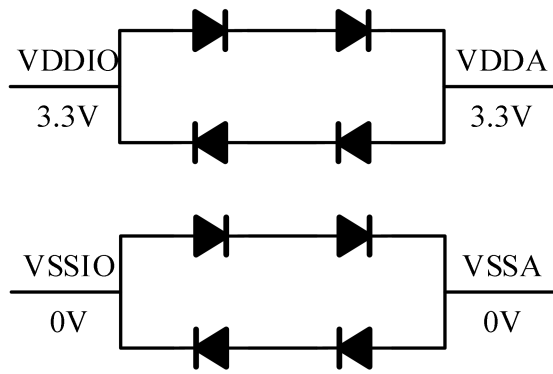
2.2 P65_1233_PAR_5

Description:

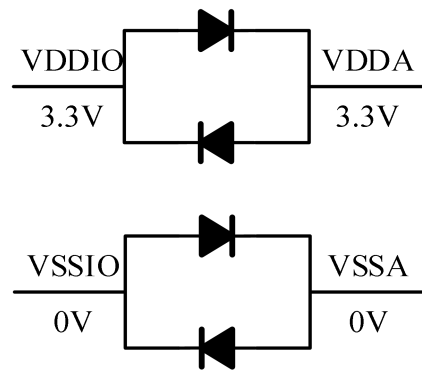
Analog pad with series resistor 5ohm, metal width is 22um and maximum allowable current 10mA.



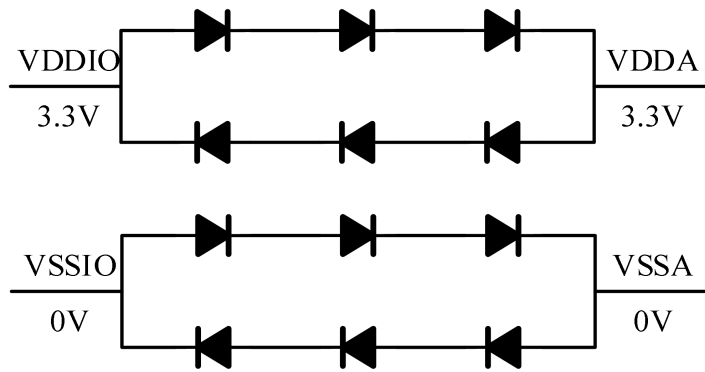
POWER CUT1



POWER CUT2



POWER CUT3



Note: POWER CUT 2 and POWER CUT 3 are delivered upon request.

Appendix: Diagram of Analog IO and Power rail (reference only)

