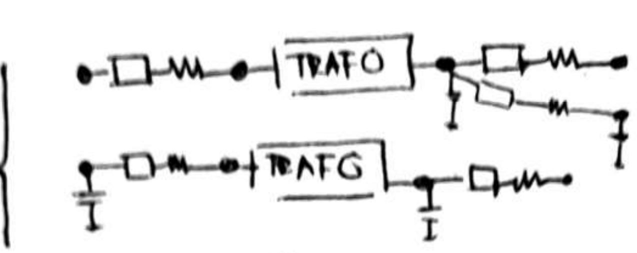
TRAFOS

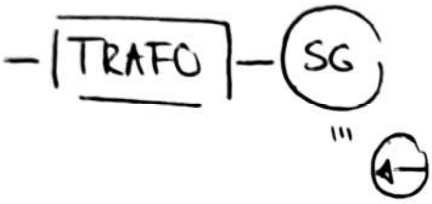
- add_trafo:



ANY RL
↳ connect_mtx_RL
T_NET

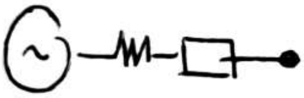
"missing" ALL Pi
individual element

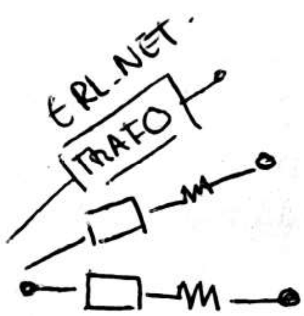
NO !! S'han de posar com RL a AC_NET. El codi no està prou ben fet (es podria automatitzar).



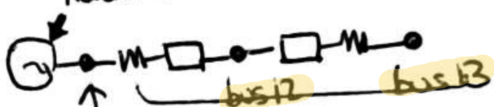
cal posar una càrrega entremig.

TH add_TH.



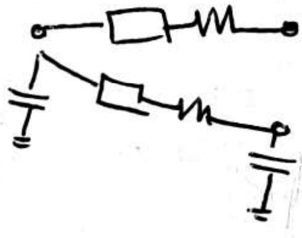


S'afegeix un bus a rl "Additional TH"

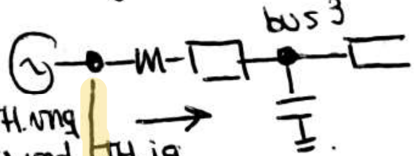


va a RL connect_mtx

v[n+1 q], v[n+1 d]. input global.



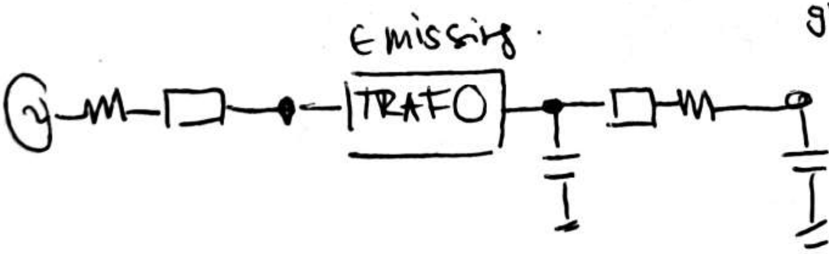
"missing"



TH.vnq, TH.vnd: input global

TH.iq, TH.id → not a bus in NET

E missing.



This case would be a problem cause TRAFO would not be in rl_net but current is the same

BUT...

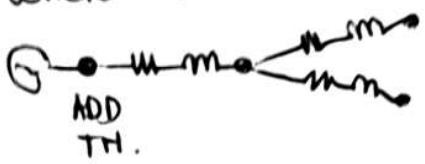
- The TRAFO goes to missing in add_trafo.
- add_trafo warns "connect to voltage source"

!

TRAFO should be added to T_NET as RL.

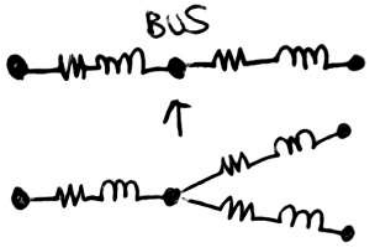
generate_general.rl.NET

rl_T_Nodes contains all buses where an  is connected

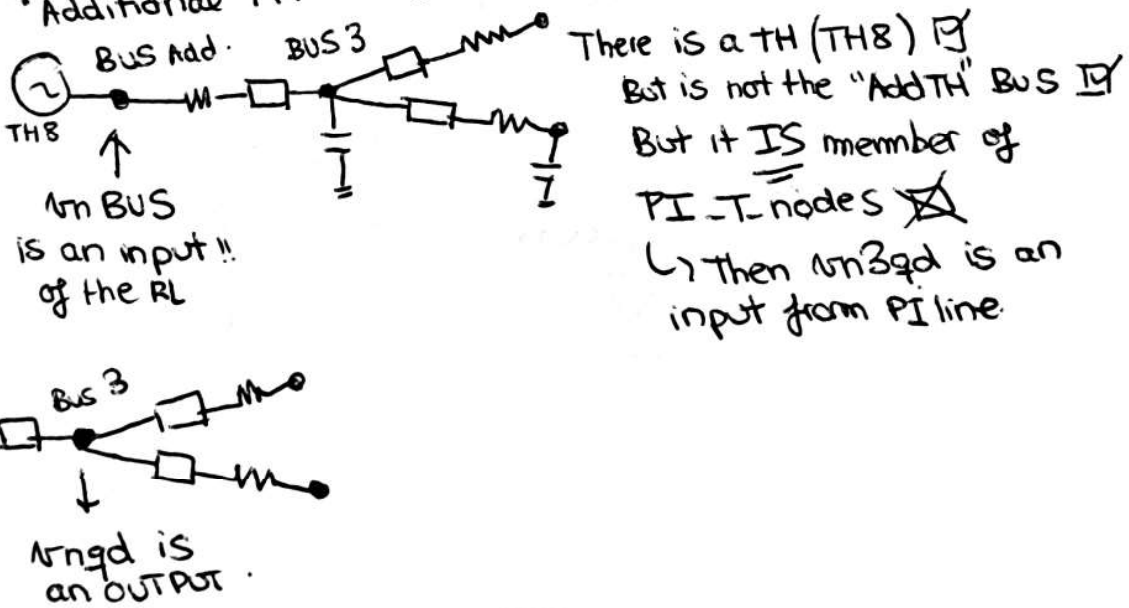
+ additional TH: 

① Generate inputs/outputs of RL_NET:

for each bus in rl_T_Nodes:

IF (rl_Tnodes ↓ empty bus & not member of PI_Tnodes) 

OR (There is a TH & The TH is NOT an additional TH & not member of PI_T_nodes)



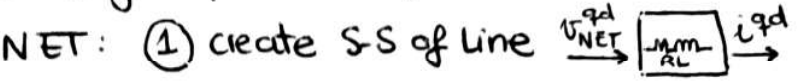
➡ outputs: n_ng, n_nd of bus

ELSE: there is something connected as voltage source / a PI line.

➡ inputs: n_ng, n_nd of bus

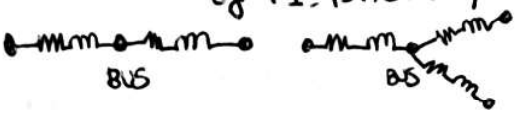
② Generate SS of RL NET:

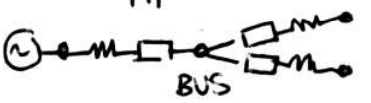
The code goes through all lines in RL NET and generates its state space.
Also, it creates the "bus voltage output" state-space in the "internal nodes.

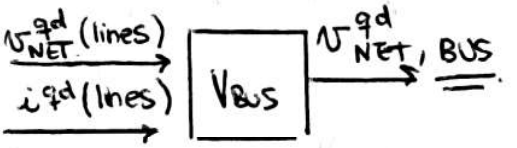
→ for each line in rl_T_NET: ① create S-S of line 

②  ⇨ check if bus_to is "internal"

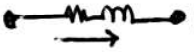
IF (there is nothing connected & not member of PI_T_nodes) OR (There is a TH & NOT an additional TH & NOT member of PI_T_nodes)





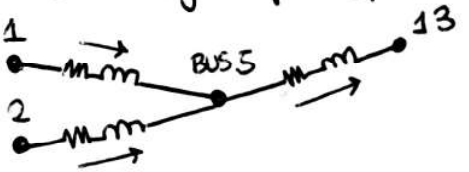
↳ Bus is internal ⇨ create 

① Identify RL lines connected to BUS

lines_in :  BUS (current flows IN)

lines_out: BUS  (current flows OUT)

② Generate "bus voltage output" q and d SS.

Example: 

I write an small example to help understand the code !!

$$\begin{cases} \frac{di_{15}}{dt} = -\frac{1}{L_{15}}\left(R_{15}\cdot i_{15}(t) - v_1(t) + v_5(t)\right) & [1] \\ \frac{di_{25}}{dt} = -\frac{1}{L_{25}}\left(R_{25}\cdot i_{25}(t) - v_2(t) + v_5(t)\right) & [2] \\ \frac{di_{513}}{dt} = -\frac{1}{L_{513}}\left(R_{513}\, i_{513}(t) + v_3(t) - v_5(t)\right) & [3] \\ i_{15} = i_{513} - i_{25} & [4] \end{cases}$$

[4] ➡ [2] $\frac{d(i_{513})}{dt} - \frac{d(i_{15})}{dt} = -\frac{1}{L_{25}}\left(R_{25}\cdot i_{25} - v_2 + v_5\right)$ (kill $d/dt\, i_{25}$)

[2] ➡ [3] $-\frac{1}{L_{513}}\left(R_{513}\, i_{513} + v_3 - v_5\right) = \frac{di_{15}}{dt} - \frac{1}{L_{25}}\left(R_{25}\cdot i_{25} - v_2 + v_5\right)$ (kill $d/dt\, i_{513}$)

[3] ➡ [1] $-\frac{1}{L_{513}}\left(R_{513}\, i_{513} + v_3 - v_5\right) = -\frac{1}{L_{15}}\left(R_{15}\cdot i_{15} - v_1 + v_5\right) - \frac{1}{L_{25}}\left(R_{25} i_{25} - v_2 + v_5\right)$ kill $d/dt\, i_{15}$

$$v_5\underbrace{\left(\frac{1}{L_{513}} + \frac{1}{L_{15}} + \frac{1}{L_{25}}\right)}_{\text{-sum}} = i_{15}\left(\frac{R_{15}}{-L_{15}}\right) + i_{25}\left(\frac{R_{25}}{-L_{25}}\right) - i_{513}\left(\frac{R_{513}}{L_{513}}\right) + v_1\left(\frac{1}{L_{15}}\right) + v_2\left(\frac{1}{L_{25}}\right) + v_3\left(\frac{1}{L_{513}}\right)$$

i_{15}, i_{25}, i_{513} v_1, v_2, v_3 → INPUTS ✓

v_5 → OUTPUT

for each line in rl_T_NET:

→ bus_to → check if "bus_to" is internal

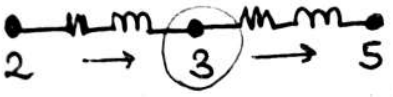
¿ what about bus_from?

⚠ In some cases, bus_from will not be detected as internal

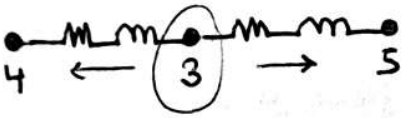
A) bus_from ∈ to PI

⇨ then ok, no need of generating V_{BUS} state-space (it will come from the PI NET)

B) bus_from ∈ to RL:



Bus 3 will be detected as internal when building line 2-3 so ok ☑

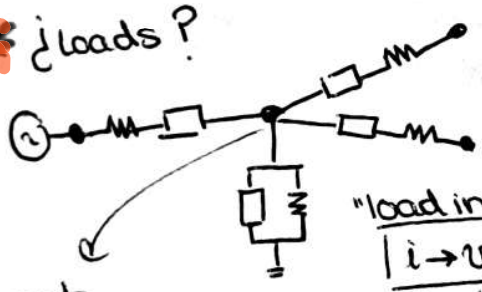


Bus 3 will NOT be detected as internal

⇨ ERROR: lines 3-5, 3-4 will expect V_{n3gd} as input but it won't exist.

this should be fixed!!!. FIXED

¿loads?



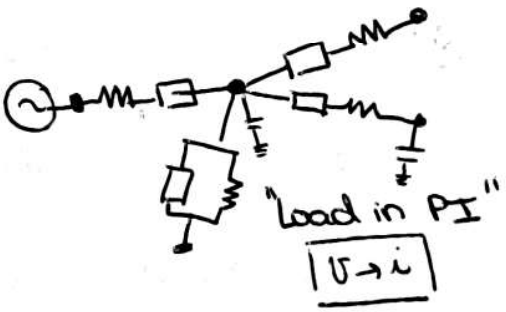
"load in RL"

$i \rightarrow V$

not internal because of load.

sum of currents from lines

↳ bus voltage



"Load in PI"

$V \rightarrow i$