How can the effectiveness of marketing 'Airbnb Seattle' be improved? – dataset of 2016

LIST Nicole , LÖHR Tim,
BOHNSTEDT Timo, PANG Tsz Ching, and BAL Kiran Jeniffer

***Abstract*—This paper presents a theoretical analysis of harmonically-terminated high-efficiency power rectifiers and experimental validation on a class-C single Schottky-diode rectifier and a class-F^{-1} GaN transistor rectifier. The theory is based on a Fourier analysis of current and voltage waveforms which arise across the rectifying element when different harmonic terminations are presented at its terminals. An analogy to harmonically-terminated power amplifier theory is discussed. From the analysis, one can obtain an optimal value for the DC [?] load given the RF circuit design. An upper limit on rectifier efficiency is derived for each case as a function of the device on-resistance. Measured results from fundamental frequency source-pull measurement of a Schottky diode rectifier with short-circuit terminations at the second and third harmonic are presented. A maximal device rectification efficiency of 72.8% at 2.45 GHz matches the theoretical prediction. A 2.14 GHz GaN pHEMT rectifier is designed based on a class-F^{-1} power amplifier. The gate of the transistor is terminated in an optimal impedance for self-synchronous rectification. Measurements of conversion efficiency and output DC voltage for varying gate RF impedance, DC load and gate bias are shown with varying input RF power at the drain. The rectifier demonstrates an efficiency of 85% for a 10 W input RF power at the transistor drain, with a DC voltage of 30 V across a 98 Ω resistor.**

***Index Terms*—harmonic terminations, high efficiency power amplifiers, load pull, microwave rectifiers, nonlinear analysis, time-domain measurements**

I. Introduction

THE first RF rectifiers were demonstrated in experiments and patents in the 1890's by Nikola Tesla in wireless power transmission for lighting applications and the method of obtaining direct from alternating current [?]. The main application of microwave power rectifiers in the early 1900's was in signal detection where crystals, vacuum tubes or diodes served as the nonlinear element [?], [?]. An excellent discussion of the early history of microwave detectors is provided in [?]. These early microwave rectifiers were aimed at extracting information rather than extracting DC power. The first published application of microwave rectifiers for extraction of DC power was performed in the 1960's using diode-based rectifiers [?], [?], [?], [?].

Renewed interest in free-space power transmission occurred in the early 1970's. An interesting microwave rectifier for production of DC power or low-frequency AC power called the Cyclotron-Wave Rectifier was introduced in [?], [?]. William C. Brown of Raytheon, one of the original researchers in the field, continued publishing diode-based rectifier work and introduced the term "rectenna" for a receiving antenna integrated with a rectifier [?], [?], [?]. Around the same time, power combining for an array of microwave power rectifiers was discussed in [?], in which the authors inadvertently graze the topic of harmonically terminated rectifiers, of which they seem to hint at a class-F rectifier.

A number of diode-based rectifiers have been demonstrated, many integrated with antennas, with a good comparison presented in [?] and in earlier works focusing on low-power rectification [?], [?]. Additional applications where rectifier efficiency is important include microwave power recycling [?], and DC-DC converters with extremely high frequency switching [?], [?]. In many of the reported microwave rectifiers, filtering of the harmonics at both the input and output has been investigated, e.g [?],[?], mainly to reduce re-radiated harmonic power. To date, very few transistor rectifier circuits have been demonstrated, most at frequencies at least three times lower than in this work. A UHF synchronous transistor class-E rectifier at 700 MHz is shown to achieve 85% efficiency with 58 mW of output power in [?], and the same authors discuss a class-E^2 10-W DC-DC converter with a synchrounous transistor rectifier at 780 MHz with 72% efficiency [?]. This design is scaled from 0.5-MHz synchronous rectifier designs demonstrated in [?] and requires an additional synchronized gate RF input signal.

Harmonic terminations are commonly applied to increase efficiency in power amplifiers (PAs). The transistor nonlinearities generate harmonic content at the output, and in a number of high-efficiency amplifier classes, specific harmonic terminations are used to shape the current and voltage waveforms. In reduced conduction angle PAs (classes A, AB, B and C), all harmonics are shorted at the virtual drain reference plane in the transistor. Other PA modes of operation specify open or

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M. Roberg is with TriQuint Semiconductor, 500 West Renner Road Richardson, TX 75080 USA (e-mail: michael.roberg@tqs.com).

T. Reveyrand is with the XLIM Laboratory, UMR 7252, University of Limoges, 87060 Limoges, France (e-mail: tibault.reveyrand@xlim.fr).

I. Ramos and Z. Popovic are with the Department of Electrical, Computer and Energy Engineering, University of Colorado, Boulder, CO, 80309-0425 USA (e-mail: ignacio.ramos@colorado.edu; zoya.popovic@colorado.edu).

E. Falkenstein is with Qualcomm Inc., 6150 Lookout Road Boulder, CO 80301 USA (e-mail: erez.falkenstein@gmail.com).

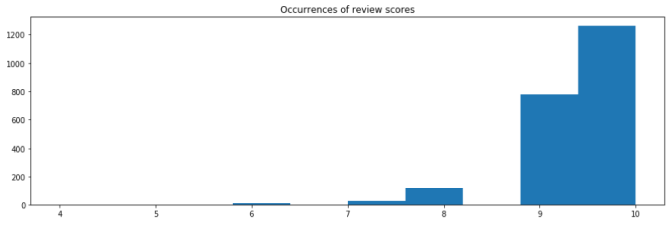

Fig. 1. Microwave rectifier circuit diagram. An ideal blocking capacitor C_b provides DC isolation between the microwave source and rectifying element. An ideal choke inductor L_c isolates the DC load R_{DC} from RF power.

short harmonic terminations for various harmonics [**?**], [**?**], [**?**]. A general analysis for arbitrary complex terminations of harmonics have recently been derived in [**?**], including a sensitivity analysis to harmonic termination impedances. In a rectifier, the nonlinear rectifying element also generates currents and voltages at the harmonics of the input frequency, and although in this case the output is at DC, the efficiency of the rectifier can be modified by terminating the harmonics. In [**?**] the harmonic termination concept for improving rectifier efficiency is applied to a class-C diode rectifier integrated with a dual-polarized patch antenna for a wireless powering application.

In this paper, we identify the similarity between power rectifiers and power amplifiers, showing that many of the efficiency improvement techniques developed for power amplifiers may be practically directly applied to power rectifiers. Particularly, the impact which harmonic terminations have on the rectification efficiency is addressed. A general rectifier analysis approach is presented in Section II, and several classes of microwave power rectifiers are introduced, focusing on class-C and F^{-1} modes, which are experimentally validated in Sections III and IV.

II. Harmonically-Terminated Power Rectifier Analysis

Consider the microwave rectifier shown in Fig. 1. A sinusoidal microwave power source with voltage magnitude V_s and impedance R_s drives the rectifying element having a resistance $R(v)$ defined as

$$R(v) = \begin{cases} \infty, & v > 0 \\ 0, & v \leq 0 \end{cases} \tag{1}$$

where v and i are the instantaneous voltage across and current through the rectifying element, respectively. The rectifying element depicted by $R(v)$ in Fig. 1 can in general be any nonlinear device that acts as a switch, such as a diode or a transistor. When a non-zero on-resistance R_{on} and non-zero threshold voltage V_{tr} are taken into account, the resistance of the rectifying element is given by

$$R(v) = \begin{cases} \infty, & v > -V_{tr} \\ R_{on}, & v \leq -V_{tr} \end{cases} \tag{2}$$

The analysis of different classes of power rectifiers will next be analyzed based on the harmonic terminations presented to the rectifying element, and independent of the physical nonlinear device which performs the rectification.

A. Class-C Rectifier Analysis

In Fig. 1, a sinusoidal microwave power source with voltage magnitude V_s and impedance R_s drives the rectifying element of resistance $R(v)$ above. The DC load seen by the rectifying element is R_{DC} while the load at the fundamental frequency f_0 and successive harmonics is set by the matching network. Assume the matching circuit presents $R_s(f_0)$ to the rectifying element with all subsequent harmonics terminated in short circuits. This is equivalent to the harmonic terminations for a canonical reduced conduction angle power amplifier. This class is useful for Schottky diode rectifiers because these diodes have nonlinear junction capacitance. Short-circuiting the harmonics fixes the harmonic terminations at the intrinsic diode by shorting this junction capacitance.

When the incident RF voltage at the ideal rectifier swings negative, it is clipped at zero given (1). The enforced harmonic terminations force the voltage waveform to contain only a DC and fundamental frequency component. Therefore, a DC component must be produced by the rectifying element such that the voltage waveform maintains its sinusoidal nature. The voltage across the rectifying element can now be expressed as

$$v(\theta) = V_{DC} + V(f_0)\sin(\theta) \tag{3}$$

where $V(f_0)$ is the fundamental frequency component of the voltage across the rectifying element, V_{DC} is the DC component, $V_{DC} = V(f_0)$ and $\theta = 2\pi f_0 t$. The current waveform contains infinite frequency components, and can be written as

$$i(\theta) = 2\pi I_{DC}\delta\left(\theta - \frac{3\pi}{2} - 2n\pi\right), \quad n = 0, 1, ..., \infty \tag{4}$$

where I_{DC} is the DC current and $\delta(\theta)$ is the Dirac delta function. When all available input power P_{in} is delivered to the rectifier, the fundamental frequency component of the current through the rectifying element $I(f_0)$ is

$$I(f_0) = \frac{2P_{in}}{V(f_0)} \tag{5}$$

and, since there is no mechanism by which the rectifier itself can dissipate power ($R_{on} = 0$ at this point), all of the available input power must be dissipated in the DC load and the conversion efficiency is 100%. Therefore,

$$P_{in} = V_{DC}I_{DC} \tag{6}$$

Substituting in (5) and rearranging gives the expression of the current at the fundamental input frequency and the DC rectified current, which is $I(f_0) = 2I_{DC}$. When all available input power is delivered to the rectifier, the RF-DC conversion efficiency is 100% because the rectifying element is ideal and cannot dissipate power itself. In order for all available input power to be delivered to the rectifier, it is straightforward to

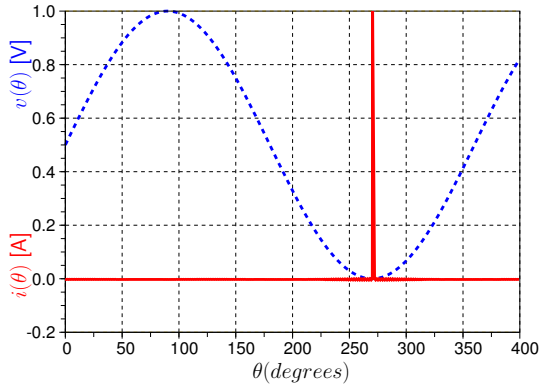

Fig. 2. Ideal normalized voltage (dashed) and current (solid) waveforms for reduced conduction angle half-wave rectifier. The waveforms have been normalized to their peak values.

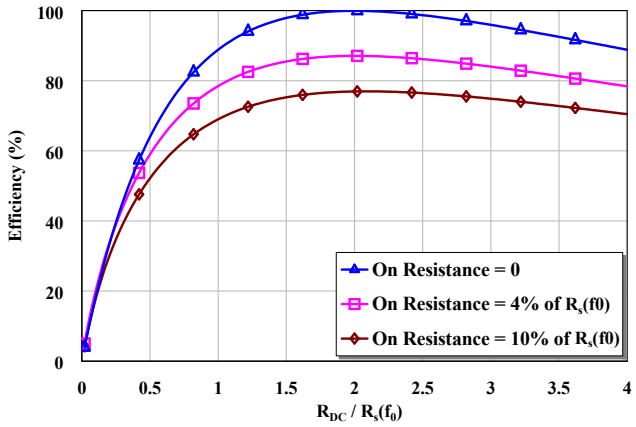

Fig. 3. Simulated efficiency of reduced conduction angle half-wave rectifier versus $R_{DC}/R_s(f_0)$ for varying rectifier on-resistance.

show that the DC load must be set relative to the fundamental frequency load as

$$R_{DC} = 2R_s(f_0) \tag{7}$$

A harmonic balance simulation of an approximately ideal rectifier with short-circuited harmonic terminations was performed in Microwave Office® using the SPICE diode model with no parasitics (PNIV) as the rectifying element. The device temperature was set to 1° K to approximate an ideal switch. The fundamental frequency excitation was set to 1 W at 1 GHz with the first 200 harmonics terminated in short-circuits. The diode was presented with 50 Ω at the fundamental frequency and the DC load was swept from 5 Ω to 200 Ω. The simulated data is then normalized to generalize the simulation results. The ideal time-domain current and voltage waveforms across the diode are shown in Fig. 2 with the RF-DC conversion efficiency as a function of $R_{DC}/R_s(f_0)$ for varying rectifier on-resistance shown in Fig. 3. It is clear that the mechanism of operation in the ideal case agrees with the theory presented above. The reduction in RF-DC conversion efficiency when the DC load is not set according to (7) is due to impedance mismatch, and is given by

$$\eta = 1 - \left(\frac{R_{DC} - 2R_s(f_0)}{R_{DC} + 2R_s(f_0)}\right)^2 \tag{8}$$

B. Class-F^{-1} Rectifier Analysis

Consider again the rectifier circuit shown in Fig. 1 and assume that all even harmonics are terminated in open circuits, while all odd harmonics are terminated in short circuits. This set of harmonic terminations is the same as for a class-F^{-1} amplifier, therefore this rectifier will be referred to as a class-F^{-1} rectifier. The fundamental frequency component of the voltage across the rectifying device is given by

$$V(f_0) = V_s(f_0) \tag{9}$$

During the second half of the RF cycle, it is evident from (1) that the voltage across the rectifying element must be zero. This condition must be met through the addition of DC and only even harmonic voltage components, and therefore the voltage waveform is expressed as

$$v(\theta) = \begin{cases} 2V(f_0)\sin\theta, & 0 \le \theta < \pi \\ 0, & \pi \le \theta < 2\pi \end{cases} \tag{10}$$

A Fourier expansion of (10) expresses the DC component of the voltage waveform as

$$V_{DC} = \frac{2V(f_0)}{\pi} \tag{11}$$

In the first half of the RF cycle, the current through the rectifying element is zero, given (1). This condition is met through the addition of a DC current and odd harmonic current components. With the current direction as in Fig. 1, the DC component of the current must be positive. Therefore, in the first half of the RF cycle, the remaining harmonics must sum to a constant value equivalent to the negative of the DC component. Since the function which is the sum of the remaining harmonics is odd, the second half of the RF cycle must sum to the DC component, and the current is given by

$$i(\theta) = \begin{cases} 0, & 0 \le \theta < \pi \\ 2I_{DC}, & \pi \le \theta < 2\pi \end{cases} \tag{12}$$

The DC component of the current waveform Fourier expansion is found to be

$$I_{DC} = \frac{\pi}{4} I(f_0) \tag{13}$$

The DC load consistent with (10) and (12) is given by

$$R_{DC} = \frac{8V(f_0)}{\pi^2 I(f_0)} = \frac{8}{\pi^2} R(f_0) \tag{14}$$

The conversion efficiency, defined as the ratio of the DC power dissipated in the load resistor to the available fundamental frequency RF power, is evaluated as

$$\eta = \frac{P_{DC}}{P(f_0)} = \frac{2V_{DC}I_{DC}}{V(f_0)I(f_0)} = \frac{2\frac{2}{\pi}V(f_0)\frac{\pi}{4}I(f_0)}{V(f_0)I(f_0)} = 1 \tag{15}$$

Therefore, the ideal half-wave rectifier converts all available RF power to DC power if the the DC loading resistance set to the value given in (14). The RF-DC conversion efficiency as a function of $R_{DC}/R_s(f_0)$ was simulated in Microwave Office® for varying rectifier on-resistance and is shown in Fig. 4. The harmonic balance settings were identical to those used for the class-C rectifier above. The peak efficiency as a function of on-resistance is higher than for the class-C rectifier, although the efficiency degrades more quickly when the non-ideal DC load is applied.

The waveforms including parasitic on-resistance and threshold voltage are next investigated assuming the rectifier impedance from (2). The time domain voltage and current waveforms are approximated as

$$v(\theta) = \begin{cases} V_{max}\sin\theta, & v(\theta) > -V_{tr} \\ -V_{tr} - I_{max}R_{on}, & v(\theta) \le -V_{tr} \end{cases} \tag{16}$$

$$i(\theta) = \begin{cases} 0, & V(\theta) > -V_{tr} \\ I_{max}, & v(\theta) \le -V_{tr} \end{cases} \tag{17}$$

As an example, Fig. 5 shows the current and voltage waveforms for a specific set of non-ideal parameters ($V_{tr} = 0.7\,\text{V}$, $V_{max} = 20\,\text{V}$, $I_{max} = 200\,\text{mA}$, and $R_{on} = 5\,\Omega$). When the device is conducting current, it creates a voltage drop across the on-resistance which is constant due to the constant current. If the on-resistance were zero, the only difference between the waveform in (16) and the ideal voltage waveform would be the minimum value, which would be $-V_{tr}$ rather than zero. The values of θ at which the transition between the conducting and non-conducting regions occurs are found to be

$$\begin{aligned} \theta_{t1} &= 2\pi - \arcsin\left(\tfrac{V_{tr}}{V_{max}}\right) \\ \theta_{t2} &= \pi + \arcsin\left(\tfrac{V_{tr}}{V_{max}}\right) \end{aligned} \tag{18}$$

The DC and fundamental frequency values of the voltage and current waveforms can be found through a Fourier analysis using the transition points in (18). The first Fourier coefficient of $v(t)$ gives the DC component of the voltage, which can be derived as

$$\begin{aligned} V_{DC} = \frac{1}{2\pi}\Bigg(&2V_{max}\sqrt{1-\left(\frac{V_{tr}}{V_{max}}\right)^2} \\ &- (V_{tr} + I_{max}R_{on})\left[\pi - 2\arcsin\left(\frac{V_{tr}}{V_{max}}\right)\right]\Bigg) \end{aligned} \tag{19}$$

The fundamental frequency voltage is found from $V(f_0) = a_v + jb_v$, where

$$a_v = \frac{1}{\pi}\int_0^{2\pi} v(\theta)\cos\theta d\theta = 0 \tag{20}$$

and b_v can be reduced to

$$\begin{aligned} b_v = \frac{1}{\pi}\Bigg(&V_{max}\arcsin\left(\frac{V_{tr}}{V_{max}}\right) + \frac{\pi V_{max}}{2} \\ &+ (V_{tr} + 2I_{max}R_{on})\sqrt{1-\left(\frac{V_{tr}}{V_{max}}\right)^2}\Bigg) \end{aligned} \tag{21}$$

Similarly, the DC component of the current waveform is found to be

$$I_{DC} = \frac{I_{max}}{2\pi}\left(\pi - 2\arcsin\left(\frac{V_{tr}}{V_{max}}\right)\right) \tag{22}$$

The fundamental frequency current $i(t) = a_i + jb_i$ has $a_i = 0$ and the coefficient b_i can be shown to be equal to

$$b_i = -\frac{2I_{max}}{\pi}\sqrt{1-\left(\frac{V_{tr}}{V_{max}}\right)^2} \tag{23}$$

The input power at the fundamental frequency is found from

$$P_{in} = \Re\left\{\frac{V(f_0)I^*(f_0)}{2}\right\} \tag{24}$$

Substituting (21) and (23) into the above results in

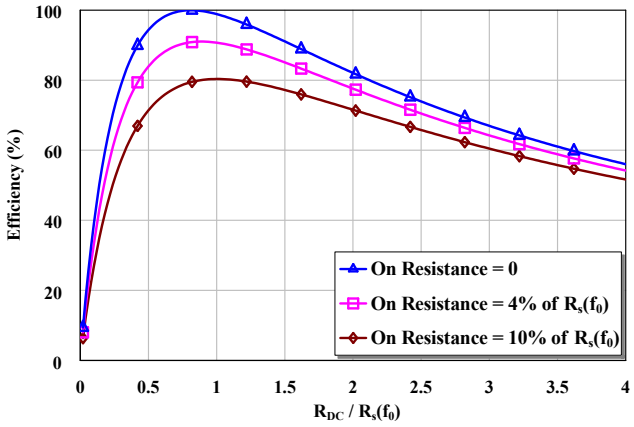

Fig. 4. Simulated efficiency of class-F^{-1} rectifier versus $R_{DC}/R_s(f_0)$ for varying rectifier on-resistance.

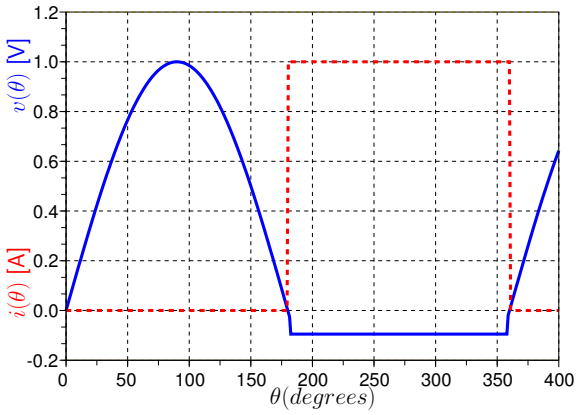

Fig. 5. Non-ideal class-F^{-1} voltage (solid) and current (dashed) waveforms, normalized to their peak respective values.

$$P_{in} = \frac{kI_{max}}{\pi^2}\left(V_{max}\arcsin\left(\frac{V_{tr}}{V_{max}}\right) + \frac{\pi V_{max}}{2} + (V_{tr} + 2I_{max}R_{on})\,k\right) \tag{25}$$

where k is defined as

$$k = \sqrt{1 - \left(\frac{V_{tr}}{V_{max}}\right)^2} \tag{26}$$

Solving for I_{max} as a function of P_{in} when R_{on} is non-zero after some arithmetic results in two solutions, one of which is negative. The positive solution for the maximal current is

$$I_{max} = \frac{\sqrt{\alpha^2 + 8\pi^2 P_{in} R_{on}} - \alpha}{4R_{on}k} \tag{27}$$

with $\alpha = V_{max}\left(\arcsin\left(\frac{V_{tr}}{V_{max}}\right) + \frac{\pi}{2} + k\frac{V_{tr}}{V_{max}}\right)$.

In the case where R_{on} is zero, (27) simplifies to

$$I_{max} = P_{in}\frac{\pi^2}{kV_{max}\left(\arcsin\left(\frac{V_{tr}}{V_{max}}\right) + \frac{\pi}{2} + k\frac{V_{tr}}{V_{max}}\right)} \tag{28}$$

Note that in the case of an ideal rectifying element, $k = 1$ and $V_{tr} = 0$, therefore

$$I_{max,ideal} = \frac{2\pi P_{in}}{V_{max}} \tag{29}$$

Now that I_{max} is fully expressed given known rectifier parameters, V_{DC} and I_{DC}, $V(f_0)$ and $I(f_0)$ may be calculated, and from this, the DC load and the load at fundamental frequency determined from the following expressions:

$$R_{DC} = \frac{V_{DC}}{I_{DC}} \tag{30}$$

$$R(f_0) = -\frac{V(f_0)}{I(f_0)} = -\frac{b_v}{b_i} \tag{31}$$

The negative impedance in (31) indicates that power is delivered to the rectifying element and gives the impedance of the source delivering power to the rectifying element. The rectifier efficiency is given by

$$\eta = \frac{P_{DC}}{P_{in}} = \frac{V_{DC}I_{DC}}{P_{in}} \tag{32}$$

C. Design example based on class-F^{-1} theory

To understand the usefulness of the presented theory, assume the rectifying element has the following parameters: $V_{max} = 10\,\text{V}$, $R_{on} = 5\,\Omega$, $V_{tr} = 0.7\,\text{V}$ and $P(f_0) = 1\,\text{W}$. First, (27) is used to calculate $I_{max} = 456.7\,\text{mA}$. Next, the DC voltage and current are evaluated using (19) and (22), respectively, to give $V_{DC} = 1.75\,\text{V}$ and $I_{DC} = 218.2\,\text{mA}$. The fundamental frequency voltage and current Fourier coefficients are then calculated to be $V(f_0) = 6.896\,\text{V}$ and $I(f_0) = -290\,\text{mA}$, respectively. The DC and fundamental frequency resistances are then calculated using (30) and (31) to be $R_{DC} = 8.02\,\Omega$ and $R(f_0) = 23.77\,\Omega$, respectively. The efficiency is then calculated using (32) to be $\eta = 38.18\,\%$. If the input power is selected as 0.1 W rather than 1 W, the resultant efficiency is 72.43 % instead. A specific rectification device will always have an approximate input drive level at which it can be most efficient, just as with power transistors in power amplifiers. To maximize efficiency, the goal is always to minimize the amount of power dissipation in the on-resistance of the rectifying element and maximize the power dissipated in the DC load resistor.

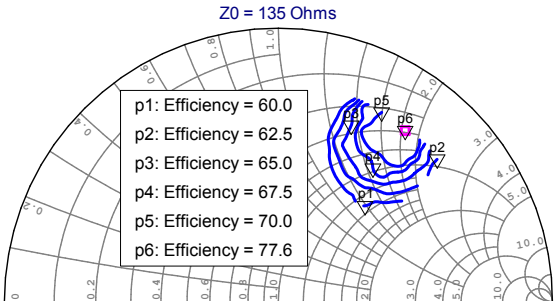

Fig. 6. Source-pull contours with available input power to the diode set to 6 dBm. The impedance is referenced to the junction capacitance of the diode, therefore the lead inductance of the package has been compensated for. Setting R_{DC} to 1080 Ω was found to result in the optimal efficiency for this input power. The highest efficiency of 77.6% is obtained at $Z_{p6} = (68 + j245)\Omega$ with V_{DC}=1.82 V.

III. Schottky-Diode Class-C Rectifier

The Skyworks SMS7630 Schottky diode in the SC-79 package was selected for the half-wave rectifier. Source-pull was performed at 2.45 GHz with 0-10 dBm available input power for various DC loads in order to identify the combination of input power, fundamental load and DC load resulting in highest efficiency. The best case occurred at 6 dBm input power, with the source-pull contours being shown in Fig. 6. The on-resistance of the SMS7630 is 20 Ω with the optimal DC load of 1080 Ω. Therefore R_{on} is approximately 2% of R_{DC}, which in theory is 4% of $R_s(f_0)$. From Fig. 3, a peak efficiency of 87% occurs with infinite harmonic terminations, therefore the achieved 77.6% is very reasonable considering only the 2nd and 3rd harmonics were explicitly terminated.

Measurements of a rectifier designed using the source-pull data show a maximum RF-DC conversion efficiency of 72.8% when matched to 50Ω, obtained after the 0.6 dB matching network loss is de-embedded. The fabricated rectifier and DC load sweep measurements are shown in Fig. 7. Open circuit shunt stubs are used to present short-circuit terminations at the second and third harmonic. A shunt capacitor is used for presenting the fundamental frequency impedance to reduce size and allow tunability. The reduction in efficiency relative to the source-pull measurements is due to the matching circuit not presenting the ideal impedance found during source-pull.

The class-C rectifier can be applied to improving the efficiency of a wireless powering reception device as demonstrated in [**?**] with a dual-linearly polarized patch rectenna, with a rectifier circuit for each polarization. In this circuit, the

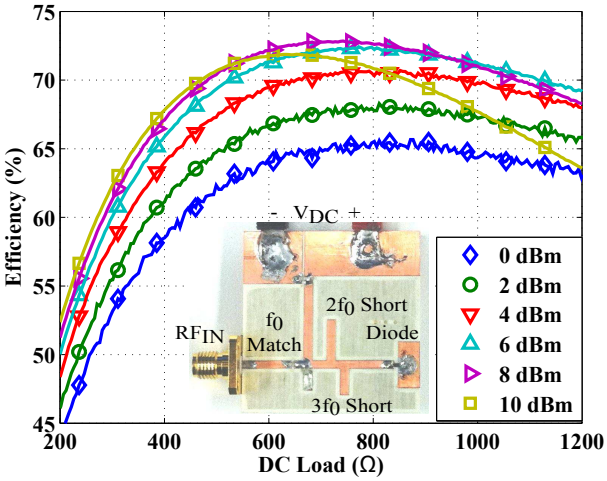

Fig. 7. RF-DC conversion efficiency versus DC load for fixed available input powers with 0.6 dB matching network loss de-embedded. The maximum efficiency of 72.8% occurred at 8 dBm with R_{DC} = 742 Ω and V_{DC}=1.91 V, which is lower than the 1080 Ω found during source-pull. However, the efficiency at 1080 Ω is 69.9% which is very close to the peak value.

first 5 harmonics are shorted and the impedances are validated by calibrated measurements and are presented in [?].

IV. Transistor Class-F^{-1} Rectifier

To prove experimentally the duality between harmonically terminated PAs and rectifiers, a high-efficiency class-F^{-1} PA was designed, measured first as an amplifier, and then as a rectifier. In the rectifier measurements, RF power is input into the drain which is unbiased. The gate is terminated in a variable impedance and biased close to pinch-off. Measurements of efficiency and DC voltage are performed in time domain as a function of input RF power, gate RF load, gate bias and drain DC load.

A. Circuit design

A 2.14-GHz power amplifier, pictured on Fig. 8, is designed using the Triquint TGF2023-02 GaN pHEMT [?]. Class F^{-1} harmonic terminations are implemented at the second and third harmonic. The performance of the PA, illustrated in Fig. 9, was characterized at 2.14 GHz with a drain voltage bias of 28 V and a bias current of 160 mA. The PA exhibits a PAE of 84% with an output power of 37.6 dBm and a gain of 15.7 dB under 3 dB compression. The same PA design was used for rectifier measurements as shown in Fig. 10. The PA is connected to an input RF source at the drain, with the drain supply disconnected. The gate terminal is biased, and connected to an impedance tuner, converting the two-port transistor PA to a one-port rectifier, corresponding to the generalized schematic of Fig. 1.

B. Measurement setup

The class-F^{-1} power amplifier described above is fully characterized in large signal in a rectifier configuration with the setup shown in Fig. 10. The commercial time-domain large

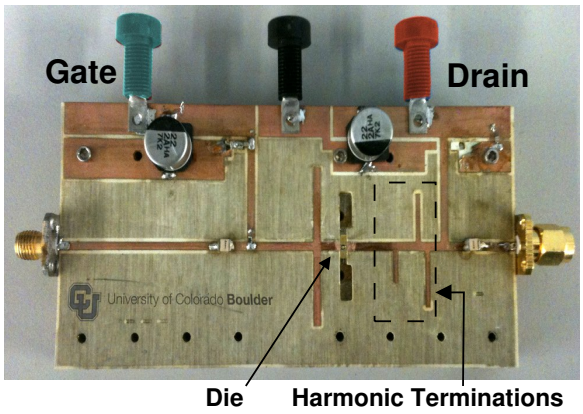

Fig. 8. Photograph of the class-F^{-1} power amplifier, working at 2.14 GHz and presented in [?].

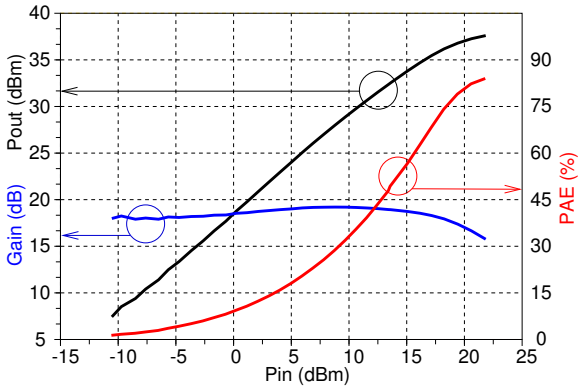

Fig. 9. Large-signal measurements performed on the class-F^{-1} power amplifier at $f_0 = 2.14$ GHz, $V_{GS} = -3.8$ V and $V_{DS} = 28$ V

signal measurement instrument is a VTD SWAP four-channel receiver [?]. In order to acquire time domain waveforms at the reference plane, an 8 error term model calibration similar to the one performed for LSNA (Large Signal Network Analyzer) measurements is applied. After an absolute VNA-like calibration [?], the RF voltage and current waveforms at the input (V1 and I1) and at the output (V2 and I2) of the DUT are measured at the coaxial reference plane. In this case, the RF input is the drain port of the PA, while the RF output is connected to the gate port. Thus, performing a load pull on this device consists of varying the load at f_0 at the RF gate port of the PA with a passive tuner. This kind of measurement is similar to large signal characterization of switch devices recently reported in [?], [?]. The gate DC path is connected to a power supply so the gate bias can be varied. The drain DC bias is the output of the rectifier and is connected to a variable resistance R_{DC}, and the DC voltage across it is measured with a voltmeter. The DC current is then found from the value of R_{DC} from (30). During the measurement, several parameters are varied systematically: the RF load impedance applied at the PA gate port $Z_g(f_0) = V_g(f_0)/I_g(f_0)$; the resistor in the DC drain output R_{DC}; and the gate bias voltage V_{GS}. The conversion efficiency of the rectifier and the DC power delivered at the drain output of the rectifier $P_{DC} = V_{DC} \cdot I_{DC}$ are measured as these parameters are varied, and as a function

of input power at the drain port $P_{in}(f_0)$.

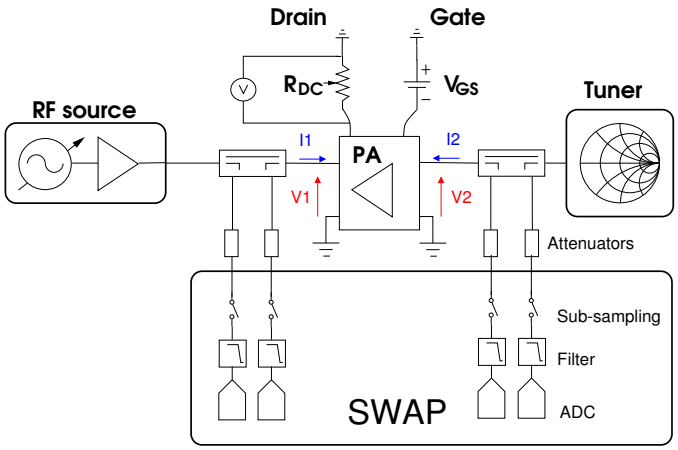

Fig. 10. Time-domain non-linear rectifier measurement block diagram. The SWAP [**?**] performs sampling of current and voltage and the calibration refers the sampled quantities to the reference planes at the DUT. The drain output DC resistance R_{DC} , the gate bias V_{GS} and the gate RF impedance Z_g are varied as the input power at the drain is swept from 10 to 42 dBm.

C. Self-synchronous transistor rectifier results

The measurements of the rectifier are performed in self-synchronous mode, i.e. there is no input RF power incident externally into the gate port of the PA, unlike in previous transistor rectifier work [**?**], [**?**]. The following parameters are varied in order, while keeping the other parameters constant and sweeping the input RF power at the drain port, and the results are described in the same order:

1) RF impedance at the gate, Z_g;
2) load resistance at drain bias output, R_{DC};
3) gate DC bias, V_{GS}.

The gate load-pull was performed to determine the optimum impedance for maximum efficiency with a constant resistive DC load of 98.5 Ω (nominally 100 Ω) and a constant transistor gate bias in pinch-off of -4.4 V. The RF signal is coupled from the drain to the gate matching network through the feedback capacitance C_{gd}, and thus the precise impedance presented at the gate of the transistor is imperative to achieving high efficiency. Fig. 11 shows the time-domain voltage and current waveforms measured at the drain and gate RF port of the amplifier when the RF input power at the drain port is swept from 11 dBm to 42 dBm. These values are chosen because the rectifier in PA operation gives up to 42 dBm output power. The feedback signal present at the gate allows for the rectifier to operate in self-synchronous mode without any additional control signal. Unlike in the synchronously driven case where an external generator is connected to the gate, here the impedance presented at the gate is always passive (inside the Smith chart), keeping the device in a safe operating mode.

Measured RF-DC conversion efficiency is shown in Fig. 12 for four different RF gate impedances. A maximal conversion efficiency of 85% is achieved with a DC output voltage of 36 V and an input power at the drain of 42 dBm with $R_{DC} = 98.5\,\Omega$. This peak efficiency is for a RF gate load of

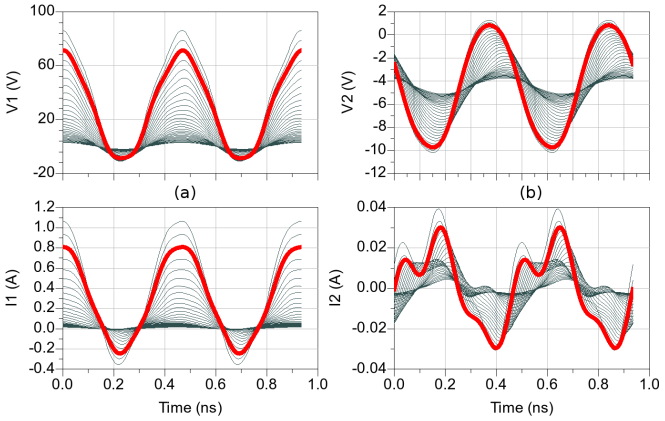

Fig. 11. Time-domain waveforms measured at drain (a) and gate (b) of the rectifier with $V_{GS} = -4.4$ V, $R_{DC} = 98.5\,\Omega$ and $Z_g(f_0) = (230 + j10)\,\Omega$. The RF input power at the drain is swept from 10 to 42 dBm, corresponding to the range of output power of the class-F^{-1} PA.

around 230 Ω (green hexagon in the Smith chart in Fig. 12), which is the highest impedance that was achievable with the specific tuner in the setup. For the low gate impedance (red triangle in the Smith chart), the efficiency is significantly lower. By observing the gate current (Fig. 12d), it can be seen that for a low RF gate impedance, the gate diode turns on at around $P_{in} = 25$ dBm. Since the input power cannot be increased much beyond this point to avoid breakdown, this limits the DC voltage at the output to around 4 V. For the gate impedance with highest efficiency (green line with hexagon symbol), the gate diode is off for input drain powers below 41 dBm, allowing for high DC voltage output.

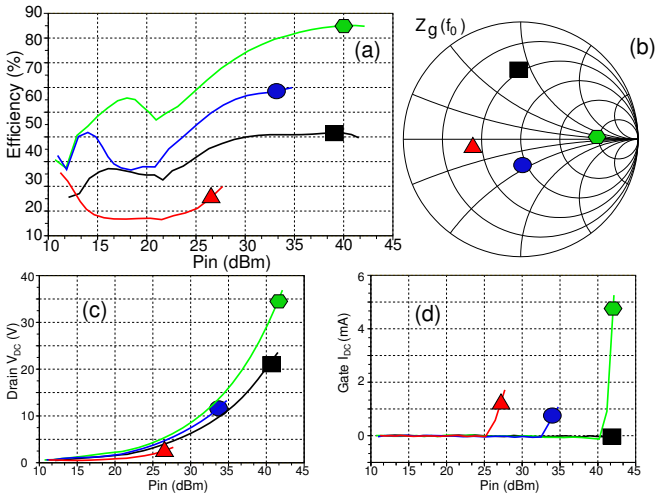

Fig. 12. Conversion efficiency, gate DC current and drain DC voltage versus input power for several RF load impedance values presented at the gate. $V_{GS} = -4.4$ V and $R_{DC} = 98.5\,\Omega$. The green point on the Smith chart corresponds to the highest efficiency point at $Z_g(f_0) = (230 + j10)\,\Omega$.

After the optimal gate impedance for highest efficiency was obtained, a power sweep for three different R_{DC} values in the drain output was obtained. From Fig. 13, a maximal efficiency of 85% was measured for a DC resistive load of 98 Ω while an efficiency drop of 13% was observed for a DC load of 21 Ω with 40 dBm input power. As expected, the DC output voltage

decreases from a maximum 30 V for $R_{DC} = 98\,\Omega$ at 40 dBm input power, to a maximum of 13.4 V for $R_{DC} = 21\,\Omega$ with the same input power. It is interesting to see how the input impedance of the rectifier at the RF drain port approaches 50 Ω as the input power increases, Fig. 14. This is expected, since the PA was designed for maximal saturated power delivered into a 50 Ω load. This again points to the similarities between the same circuit operated as a power rectifier and a power amplifier.

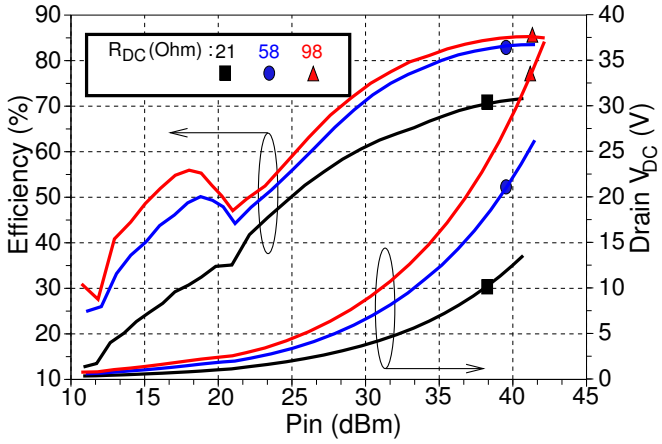

Fig. 13. Conversion efficiency and drain DC output voltage versus input power for several DC drain resistor values. $V_{GS} = -4.4V$ and $Z_g(f_0) = (230 + j10)\,\Omega$. The highest efficiency of 85% is obtained at P_{in}=40 dBm with a V_{DC}=30 V.

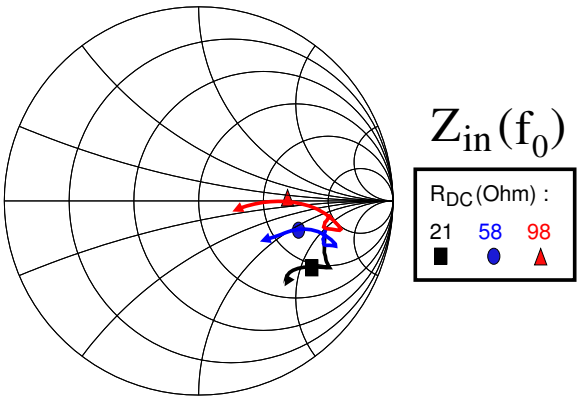

Fig. 14. RF impedance at f_0 measured at the input (drain port) versus input power for several DC drain resistor values. $V_{GS} = -4.4V$ and $Z_g(f_0) = (230 + j10)\,\Omega$.

Finally, the effect of the gate bias V_{GS} on the rectifier efficiency, output voltage and input impedance was investigated. The gate impedance in this case was set for highest efficiency (230 Ω), and a DC load of 58 Ω was selected in order to protect the transistor from high drain voltages that occur for the 98 Ω load that corresponds to the highest efficiency. The measurements were performed for six different values of gate bias V_{GS} as shown in Fig. 15. With $R_{DC} = 58\Omega$, a maximum efficiency of 83% was obtained with the transistor biased deeply into the pinch-off region with $V_{GS} = -4.4$ V, and a drop of only 3% was measured for $V_{GS} = -3.5$ V. Furthermore, the gate bias has a minimal impact on the output DC voltage or on the drain impedance.

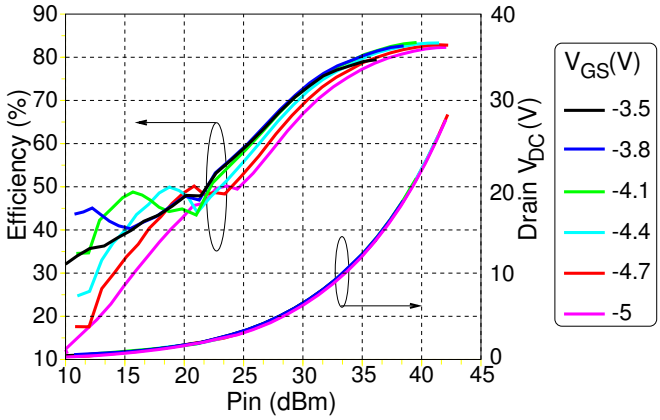

Fig. 15. Measured conversion efficiency and drain DC voltage versus input power for several DC gate voltage biases. For this data, $R_{DC} = 58\Omega$ and $Z_g(f_0) = (230 + j10)\,\Omega$.

V. Conclusion

In summary, this paper addresses high-efficiency power rectifiers designed with harmonic terminations at the RF input, in analogy to high-efficiency power amplifier design with harmonic terminations at the output. The applications of such power rectifiers include wireless power beaming [**?**], recycling power in high-power circuits [**?**] and ultra-fast switching integrated DC-DC converters with no magnetics [**?**].

The theory for an ideal rectification element is based on Fourier analysis and establishes the basic design parameters such as the relationship between output DC resistance and impedance at the fundamental frequency at the rectifier input which optimizes efficiency. The analysis also predicts the time-domain waveforms at the terminals of the rectification element and the efficiency as a function of on-resistance and DC output resistance. Specific results are derived for class-C and class-F^{-1} classes of operation, as they are defined for power amplifiers. These two cases are chosen for experimental validation with a 2.45 GHz diode and 2.14 GHz transistor rectifier, respectively. It is straightforward to repeat the derivation for other classes of operation, such as class-F as shown in detail in [**?**].

The experimental results show that good agreement can be reached between theory and experiment with a Schottky-diode single-ended rectifier with finite class-C harmonic terminations, resulting in 72.8% efficiency for input power levels in the mW range, intended for wireless power harvesting detailed in [**?**], [**?**]. A GaN pHEMT class-F^{-1} power rectifier achieved 85% efficiency with 40 dBm input power across 98-Ω DC load with a DC output voltage $V_{DC} = 30V$. The efficiency and output voltage of the self-synchronous rectifier are shown to depend on the input power at the drain, the impedance at the gate port and the DC load at the output drain bias line, but not on the gate bias.

Time-domain large-signal measurements of a class-F^{-1} power amplifier configured as a rectifier show that one can

accomplish the same rectifier efficiency as the amplifier drain efficiency in self-synchronous mode without external gate RF drive. This is somewhat surprising, and to the best of our knowledge, the first time this type of high-efficiency rectifier has been demonstrated.

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REFERENCES

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