TDTS07 Lab 3 Report

Mario Impesi and Moritz Fröhlich

March 9, 2023

1 Assignment 1: Design-Space Exploration for Energy Minimization

Our measurements for the configurations we tried are shown in Table 1. All of the configurations shown had execution times less than 20ms, which is why we omitted them from the results.

Configuration	Simulator flags	Energy Consumption
Baseline	-	45038855.45 pJ
Direct mapped data cache	`--dt=1`	44921338.52 pJ
2-way data cache	`--dt=2`	44891218.91 pJ
2-way instruction cache	`--it=2`	44299954.06 pJ
4-way instruction cache	`--it=4`	45786569.07 pJ
2-way both caches	`--dt=2 --it=2`	44152317.52 pJ
Halved frequency	`-F 1,2`	53037481.87 pJ
Data cache size 2^{12}	`--ds=12`	44759670.08 pJ
Data cache size 2^{11}	`--ds=11`	44759670.08 pJ
Instruction cache size 2^{12}	`--is=12`	36239529.12 pJ
Instruction cache size 2^{9}	`--is=9`	30075535.76 pJ
Best combined	`--td=2 --ds=11 --it=2 --is=9`	30456137.67 pJ

Table 1: Energy consumption measurements GSM codec

We started by taking a baseline with with the default configuration and then varied the cache associativity for the data cache and the instruction cache. We observed, that we can only make small improvements by varying the associativity of the caches and achieved the best result when using 2-way associativity for both caches together (`--dt=2 --it=2`). However, this improvement was only $1-(44152317.52/45038855.45) \approx 2\%$.

We then tried reducing the frequency by settings the divider to 2 (`-F 1,2`), but saw that this greatly increases the energy consumption.

We saw the biggest improvements when varying the size of the instruction cache and achieved the best result with a instruction cache size of 2^9 (`is=9`). By changing only the cache size, we made a $1 - (30075535.76/45038855.45) \approx 33\%$ improvement.

Finally, we tried the combination of the configurations for the cache associativity and cache size that had the best results when configured individually (`--td=2 --ds=11 --it=2 --is=9`). This configuration produced slightly worse results than just varying the size of the instruction cache at an improvement of roughly $1 - (30456137.67/45038855.45) \approx 32\%$.

The fact that the instruction cache size can be reduced significantly to reduce the energy consumption of the processor suggests that either many of the instructions stored in the instruction cache will not be executed or that there are less instructions during the execution of the program, than the instruction cache has size for.

2 Assignment 2: Shared Memory vs. Distributed Message Passing

We ran the two versions and compared the data we think is useful. The following table contains what we collected.

	Shared Memory	Distributed Message Passing
Runtime	$14123450ns$	$9979355ns$
Bus Utilization	44.89% of 2061534	56.25% of 1320905
Energy Consumption	$894585224.39pJ$	$605463650.53pJ$
Shared Reads	21050	8636
Read Waits	55134	23852
Shared Writes	6693	3876

Table 2: Baseline data

The first thing that we noticed is that the runtime is lower in the Distributed Message Passing version, which appears to be the better solution to this problem. The bus utilization is relatively higher, but the absolute amount is actually lower in the message passing version. We also notice a significant reduction in energy consumption.

Reading and Writing To explain these results, we can look at the number of reads and writes on the shared memory, and how often the processes have had to wait to do so. In the Distributed Message Passing there is a substantial reduction in all three of these values. This is of course because with such a solution, a significant part of these operations can be executed on private scratchpads.

2.1 Frequency Selection

We then tried to change the system frequency and study the effects. We first tried changing the frequency statically, and then dynamically. The following data is relative to a system using the Shared Memory solution (f is the base frequency).

	Static $f/2$	Static $f/3$	Static $f/4$	Dynamic
Runtime	$23629245ns$	$35026190ns$	$46163825ns$	$14263300ns$
Bus Utilization	49.73% of 3559297	51.75% of 5290974	52.18% of 6983711	38.79% of 1979570
Energy Consumption	$760393653.32pJ$	$860879245.15pJ$	$952301480.04pJ$	$927342748.29pJ$

Table 3: Frequency selection data

Changing the frequency statically does not seem to provide any particular benefit to the system. On the other hand, changing the frequency dynamically improves all three parameters we are interested in.

3 Assignment 3: Mapping/Scheduling Exercise

Without changing the process mapping, we can reduce the schedule length from 45 to 35, with the following schedule:

t	Proc 1	Proc 2
0-5	-	T1
5	T3	-
10	T3	-
15	T2	T5
20	T2	T5
25	T4	T5
30-35	-	T5

Table 4: Schedule without changing mapping

Changing the mapping, we can move `T3` to `Processor 2`. This produces a schedule with the same length as the previous one.

t	Proc 1	Proc 2
0-5	T2	T1
5	T2	T3
10	T4	T3
15	-	T5
20	-	T5
25	-	T5
30-35	-	T5

Table 5: Caption