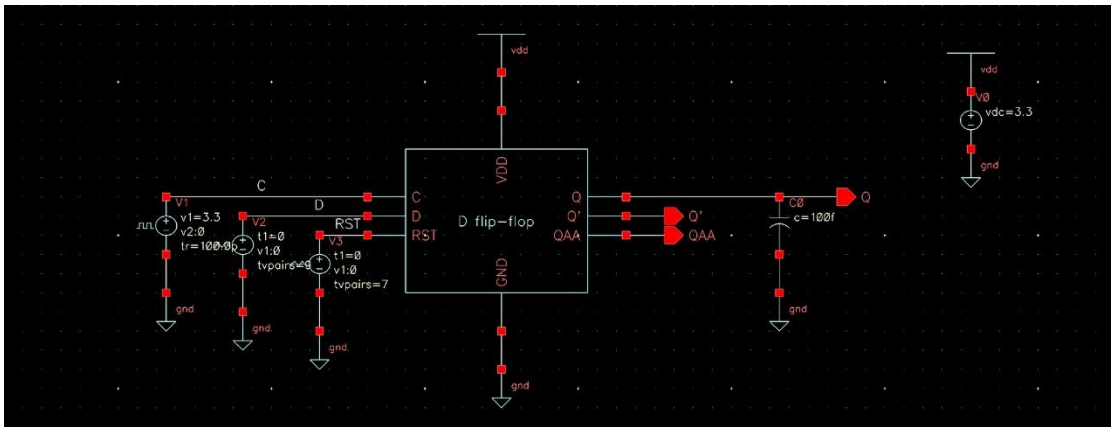
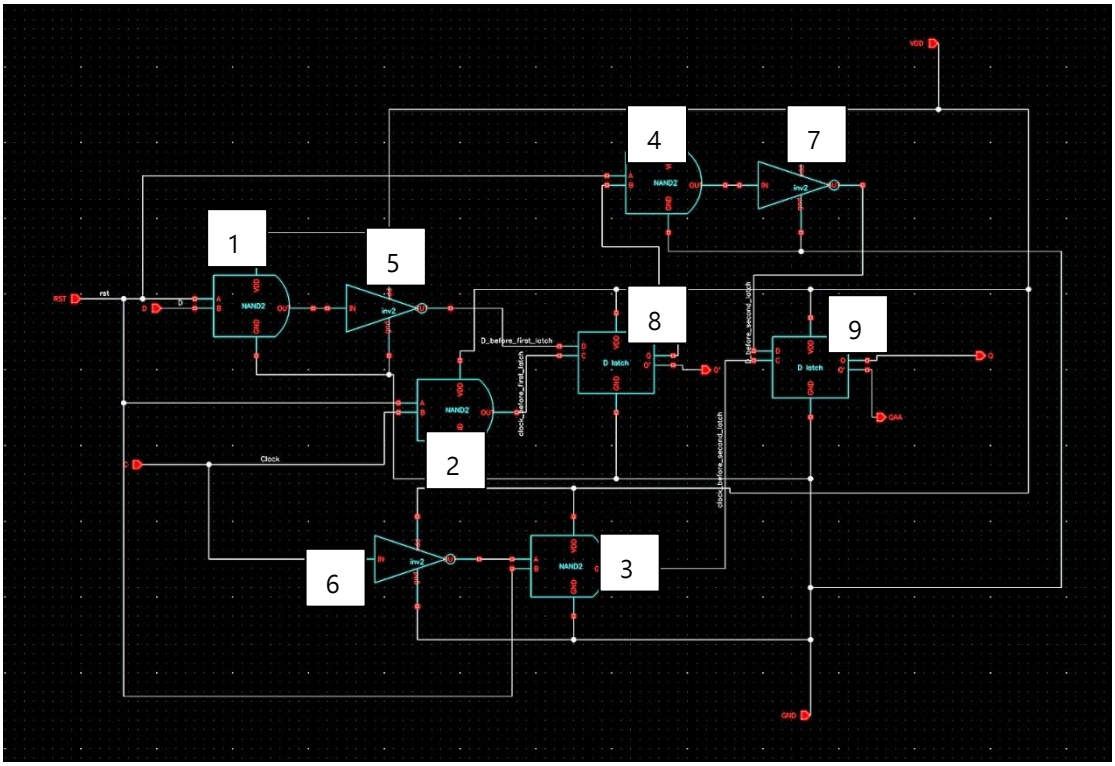
1.schematic of DFF

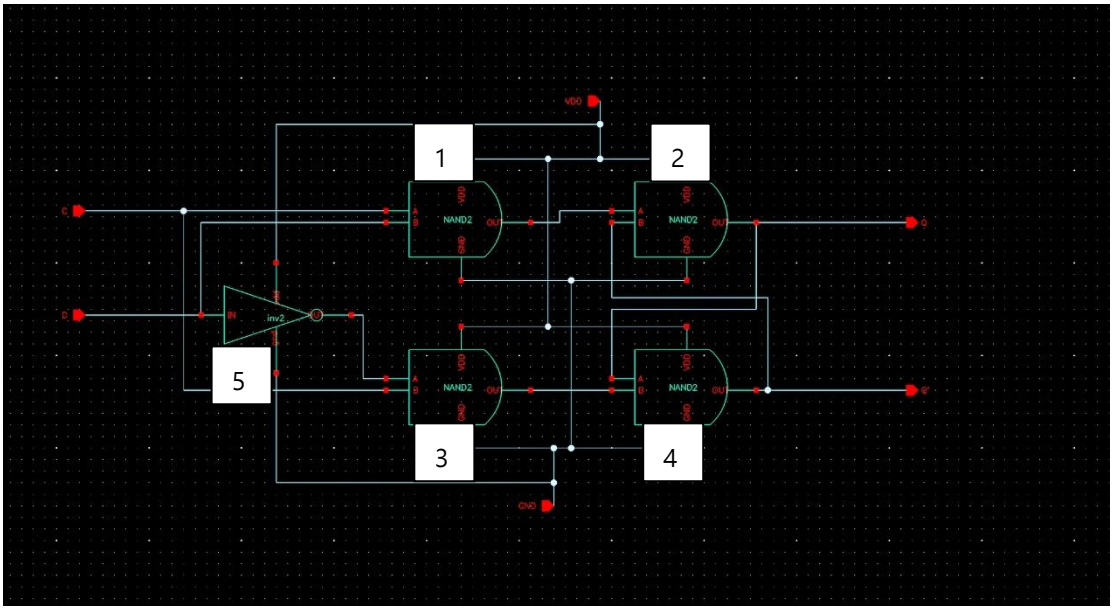
top level



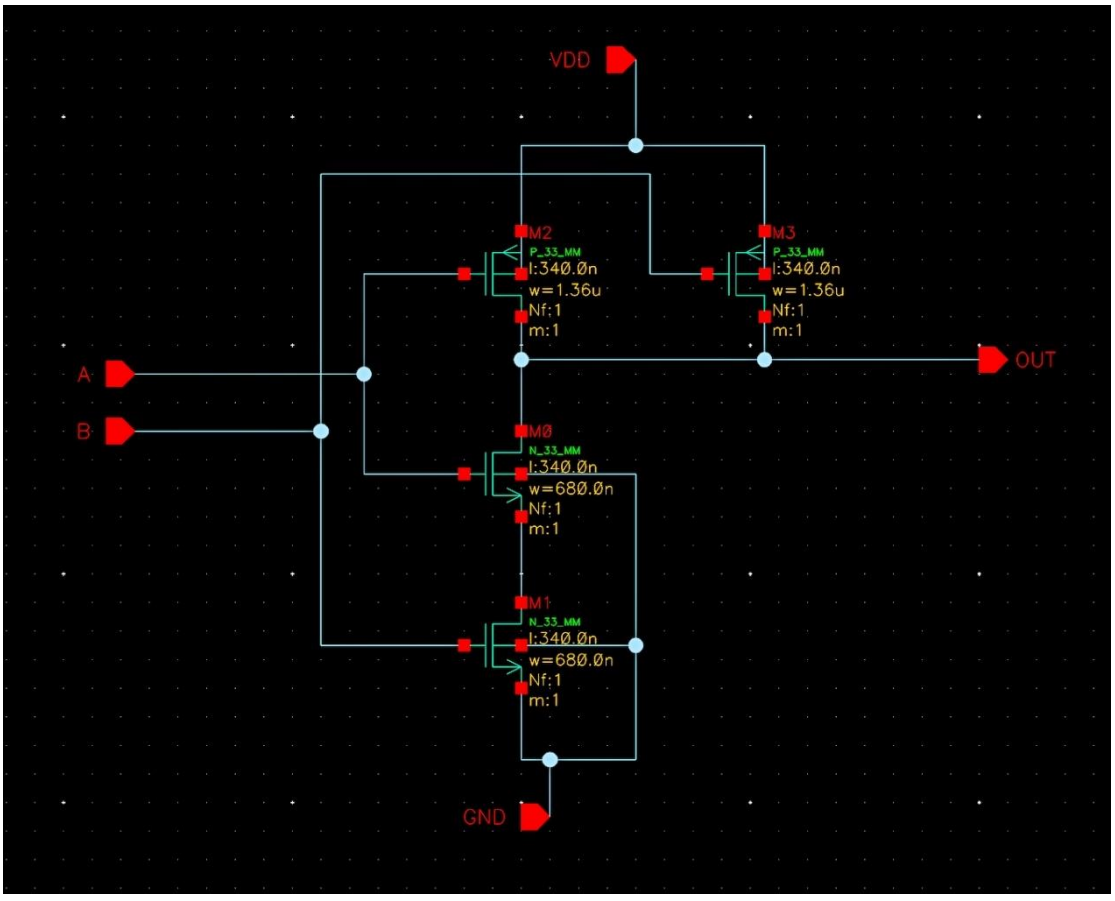
inside d flipflop(編號是為了等一下的列表(number



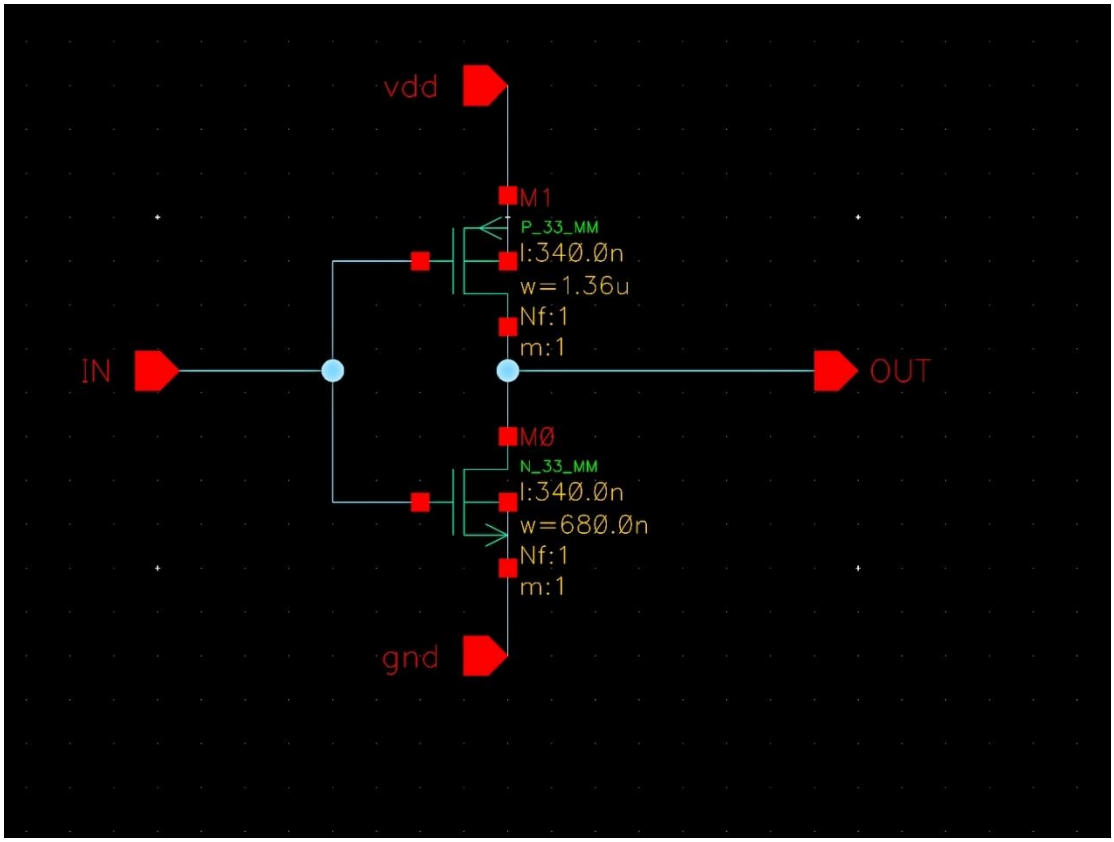
inside D latch(編號是為了等一下的列表(subnumber



inside nand



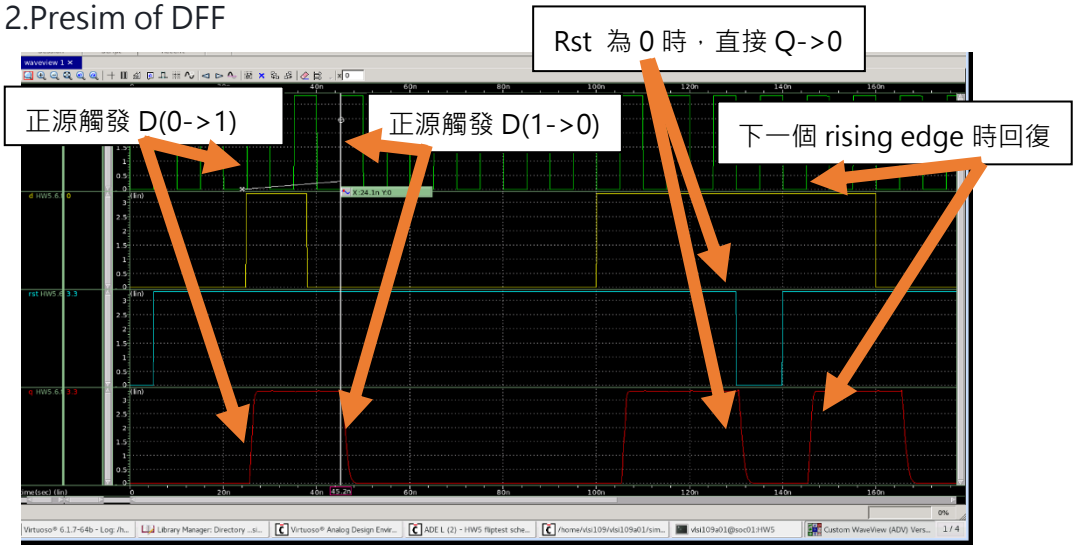
inside inv



number	subnumber				
1		M0	n_33_mm	w=680e-9	l=340e-9
		M1	n_33_mm	w=680e-9	l=340e-9
		M2	p_33_mm	w=1.36e-6	l=340e-9
		M3	p_33_mm	w=1.36e-6	l=340e-9
2		M0	n_33_mm	w=680e-9	l=340e-9
		M1	n_33_mm	w=680e-9	l=340e-9
		M2	p_33_mm	w=1.36e-6	l=340e-9
		M3	p_33_mm	w=1.36e-6	l=340e-9
3		M0	n_33_mm	w=680e-9	l=340e-9
		M1	n_33_mm	w=680e-9	l=340e-9
		M2	p_33_mm	w=1.36e-6	l=340e-9
		M3	p_33_mm	w=1.36e-6	l=340e-9
4		M0	n_33_mm	w=680e-9	l=340e-9
		M1	n_33_mm	w=680e-9	l=340e-9
		M2	p_33_mm	w=1.36e-6	l=340e-9
		M3	p_33_mm	w=1.36e-6	l=340e-9
5		M0	n_33_mm	w=680e-9	l=340e-9
		M1	p_33_mm	w=1.36e-6	l=340e-9

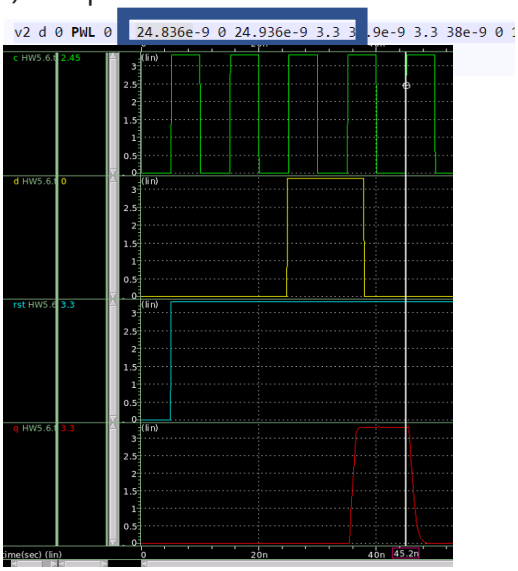
6		M0	n_33_mm	w=680e-9	l=340e-9
		M1	p_33_mm	w=1.36e-6	l=340e-9
7		M0	n_33_mm	w=680e-9	l=340e-9
		M1	p_33_mm	w=1.36e-6	l=340e-9
8	1	M0	n_33_mm	w=680e-9	l=340e-9
		M1	n_33_mm	w=680e-9	l=340e-9
		M2	p_33_mm	w=1.36e-6	l=340e-9
		M3	p_33_mm	w=1.36e-6	l=340e-9
	2	M0	n_33_mm	w=680e-9	l=340e-9
		M1	n_33_mm	w=680e-9	l=340e-9
		M2	p_33_mm	w=1.36e-6	l=340e-9
		M3	p_33_mm	w=1.36e-6	l=340e-9
	3	M0	n_33_mm	w=680e-9	l=340e-9
		M1	n_33_mm	w=680e-9	l=340e-9
		M2	p_33_mm	w=1.36e-6	l=340e-9
		M3	p_33_mm	w=1.36e-6	l=340e-9
	4	M0	n_33_mm	w=680e-9	l=340e-9
		M1	n_33_mm	w=680e-9	l=340e-9
		M2	p_33_mm	w=1.36e-6	l=340e-9
		M3	p_33_mm	w=1.36e-6	l=340e-9
	5	M0	n_33_mm	w=340e-9	l=340e-9
		M1	p_33_mm	w=680e-9	l=340e-9
9	1	M0	n_33_mm	w=680e-9	l=340e-9
		M1	n_33_mm	w=680e-9	l=340e-9
		M2	p_33_mm	w=1.36e-6	l=340e-9
		M3	p_33_mm	w=1.36e-6	l=340e-9
	2	M0	n_33_mm	w=680e-9	l=340e-9
		M1	n_33_mm	w=680e-9	l=340e-9
		M2	p_33_mm	w=1.36e-6	l=340e-9
		M3	p_33_mm	w=1.36e-6	l=340e-9
	3	M0	n_33_mm	w=680e-9	l=340e-9
		M1	n_33_mm	w=680e-9	l=340e-9
		M2	p_33_mm	w=1.36e-6	l=340e-9
		M3	p_33_mm	w=1.36e-6	l=340e-9
	4	M0	n_33_mm	w=680e-9	l=340e-9
		M1	n_33_mm	w=680e-9	l=340e-9
		M2	p_33_mm	w=1.36e-6	l=340e-9
		M3	p_33_mm	w=1.36e-6	l=340e-9
	5	M0	n_33_mm	w=340e-9	l=340e-9
		M1	p_33_mm	w=680e-9	l=340e-9

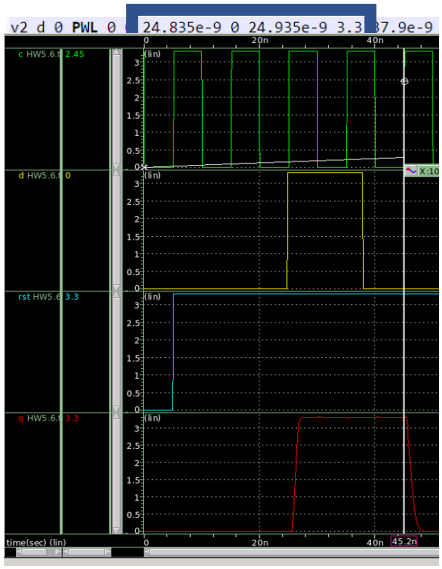
2.Presim of DFF



3.Setup time and Hold time

(1)Setup time



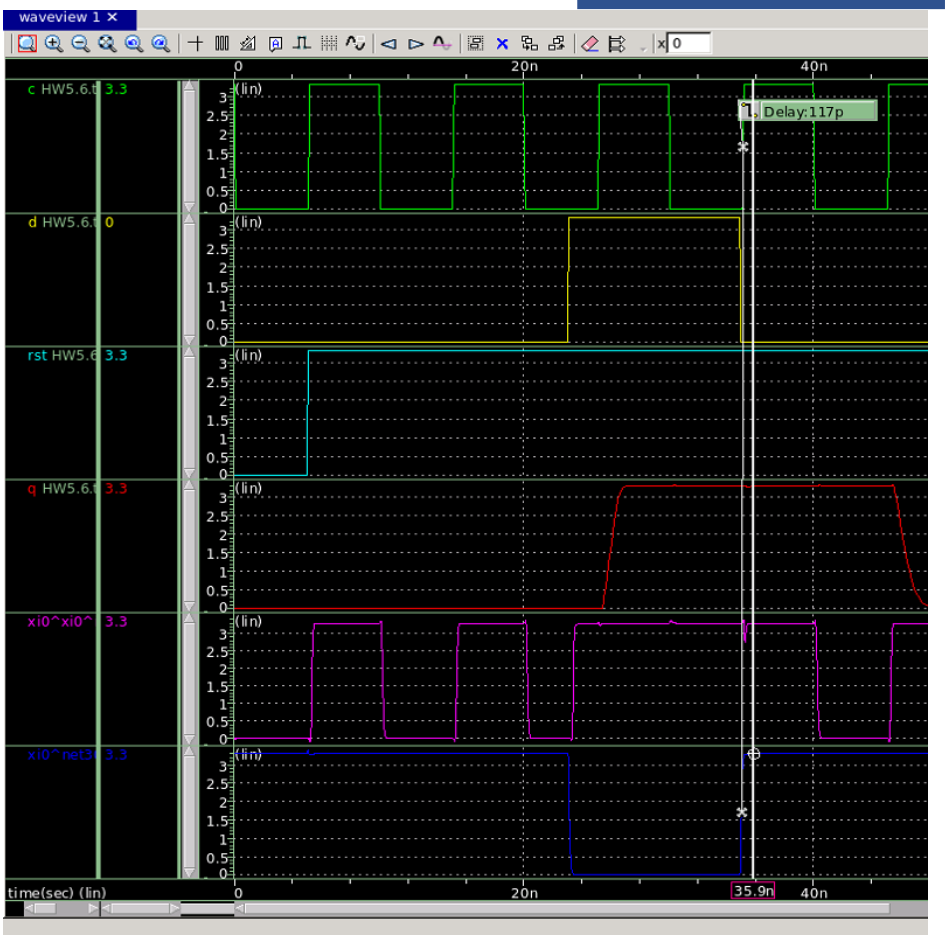


Clk edge is 25ns

25-24.935=0.065(ns)

(2)Hold time

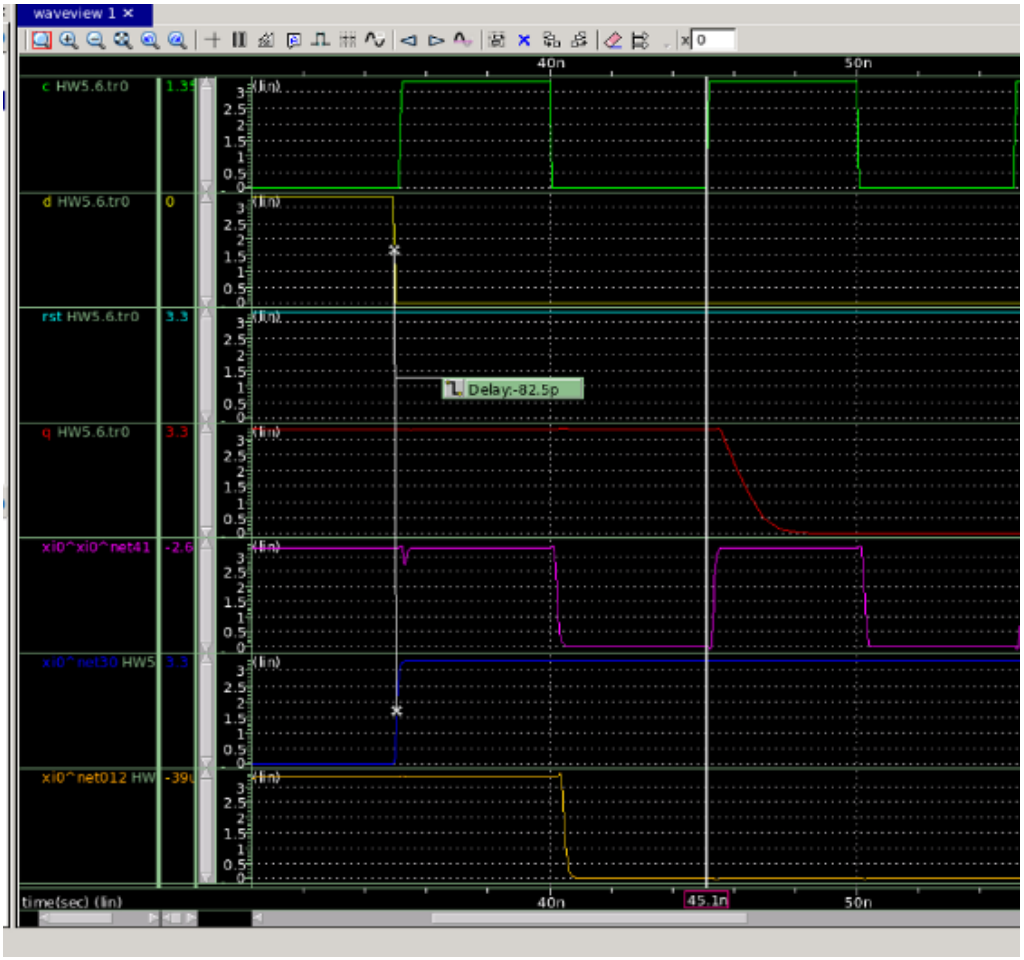
```
93    v2 d 0 PWL 0 0 23e-9 0 23.1e-9 3.  34.9e-9 3.3 35e-9 0 100e-9
```



出乎意料的 Hold time =0

解釋 1:在每個 edge 時，確實兩個 D latch 都有同時開啟的可能(也就是 transparent latch)，但這個同時開啟的時間太小，所以下降也沒有太多，還在 slave latch 可容忍範圍內，slave 的電位自動回復到 vdd，同時 master 也自動回復。

解釋 2:這次為了做到可以 reset 的 flipflop，在前面有增加一些邏輯閘，所以在 D 的傳遞也是有受到一些 delay 的



如圖:藍色是 master latch D input

確實有比原本的 D 訊號慢一些

粉紅色是 latch 的 nand，確實有被 D 的改變受到影響，但很快 Clk 關閉，而粉紅色也自動回復

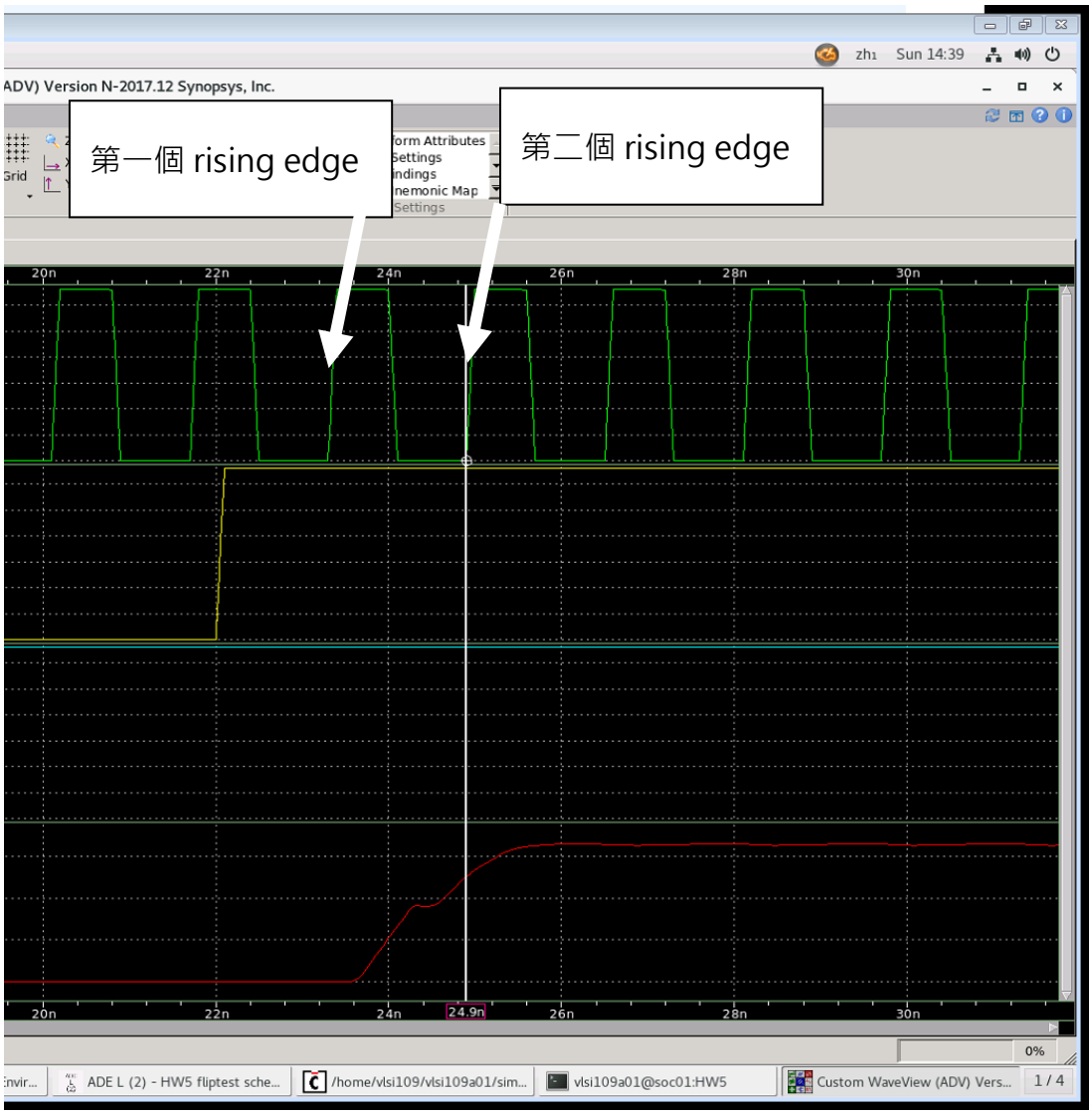
4.Maximum clock rate

定義我的正常運作 D 從 0->1，clk 到第二次 rising edge 時，Q 的電位要高於

3.3*0.7=(2.31)V

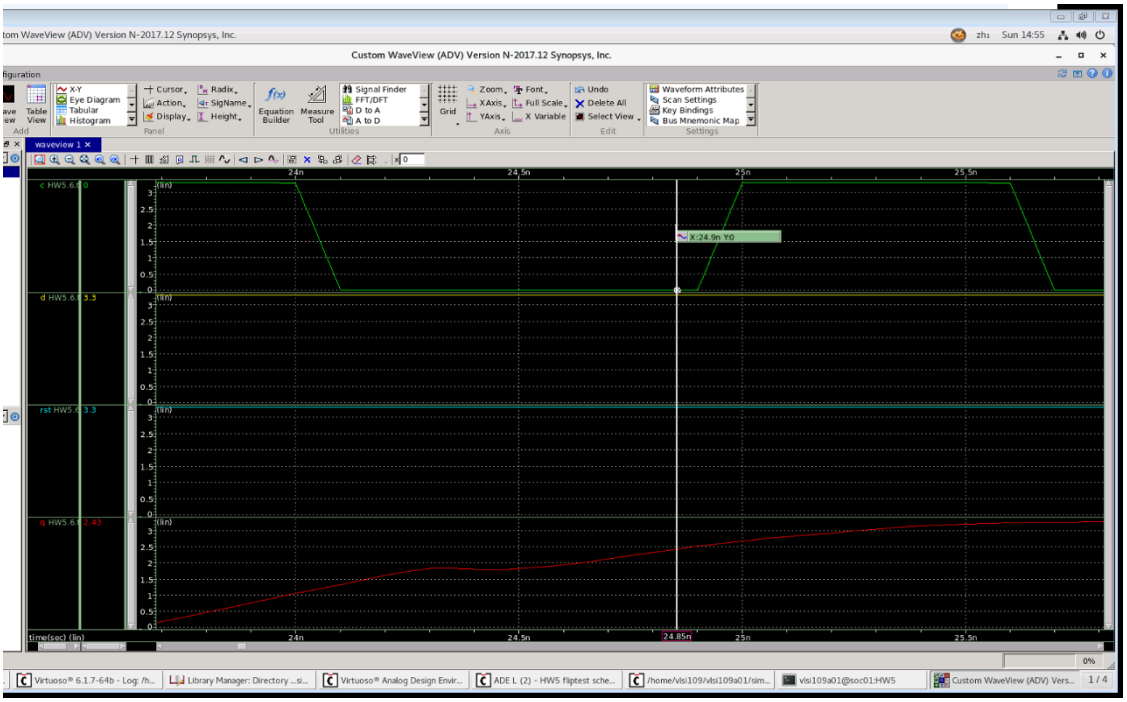
同理定義正常運作 D 從 1->0，clk 到第二次 rising edge 時，Q 的電位要低於

3.3*0.3=(0.99)V

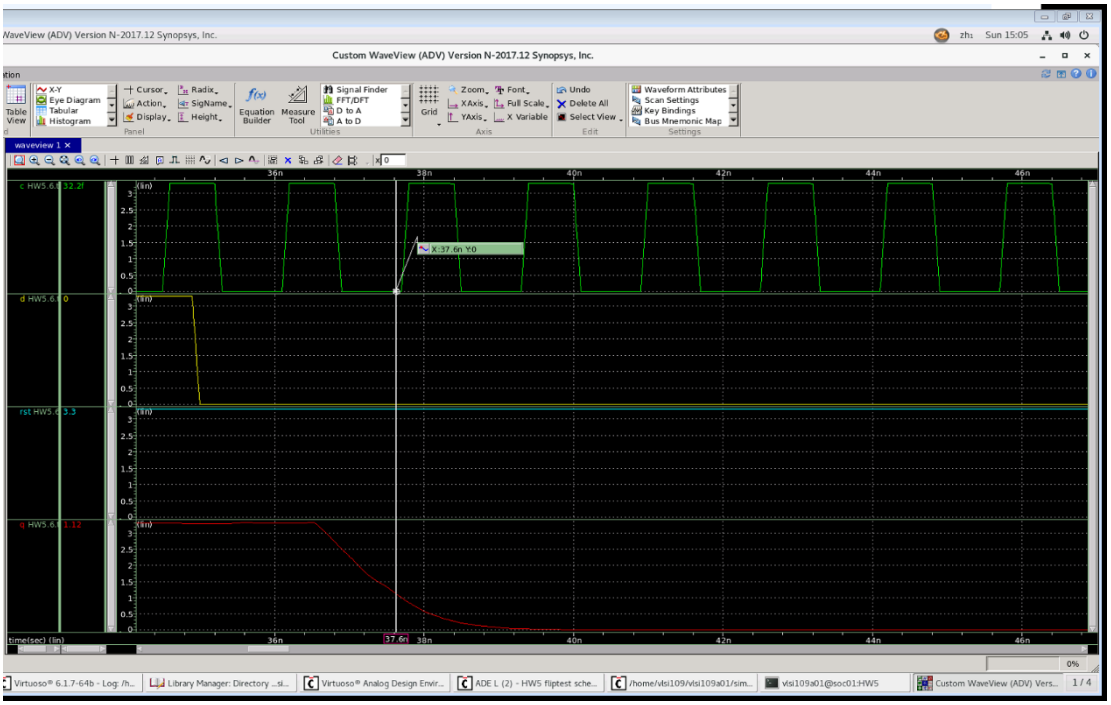


```
90    c0 q 0 100e-15
91    v1 c 0 PULSE 3.3 0 0 100e-12 100e-12 0.8e-9 1.6e-9
92    v3 rst 0 PWL 0 0 5e-9 0 5 1e-9 3 3 130e-9 3 3 130 1e-
```

clk=1.6e-9 = 625000000Hz



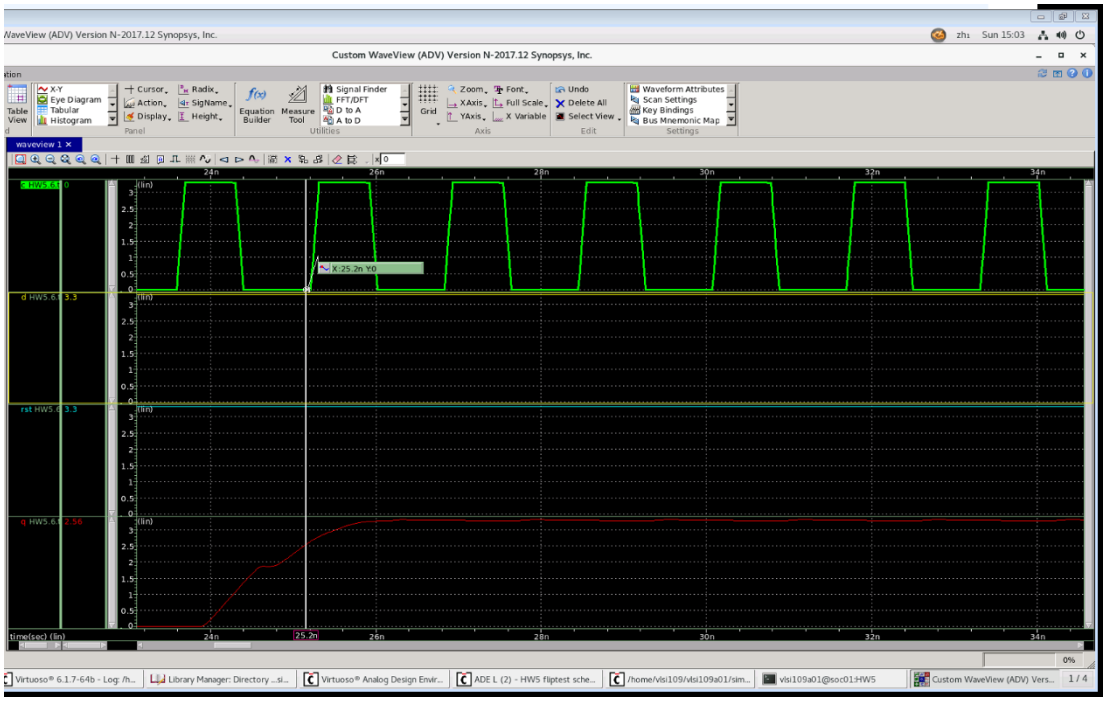
0->1，上升狀況 Q=2.43(符合)



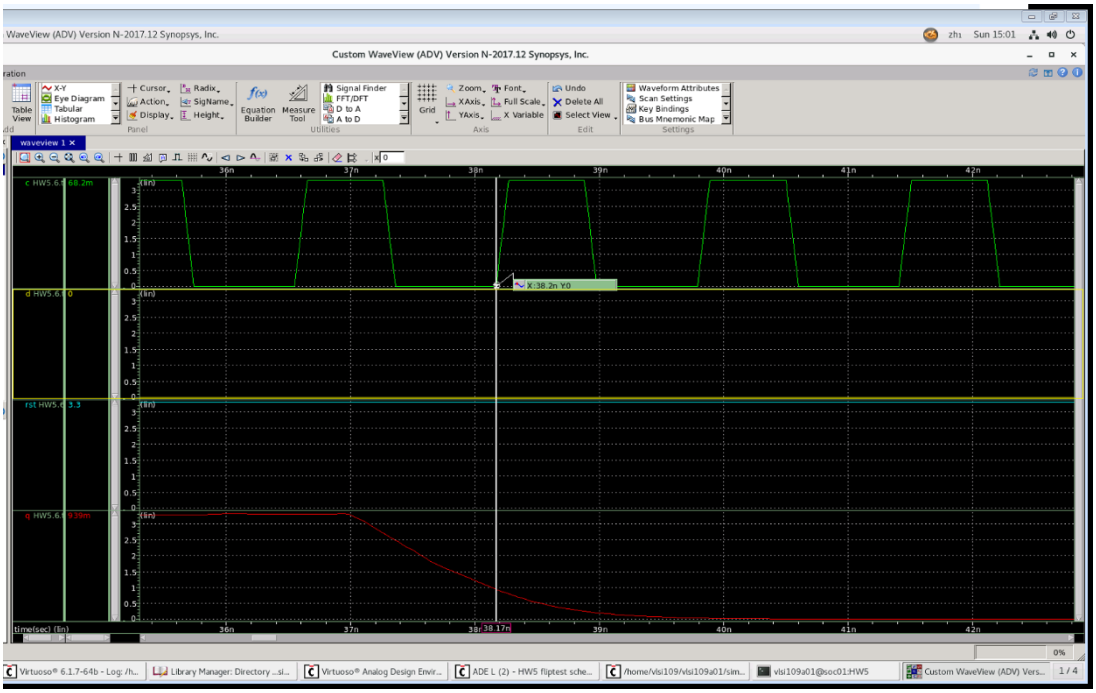
1->0，下降狀況 Q=1.12(不符合)

```
90    c0 q 0 100e-15
91    v1 c 0 PULSE 3.3 0 0 100e-12 100e-12 0.81e-9 1.62e-9
```

clk=1.62e-9 ≒ 617283950Hz



0->1，上升狀況 Q=2.56(符合)



1->0，下降狀況 Q=0.939(符合)

Maximum clock rate ≒ 617283950Hz