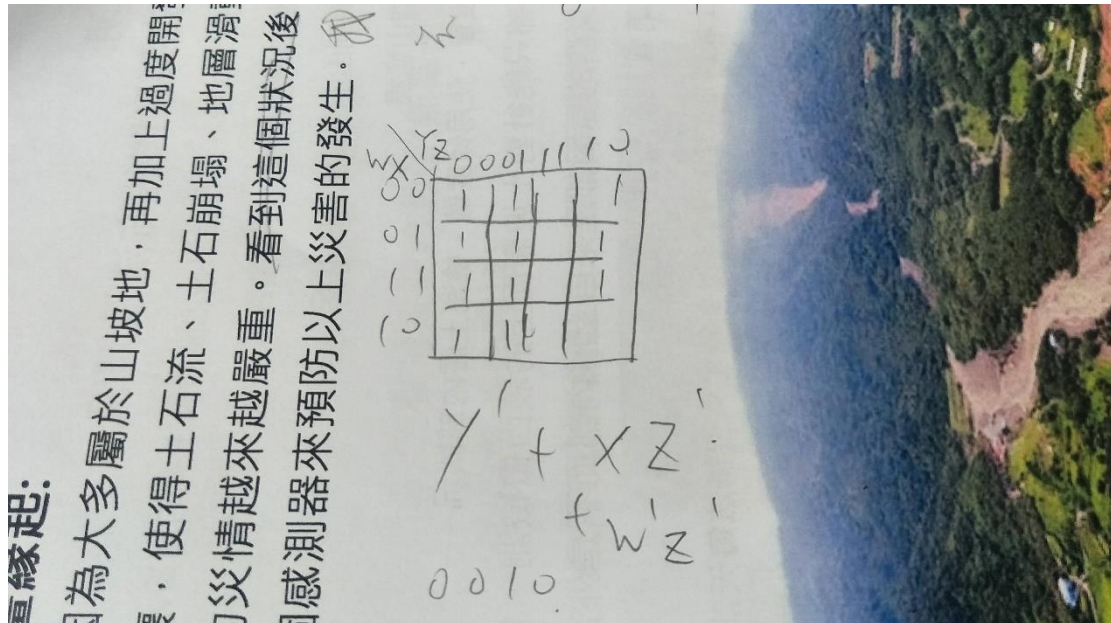


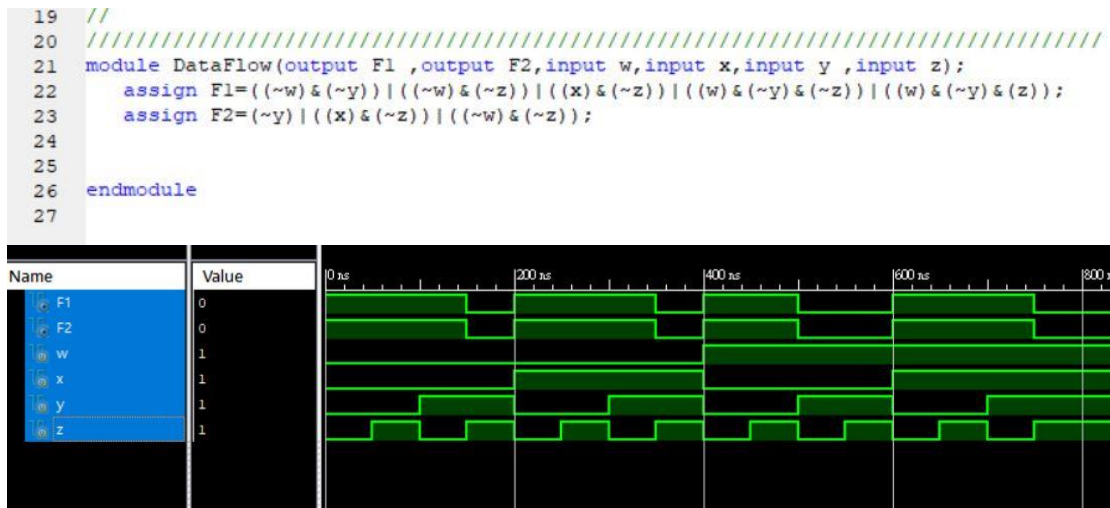
這次的實驗為卡諾圖化簡電路後，證實與原式相等

第一個實驗

題目的卡諾圖:



化簡成為 $y' + xz'$



證實原式(F1)相等於卡諾圖化簡後式(F2)

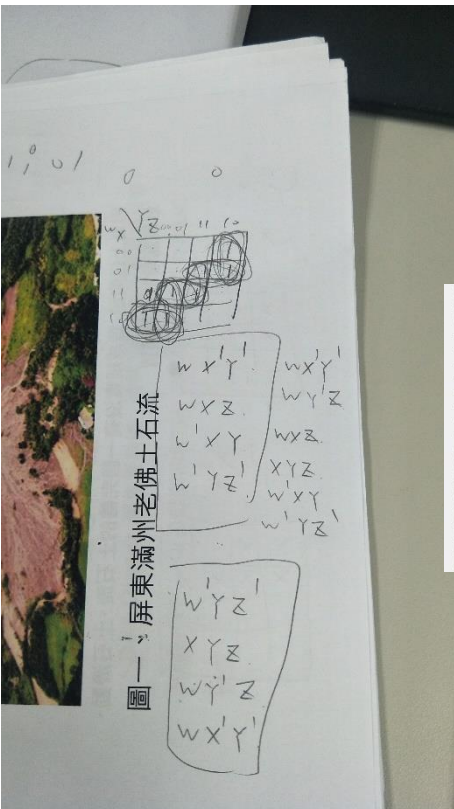
第二個實驗

化簡後理論上應該只有兩個最佳解

因此加上另一個組合

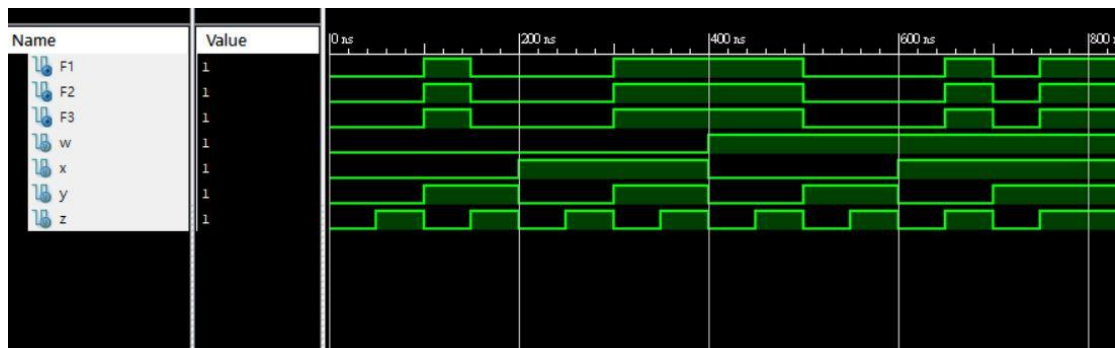
證明 $wx'y' + wxz + w'xy + w'yz' = w'yz' + xyz + wy'z + wx'y' =$

$wx'y' + wy'z + wxz + xyz + w'xy + w'yz'$



The image shows a handwritten Karnaugh map and a circuit diagram. The Karnaugh map is a 4x4 grid with variables w, x, y, z. The circuit diagram is a Verilog module named 'modu' with inputs w, x, y, z and outputs F1, F2, F3. The module implements the logic for the Karnaugh map.

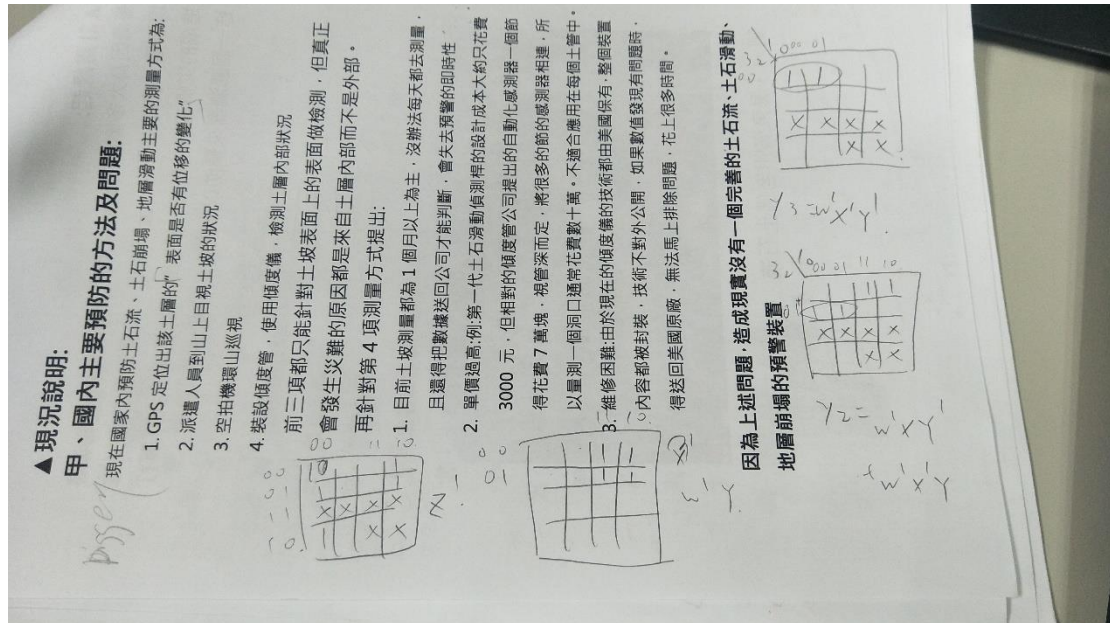
```
21 module modu(output F1,output F2,output F3,input w,input x,input y,input z);
22   wire not_w;
23   wire not_x;
24   wire not_y;
25   wire not_z;
26
27   not(not_w,w);
28   not(not_x,x);
29   not(not_y,y);
30   not(not_z,z);
31
32   wire F1_A,F1_B,F1_C,F1_D;
33   and(F1_A,w,not_x,not_y);
34   and(F1_B,w,x,z);
35   and(F1_C,not_w,x,y);
36   and(F1_D,not_w,y,not_z);
37
38   or(F1,F1_A,F1_B,F1_C,F1_D);
39
40   wire F2_A,F2_B,F2_C,F2_D;
41   and(F2_A,not_w,y,not_z);
42   and(F2_B,x,y,z);
43   and(F2_C,w,not_y,z);
44   and(F2_D,w,not_x,not_y);
45
46   or(F2,F2_A,F2_B,F2_C,F2_D);
47
48   wire F3_A,F3_B,F3_C,F3_D,F3_E,F3_F;
49   and(F3_A,w,not_x,not_y);
50   and(F3_B,w,not_y,z);
51   and(F3_C,w,x,z);
52   and(F3_D,x,y,z);
53   and(F3_E,not_w,x,y);
54   and(F3_F,not_w,y,not_z);
55
56   or(F3,F3_A,F3_B,F3_C,F3_D,F3_E,F3_F);
57 endmodule
58
```



證實化簡(F1)=化簡(F2)=化簡(F3)

第三個實驗

為 9 補數電路實作，利用真值表及卡諾圖化簡(有關 don' t care)

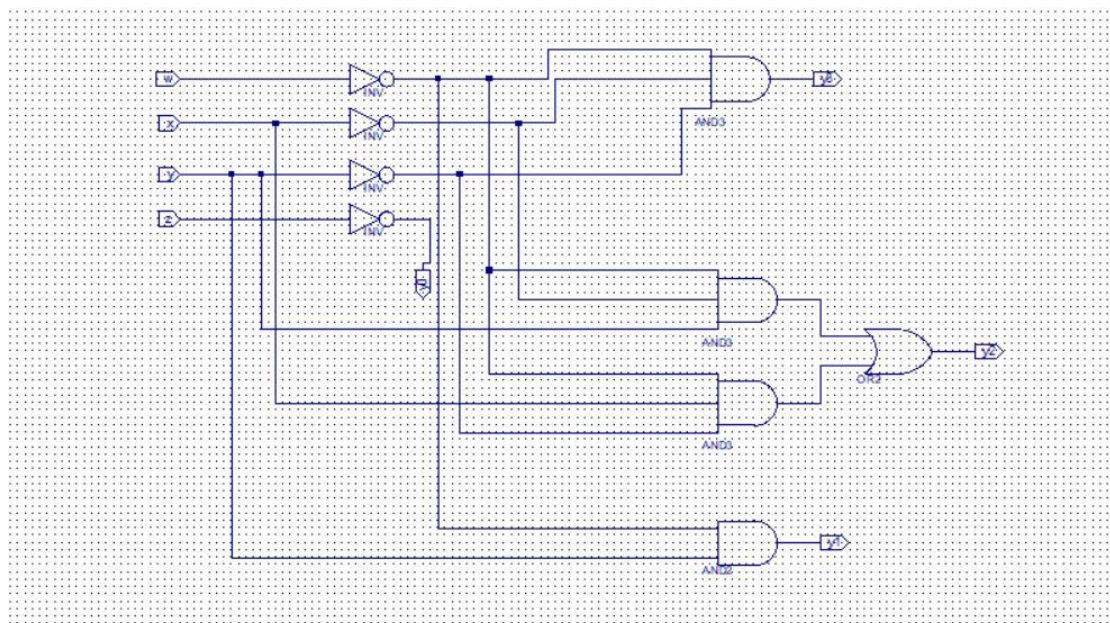


歸納出 $y_3 = w' x' y'$

$y_2 = w' xy' + w' x' y$

$y_1 = w' y$

$y_0 = z'$ (有利用到 don' t care 原則)





經過檢查後，證實此 F 電路為 Input 9 補數電路