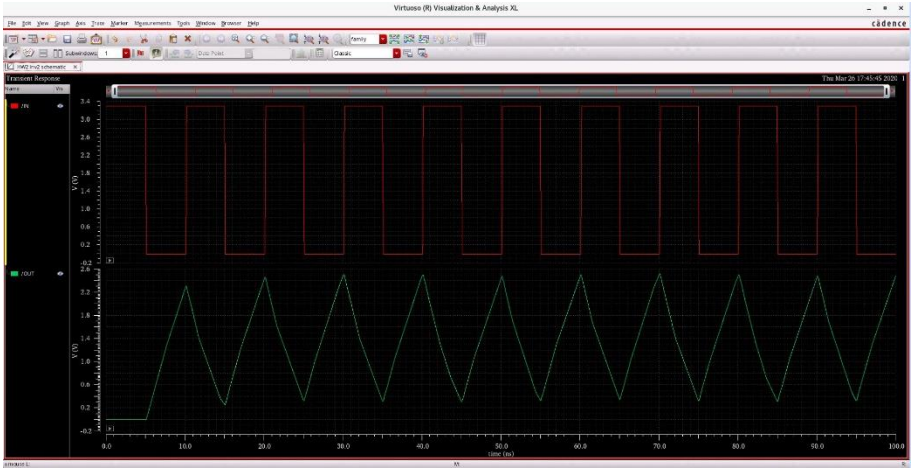
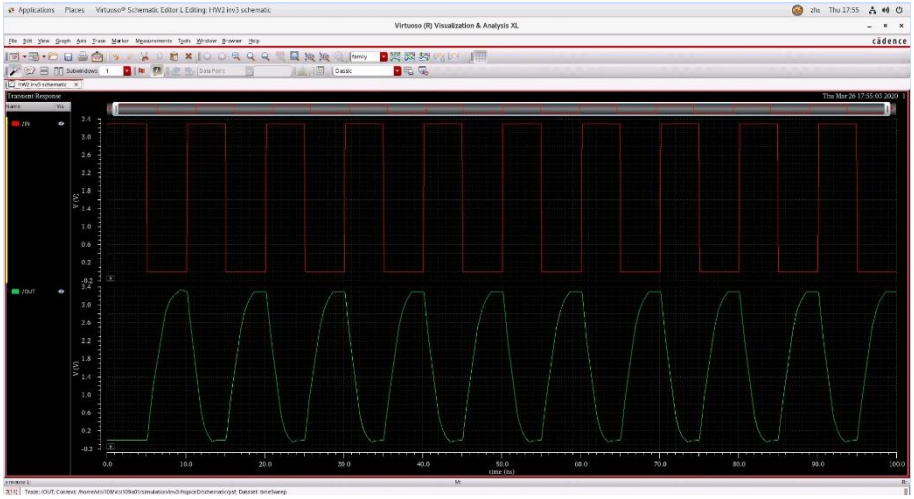
(1) inverters with different width and length

i. PU:PD = (2/1 : 1/1)

ii. PU:PD = (6/1 : 3/1)



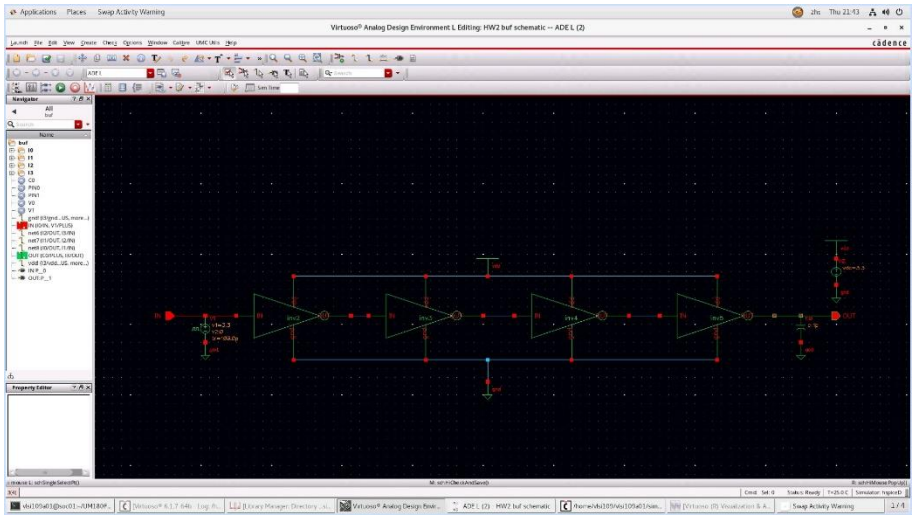
iii. PU:PD = (18/1 : 9/1)



iv. PU:PD = (48/1 : 24/1)

v. PU:PD = (144/1 : 72/1)

(2) buffer schematic



(3) buffer analysis

$Time_r$:717.1053ps

$Time_f$:643.4771ps

$delay_{pL->H}$:935.3662ps

$delay_{pH->L}$:852.1278ps