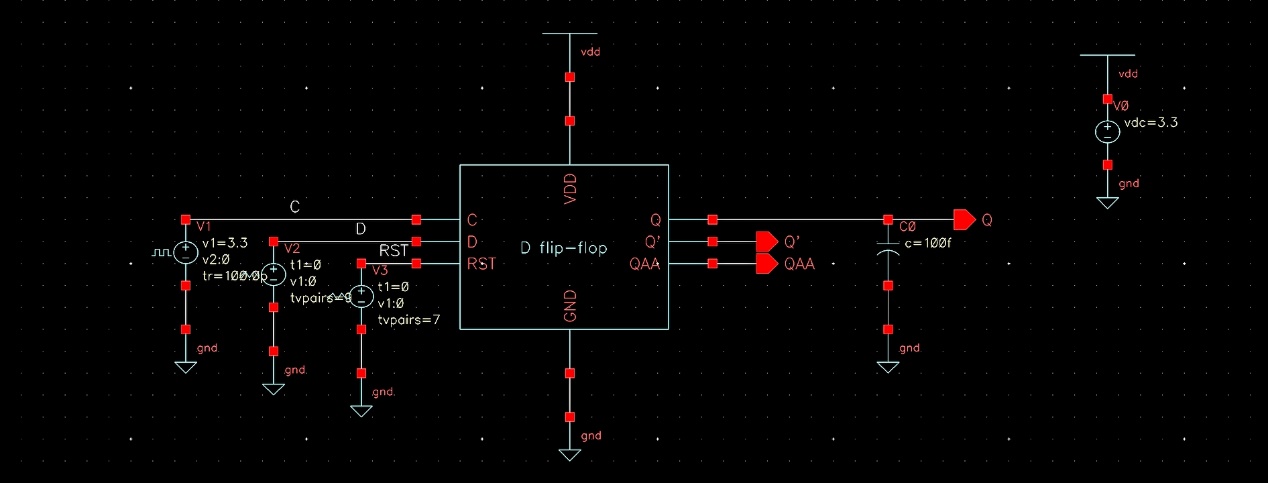
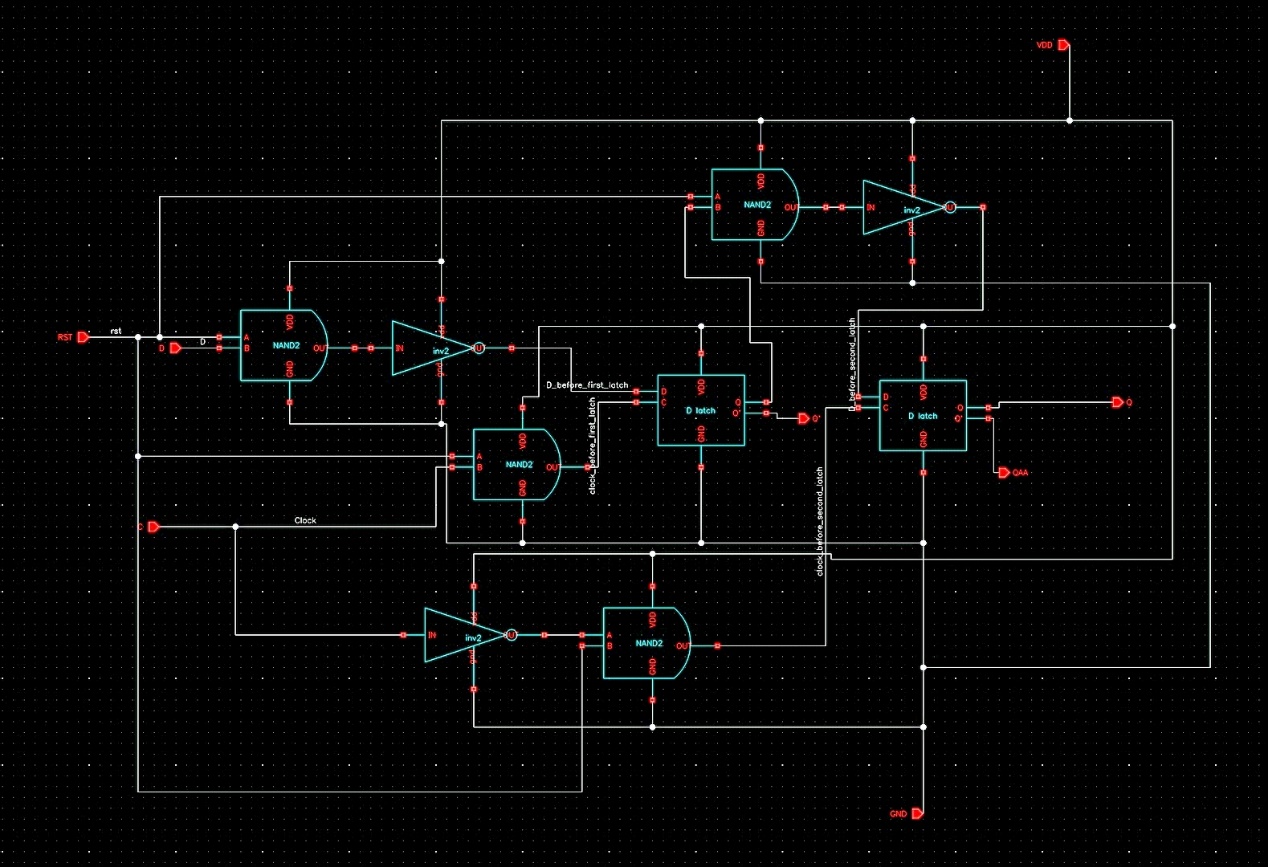
1.schematic of DFF

top level

inside d flipflop(編號是為了等一下的列表(number

9

8

7

6

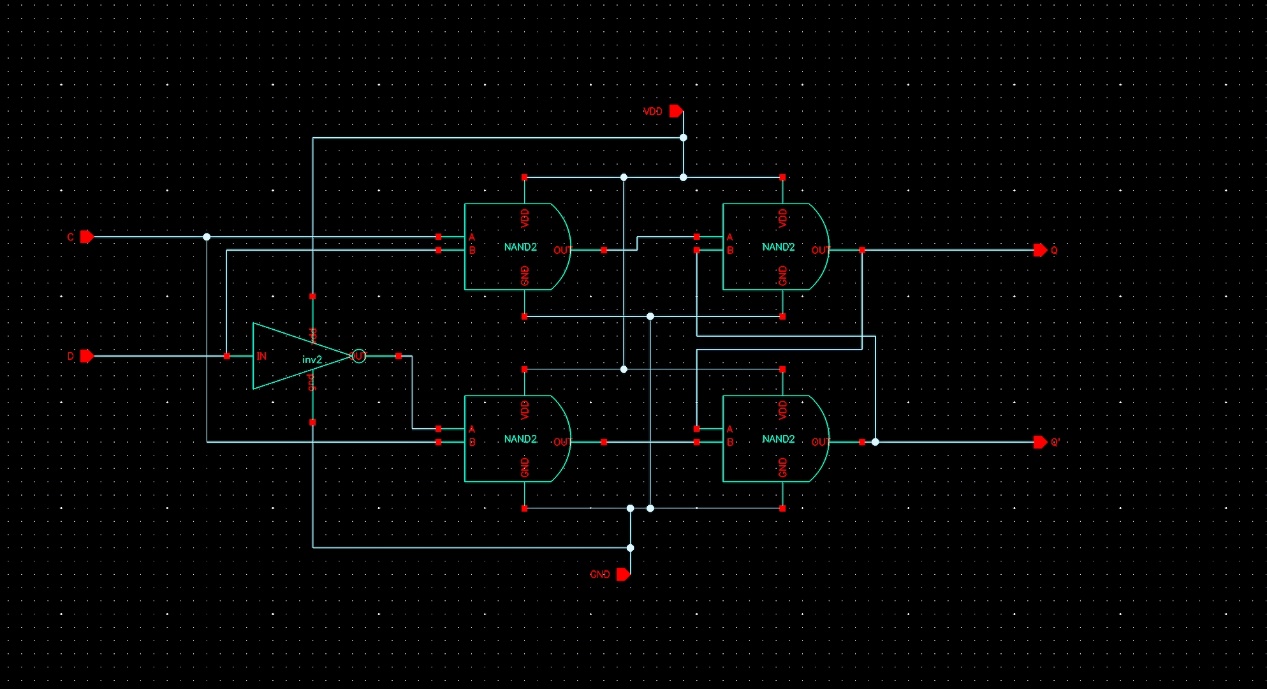
5

4

3

2

1

inside D latch(編號是為了等一下的列表(subnumber

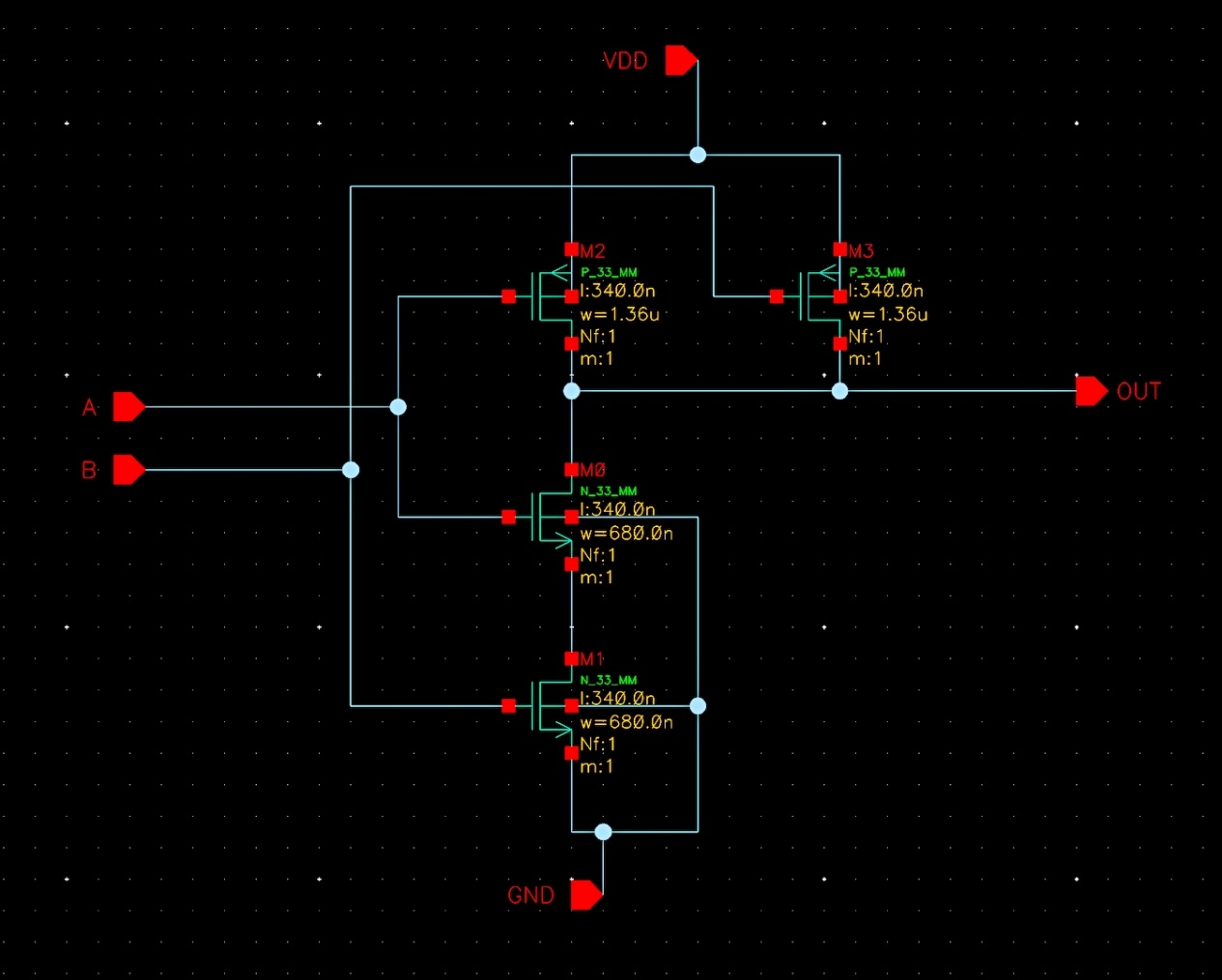
5

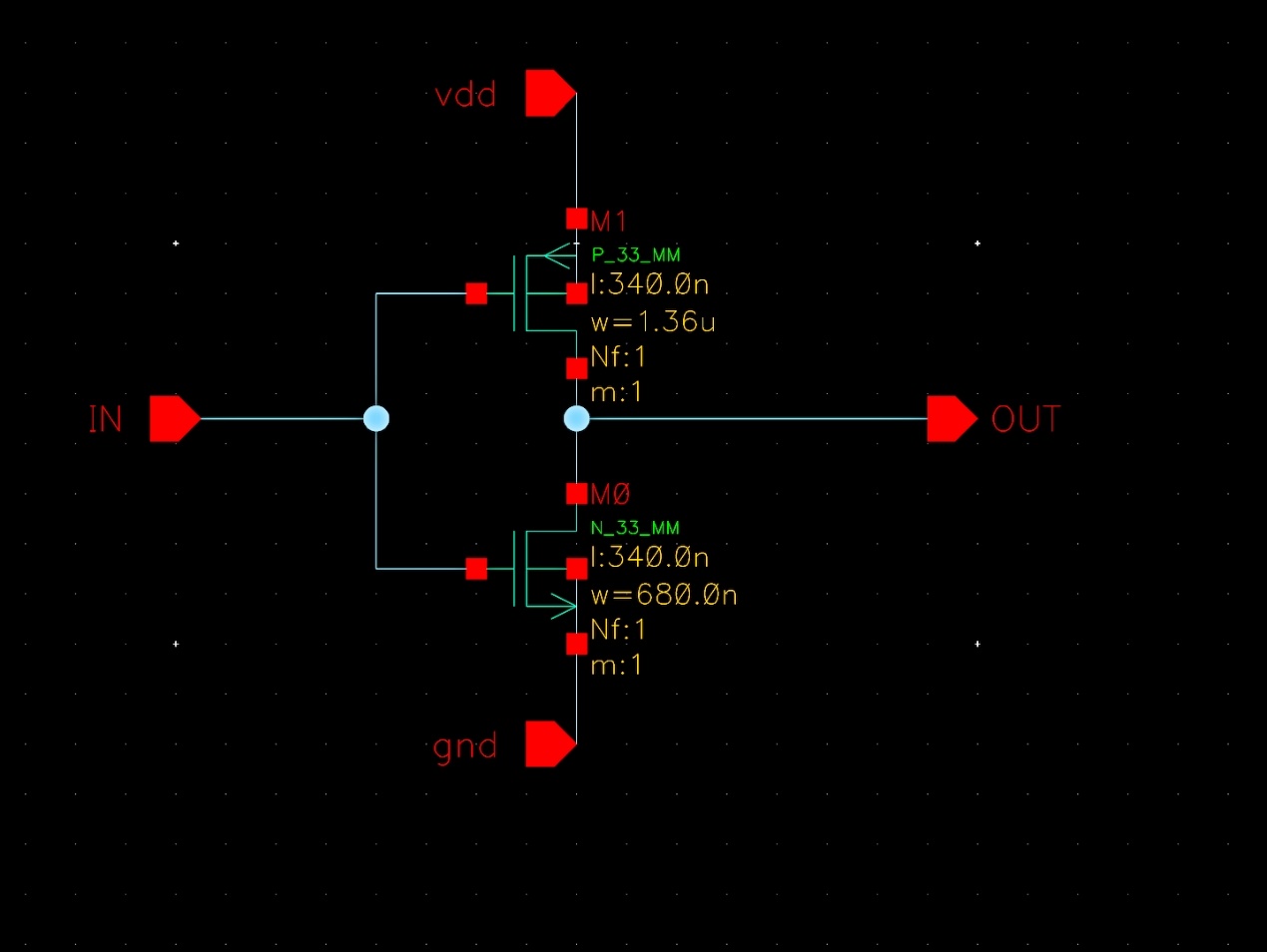
4

3

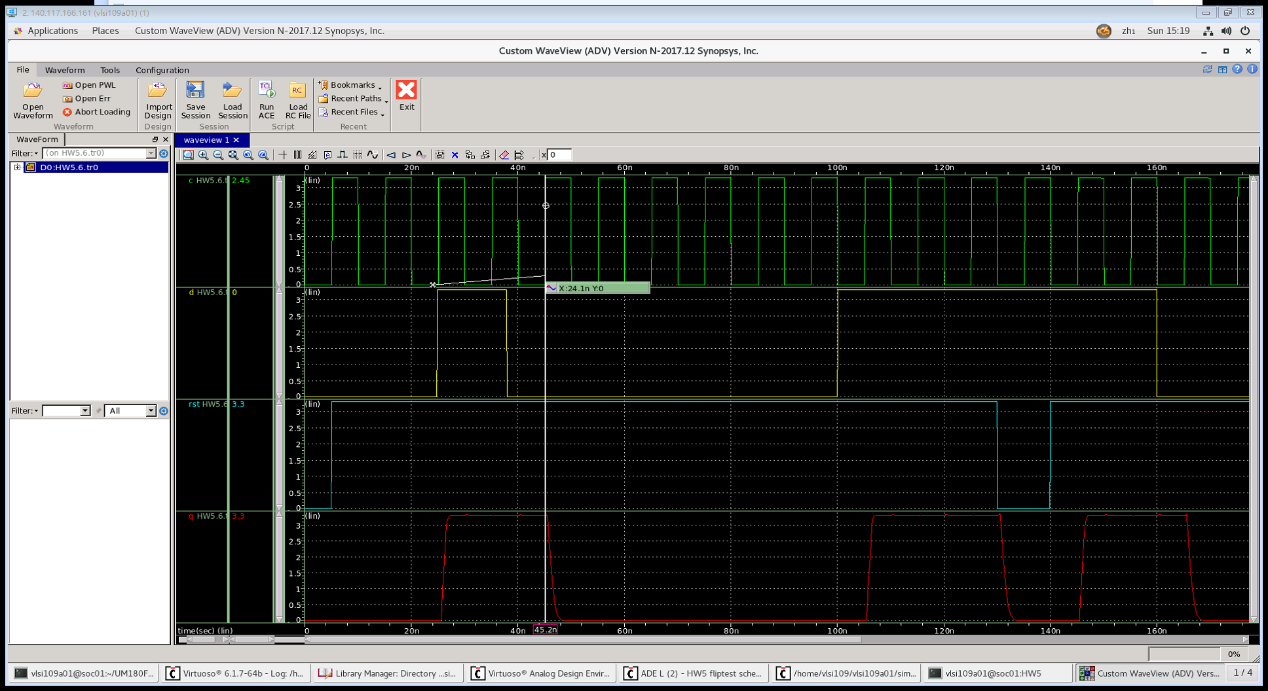
2

1

inside nand

inside inv

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| number | subnumber |  |  |  |  |
| 1 |  | M0 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M1 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M2 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
|  |  | M3 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
| 2 |  | M0 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M1 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M2 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
|  |  | M3 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
| 3 |  | M0 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M1 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M2 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
|  |  | M3 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
| 4 |  | M0 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M1 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M2 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
|  |  | M3 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
| 5 |  | M0 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M1 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
| 6 |  | M0 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M1 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
| 7 |  | M0 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M1 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
| 8 | 1 | M0 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M1 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M2 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
|  |  | M3 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
|  | 2 | M0 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M1 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M2 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
|  |  | M3 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
|  | 3 | M0 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M1 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M2 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
|  |  | M3 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
|  | 4 | M0 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M1 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M2 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
|  |  | M3 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
|  | 5 | M0 | n\_33\_mm | w=340e-9 | l=340e-9 |
|  |  | M1 | p\_33\_mm | w=680e-9 | l=340e-9 |
| 9 | 1 | M0 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M1 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M2 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
|  |  | M3 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
|  | 2 | M0 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M1 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M2 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
|  |  | M3 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
|  | 3 | M0 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M1 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M2 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
|  |  | M3 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
|  | 4 | M0 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M1 | n\_33\_mm | w=680e-9 | l=340e-9 |
|  |  | M2 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
|  |  | M3 | p\_33\_mm | w=1.36e-6 | l=340e-9 |
|  | 5 | M0 | n\_33\_mm | w=340e-9 | l=340e-9 |
|  |  | M1 | p\_33\_mm | w=680e-9 | l=340e-9 |

2.Presim of DFF

下一個rising edge時回復

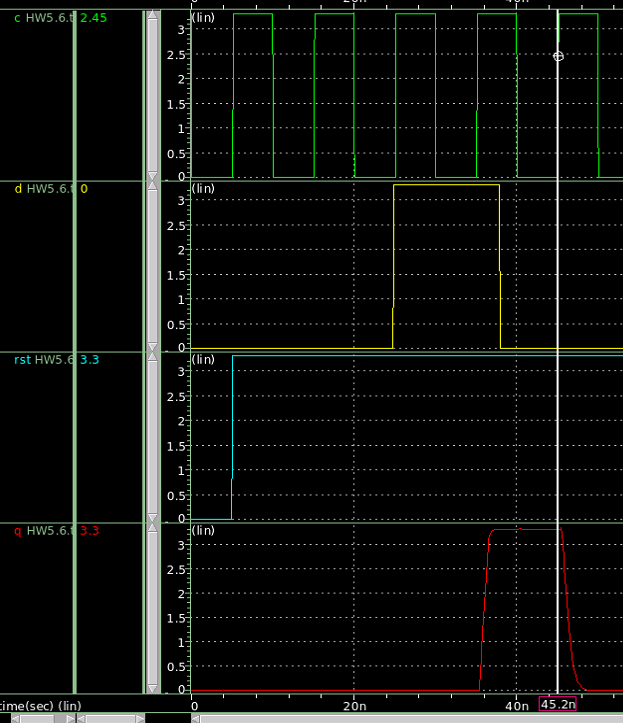
正源觸發D(0->1)

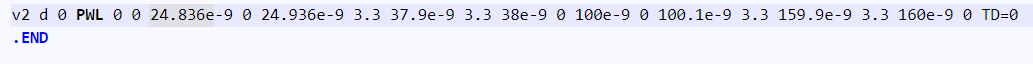
正源觸發D(1->0)

Rst 為0時，直接Q->0

3.Setup time and Hold time

一張含有 電腦 的圖片

自動產生的描述 (1)Setup time



Clk edge is 25ns

25-24.935=0.065(ns)

一張含有 電腦 的圖片

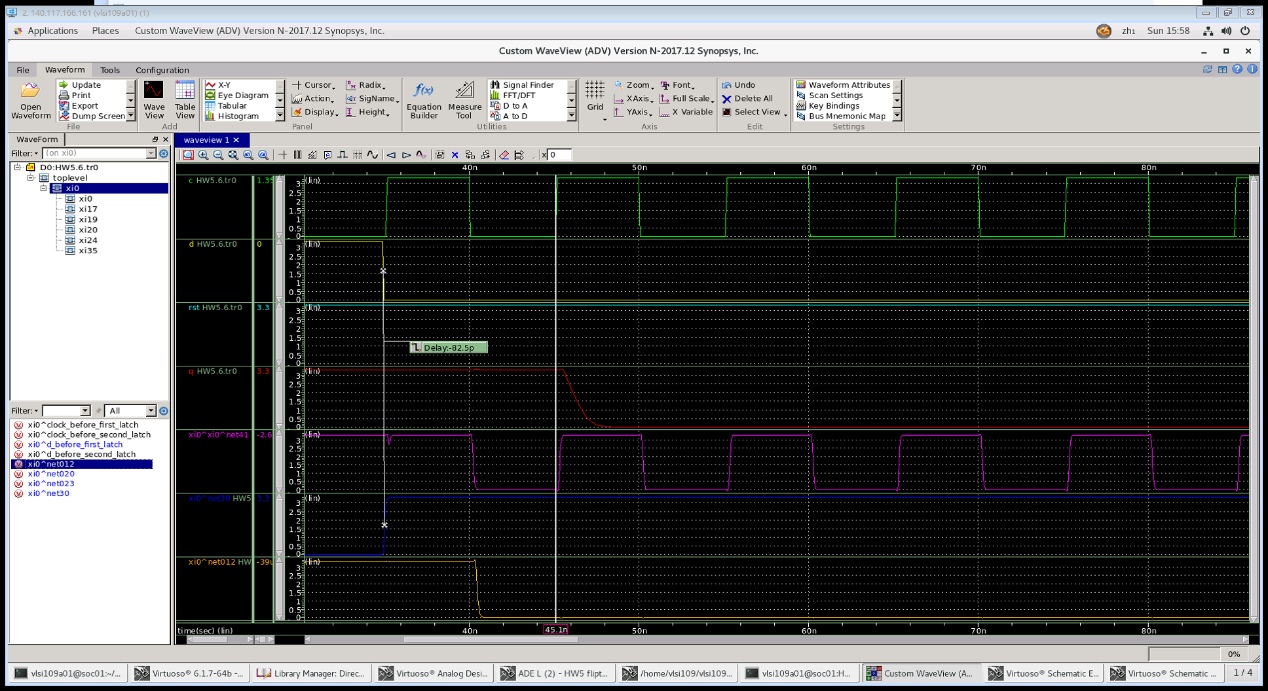
自動產生的描述 (2)Hold time



出乎意料的Hold time =0

解釋1:在每個edge時，確實兩個D latch都有同時開啟的可能(也就是transparent latch)，但這個同時開啟的時間太小，所以下降也沒有太多，還在slave latch可容忍範圍內，slave的電位自動回復到vdd，同時master也自動回復。

解釋2:這次為了做到可以reset的flipflop，在前面有增加一些邏輯閘，所以在D的傳遞也是有受到一些delay的

如圖:藍色是master latch D input

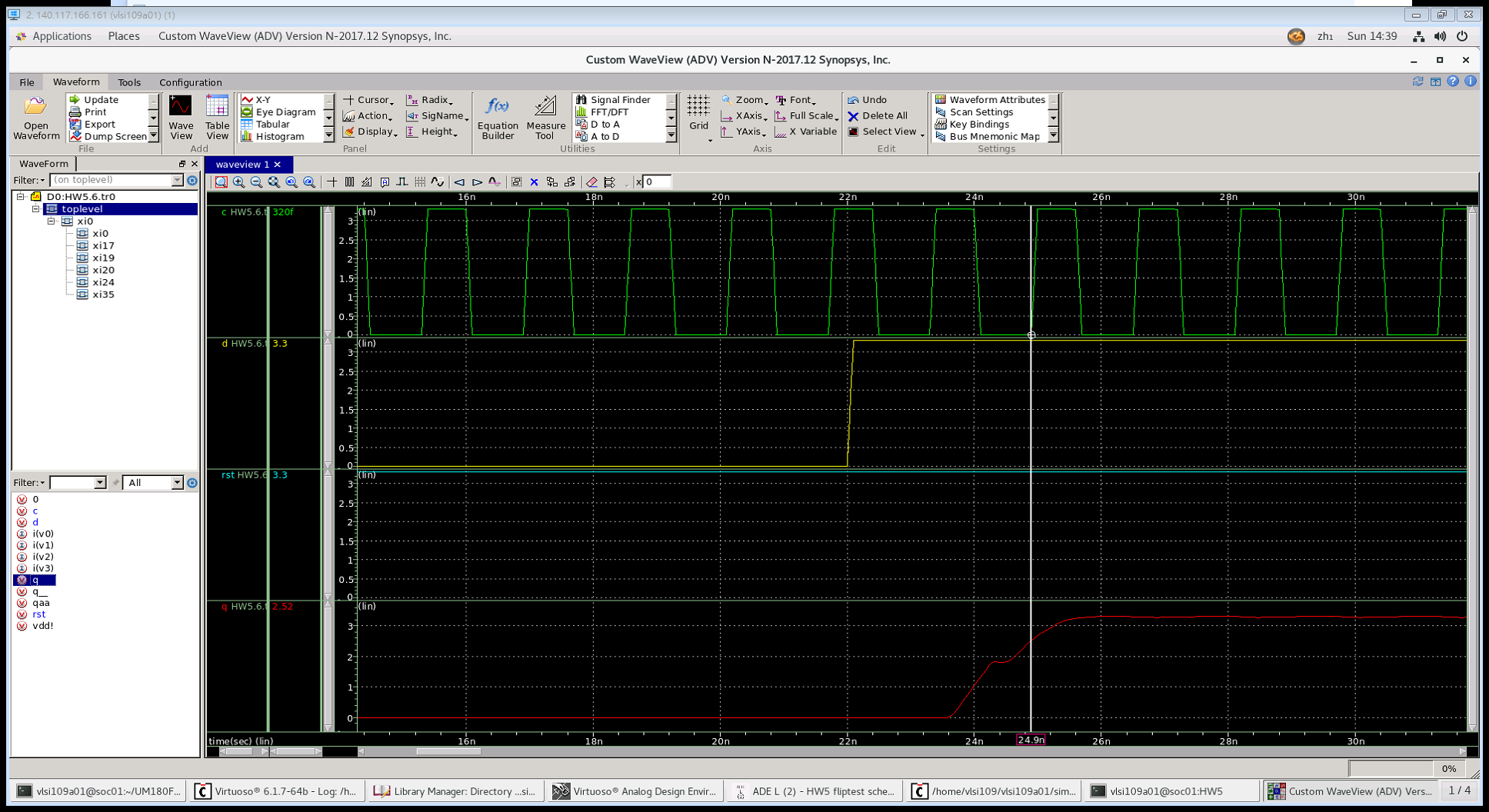
確實有比原本的D訊號慢一些

粉紅色是latch的nand，確實有被D的改變受到影響，但很快Clk關閉，而粉紅色也自動回復

4.Maximum clock rate

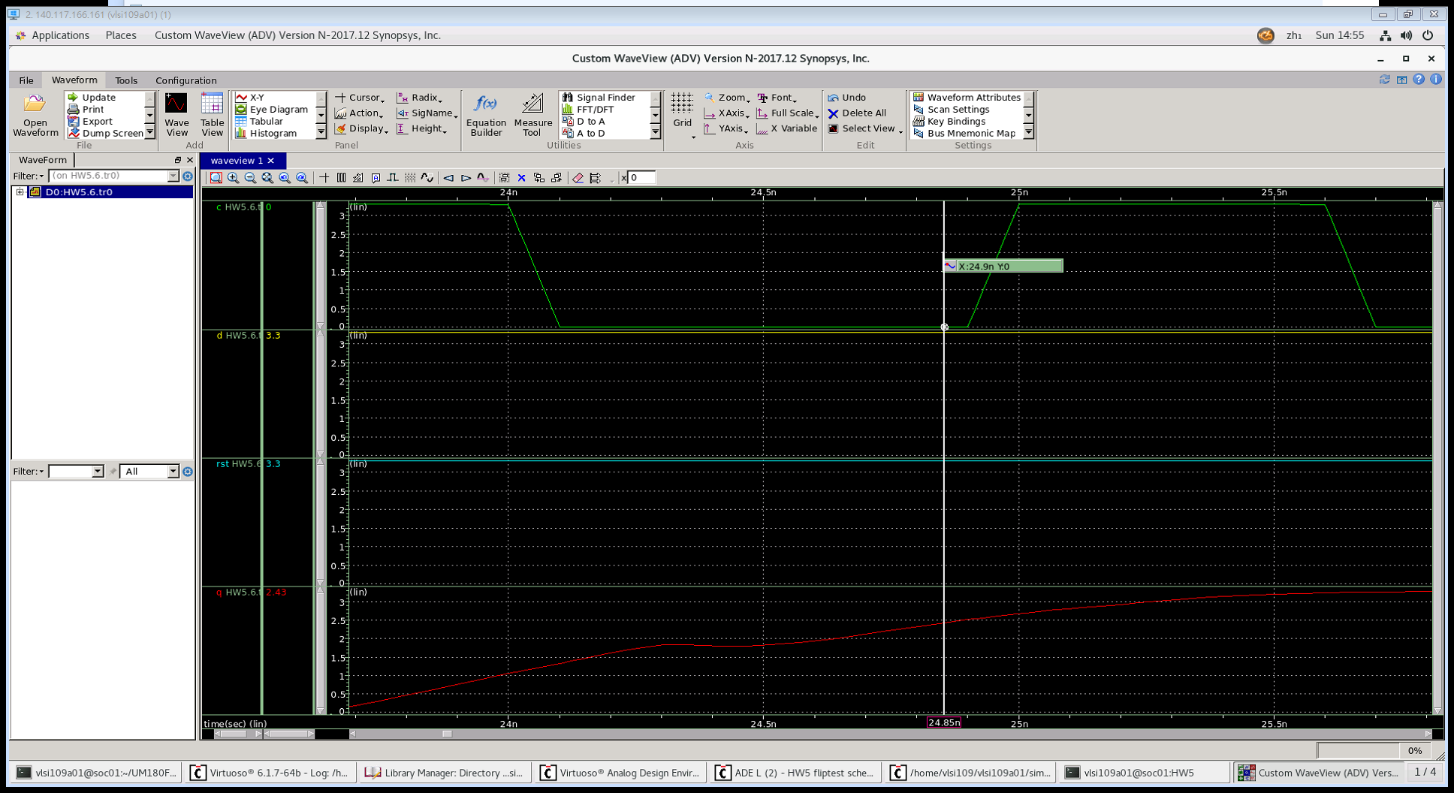
定義我的正常運作D 從0->1，clk到第二次rising edge時，Q的電位要高於3.3\*0.7=(2.31)V

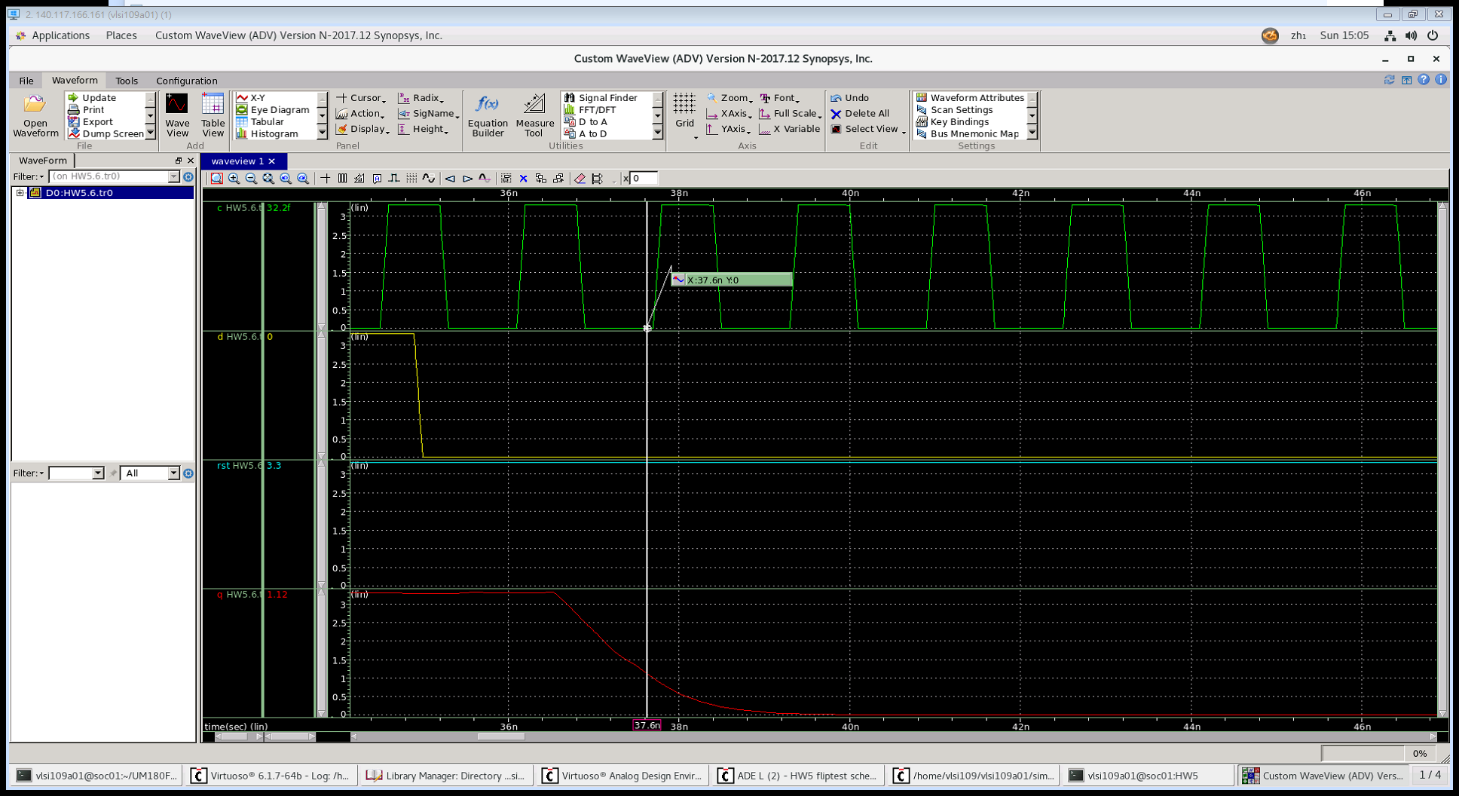
同理定義正常運作D 從1->0，clk到第二次rising edge時，Q的電位要低於3.3\*0.3=(0.99)V



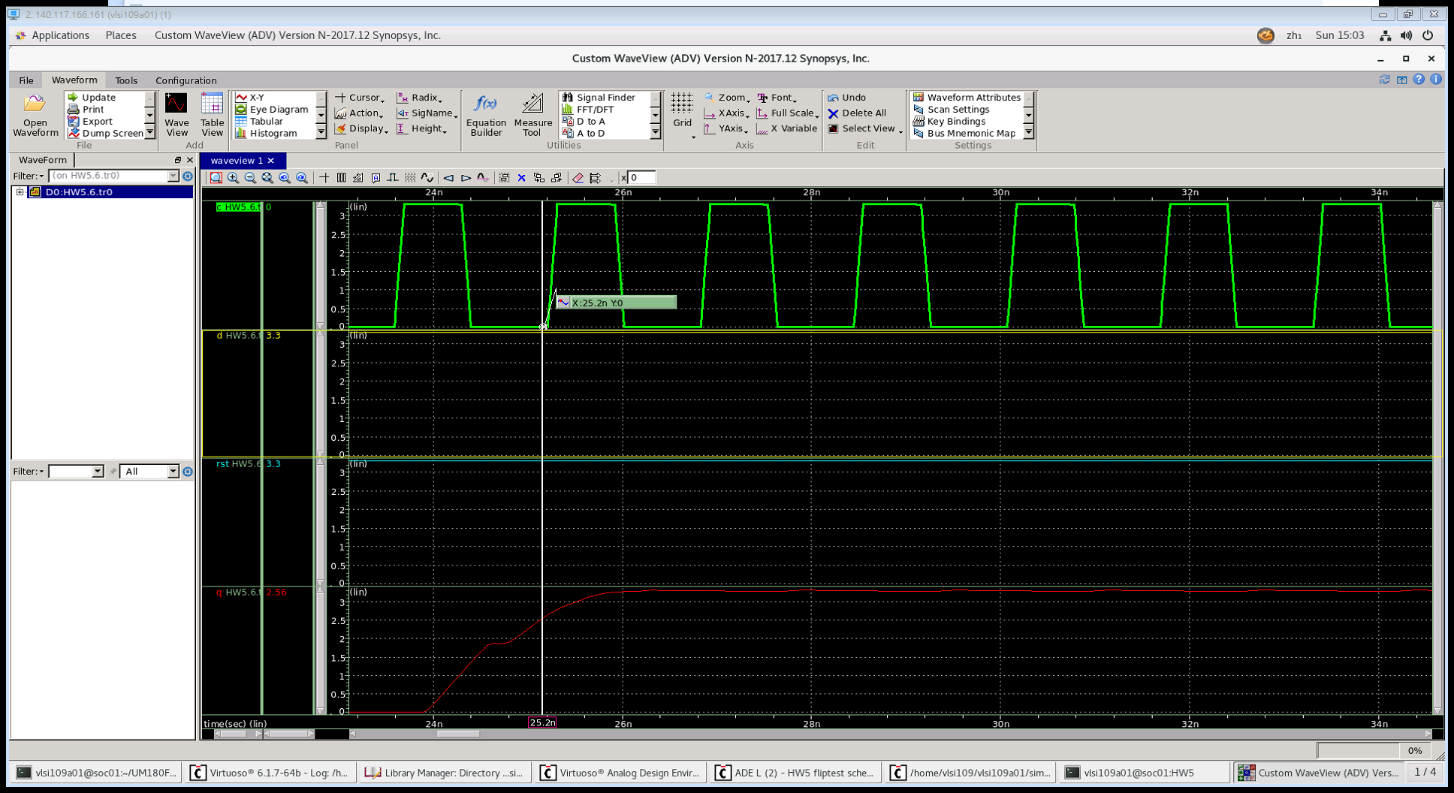
第一個rising edge

第二個rising edge

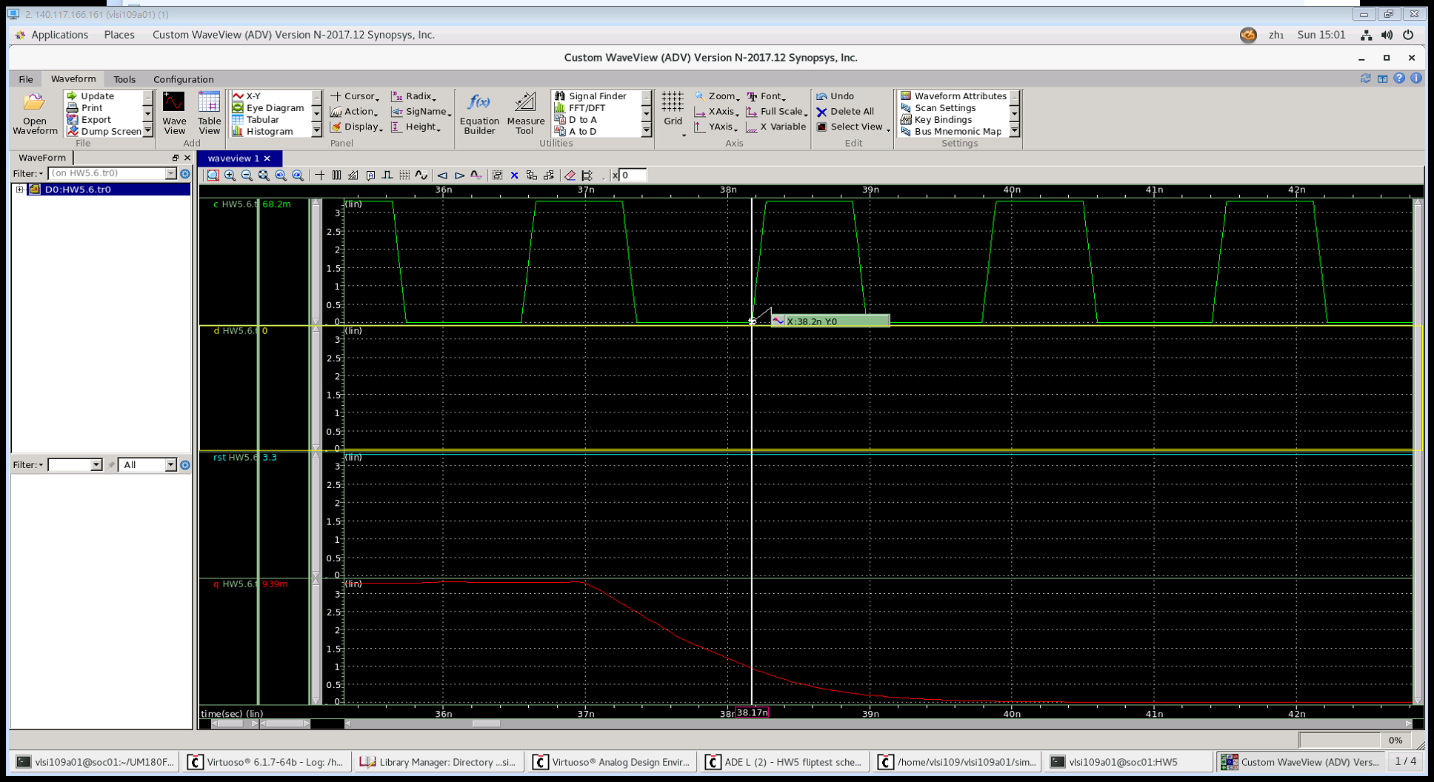
clk=1.6e-9 = 625000000Hz

0->1，上升狀況Q=2.43(符合)

1->0，下降狀況Q=1.12(不符合)

一張含有 時鐘, 橙色, 螢幕, 房間 的圖片

自動產生的描述clk=1.62e-9 ≒ 617283950Hz

0->1，上升狀況Q=2.56(符合)

1->0，下降狀況Q=0.939(符合)

Maximum clock rate ≒ 617283950Hz