Digital Systems Sessional

CSE 2205

Lab Manual

Department of Computer Science and Engineering

Pabna University of Science and Technology

Experiment No. 01: Familiarization with necessary resources (ICs, devices, components etc.) of Digital Electronics Sessional.

1.1 Objectives:

1. To familiarize with digital electronics trainer kit.
2. Familiarization with IC Tester.
3. To familiarize with digital ICs.

1.2 Experiment Requirements:

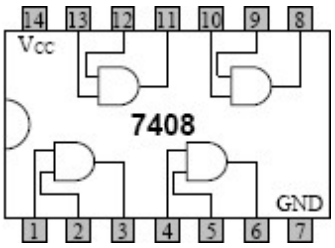
1. Digital Electronics Trainer Kit.
2. Digital IC Tester.
3. DC power supply unit.
4. Digital ICs: 7408, 7432, 7404, 7400, 7402, 7486, 7410, 7420, 74107

1.3 Experiment Procedures:

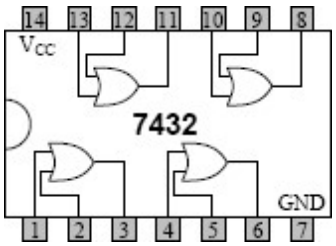
1. Observe the functionalities and operating procedures of trainer kit.
2. Observe the functionalities and operating procedures of dc power supply unit.
3. Observe the operating procedure of Digital IC Tester.
4. Familiarize with following digital ICs, their pin diagram and pin functions.

1.4 Digital IC's:

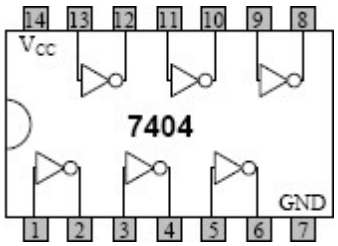
a. Name of the IC: **IC 7408, AND** gate

PIN diagram	PIN description			
	PIN no.	Function	PIN no.	Function
	7	Ground	14	+Vcc
	1,2	Input	3	Output
	4,5	Input	6	Output
	13,12	Input	11	Output
	10,9	Input	8	Output

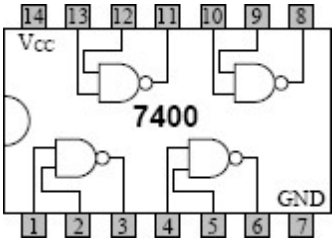
b. Name of the IC: **IC 7432, OR** gate

PIN diagram	PIN description			
	PIN no.	Function	PIN no.	Function
	7	Ground	14	+Vcc
	1,2	Input	3	Output
	4,5	Input	6	Output
	13,12	Input	11	Output
	10,9	Input	8	Output

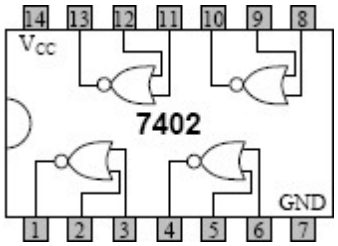
c. Name of the IC: **IC 7404, NOT** gate

PIN diagram	PIN description			
	PIN no.	Function	PIN no.	Function
	7	Ground	14	+Vcc
	1	Input	2	Output
	3	Input	4	Output
	5	Input	6	Output
	13	Input	12	Output
	11	Input	10	Output
	9	Input	8	Output

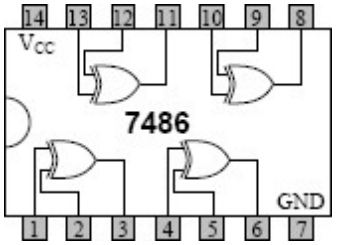
d. Name of the IC: **IC 7400, NAND** gate

PIN diagram	PIN description			
	PIN no.	Function	PIN no.	Function
	7	Ground	14	+Vcc
	1,2	Input	3	Output
	4,5	Input	6	Output
	13,12	Input	11	Output
	10,9	Input	8	Output

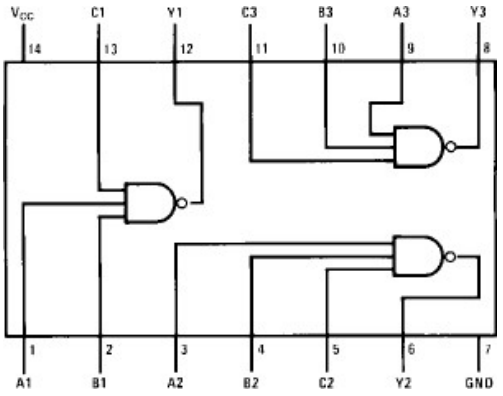
e. Name of the IC: **IC 7402, NOR** gate

PIN diagram	PIN description			
	PIN no.	Function	PIN no.	Function
	7	Ground	14	+Vcc
	2,3	Input	1	Output
	5,6	Input	4	Output
	11,12	Input	13	Output
	8,9	Input	10	Output

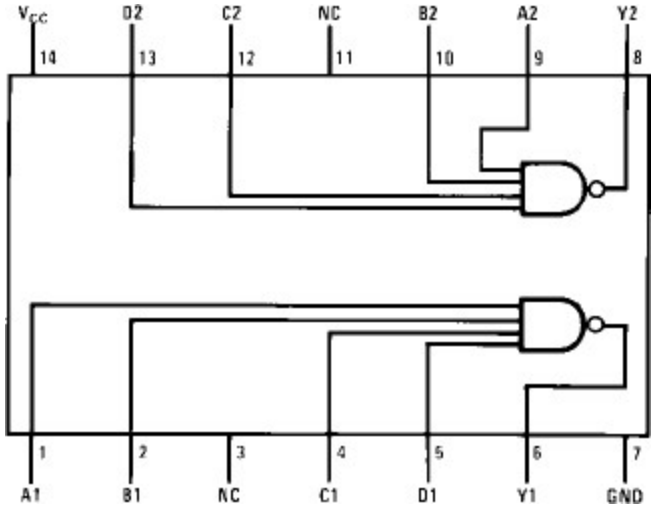
f. Name of the IC: **IC 7486, XOR** gate

PIN diagram	PIN description			
	PIN no.	Function	PIN no.	Function
	7	Ground	14	+Vcc
	1,2	Input	3	Out put
	4,5	Input	6	Out put
	13,12	Input	11	Out put
	10,9	Input	8	Out put

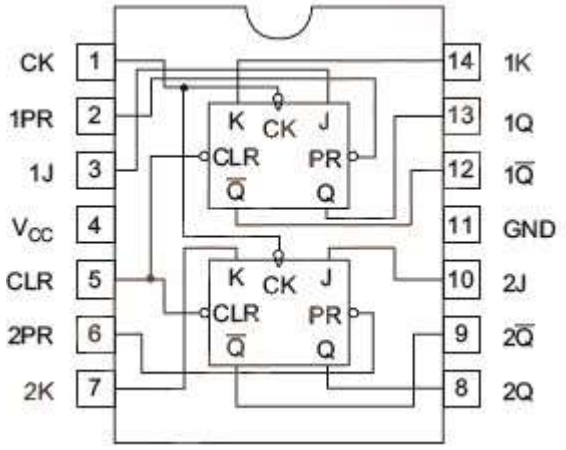
g. Name of the IC: **IC 7410**, **3-Input NAND gate**

PIN diagram	PIN description			
	PIN no.	Function	PIN no.	Function
	7	Ground	14	+Vcc
	1,2,13	Input	12	Out put
	3,4,5	Input	6	Out put
	9,10,11	Input	8	Out put

h. Name of the IC: **IC 7420, 4-Input NAND gate**

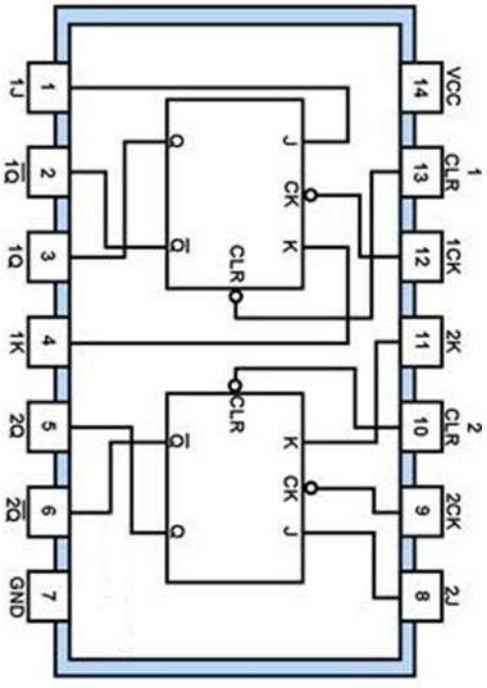
PIN diagram	PIN description			
	PIN no.	Function	PIN no.	Function
	7	Ground	14	+Vcc
	1,2,4,5	Input	6	Out put
	9,10,12,13	Input	8	Out put
	3,11	Not used	-	-

i. HD74LS78A Dual J-K Flip-Flops with Preset, Common Clear, and Common Clock



	PIN description			
	PIN no.	Function	PIN no.	Function
	3,14	1J, 1K	1	CLK
	13, 12	1Q, 1 $\overline{Q}$	4, 11	Vcc, Gnd
	7, 10	2K, 2J	2, 6	1PR, 2PR
	8, 9	2Q, 2 $\overline{Q}$	5	CLR

j. 74107 Dual Negative Edge triggered J-K Flip-Flops with Reset



	PIN description			
	PIN no.	Function	PIN no.	Function
	2,6	Output ($\overline{Q}$ A, $\overline{Q}$ B)	3,5	Output QA, QB
	12,9	CLKA, CLKB	13,10	Reset (RA,RB)
	1,8	Input (JA,JB)	7	GND
	4,11	Input (KA,KB)	14	Vcc

Experiment No. 02: Simulation of Digital Circuit in Proteus.

2.1 Objectives:

1. To learn the simulation of Digital Electronics circuit in Proteus.

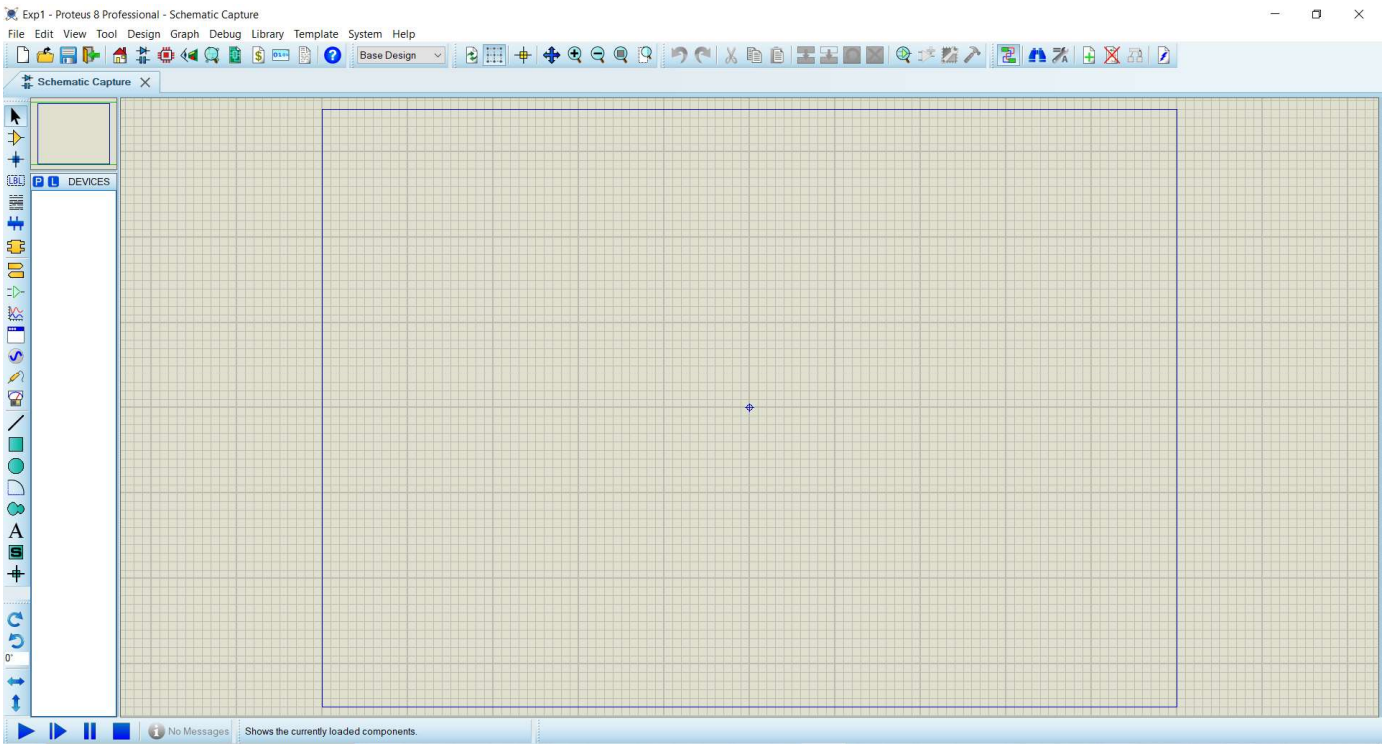
2.2 Experiment Requirements:

1. Computer
2. Proteus Software

2.3 Experiment Procedures:

2.3.1 Starting Simulation:

2.3.1.1 Install PROTEUS in your PC
2.3.1.2 Go to Start Manu> then open Proteus 8 Professional
2.3.1.3 After opening Proteus 8 Professional, you will see the following window
2.3.1.4 Then click *New Project* to create new project, after that you will see the following window.

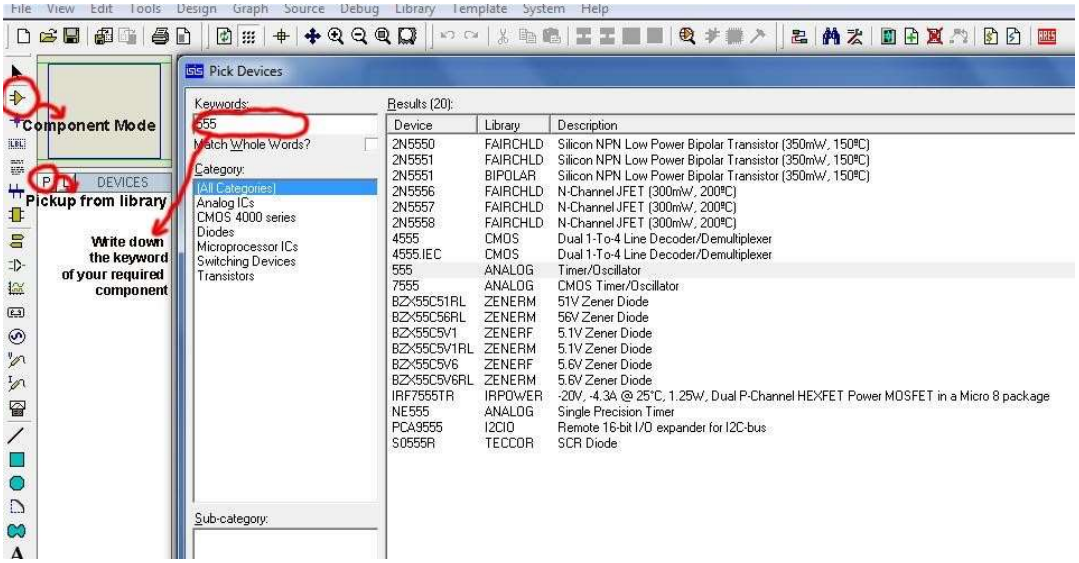


2.3.2 Circuit Construction & Assembly:

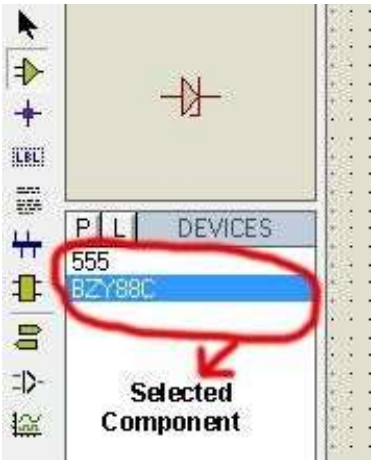
2.3.2.1 Select component mode

2.3.2.2 Click on Pick Device/Symbol or just click on "P" to pick component or device.

2.3.2.3 Write down the name of your component in the dialogue box known as "Keywords". All steps are shown in the following figure-



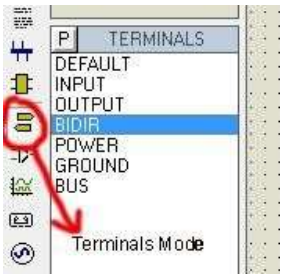
2.3.2.4 The selected component can be located on the left side window of the design diagram.



2.3.2.5 To put the component to the design sheet, just left click the component and put it to the sheet.

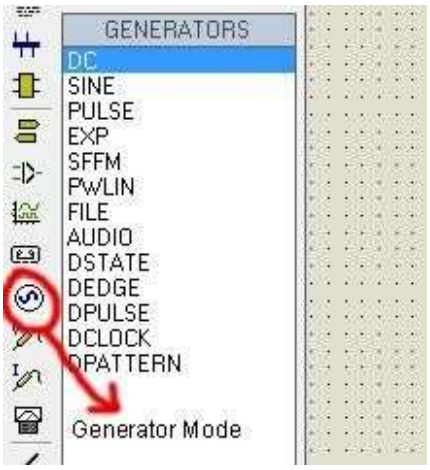
2.3.2.6 **To move the components**, simply right click on the component (the component will be red-lighted), and left click and drag the component to the desired location.

2.3.2.7 **Selection of power and ground terminals:** For power terminal and ground, the component is NOT selected from the library. Select the "terminals mode" icon at the left- side toolbar. Select POWER and GROUND terminals.



2.3.2.8 **Component Parameter Settings:** To edit the component, select the component (right- click) and left-click to open the Edit Component dialog. The dialog is different according to the devices. Set the parameters as your circuit requirement.

2.3.2.9 **Power source and signal input:** To supply circuit power and different input signals such as DC, SIN, PULSE, Clock and Audio etc select Generator Mode. You can also select voltage and current sources from library.



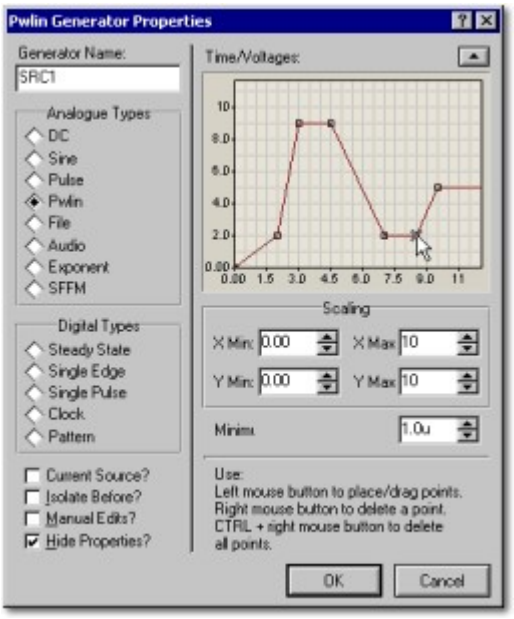
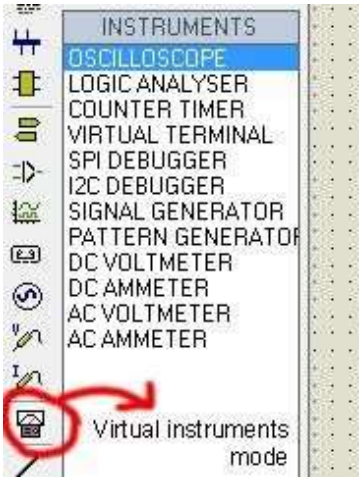


Fig: Piecewise Linear Generator Type.

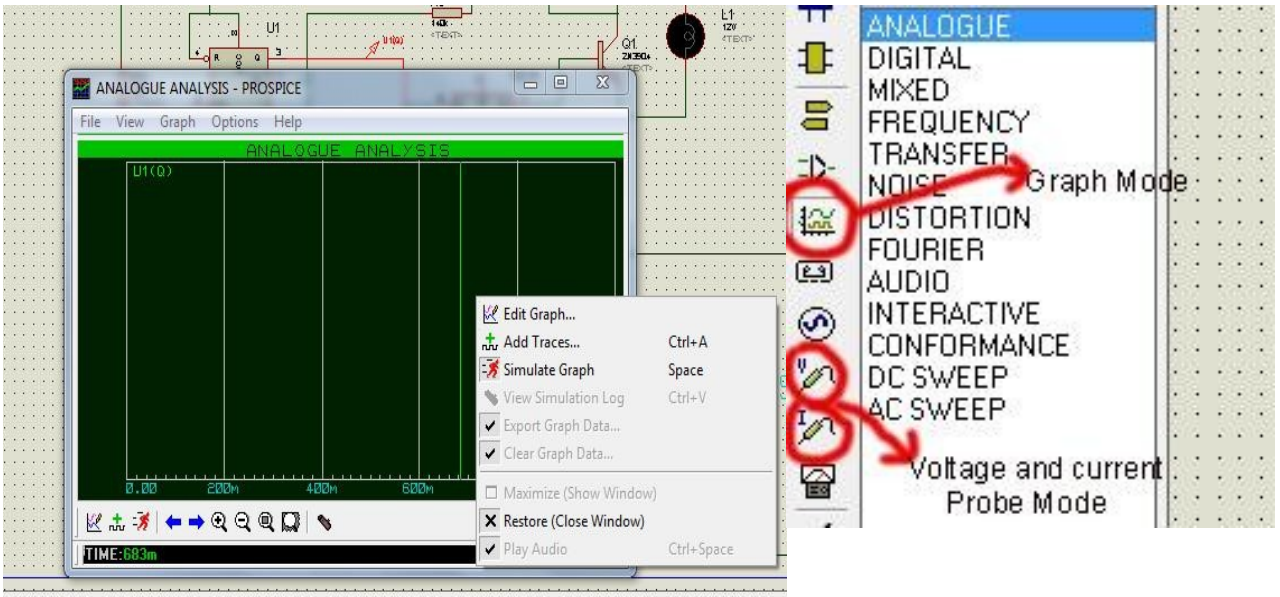
2.3.2.10 **Measuring Instruments:** To measure different parameters of the designed circuit select Virtual Instrument Mode. You will get oscilloscope, ammeter, voltmeter, signal generator etc in virtual instrument mode.



2.3.2.11 **Graphs:** To trace the graphs the following three modes are required.

a) Graph Mode.
b) Voltage Probe Mode.
c) Current Probe Mode.

Having drawn the schematic, you choose the type of circuit analysis you require (transient, frequency, noise, etc.) by placing a Graph of the appropriate type on the schematic. You can place as many graphs as you want and can even have several graphs of the same type if you wish. Graph types supported include: Analogue, Digital and Mixed transient graphs as well as Frequency, Transfer, Noise, Distortion, Fourier, AC Sweep and DC Sweep and Audio graphs. Set voltage probe or current probe to the circuit node or branch in which you want to see the graphs. Then drag the probe to graph box or right click the graph box to add probe parameter by "Add Traces" option. Finally right click the graph box and select "Simulate Graph" option.

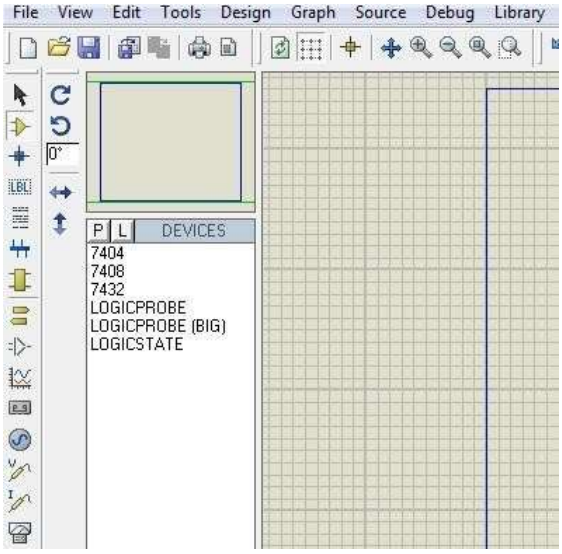


2.3.3 Simulation Example

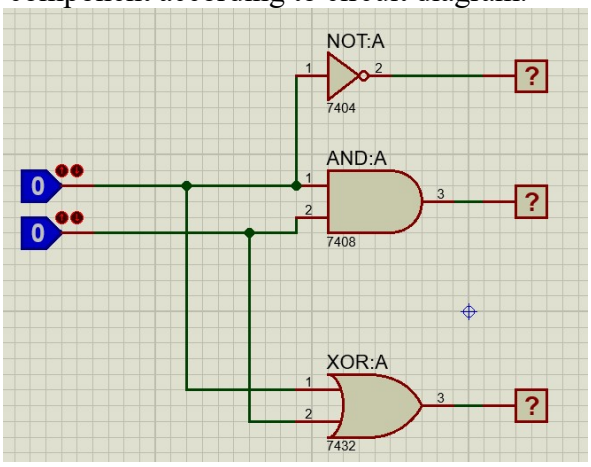
Example1. Simulation of different logic gates.

Step1: Pick the following components from component library.

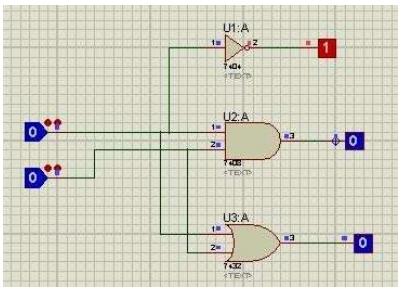
7408,7432,7404, Logic Probe, Logic State

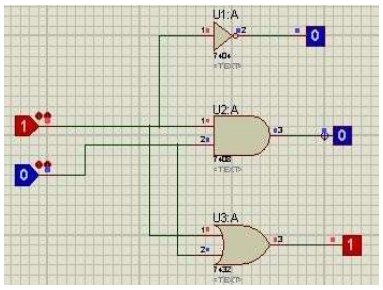


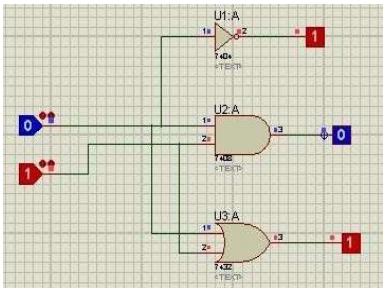
Step2: Place and connect the component according to circuit diagram.



Step3: Play and observe the output logic for different combination of input logic.







Experiment No. 03: Verification of operation of different Logic Gate IC (AND, OR, NOT, NAND, NOR and XOR).

3.1 Objectives:

1. To examine the operation of fundamental logic gates AND, OR, NOT, NAND, NOR, XOR and determine their logical properties.

2. To derive the truth tables of logic gates and verify their logic equations.

3.2 Circuit Diagrams:

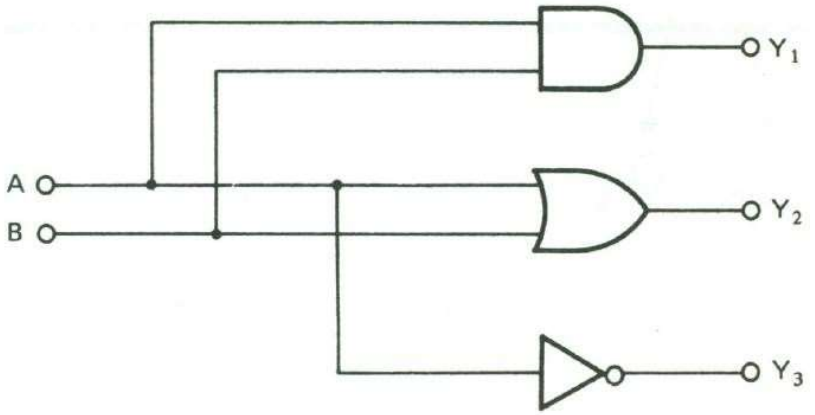


Figure 3.1: AND, OR and NOT gates

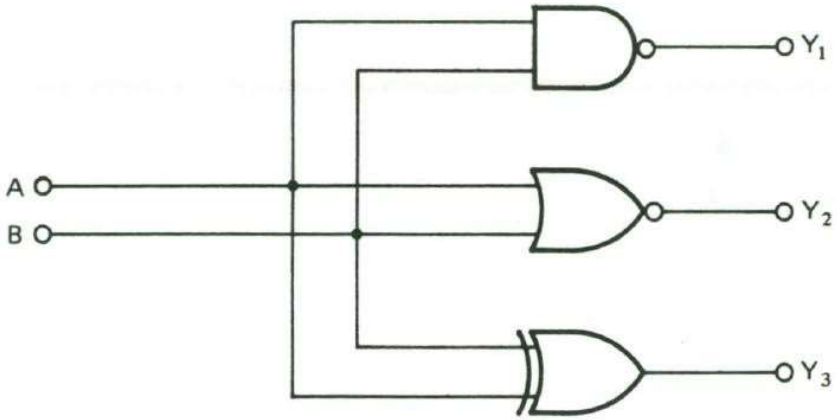
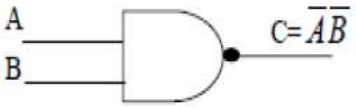
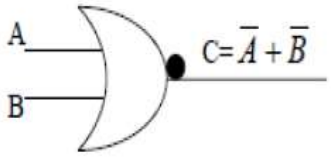
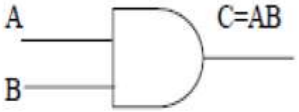
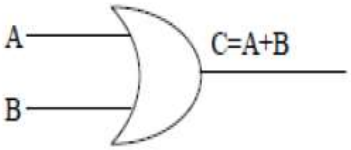
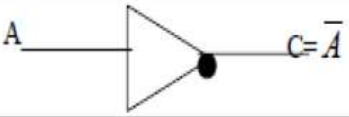
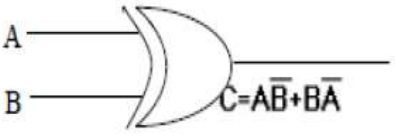


Figure 3.2: NAND, NOR and XOR gates

3.3 Truth Table of Logic Gates:

S.NO	GATE	SYMBOL	INPUTS		OUTPUT
			A	B	C
1.	NAND IC 7400		0	0	1
			0	1	1
			1	0	1
			1	1	0
2.	NOR IC 7402		0	0	1
			0	1	0
			1	0	0
			1	1	0
3.	AND IC 7408		0	0	0
			0	1	0
			1	0	0
			1	1	1
4.	OR IC 7432		0	0	0
			0	1	1
			1	0	1
			1	1	1
5.	NOT IC 7404		1	-	0
			0	-	1
6.	EX-OR IC 7486		0	0	0
			0	1	1
			1	0	1
			1	1	0

3.4 Experiment Requirements:

3.4.1 Digital Electronics Trainer Kit.
3.4.2 IC Tester.
3.3.3 IC (7404, 7408, 7432, 7400, 7402, 7486).
3.3.4 Multimeter.

3.5 Experiment Procedures:

3.5.1 Place the components of the circuit shown in figure 3.1 on the trainer board and link the connections correctly.

3.5.2 Use the data switches for input and LEDs for output.

3.5.3 Power on the trainer board.

3.5.4 Observe the outputs for different input configurations and fill in the data table.

3.5.5 Follow procedure 1 to 4 for circuit of figure 3.2.

3.5.6 Verify the truth tables and output equations obtained for different logic gates.

3.6 Data Table:

A	**B**	**Y_1 (Fig. 3.1)**	**Y_2 (Fig. 3.1)**	**Y_3 (Fig. 3.1)**	**Y_1 (Fig. 3.2)**	**Y_2 (Fig. 3.2)**	**Y_3 (Fig. 3.2)**
0	0						
0	1						
1	0						
1	1						
Output Equations							

3.7 Lab Report:

You are responsible for documenting your work and your report must include (at minimum) the following:

3.7.1 Cover sheet (Showing your Name, ID, Semester, Section, Exp. Name, Course Title, Course Code at least)
3.7.2 Objectives of the experiment.
3.7.3 List of Components.
3.7.4 Draw proper circuit diagrams and figures.
3.7.5 List the output of the circuit and include it with your report.
3.7.6 The circuit is working properly or not. If not, where did you think the errors lie?
3.7.7 Simulate the circuit in PROTEUS and attach simulation result in lab report.
3.7.8 Answer the following questions:
  3.7.8.1 How you can construct NAND and NOR gates using the basic logic gates AND, OR, NOT?
  3.7.8.2 Why NAND and NOR gates are called universal gate?
  3.7.8.3 Construct AND, OR and NOT gate by using NAND gate only. Also, construct these gates by using NOR gate only.

Experiment No. 04: Implementation of basic logic gates by diodes, transistors and resistors.

4.1 Objectives:

1. To examine the operation of diode-resistor (AND, OR) and transistor-resistor (NOT) logic gates and determine their logical properties.

2. To derive the truth tables of logic gates and verify their logic equations.

4.2 Circuit Diagrams:

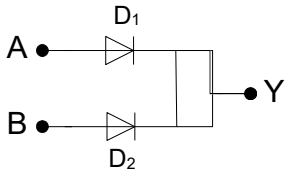


Figure 4.1: OR gate ($Y=A+B$)

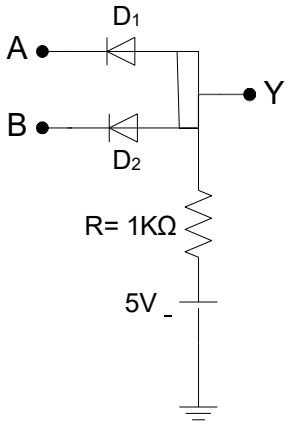


Figure 4.2: AND gate ($Y=A\cdot B$)

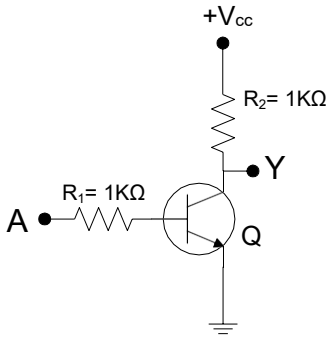


Figure 4.3: NOT gate ($Y=\overline{A}$)

4.3 Experiment Requirements:

4.3.1 Digital Electronics Trainer Kit.
4.3.2 IC Tester.
4.3.3 Diodes.
4.3.4 Transistors.
4.3.5 Resistor (1KΩ).

4.4 Experiment Procedures:

4.4.1 Place the components of the circuit shown in figure 4.1 on the trainer board and link the connections correctly.

4.4.2 Use the data switches for input and LEDs for output.

4.4.3 Power on the trainer board.

4.4.4 Observe the outputs for different input configurations and fill in the data table.

4.4.5 Follow procedure 1 to 4 for circuit of figure 4.2.

4.4.6 Follow procedure 1 to 4 for circuit of figure 4.3.

4.4.7 Verify the truth tables and output equations obtained for different logic gates.

4.5 Data Table:

A	B	Y (Fig. 4.1)	Y (Fig. 4.2)	Y (Fig. 4.3)
0	0			
0	1			
1	0			
1	1			
Output Equations				

4.6 Lab Report:

You are responsible for documenting your work and your report must include (at minimum) the following:

4.6.1 Cover sheet (Showing your Name, ID, Year, Semester, Exp. Name, Course Title, Course Code at least)
4.6.2 Objectives of the experiment.
4.6.3 List of Components.
4.6.4 Draw proper circuit diagrams and figures.
4.6.5 Discuss the function of every component that you have used to make the circuit.
4.6.6 List the output of the circuit and include it with your report.
4.6.7 The circuit is working properly or not. If not, where did you think the errors lie?
4.6.8 Simulate the circuit in PROTEUS and attach simulation result in lab report.
4.6.9 Answer the following questions :
    4.6.9.1 Draw the circuit diagram of a NOR gate using diodes, transistors and resistors.
    4.6.9.2 Draw the circuit diagram of a NAND gate using diodes, transistors and resistors.

Experiment No. 05: Implementation of Boolean function by basic logic gates.

5.1 Objectives:

1. To implement the given Boolean function and develop the truth table.

$$F = \acute{X}\acute{Y}Z + \acute{X}YZ + X\acute{Y}$$

2. To simplify the function and develop the truth table and verify it.

5.2 Logic Diagrams:

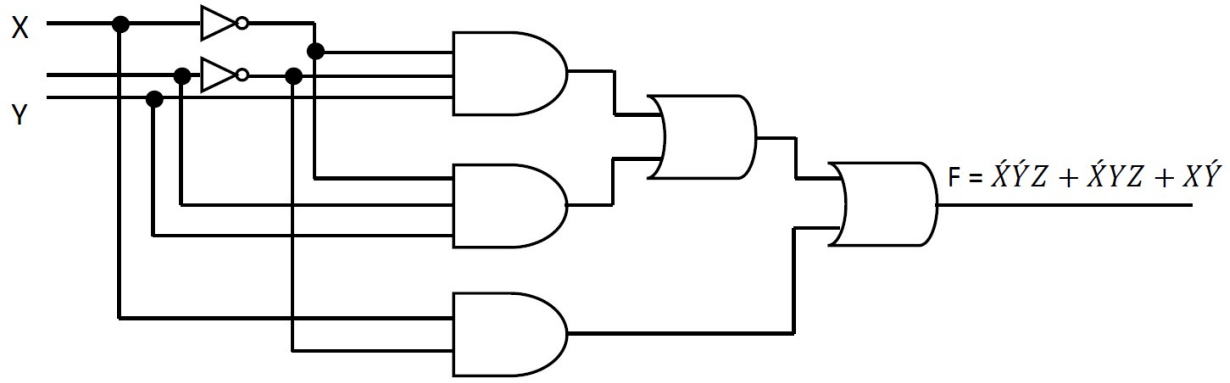


Figure 5.1: Logic diagram.

5.3 Experiment Requirements:

5.3.1 Digital Electronics Trainer Kit.
5.3.2 IC Tester
3. IC (7404, 7432, 7411, 7408).
4. Multimeter.

5.4 Experiment Procedures:

5.4.1 Place the components of the circuit shown in figure 5.1 on the trainer board and link the connections correctly.

5.4.2 Use the data switches for input and LEDs for output.

5.4.3 Power on the trainer board.

5.4.4 Observe the outputs for different input configurations and fill up the truth table.

5.4.5 Simplify the function to minimum number of literals.

5.4.6 Draw the logic diagram for simplified function.

5.4.7 Follow procedure 1 to 4 for the simplified logic diagram.

5.4.8 Verify the truth table obtained from the simplified logic diagram.

5.5 Truth Table:

X	Y	Z	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	
		Output Equations	

5.6 Lab Report:

You are responsible for documenting your work and your report must include (at minimum) the following:

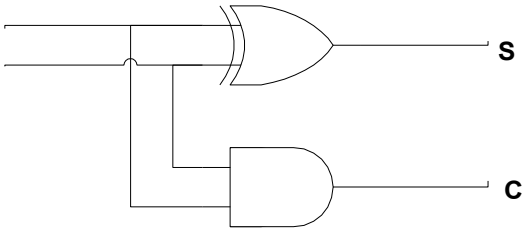
5.6.1 Cover sheet (Showing your Name, ID, Semester, Year, Exp. Name, Course Title, Course Code at least)
5.6.2 Objectives of the experiment.
5.6.3 List of Components.
5.6.4 Draw proper circuit diagrams and figures.
5.6.5 List the output of the circuit and include it with your report.
5.6.6 The circuit is working properly or not. If not, where did you think the errors lie?
5.6.7 Simulate the circuit in PROTEUS and attach simulation result in lab report.
5.6.8 Answer the following questions:
5.6.8.1 Draw the logic diagram for given Boolean function.
5.6.8.2 Discuss some important postulates of Boolean algebra.

Experiment No. 06: Implementation of a Half-adder and Full-adder.

6.1 Objectives:

1. To implement a Half-adder.
2. To implement a Full-adder by the help of Half-adders.

6.2 Logic Diagrams:



S = X Y and C = XY

Figure 6.1: Implementation of a Half-adder

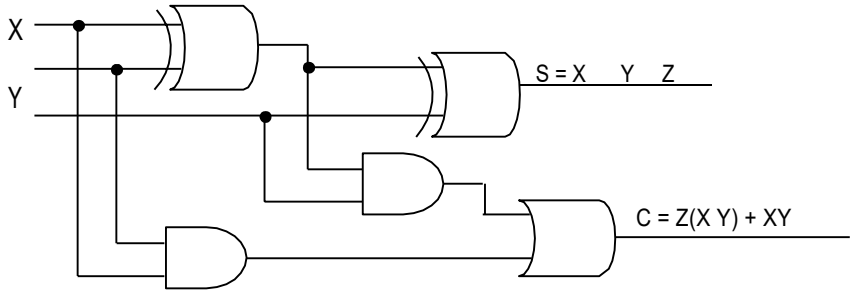


Figure 6.2: Implementation of a Full-adder with two half adder and an OR gate.

6.3 Experiment Requirements:

6.3.1 Digital Electronics Trainer Kit.
6.3.2 IC Tester
6.3.3 IC (7408, 7432, 7486).
6.3.4 Multimeter.

6.4 Experiment Procedures:

6.4.1 Place the components of the circuit shown in figure 6.1 on the trainer board and link the connections correctly.

6.4.2 Use the data switches for input and LEDs for output.

6.4.3 Power on the trainer board.

6.4.4 Observe the outputs for different input configurations and fill up the truth table.

6.4.5 Follow procedure 1 to 4 for the circuits shown in figure 6.2.

6.4.6 Verify the obtained truth tables with output Boolean functions.

6.5 Truth Tables:

For figure 6.1. (Half-adder)

X	***Y***	***S***	***C***
0	0		
0	1		
1	0		
1	1		
Output Equations			

For figure 6.2. (Full-adder)

X	***Y***	***Z***	***S***	***C***
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		
Output Equations				

6.6 Lab Report:

You are responsible for documenting your work and your report must include (at minimum) the following:

6.6.1 Cover sheet (Showing your Name, ID, Semester, Section, Exp. Name, Course Title, Course Code at least)
6.6.2 Objectives of the experiment.
6.6.3 List of Components.
6.6.4 Draw proper circuit diagrams and figures.
6.6.5 List the output of the circuit and include it with your report.
6.6.6 The circuit is working properly or not. If not, where did you think the errors lie?
6.6.7 Simulate the circuit in PROTEUS and attach simulation result in lab report.
6.6.8 Answer the following questions :
6.6.8.1 What do you mean by combinational circuit? Write down the procedure to design a combinational circuit.
6.6.8.2 Mention some application of combinational circuit.

Experiment No. 07: Familiarization with flip-flops.

7.1 Objectives:

1. To implement a R-S Flip-Flop.
2. To implement a D Flip-Flop.
3. To implement a JK Flip-Flop.
4. To implement a T Flip-Flop.

7.2 Logic Diagrams:

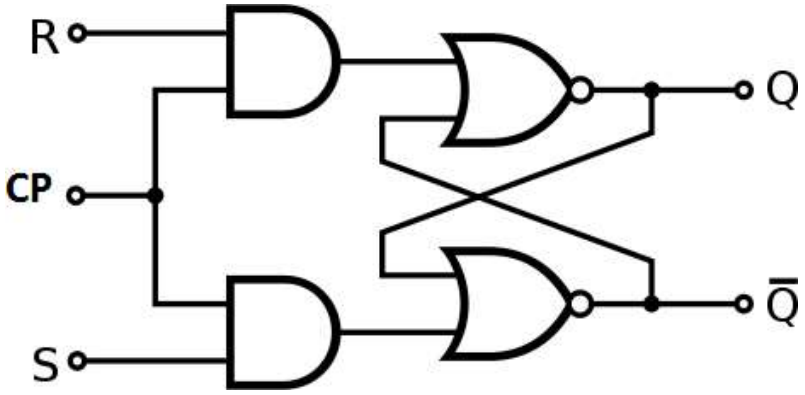


Figure 7.1: R-S Flip Flop

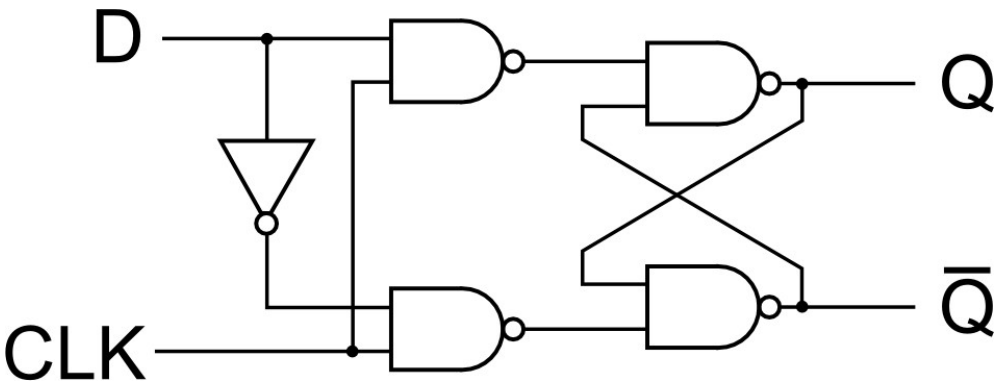


Figure 7.2: D Flip-Flop

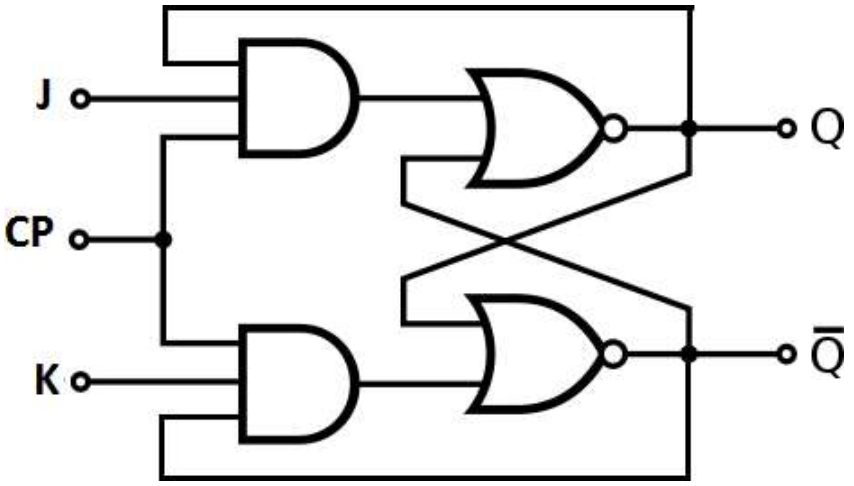


Figure 7.3: J-K Flip Flop

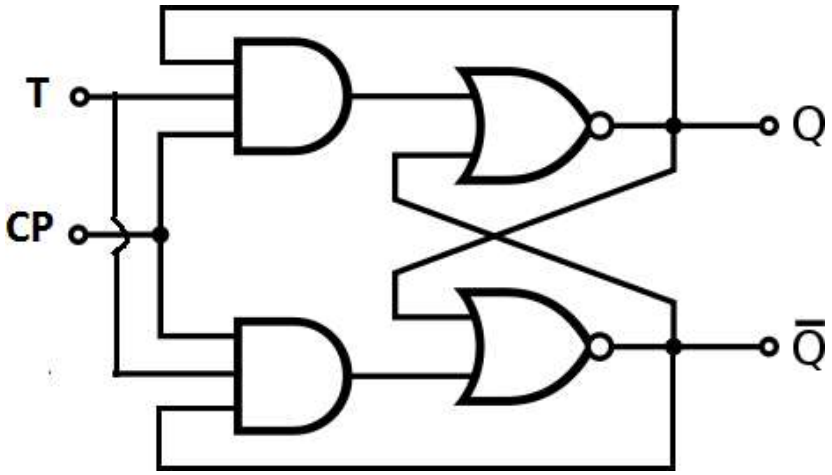


Figure 7.4: T Flip Flop

7.3 Experiment Requirements:

7.3.1 Digital Electronics Trainer Kit.
7.3.2 IC Tester
7.3.3 IC (7400, 7404, 7408, 7432).
7.3.4 Multimeter.

7.4 Experiment Procedures:

7.4.1 Place the components of the circuit shown in figure 8.1 on the trainer board and link the connections correctly.

7.4.2 Use the data switches for input and LEDs for output.

7.4.3 Power on the trainer board.

7.4.4 Observe the outputs for different input configurations and fill up the truth table.

7.4.5 Follow procedures 1 to 4 for the circuits shown in figure 8.2.

7.4.6 Follow procedures 1 to 4 for the circuits shown in figure 8.3.

7.4.7 Verify the obtained truth tables output Boolean functions.

7.5 Truth Tables:

For figure 7.1 (R-S Flip Flop)

Q(t)	C	S	R	Q(t+1)	Q´(t+1)	Remarks
	0	0	0			
	0	0	1			
	0	1	0			
	0	1	1			
	1	0	1			
	1	0	0			
	1	1	1			
	1	1	0			
	1	0	0			
	1	1	1			
Output Equations						

For figure 7.2. (D Flip-Flop)

Q(t)	C	D	Q(t+1)	Q´(t+1)	Remarks
	0	0			
	0	1			
	1	1			
	1	0			
	1	1			
	1	0			
Output Equations					

For figure 7.3. (JK Flip-Flop)

Q(t)	C	J	K	Q(t+1)	Q´(t+1)	Remarks
	0	0	0			
	0	0	1			
	0	1	0			
	0	1	1			
	1	0	1			
	1	0	0			
	1	1	1			
	1	1	0			
	1	0	0			
	1	1	1			
Output Equations						

For figure 7.4. (T Flip-Flop)

Q(t)	C	T	Q(t+1)	Q´(t+1)	Remarks
	0	0			
	0	1			
	1	1			
	1	1			
	1	1			
	1	0			
	1	0			
Output Equations					

7.6 Lab Report:

You are responsible for documenting your work and your report must include (at minimum) the following:

7.6.1 Cover sheet (Showing your Name, ID, Semester, Section, Exp. Name, Course Title, Course Code at least)

7.6.2 Objectives of the experiment.

7.6.3 List of Components.

7.6.4 Draw proper circuit diagrams and figures.

7.6.5 List the output of the circuit and include it with your report.

7.6.6 The circuit is working properly or not. If not, where did you think the errors lie?

7.6.7 Simulate the circuits in PROTEUS and attach simulation result in lab report.

7.6.8 Answer the following questions :

7.6.8.1 What is sequential circuit? Differentiate between combinational and sequential circuit.

7.6.8.2 What is the difference between latch and flip-flop?

7.6.8.3 How can you convert a D flip-flop into J-K Flip-flop and T Flip Flop?

7.6.8.4 How can you convert a J-K flip-flop into D and T flip-flop?

7.6.8.5 Suppose that there are 4 floors in a building. There is a light in the main gate of the building. Design a digital logic circuit such that persons from any floor will be able to ON or OFF the light.