High Density Memory Compiler Power Gating Application Note

Confidential

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ARM PAN 0038A

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Proprietary Notice

Confidentiality Status

Revision History.

Part Number	Date	Comments
ARM PAN 0038A	6 May 2010	First release

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1 Overview

This document provides details about the memory compiler power gating modes - standby, data retention, and power down. Various configurations provide different results to help you achieve extremely low power while still meeting your system performance requirements.

The following terms are used in this section:

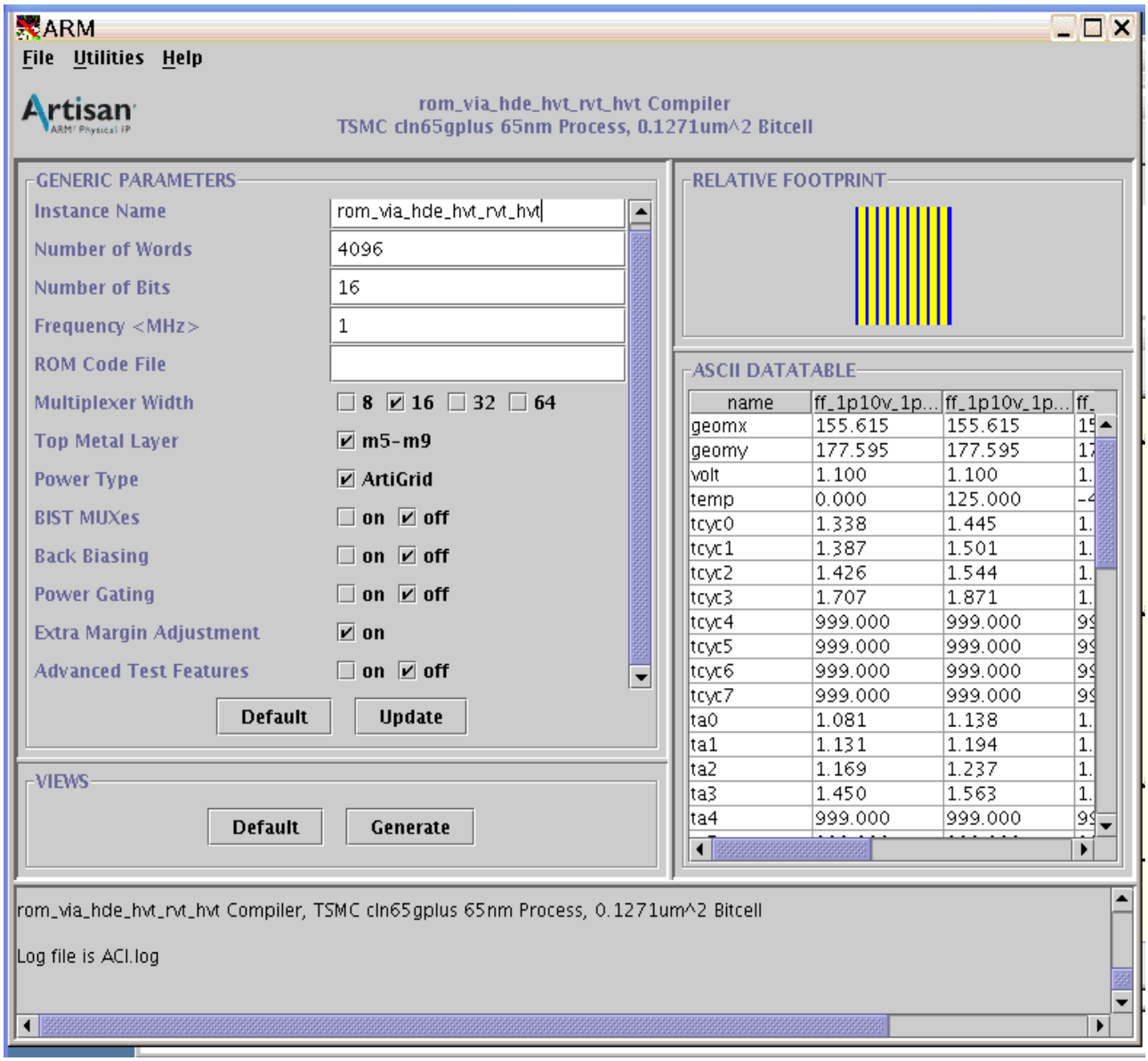
- Power Gating – a technique that uses HV_T transistors to isolate local power from the global power supply.
- Power terminals –
  VDD is the common power supplied to the memory instance
  VSS is the common ground supplied to the memory instance
  VDDC/VDDCE are the VDD supplied to the core array
  VDDP/VDDPE are the VDD supplied to the peripheral circuitry
- PGEN – Power mode enable, active low
- RETN – Retention mode enable, active low
- Output pin clamping - when in retention mode, the output pins are clamped to ground

1.1 General Configuration

Power gating can be external to the memory or integrated into the memory instance. For integrated power gating, the power gating is part of the memory instance as opposed to outside of the memory instance (as in external power gating).

Integrated power gating is accomplished by selecting the GUI Power Gating option to “on” as part of the overall GUI setup. See Figure 1 for the relative position of the Power Gating option on the GUI.

Figure 1. Sample Compiler GUI



The power gating feature is only supported with the power ring structure.

For 65nm SRAM and Register file compilerss, VDDCE is the VDD supplied to the core array and VDDPE is the VDD supplied to the peripheral circuitry.

2 Rings Based Power Gating

Figure 2 shows the basic arrangement for standard option ring power routing. A standard option is considered to have no features (BIST mux, pipeline, redundancy, etc.) selected.

Figure 2. Ring Based Power Routing; power_gate = off

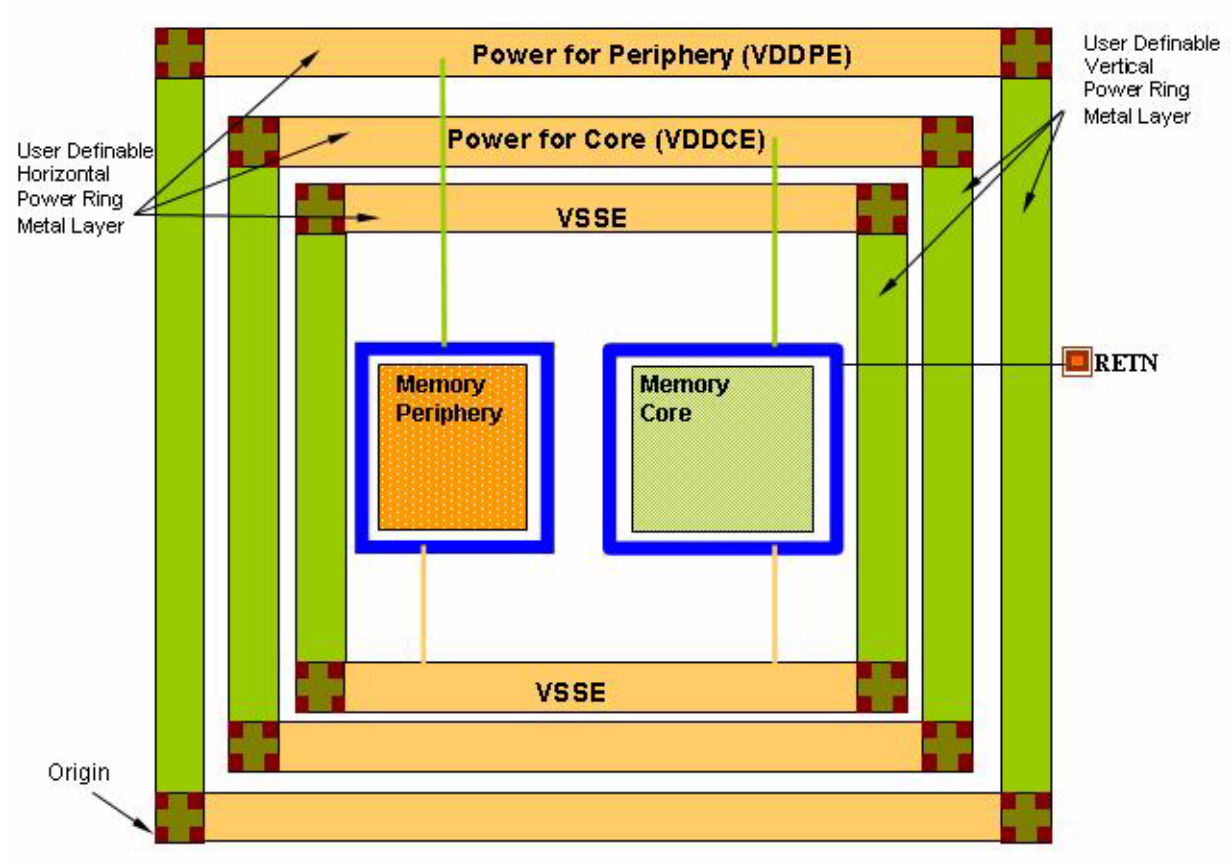
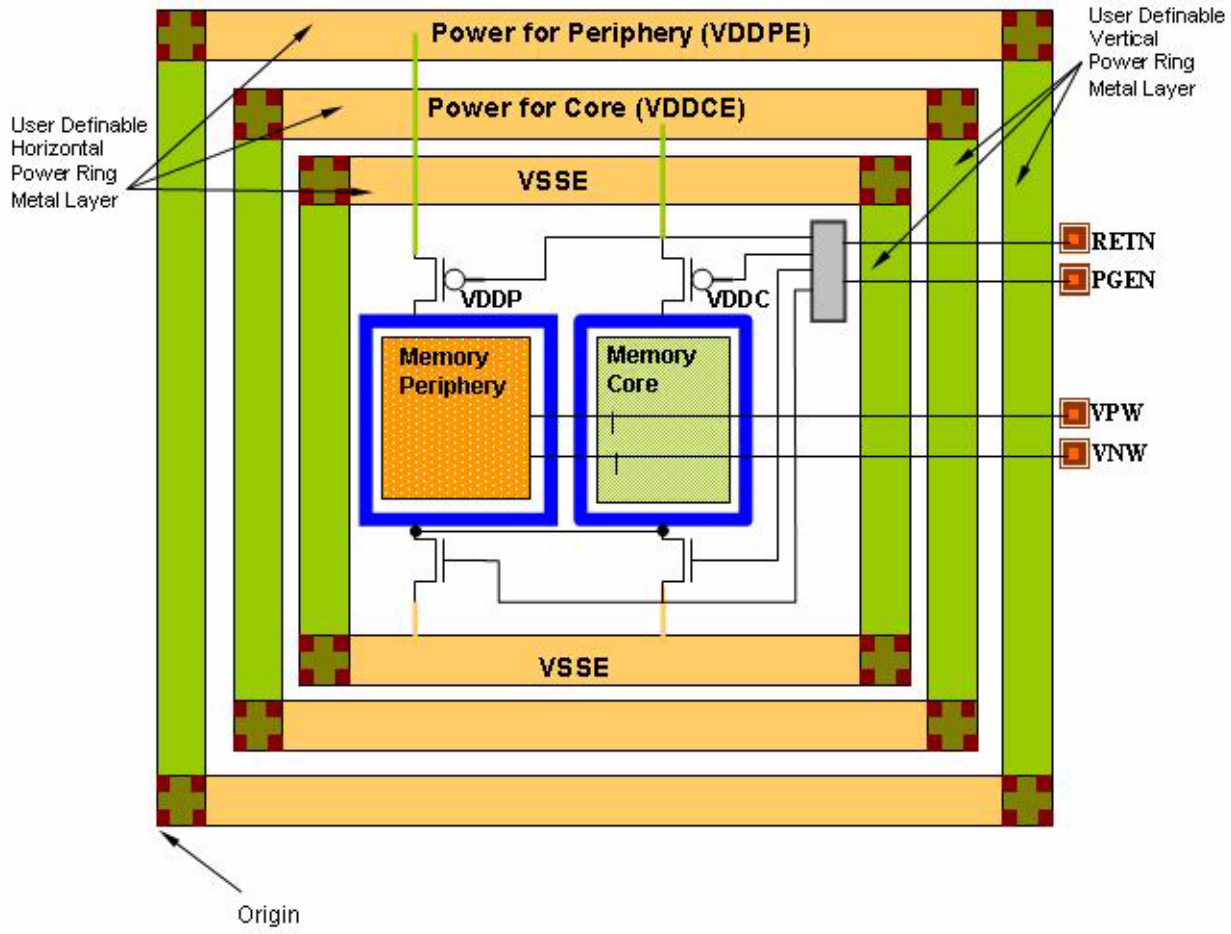


Figure 3 shows the basic arrangement for power gating option ring power routing.

Figure 3. Ring Based Power Routing; power_gate = on



3 Power Configuration

Table 1: Power Configurations and Operational Modes 65nm

Compilers	GUI	Standby Mode	Data Retention Mode	Power Down Mode	Power Supply	Configuration
SRAM-SP	Power-gating = off	x	x		VDDCE, VDDPE, VSSE	External Power Gating
	Power-gating = on	x	x	x	VDDCE, VDDPE, VSSE	Integrated Power Gating
SRAM-DP	Power-gating = off	x	x		VDDCE, VDDPE, VSSE	External Power Gating
	Power-gating = on	x	x	x	VDDCE, VDDPE, VSSE	Integrated Power Gating
RF-SP	Power-gating = off	x	x		VDDCE, VDDPE, VSSE	External Power Gating
	Power-gating = on	x	x	x	VDDCE, VDDPE, VSSE	Integrated Power Gating
RF-2P	Power-gating = off	x	x		VDDCE, VDDPE, VSSE	External Power Gating
	Power-gating = on	x	x	x	VDDCE, VDDPE, VSSE	Integrated Power Gating
ROM	Power-gating = off	x			VDD, VSS	Standard
	Power-gating = on	x		x	VDD, VSS	Integrated Power Gating

In the External Power Gating configuration, the core and peripheral power terminals are split but power gating switches are external to the memory. The PGEN and RETN signals enable the different modes in this configuration.

Table 2: Power Configurations and Operational Modes 90nm

Compilers	GUI	Standby Mode	Data Retention Mode	Power Down Mode	Power Supply	Configuration
SRAM-SP	Power-gating = off; retention = off	x			VDD,VSS	Standard
	Power-gating = off; retention = on	x	x		VDDC,VDDP,VSS	External Power Gating
	Power-gating = on; retention = on	x	x	x	VDD,VSS	Integrated Power Gating
SRAM-DP	Power-gating = off; retention = off	x			VDD, VSS	Standard
	Power-gating = off; retention = on	x	x		VDDC,VDDP,VSS	External Power Gating
	Power-gating = on; retention = on	x	x	x	VDD,VSS	Integrated Power Gating
RF-SP	Power-gating = off; retention = off	x			VDD, VSS	Standard
	Power-gating = off; retention = on	x	x		VDDC,VDDP,VSS	External Power Gating
	Power-gating = on; retention = on	x	x	x	VDD,VSS	Integrated Power Gating
RF-2P	Power-gating = off; retention = off	x			VDD, VSS	Standard
	Power-gating = off; retention = on	x	x		VDDC,VDDP,VSS	External Power Gating
	Power-gating = on; retention = on	x	x	x	VDD,VSS	Integrated Power Gating
ROM	Power-gating = off	x			VDD,VSS	Standard
	Power-gating = on	x		x	VDD, VSS	Integrated Power Gating

The memory is in the Standard configuration when the core and power terminals are not split. In the External Power Gating configuration, the core and peripheral power terminals are split but power gating switches are external to the memory. The Integrated Power Gating configuration internally splits the core and peripheral power terminals but the external interface shows only one common VDD and VSS. The PGEN and RETN signals enable the different modes in this configuration.

4 Pin Description

Table 3 shows how to reach the different power management modes for SRAM-SP, SRAM-DP, RF-SP, and RF-2P when power gating is “on.” The memory instance has to go into Power Down Transition mode prior to going into the Data Retention mode.

Table 3: Power Management Mode Access - Power Gating = ON

Power Management Mode	CEN	PGEN	RETN	Power to Core	Power to Periphery
Standby	H	L	H	Yes	Yes
Power Down Transition	H	L	L	Yes	Yes
Data Retention	H	H	L	Yes	No
Power Down	H	H	H	No	No
Normal Operation	L	L	H	Yes	Yes
	L	H	L	Illegal	Illegal

Table 4 shows how to reach the different power management modes for SRAM-SP, SRAM-DP, RF-SP, and RF-2P when power gating is “off.” Please note that in this configuration there is no PGEN pin available.

Table 4: Power Management Mode Access - Power Gating = OFF

Power Management Mode	CEN	RETN	Power to Core	Power to Periphery
Standby	H	H	Y (EXT)	Y (EXT)
Data Retention	H	L	Output = 0; Y (EXT)	N (EXT)
Power Down	H	H	N (EXT)	N (EXT)
Normal Operation	L	H	Y	Y
	L	L	Illegal	Illegal

There are no Data Retention or Transition modes for the ROM. See page 12.

Table 5: ROM Power Management Mode Access

Power Management Mode	CEN	PGEN	Power to Periphery
Standby	H	L	Y
Power Down	H	H	N
Normal	L	L	Y

Table 6: Power Gating Support Pins

Name	Type	Description	Note
RETN	Input	Retention mode enable (Active low)	1
PGEN	Input	Power down mode enable 1 = power down, 0 = normal	

1 When PGEN = 0, RETN active starts clamping the output to ground. RETN active with PGEN = 1; memory is in retention mode

5 Timing

The timing relationship between the PGEN and RETN pins in the SRAM and Register File compilers is shown in Tables 7 and 8 as well as Figures 4 and 5. Refer to the postscript datasheet or ASCII datatable for your compiler for instance-specific timing values. The chip enable CEN must be set to “high” (inactive) before going into retention mode or power down mode. The CEN must remain in “high” during retention and power down.

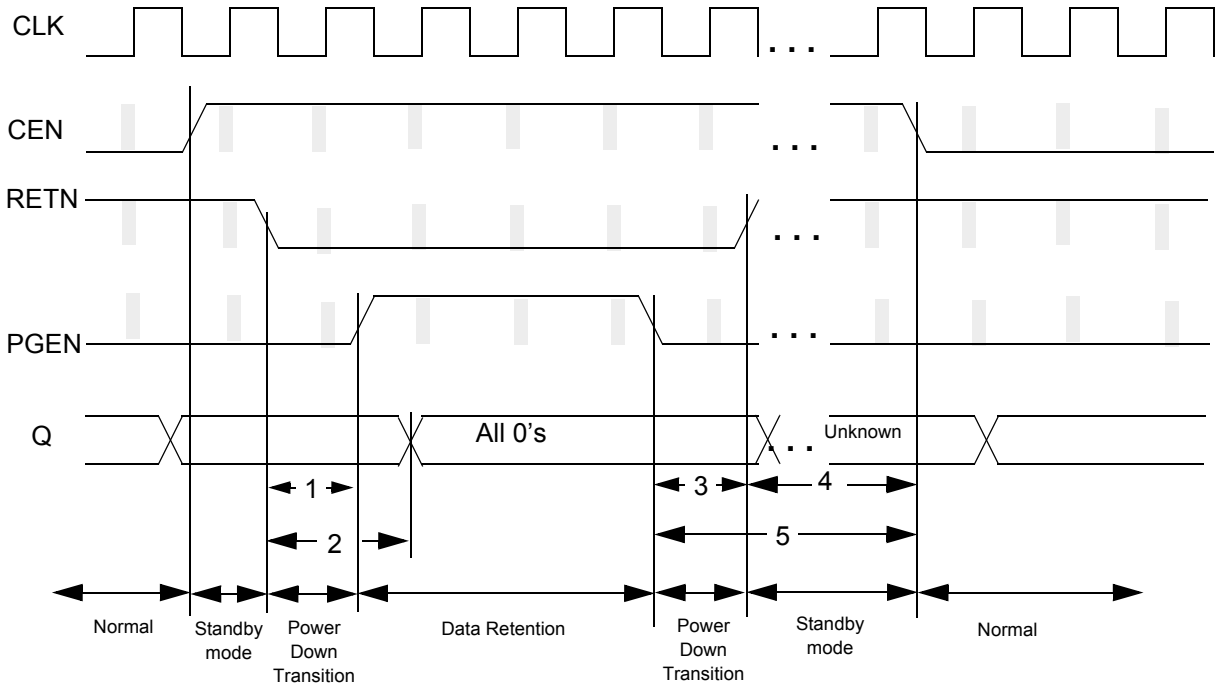
There is a power sequence when the memory is put from active to retention and back to active. Before going into retention, the memory needs to be in standby mode by setting CEN = 1 (PGEN = 0, RETN = 1). Once this is accomplished, set the RETN = 0 (CEN = 1, PGEN = 0). The power still supplied to memory core and periphery. At this moment, the memory is in transition mode.

When PGEN = 1 (CEN = 1, RETN = 0), the power to the periphery is cut off but there is power to the core. This puts the memory in retention mode. Before going into active mode, the memory needs to be in transition mode and then standby mode.

Table 7: Data Retention Mode - Integrated Power Gating: SRAM-SP, SRAM-DP, RF-SP, RF-2P

Mode	Delay Parameter	Description
Integrated Power Gating	t_{pgen_retnh}	RETN falling to PGEN rising, hold time
	t_{retn_pgenh}	PGEN falling to RETN rising, hold time
	t_{retnq}	RETN falling to Output clamped to zeros
	t_{cen_retnh}	RETN falling to chip enabled, hold time
	t_{cen_pgenh}	PGEN falling to chip enabled, hold time
	$t_{cen\_retsetup}$	CEN rising to RETN falling

Figure 4. Integrated Power Gating Timing: SRAM-SP, SRAM-DP, RF-SP, RF-2P



= CEN, PGEN, and RETN have setup and hold (S/H) window with respect to CLK

1: t_{pgen_retnh}

2: t_{retnq}

3: t_{retn_pgenh}

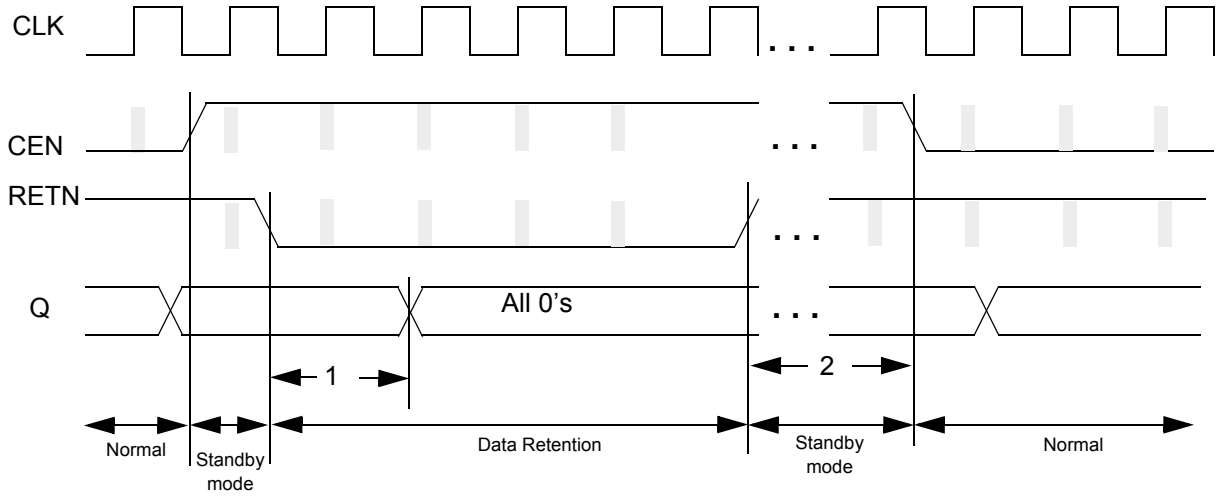
4: t_{cen_retnh}

5: t_{cen_pgenh}

Table 8: Data Retention Mode - External Power Gating: SRAM-SP, SRAM-DP, RF-SP, RF-2P

Mode	Delay Parameter	Description
External Power Gating	t_{retnq}	RETN falling to output clamped to zeros
	t_{cen_retnh}	RETN rising to chip enabled, hold time

Figure 5. External Power Gating Timing: SRAM-SP, SRAM-DP, RF-SP, RF-2P



= CEN and RETN have setup and hold (S/H) window with respect to CLK

1: t_{retnq}

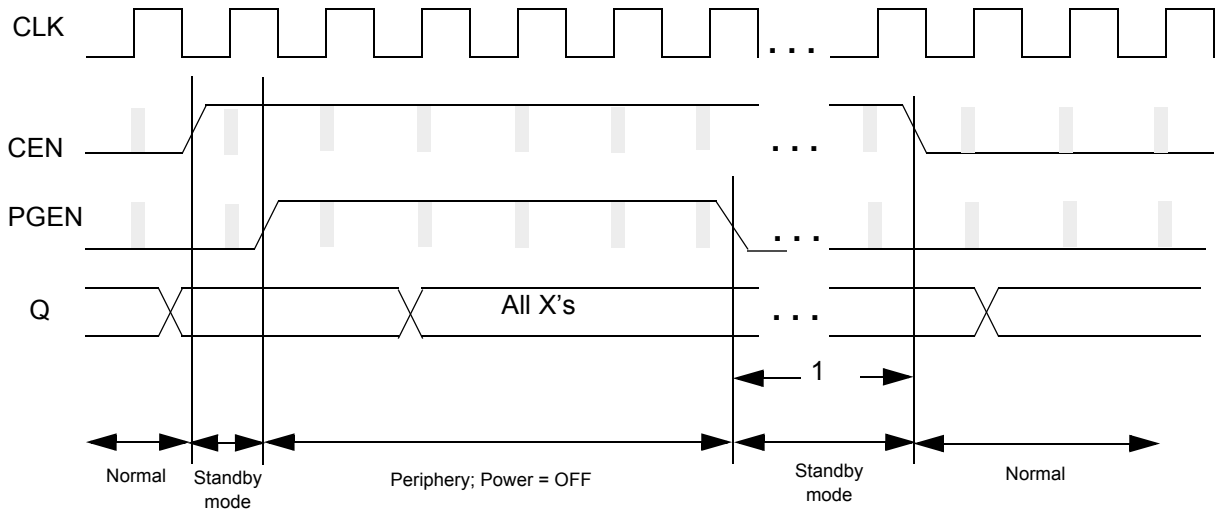
2: t_{cen_retnh}

The timing relationship between the PGEN and CEN pins in the ROM compiler is shown inTable 9 and Figure 6. Refer to the postscript datasheet or ASCII datatable for your compiler for instance-specific timing values.

Table 9: Power Down Mode: ROM - Power Gating = ON

Mode	Delay Parameter	Description
Power Gating	t_{cen_pgenh}	PGEN inactive to chip enabled, hold time

Figure 6. PGEN - CEN Timing: ROM



= CEN and PGEN have setup and hold (S/H) window with respect to CLK 1: t_{cen_pgenh}

Appendix A- Revisions

This appendix describes the technical changes between released issues of this bookIssue A

Table A-1. Issue A

Change	Location	Affects
No change, first release	-	-