High Density 65nm/90nm Low Power Memory Compiler Application Note

Confidential

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Proprietary Notice

Confidentiality Status

Revision History

Part Number	Comments
app_metro_lp_2005q3v1	Initial release
app_metro_lp_2005q3v2	Update delay parameters and descriptions
app-metro-lp-2006q1v1	Add confidentiality material and format upgrade
app-metro-lp-2006q2v1	Update Table 1 heading
app-metro-lp-2006q3v1	Updated power configurations and operational modes
app-metro-lp-2007q2v1	Update copyright and preface
app-metro-lp-2007q3v1	Update retention description
app-metro-lp-2008q2v1	Update Table 3
app-metro-lp-2008q4v1	Add a comprehensive description of low power operating modes, add t_{retn_cenh} and t_{pgen_cenh} delay parameters.
ARM PAN 0031A	Replaced Metro product name with high density, updated copyright information and added revision appendix page.

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Typographic Conventions

The following typographic conventions are used to assist you in distinguishing special notations, values, and elements described in this manual.

Visual Cue	Meaning
(Bullet) •	Bulleted list of important items.
`Courier Type`	Commands typed on the keyboard, either examples or instructions.
Dash (-) `Courier Type`	Text set in Courier type and preceded by a dash represents a command name (for example, -`libname`).
<italic type> *italic type*	Variable names you select, such as file and directory names are enclosed within angle brackets (< >). Italic type is used to show variable values, file, and directory names.
(Ellipsis) …	Indicates commands or options that may be added.
Italic Type with Initial Capital Letters	Document, chapter, section and reference manual names.

This document provides details about the high density memory compiler power down modes - standby, data retention, and power down. Various configurations provide different results to help you achieve extremely low power while still meeting your system performance requirements.

The following terms are used in this section:

- Power Gating – a technique that uses HV_T transistors to isolate local power from the global power supply.
- Power terminals –
  VDD is the common power supplied to the memory instance
  VSS is the common ground supplied to the memory instance
  For 90nm compilers and 65nm ROM compilers all VDDC is the VDD supplied to the core array
  For VDDP is the VDD supplied to the peripheral circuitry
  When pwr_gnd_rename renames powers into the same VDD, two rings are generated. When this happens, RETN needs to be tied high.
- PGEN – Power gating enable, active low
- RETN –
  Retention mode enable, active low
  Tie RETN to high when powers are renamed to the same name.
  high density v1.0: on, off, default off; retention is defaulted to on when power gating is on and can be on or off when power gating is off
  high density v1.2: retention is always on
- Output pin clamping - when in retention mode, the output pins are clamped to ground

Power gating is a technique that uses header, footer, or a combination of both to isolate local power from the global power. Internal power gating (header, footer and combo) is an option provided in the ARM compiler. You can opt for either internal or external power gating. With the internal power gating option, ARM pre-determines power, performance, and other key features. With the external power gating option, you determine key feature settings.

Power gating has three (3) available operating modes. Selection of a mode is controlled by the PGEN and RETN pins.

- Standby mode: As shown in Table 1, this is the standby mode where VDD and VSS are the power pins. The core and the power terminals are not split.
- Data retention mode: When power gating is external to the memory, only RETN pins are needed and the power gating PGEN pin is not required. Therefore, the PGEN pin is not available.
- Power gating mode: This mode is when power gating is internal to the memory. This mode requires both PGEN and RETN pins to go into power down transition mode prior to going into data retention mode. The RETN transistor should be enabled first. Then disable the PGEN transistor to retain data.

Power gating can be external to the memory or integrated into the memory instance. For integrated power gating, the power gating is part of the memory instance as opposed to outside of the memory instance (as in external power gating). Tables 1 and 2 show power configurations and operational modes for all high density memory compilers.

For 65nm SRAM and Register file compilers, VDDCE is the VDD supplied to the core array and VDDPE is the VDD supplied to the peripheral circuitry.

In 65nm integrated power, the core and periphery power terminals are split and the pins are external. See Table 1.

Table 1: Power Configurations and Operational Modes 65nm

compiler	Configuration	Standby Mode	Data Retention Mode	Power Down Mode	Power Supply
SRAM-SP	Standard	x			VDD, VSS
	External Power Gating	x	x		VDDCE, VDDPE, VSSE
	Integrated Power Gating	x	x	x	VDDCE, VDDPE, VSSE
SRAM-DP	Standard	x			VDD, VSS
	External Power Gating	x	x		VDDCE, VDDPE, VSSE
	Integrated Power Gating	x	x	x	VDDCE, VDDPE, VSSE
RF-SP	Standard	x			VDD, VSS
	External Power Gating	x	x		VDDCE, VDDPE, VSSE
	Integrated Power Gating	x	x	x	VDDCE, VDDPE, VSSE
RF-2P	Standard	x			VDD, VSS
	External Power Gating	x	x		VDDCE, VDDPE, VSSE
	Integrated Power Gating	x	x	x	VDDCE, VDDPE, VSSE
ROM	Standard	x			VDD, VSS
	Integrated Power Gating	x		x	VDD, VSS

The memory is in the Standard configuration when the core and power terminals are not split. In the External Power Gating configuration, the core and power terminals are split but power gating switches are external to the memory. The PGEN and RETN signals enable the different modes in this configuration.

Table 2: Power Configurations and Operational Modes 90nm

compiler	Configuration	Standby Mode	Data Retention Mode	Power Down Mode	Power Supply
SRAM-SP	Standard	x			VDD,VSS
	External Power Gating	x	x		VDDC,VDDP,VSS
	Integrated Power Gating	x	x	x	VDD,VSS
SRAM-DP	Standard	x			VDD, VSS
	External Power Gating	x	x		VDDC,VDDP,VSS
	Integrated Power Gating	x	x	x	VDD,VSS
RF-SP	Standard	x			VDD, VSS
	External Power Gating	x	x		VDDC,VDDP,VSS
	Integrated Power Gating	x	x	x	VDD,VSS
RF-SP	Standard	x			VDD, VSS
	External Power Gating	x	x		VDDC,VDDP,VSS
	Integrated Power Gating	x	x	x	VDD,VSS
ROM	Standard	x			VDD,VSS
	Integrated Power Gating	x		x	VDD, VSS

The memory is in the Standard configuration when the core and power terminals are not split. In the External Power Gating configuration, the core and power terminals are split but power gating switches are external to the memory. The Integrated Power Gating configuration internally splits the core and periphery power terminals but the external interface shows only one common VDD and VSS. The PGEN and RETN signals enable the different modes in this configuration.

Table 3 shows how to reach the different power management modes for SRAM-SP, SRAM-DP, RF-SP, and RF-2P when power gating is integrated into the memory instance. The memory instance has to go into Power Down Transition mode prior to going into the Data Retention mode.

Table 3: Power Management Mode Access - Memory Instance Internal

Power Management Mode	CEN	PGEN	RETN
Standby	H	L	H
Data Retention	H	H	L
Power Down	H	H	H
Power Down Transition	H	L	L

Table 4 shows to reach the different power management modes for SRAM-SP, SRAM-DP, RF-SP, and RF-2P when power gating is external to the memory instance. Please note that in this configuration there is no PGEN pin available.

Table 4: Power Management Mode Access - Memory Instance External

Power Management Mode	CEN	RETN
Standby	H	H
Data Retention	H	L
Power Down	H	H

There are no Data Retention or Transition modes for the ROM.

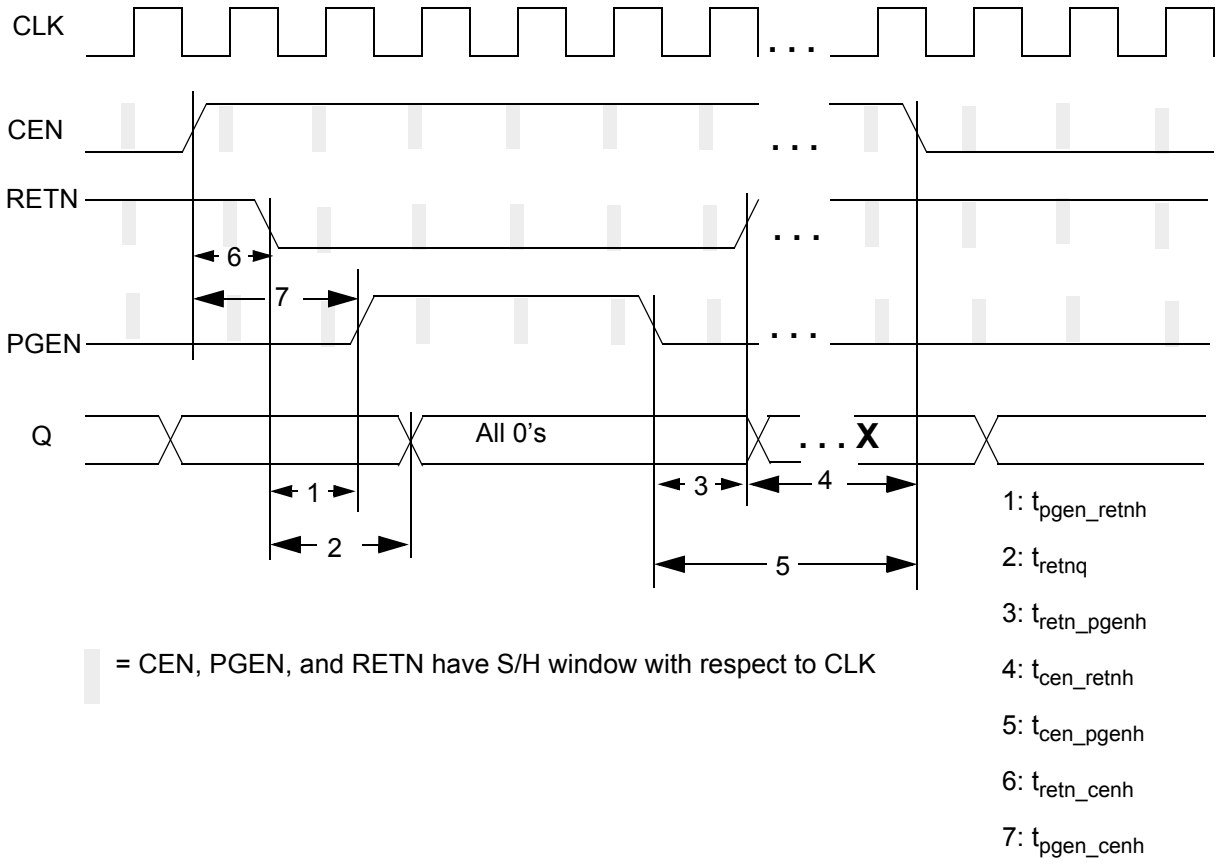
Block diagram of the Memory instance with PGEN, RETN, and power rings. We can choose the diagram from the product specs PDF document where the Program managers normally keep in the project directory.

The timing relationship between the PGEN and RETN pins in the SRAM and Register File compilers is shown in the Tables 5 and 6 , and Figures 1 and 2 . Refer to the postscript datasheet or ASCII datatable for your compiler for instance-specific timing values.

Table 5: Data Retention Mode - Integrated Power Gating: SRAM-SP, SRAM-DP, RF-SP, RF-2P

Mode	Delay Parameter	Description
Integrated Power Gating	t_{pgen_retnh}	RETN active to PGEN active, hold time
	t_{retnq}	RETN active to Output clamped to zeros
	t_{retn_pgenh}	PGEN inactive to RETN inactive, hold time
	t_{cen_retnh}	RETN inactive to chip enabled, hold time
	t_{cen_pgenh}	PGEN inactive to chip enabled, hold time
	t_{retn_cenh}	CEN disable to RETN active, hold time
	t_{pgen_cenh}	CEN disable to PGEN active, hold time

Figure 1: Integrated Power Gating Timing: SRAM-SP, SRAM-DP, RF-SP, RF-2P



Regarding the waveform timing window legend in Figure 1:

(1) `tpgen_retnh`: This maintains the data in the core. You first switch on a weak supply to the core (RETN). This retains the data. Then, the PGEN is switched off.

(2) `tretnq`: When RETN is active, output is clamped to zeros.

(3) `tretn_pgenh`: This ensures that the data is retained during this transition mode when PGEN goes low as RETN goes high. Memory enters an active cycle. Turn ON the PGEN first, then turn OFF the RETN.

(4) `tcen_retnh`: RETN to CEN hold time.

(5) `tcen_pgenh`: This is required to build a stable internal power before the memory actually switches to the standard mode.

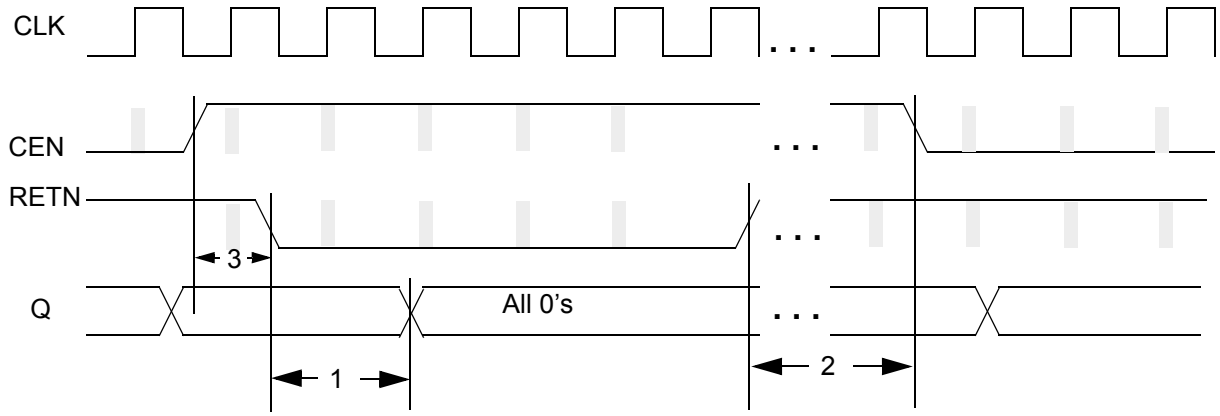
(6) `tretn_cenh`: This ensures that memory is inactive before the clamping of internal signals.

(7) `tpgen_cenh`: This is the minimum time needed to start the power down.

Table 6: Data Retention Mode - External Power Gating: SRAM-SP, SRAM-DP, RF-SP, RF-2P

Mode	Delay Parameter	Description
External Power Gating	t_{retnq}	RETN active to output clamped to zeros
	t_{cen_retnh}	RETN inactive to chip enabled, hold time
	t_{retn_cenh}	CEN disable to RETN active, hold time

Figure 2: External Power Gating Timing: SRAM-SP, SRAM-DP, RF-SP, RF-2P



= CEN and RETN have S/H window with respect to CLK

1: t_{retnq}

2: t_{cen_retnh}

3: t_{retn_cenh}

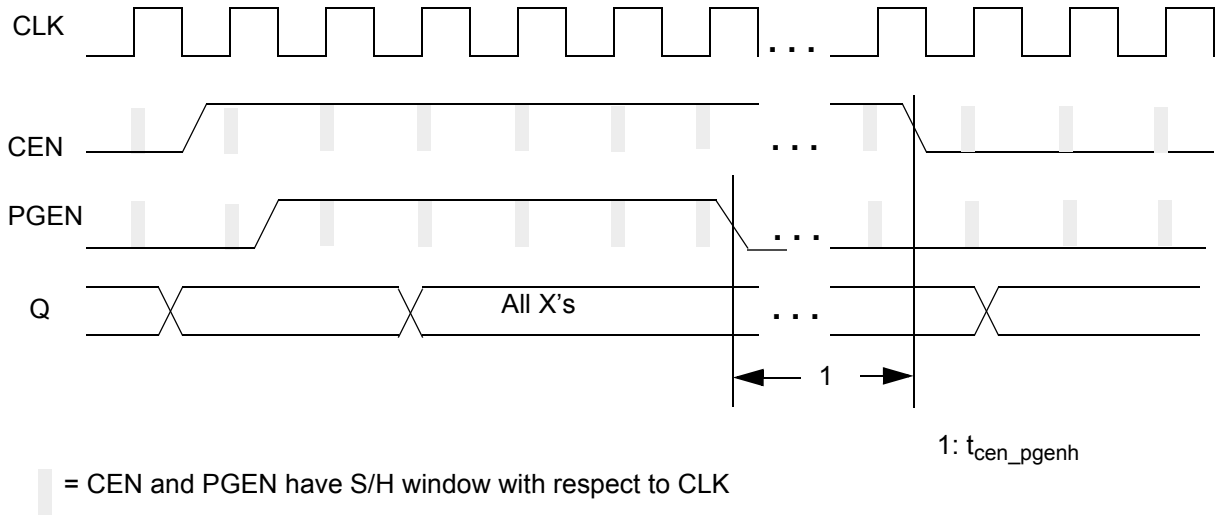
The timing relationship between the PGEN and CEN pins in the ROM compiler is shown in Table 7 and Figure 3 . Refer to the postscript datasheet or ASCII datatable for your compiler for instance-specific timing values.

ROM does not need the RETN pin. ROM requires only deep power down mode.

Table 7: Power Down Mode: ROM

Mode	Delay Parameter	Description
Power Gating	t_{cen_pgenh}	PGEN inactive to chip enabled, hold time

Figure 3: PGEN - CEN Timing: ROM



Appendix A- Revisions

This appendix describes the technical changes between released issues of this book.

Table A-1. Issue A

Change	Location
Replaced Metro product name with High Density	Entire book