TSMC 65nm CLN65G+ RVT Process 1.0-Volt 10-Track Advantage™ v2.1 Standard Cell Library Databook

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Preface

Revision History

This document contains the release history for the TSMC 65nm CLN65G+ RVT Process 1.0-Volt 10-Track Advantage™ v2.1 Standard Cell Library Databook.

Part Number	Release Number	Date of Release	Updates
DB-Advantage-TSM087-1.0/65@1.0-1.0	1.0	August 2006	Initial Release
DB-Advantage-TSM087-2.0/65@1.0-1.0	2.0	December 2006	Updated for LAT Family functional descriptions
DB-Advantage-TSM087-3.0/65@1.0-1.0	3.0	March 2007	Recharacterized with new Spectre models

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Introduction

ARM's Artisan Physical IP Advantage™ standard cell library builds upon the SAGE architecture, producing the optimum combination of high-density with high-performance. The cell line-up is derived from extensive customer design, synthesis, and place-and-route benchmark analysis. Library optimization is achieved by carefully matching the library functions and drive strengths to leading synthesis and place-and-route tools, producing superior RTL-to-GDSII results.

How This Book Is Organized

This introduction is organized into three sections:

- ***Global Parameters*** provides an overview of parameters specific to your Advantage library.
- ***Special Cells*** details the types of special cells that may be included in your library.
- ***Reading the Datasheet*** describes the components of each datasheet.

Datasheets for each cell in this library are provided after the introduction. The datasheets are included in alphabetical order.

Global Parameters

This section specifies global parameters for the TSMC 65nm CLN65G+ RVT Process 1.0-Volt 10-Track Advantage™ v2.1 Standard Cell Library. Some of the following sections may be covered: physical specifications, electrical specifications, derating factors, propagation delay calculation, timing constraints, power calculation, and power-rail strapping.

Physical Specifications

Table 1 shows the physical design specifications of this library.

Table 1. Physical Specifications

Drawn Gate Length (um)	0.06
Layers of Metal	1
Layout Grid (um)	0.005
Vertical Pin Grid (um)	0.2
Horizontal Pin Grid (um)	0.2
Cell Power and Ground Rail Width (um)	0.3
Cell Height (um)	2.0

In the Advantage library, all pins are located on the vertical and horizontal pin grids. Most place-and-route tools work more efficiently with all pins on grids, and some tools even require it.

The Advantage library also supports designs with six, seven, eight, or nine layers of metal. You may need to change the design rules in the technology file, because the top-level metal has a greater minimum width and greater minimum spacing requirement. See "TSMC 65nm CMOS Logic Design Rule Manual Version 1.2" design rule manual. You must define these rules correctly for the place-and-route tool.

Table 2 describes the electrical specifications for this library.

Table 2. Electrical Specifications

Parameter	Minimum	Typical	Maximum
DC Supply Voltage (Vdd)	0.9V	1.0V	1.1V
Junction Temperature	-40°C	25°C	125°C

Table 3 shows the derating factors for this library.

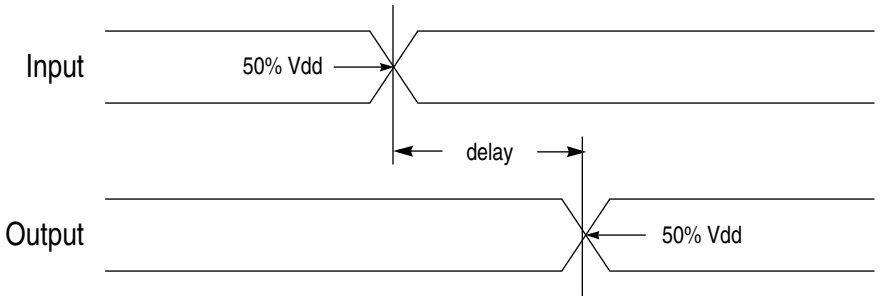
Table 3. Derating Factors

$K_{Process}$ (slow)	1.375
$K_{Process}$ (typical)	1.000 (by definition)
$K_{Process}$ (fast)	0.76
K_{Volt} (1.0V to 0.9V)	-2.507/V
K_{Volt} (1.0V to 1.1V)	-1.636/V
K_{Temp} (25°C to -40°C)	0.00029/°C
K_{Temp} (25°C to 125°C)	0.00041/°C

Propagation Delay and Transition Time

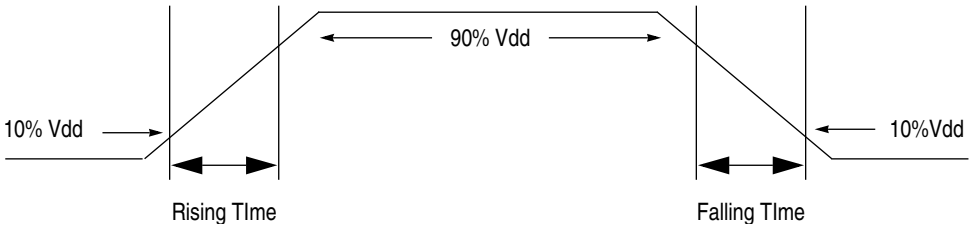
The propagation delay through a cell is the sum of the intrinsic delay, the load-dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing 50% of Vdd and the output crossing 50% of Vdd. Figure 1 illustrates the propagation delay.

Figure 1. Propagation Delay



The transition times (slews) on input and output pins are defined as the time interval between the signal crossing 10% of Vdd and 90% of Vdd. Figure 2 illustrates transition time measurements for rising and falling signals.

Figure 2. Transition Time



Factors that affect propagation delays and transition time include: temperature, supply voltage, process variations, fanout loading, interconnect loading, input-transition time, input-signal polarity, and timing constraints. The timing models provided with this library include the effects of input-transition time on propagation delays. Also, all timing models use a table lookup method to calculate accurate timing. To simplify calculations, the standard cell datasheets provide all timing numbers for an input slew of 0.01055ns and a linearized load factor, K_{load}, which is not as accurate as the timing models. All cells have been characterized with a fully populated metal2 (0.2um horizontal pitch) and metal3 (0.2um vertical pitch) routing grid across the entire cell layout.

The Advantage library may contain negative propagation delays. Although most third-party verification tools can handle negative propagation delays, some tools will turn negative delays into a zero value.

Derating Factors

Derating factors are coefficients that the typical process characterization data is multiplied by to arrive at timing data that reflects appropriate operating conditions. The deratings table provides derating factors for variations in process case, temperature, and voltage.

Derating factors are derived by averaging the performance of many different cells in the library. A particular combination of cells may perform better or worse than indicated by these derating factors.

Delay Calculation

Using the delay data in the datasheets ($t_{intrinsic}$, K_{load}, and C_{load}) and the delay derating factors, the estimated total propagation delay is calculated as such:

$$t_{TPD} = (K_{Process}) * [1 + (K_{Volt} * \Delta Vdd)] * [1 + (K_{Temp} * \Delta T)] * t_{typical}$$

$$t_{typical} = t_{intrinsic} + (K_{load} * C_{load})$$

where:

t_{TPD} = total propagation delay (ns);

$t_{typical}$ = delay at typical corner-1.0V, 25°C, typical process (ns);

$t_{intrinsic}$ = delay through the cell when there is no output load (ns);

K_{load} = load delay multiplier (ns/pF);

C_{load} = total output load capacitance (pF);

$K_{Process}$ = process derating factor, where process is slow, typical, or fast;

K_{Volt} = voltage derating factor (/V);

$\Delta Vdd = Vdd - 1.0V;$

K_{Temp} = temperature derating factor (/°C);

ΔT = junction temperature - 25°C.

Timing Constraints

Timing constraints define minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing constraints include: setup time, hold time, recovery time, and minimum pulse width.

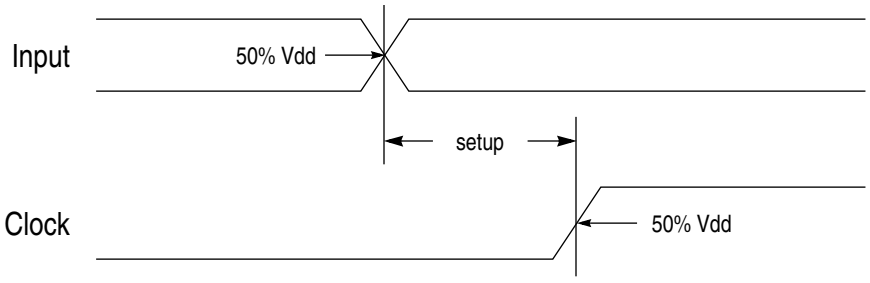
The sequential-cell timing models provided with this library include the effects of input-transition time and data-signal and clock-signal polarity on timing constraints. To simplify calculations, the datasheets specify timing constraint values for 0.01055ns data slew and 0.01055ns clock slew. Other factors that affect timing constraints include temperature, supply voltage, and process case variations. All cells have been characterized with a fully populated metal2 (0.2um horizontal pitch) and metal3 (0.2um vertical pitch) routing grid across the entire cell layout.

Timing constraints can affect propagation delays. The intrinsic delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, and pulse widths). The use of shorter timing constraint intervals may increase delay. Each cell is considered functional as long as the actual delay does not exceed the delay given in the datasheets by more than 10%.

Setup Time

The setup time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%. Setup-constraint values are measured as the interval between the data signal crossing 50% of Vdd for rising data (or 50% of Vdd for falling data) and the clock signal crossing 50% of Vdd for rising clocks (or 50% of Vdd for falling clocks). For the measurement of setup time, the data input signal is kept stable after the active clock edge for an infinite hold time. Figure 3 illustrates setup time for a positive-edge-triggered sequential cell.

Figure 3. Setup Time

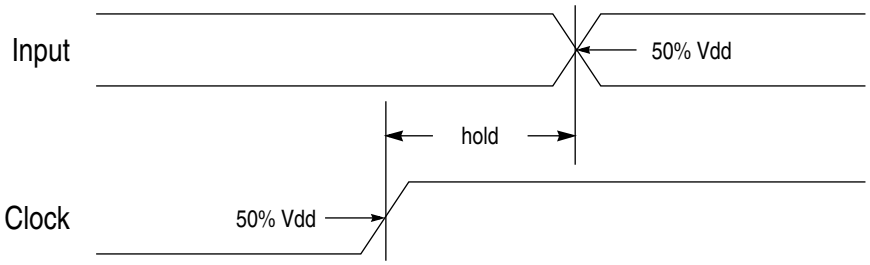


Hold Time

The hold time for a sequential cell is the minimum length of time the data-input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%. Hold-constraint values are measured as the interval between the data signal crossing 50% of Vdd for rising data (or 50% of Vdd for falling data) and the clock signal crossing 50% of Vdd for rising clocks (or 50% of Vdd for falling clocks). For the measurement of hold time, the data input signal is held stable before the active clock edge for an infinite setup time. Figure 4 illustrates hold time for a positive-edge-triggered sequential cell.

NOTE: ARM does not incorporate any hold time margins in the Synopsys, TLF, StarDC, or any other timing models. Chip designers should develop a timing methodology to account for chip-level timing inaccuracies inherent to extraction and timing analysis tools.

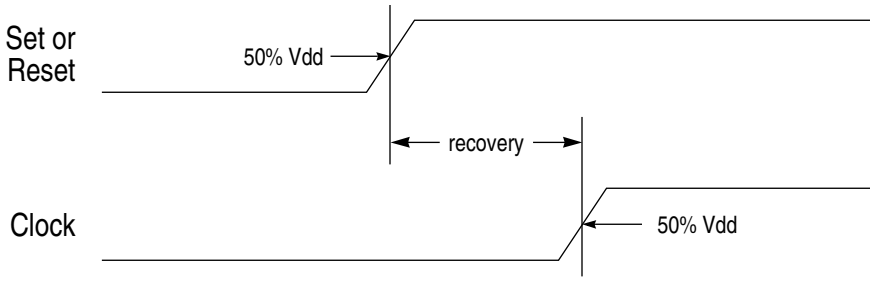
Figure 4. Hold Time



Recovery Time

Recovery time for sequential cells is the minimum length of time that the active-low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the set or reset signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd for rising clocks (or 50% of Vdd for falling clocks). For the measurement of recovery time, the set or reset signal is held stable after the active clock edge for an infinite hold time. Figure 5 illustrates recovery time.

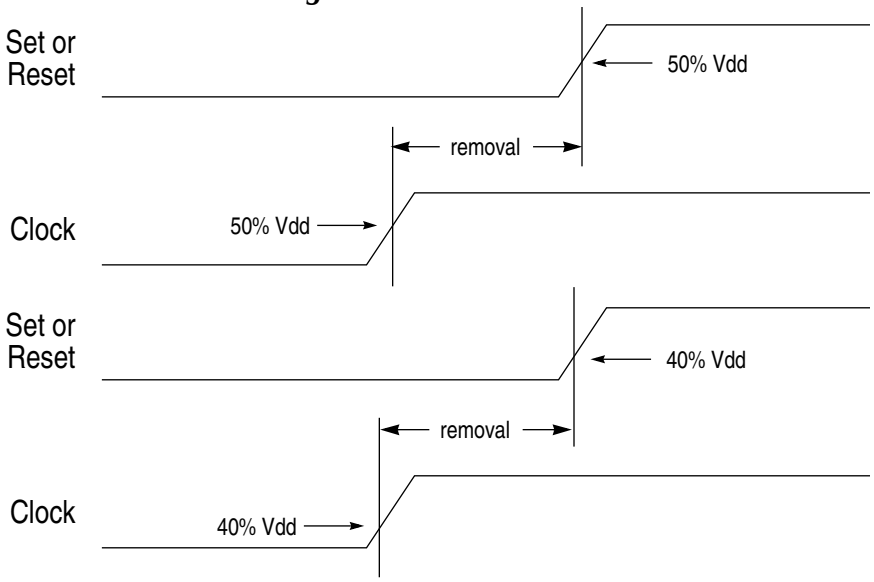
Figure 5. Recovery Time



Removal Time

Removal time for sequential cells is the minimum length of time that the active low set or reset signal must remain low after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the active clock edge does not latch in a new data value from that programmed by the asynchronous set or reset signal. Removal constraint values are measured as the interval between the set or reset signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd for rising clocks (or 50% of Vdd for falling clocks). For the measurement of removal time, the set or reset signal is held stable before the active clock edge for an infinite setup time. Figure 6 illustrates removal time.

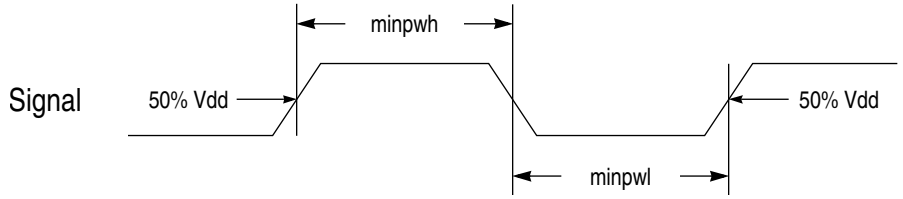
Figure 6. Removal Time



Minimum Pulse Width

Minimum pulse width is the minimum length of time between the leading and trailing edges of a pulse waveform. Minimum pulse width high (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of Vdd and the falling edge of the signal crossing 50% of Vdd. Minimum pulse width low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of Vdd and the rising edge of the signal crossing 50% of Vdd. Figure 7 illustrates minimum pulse width.

Figure 7. Minimum Pulse Width



Minimum pulse width is defined as 0.883028ns for all set/reset pins (SN, RN) and 0.883028ns for all clock pins (G, GN, CK, CKN). These are the largest minimum pulse widths measured from all the cells in the library. An input pulse of shorter duration will produce unpredictable results.

Electromigration

min_period Property

All sequential cells in the .lib file have this clock pin property set:

min_period : 1.000000;

This property has the effect of limiting a design's clock frequency to 1.0GHz. Commonly used design flows may not be able to support the required accuracy for designs targeted for clock frequencies higher than this limit. Contact ARM technical support for designs targeting higher clock frequencies.

Electromigration Guideline Compliance

Artisan standard cell libraries are designed to meet foundry electromigration guidelines for normal chip design usage; however, it is the chip designer's responsibility to ensure that electromigration guidelines are met at the chip level with regard to foundry guidelines as well as ARM's guidelines for how the library will be used. The following three Electromigration guidelines must be met in order to ensure safe use of the standard cell library within the electromigration guidelines of the foundry.

1. The width of the Metal1 VDD and VSS power buses in the standard cells has been sized to provide adequate current to the cells. Vertical power straps must be placed with sufficient frequency to provide adequate current distribution to the standard cell power buses. For more details, see the section entitled Power-Rail Strapping in the standard cell user guide.

2. The output pin metal for each standard cell has been sized to accommodate multiple vias necessary (for worst case electromigration conditions) to meet via electromigration guidelines, although oversized Metal1 output pins do not necessarily require multiple vias. The number of vias required to meet electromigration guidelines is design dependent, and the chip designer must use an appropriate number of vias and wire width when routing from an output pin.

3. The internal layouts of the standard cells have been designed and verified to comply with the manufacturer's electromigration guidelines under normal usage. Normal usage is defined as follows:

- The current required by the cell does not exceed the maximum current that can be supplied by the Metal1 power buses.

- The output transition times (measured using 10% and 90% thresholds), for a cell outside the clock tree network, must be no greater than 20% of the total cycle time, or must be no greater than 10% of the cycle time for any of the output pins of that particular cell. Limiting the output transition time has the effect of limiting the load driven by the cell which will reduce the cell's current draw, making it comply with electromigration guidelines. Ratios larger than 20% are not appropriate for commonly used design flows and are unlikely to be encountered in normal designs.
- For a cell in the clock tree network, transition times must not exceed 10% of the total cycle time for that cell.

Power Dissipation

The Advantage library is designed to dissipate only AC power, except for the small reverse-bias leakage currents which are normally present in all CMOS circuits.

The power dissipation internal to a cell when a given input switches is primarily dependent upon the cell design itself. The power dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The Advantage library datasheets contain both an AC power table which documents the internal energy consumption of each cell and a pin capacitance table which gives input-pin capacitance data used to compute output loading. This information, coupled with design-specific information, can be used to estimate the total power dissipation of a cell within a design.

The AC power tables specify the amount of energy consumed within a cell (uW/MHz) when the corresponding pin changes state at 25°C, 1.0V, and typical process. The energy data in the tables were measured for an input slew of 0.01055ns and no loading at the outputs.

For combinatorial cells, energy values are provided for only input pins. The energy value for each input pin is the average of energies associated with the input transitions which result in an output transition.

For sequential cells, the energy associated with each input pin is the average energy of those input transitions which *do not* result in an output transition. The energy associated with the output pin of a sequential cell is the average energy of all cases where an output transition is the result of a clock-input transition, minus the energy associated with the clock input pin. In the event that a sequential cell has multiple outputs, all output energy data will be associated with only one output pin.

Power Calculation

Power dissipation is dependent upon the power-supply voltage, frequency of operation, internal capacitance, and output load. The power dissipated by each cell is:

$$P_{avg} = \sum_{n=1}^{x}(E_{in} * f_{in}) + \sum_{n=1}^{y}(C_{on} * Vdd^2 * \frac{1}{2}f_{on}) + E_{os} * f_{01}$$

where:

P_{avg} = average power (uW);

x = number of input pins;

E_{in} = energy associated with the nth input pin (uW/MHz);

f_{in} = frequency at which the nth input pin changes state during the normal operation of the design (MHz);

y = number of output pins;

C_{on} = external capacitive loading on the nth output pin, including the capacitance of each input pin connected to the output driver, plus the route wire capacitance, actual or estimated (pF);

Vdd = operating voltage = 1.0V;

f_{on} = frequency at which the nth output pin changes state during the normal operation of the design (MHz);

E_{os} = energy associated with the output pin for sequential cells only (uW/MHz).

The switching frequency of inputs and outputs of a particular cell in a design can be obtained from a gate-level logic simulator (e.g. Verilog) by applying typical input stimuli and measuring the activity on each node of interest. The total average power for the design can be computed by adding the average power for each cell.

EXAMPLE: Calculating Power for a DFFXL Cell

For this exercise, assume that a DFFXL cell has clock switching at 133MHz (clock frequency = 66.5MHz), input and output pins switching at 20MHz, and an external capacitive loading on the output pin of 0.02pF. Using the AC Power table provided in the **sample** DFF datasheet at the end of the introduction, the power dissipated by the DFFXL can be calculated by using the following equation:

$$P_{avg} = \sum_{n=1}^{x}(E_{in} * f_{in}) + \sum_{n=1}^{y}(C_{on} * Vdd^2 * \frac{1}{2}f_{on}) + E_{os} * f_{01}$$

Given:

x = 2;

E_{i1} = 0.0056 <uW/MHz;

E_{i2} = 0.0063 uW/MHz;

f_{i1} = 20 MHz;

f_{i2} = 133 MHz;

y = 2;

C_{o1} = 0.02 pF;

C_{o2} = 0.02 pF;

Vdd = 1.0V;

f_{o1} = 20 MHz;

f_{o2} = 20 MHz;

E_{os} = 0.0060 uW/MHz,

we have:

$$P_{avg} = \sum_{n=1}^{2}(E_{in} * f_{in}) + \sum_{n=1}^{2}(C_{on} * Vdd^2 * \frac{1}{2}f_{on}) + E_{os} * f_{01}$$

$$P_{avg} = (E_{i1} * f_{i1}) + (E_{i2} * f_{i2}) + (C_{o1} * VDD^2 * \frac{1}{2}f_{o1})$$
$$+ (C_{o2} * VDD^2 * \frac{1}{2}f_{o2}) + (E_{os} * f_{01})$$

$$P_{avg} = (0.0056 * 20) + (0.0063 * 133) + \left(0.02 * 1.0 * \frac{1}{2}(20)\right)$$
$$+ \left(0.02 * 1.0 * \frac{1}{2}(20)\right) + (0.0060 * 20)$$

P_{avg} = 1.46 uW

Power-Rail Strapping

You must determine the required amount of vertical power-rail strapping to satisfy all requirements imposed by the design methodology for a given design. Power-rail strapping should be sized small enough to optimize standard cell height and maximize router efficiency, yet it must be large enough to provide sufficient power to the cells.

The guidelines below provide a rough estimate with many simplifying assumptions. For a given module design, you can estimate the amount of vertical power-rail strapping that is required to fulfill electromigration requirements.

Given:

I_{avg} = total average current for the module, calculated from previous section (mA);

w_{m1} = VSS/VDD metal1 wire width (um), see Physical Specifications;

r = number of rows in module;

d_{m1} = maximum metal1 current density allowed for the process (mA/um);

d_{m2} = maximum metal2 current density allowed for the process (mA/um);

I_{m1} = maximum current that can be supported by all horizontal metal1 wires (mA);

I_{strap} = total current that must be supported by the vertical metal2 strapping (mA);

w_{m2} = metal2 wire width required for vertical strapping (um);

c = minimum number of metal2 straps;

we have:

$I_{m1} = w_{m1} * r * 2 * d_{m1}$,

where multiplying by 2 assumes metal1 wires are supplied from both ends;

$$I_{strap} = \frac{(I_{avg} - I_{m1})}{2},$$

where dividing by 2 assumes the metal2 vertical strap wires are supplied from both ends;

$$w_{m2} = \frac{I_{strap}}{d_{m2}},$$

It is recommended that the metal2 wire width, $w_{m2,}$ be divided into c equal portions which are spaced equidistant across the module, where

$c = \frac{I_{avg}}{I_{m1}}$, rounded up to the next integer.

The same consideration must be given to the number of vias used to connect the metal1 and metal2 straps.

Adding Routing Channels

In the Advantage library, each cell is designed with a uniform cell height of 2.0um (i.e., 10 tracks tall with 0.2um per track). The cell layouts allow neighboring rows of cells to share common power or ground rails when cells abut each other at the top and bottom edges of the cell bounding box. The sea-of-cells layout with no channels between rows will usually yield the minimum area. In case of extremely congested areas, you may want to separate some rows of cells to increase the number of routing channels within a particular layout region. Because geometries must overlap cell boundaries, a particular spacing between the rows may result in DRC violations for layer spacing. It is recommended that you do not use spacings that cause DRC violations. If these spacings must be used, the DRC violations must be fixed manually by filling the void between the rows with the appropriate layer(s).

Table 4 indicates which DRC violations to expect and how to correct them for a separation between rows of cells.

Table 4. Correcting DRC Violations

Row Separation in Number of Grids	Expected DRC Violations	Action to Correct DRC Violations
0 (Rows Abut)	None	None
1	None	None
2	None	None
3	NWELL space < 0.47um	Draw NWELL layer between rows to merge NWELL regions above and below row separation
4	NWELL space < 0.47um	Draw NWELL layer between rows to merge NWELL regions above and below row separation
5 or more	None	None

Special Cells

This section discusses special cells that may be included in your library.

Antenna-Fix Cell

The library contains an antenna-fix cell which must be inserted manually. However, most place and route tools will indicate which nets require the antenna-fix cell. The TSMC antenna effect prevention guideline, "TSMC 65nm CMOS Logic Design Rule Manual Version 1.2", specifies a maximum wire length. During place and route, the router may connect wires to the input gates of cells that are longer than the maximum length allowable by the guideline. The antenna cell can be used in this case to add an optional diode on the net close to the input gates which do not meet the guideline. Pin A on the antenna cell connects to a diode, reverse biased to ground. A diode can be added to either P or N.

Delay Cells

The library contains delay cells that have the same width. These delay cells allow you to adjust a given delay path with a simple cell substitution after place and route.

FILL Cells

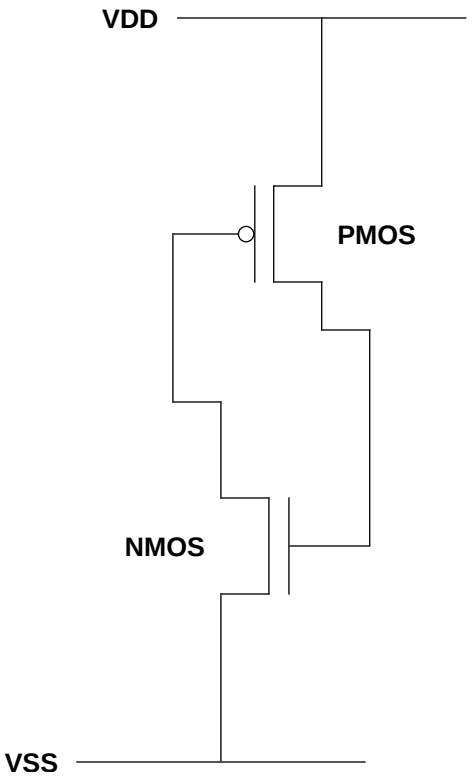
The library contains several filler cells named FILL<n>, where <n> in the cell name denotes the width of the cell in tracks.

During place and route, the FILL cells are used to connect power and ground rails across an area containing no cells. The FILL cells are also used to ensure gaps do not occur between well or implant layers which could cause design rule violations. Using wider cells where appropriate reduces the size of the layout database.

FILLCAP Cells

FILLCAPs function as FILL cells. Inside the FILLCAP, PMOS and NMOS devices form decoupling capacitors between the VDD and VSS rails, reducing ground bounce in the power grids. Figure 8 illustrates the FILLCAP functional schematic.

Figure 8. FILLCAP Functional Schematic



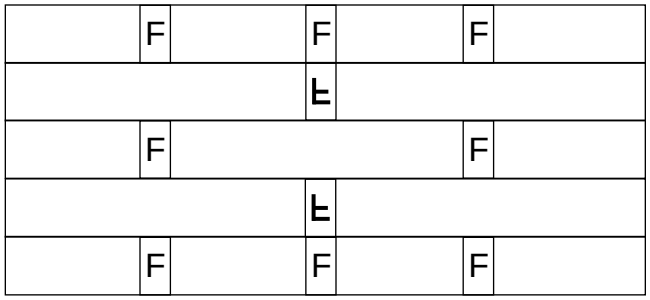
Low-Power (XL) Cells

The library contains a wide variety of cells, denoted by an "XL" suffix in the cell name, that are designed specifically for low-power applications. Input capacitance for the XL cells is much lower than that for corresponding X1 (1x drive strength) cells. Because XL cells have been designed for the sole purpose of reducing power consumption, output rise and fall times for these cells may not be equal, and due to the low-drive capability of the XL cells, these cells are not intended for use in critical timing paths, or to drive heavily loaded nets.

NWELL and Substrate Tie Cell

The library does not have well or substrate ties inside the cells. You are required to tie the NWELLS to Vdd and the substrate to Vss before place-and-route using the FILLTIE cell. Before place-and-route, pre-place the FILLTIE cell periodically in every placement row. You must place the FILLTIE cell as frequently as the design requires. For example, if the design rules require a well or substrate connection every 20um, then the FILLTIE cell must be pre-placed every 20um. See Figure 9.

Figure 9. Sample Placement of FILLTIE Cells for 20um NWELL and Substrate Tie Design Rule



Note: The letter "F" indicates a FILLTIE cell placed in normal orientation, and the letter "F" flipped upside down indicates a FILLTIE cell placed in MY orientation.

In all rows except for the top and bottom rows, the NWELL and substrate are shared by two adjacent placement rows. This allows you to place the FILLTIE cell only half as frequently as the design rules require. But don't forget to stagger the placement in the adjacent rows by an amount equal to the design row.

Assuming that the rule is every 20um, you will need to place FILLTIE cells every 20um in the top and bottom rows. If you stagger the placement by 20um between adjacent rows, you can place FILLTIE cells every 40um for all rows between the top and bottom rows. This method will allow every row to have well and substrate ties every 20um.

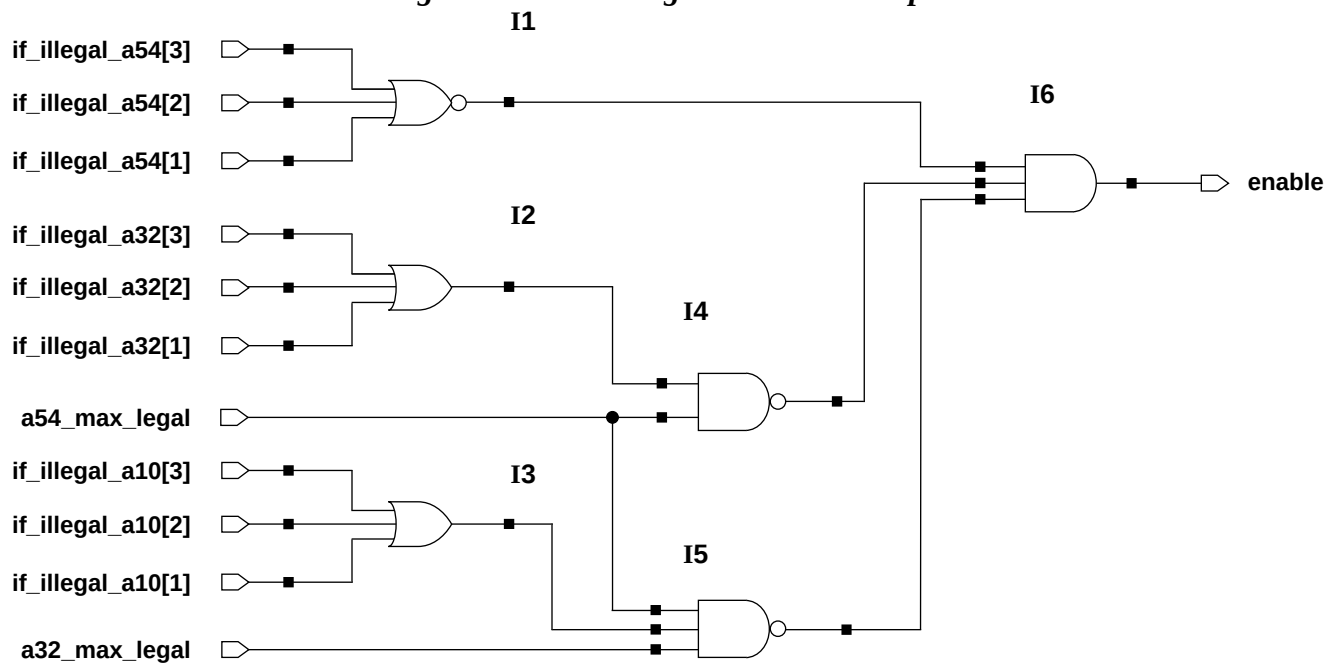
Register File Cells

Register file cells (RF*) are provided to support creating very small memories from standard cells. The register file bit cells (RF1R1W, RF2R1W) have tri-state outputs. Users must tie these tri-state outputs together on a bit line and have this bit line drive function as an output buffer. The library contains a number of inverting and non-inverting buffers (INV*, BUF*, TRI*) that can buffer the bit lines.

It is possible to make a memory that has a non-power-of-two word depth. If this is employed, it is possible to input an address to the memory such that none of the bit cells are addressed and nothing is driving the bit line. A floating bit line can cause the logic following it to go into a high power state, therefore, users must take special care when designing a memory with a non-power-of-two word depth. Users must guarantee that the bit line is never allowed to float by ensuring that at least one bit cell is always driving the bit line, or that a floating bit line does not cause subsequent logic to go into a high power state. One way to achieve the latter is to use an output buffer with an enable. NAND or AND gates or tri-state output buffers (NAND*, AND*, TRI*) can be used for this purpose. Whichever is used, be sure to generate an enable signal that only enables the output buffer when the bit line is not floating.

Figure 10 shows a sample circuit for generating an enable signal when the bit line is not floating in a register file of up to 64 words.

Figure 10. Enable Signal Circuit Example

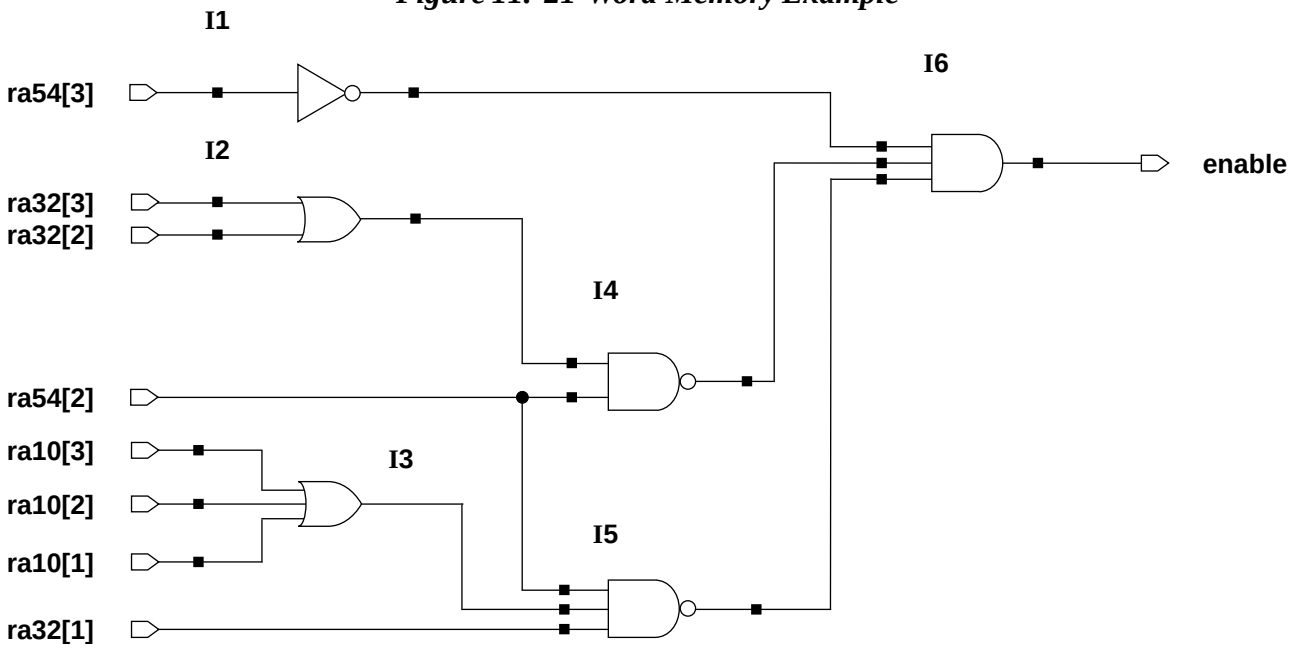


The circuit in Figure 10 assumes the address lines are pre-decoded in pairs. The circuit is a comparator. Program it with the number of words in the memory. The circuit compares the address input of the memory to the pre-programmed number of words. When the address is less than or equal to the size of the memory, it generates an enable signal for the output buffers. When the address input is higher than the number of words in the memory, the output of the comparator is false and the outputs are disabled, which prevents them from going into a high power state.

To program the example comparator, connect predecoded address lines to gates I1, I2 and I3 if the address should be larger than the size of the memory when those signals are active, and more significant address bits have not resolved the comparison. If, when those signals are active, the address should not be larger than the size of the memory, either ground that pin or reduce the number of inputs to the gate. To enable the comparison of lower address bits, connect to gates I4 and I5 signals that signify that the higher address bits have not been able to resolve the comparison. To I4, connect the signal that is true when the most significant two address bits are exactly equal to what they are in the highest address that exists in the memory. To I5, connect the signals that are true when the most significant for bits are exactly equal to what they are in the highest address that exists in the memory.

Figure 11 shows an example for a memory that has 21 words.

Figure 11. 21-Word Memory Example



In binary mode, the highest address that exists in the memory is 100100. The read address RA[5:0] is pre-decoded into RA54[3:0] which are the four possible combinations of the two most significant address bits. RA32[3:0] is the four possible combinations of address bits 3 and 2. RA10[3:0] is the four possible combinations of address bits 1 and 0. If RA54[3] is true, we are accessing address 11XXXX in the memory. This address does not exist, so the comparison does not need to continue to the remaining address bits. Gate I1 needs only RA54[3] as an input because this is the only combination of these 2 address bits which is never in the memory. We connect RA54[2] to gate I4 because if this signal is true we don't know if the address exists and we have to continue the comparison to the next pair of addresses. To gate I2 we connect RA32[3] and RA32[2] because if RA54[2] is true and either of RA32[3] or RA32[2] are true, the address doesn't exist and we are done. If RA54[2] and RA32[1] are true, we are addressing word 1001XX which might be in the memory so we connect these two signals to I5 and check RA10. We connect RA10[3], RA10[2] and RA10[1] to I3 because of the memory addresses 1001XX, only 100100 exists in the memory. I6 generates the enable signal based on the results of all of the comparisons.

TIEHI/LO Cells

The library contains a TIEHI cell and a TIELO cell. The outputs of the TIEHI and TIELO cells are driven through diffusion to provide isolation from the power and ground rails for better ESD protection. The standard cell abstract methodology assumes that the TIEHI and TIELO cells are used to tie off any inputs to power and ground. If these cells are not used and the router is allowed to drop vias on the power rail, DRC errors or shorts may result.

Advantage Naming Conventions

1. Cell Name Fields

The Advantage 65 library cell name has four separate fields. They are the root, drive strength, library identifier, and threshold voltage identifier.These four components are concatenated together in the following order:

[root][drive strength][library identifier][threshold voltage];

For Example:

SDFFQX1MA12TR

SDFFQ : root field (mux-d flop with non-inverting output)

X1M : drive strength field (1 fold output stage with an M beta ratio)

A12 : library identifier field (Advantage library at a 12 track pitch)

TR : threshold voltage field (Regular or nominal threshold voltage cell)

BUFHX2P5BA10TL

BUFH : root field (high speed buffer)

X2P5B : drive strength field (2.5 fold output stage with a B beta ratio)

A10 : library identifier field (Advantage library at a 10 track pitch)

TL : threshold voltage field (low threshold voltage cell)

2. Root

This portion of the cell name defines the logical function of the cell. There is a large degree of variation in this field. A full definition of the root names are provided in later sections, broken out by major function. Some examples of what this field includes are NAND2, AOI21, INV, SDFF, etc.

3. Drive Strength

The Advantage 65 library contains multiple beta ratios for some of the topologies. This requires a naming convention be adopted which indicates the different beta ratios. The convention is:

X[number][beta ratio letter];

The X plus the number field indicates how many folds are present. One fold is indicated by X1 while X4 indicates four folds. Think of the X as a mnemonic for multiplied by. The library also makes use of non-integer folds. This is useful for improving performance as well as reducing power consumption. When a non-integer fold is present, a P indicates the decimal place. For example, a cell that contains 1.4 folds is indicated with X1P4. If the fold size is less than one, then a zero prefixes the P. Currently, only one significant digit is used after the decimal place as it is believed this provides enough granularity.

There are many potentially useful beta ratios. Table 5 lists all the beta ratios we currently have defined. Note that since the most recent SAGE-X libraries are flood-filled and no letter was used in the SAGE-X naming convention we adopted the convention of null or no character for indicating flood-filled.

Table 5. Beta Ratio Letter Definition

Letter	Description
null	Devices are drawn at the maximum size possible regardless of topology
A	Tuned to minimize the average delay between the input edges
B	The delay for both edges are equal when the input driver is a balanced inverter
E	The output rising and falling edge rates are equal assuming the input driver has equal rising and falling edge rates
M	Tuned to minimize the maximum delay between the input edges

With the addition of the beta ratio indicator to the drive strength field the CLK prefix has been dropped since this prefix was really just indicating a B type beta ratio in previous SAGE-X libraries.

4. Library Identifier

In order to support the mixing of different libraries on a single die, all ARM libraries have a unique library identifier field. The field has two parts. The first is the library letter and the second is a number indicating the library's cell pitch in tracks. The letter A denotes an Advantage library and the letter M denotes a Metro library. A twelve-track Advantage library's identifier is A12.

5. Threshold Voltage

This field differentiates the different threshold voltages versions of a cell. The syntax is:

T[threshold letter]

The defined threshold letters and their meaning are provided in Table 6

Table 6. Threshold Voltage Letter Definition

Letter	Description
H	High Threshold Voltage
L	Low Threshold Voltage
R	Regular (Nominal) Threshold Voltage

For a cell containing low threshold voltage devices, this field would be TL.

6. Root Name

Flops

[logic][root][clock][async][scanout][output][ppa];

logic : null, An, On, AOmn, OAmn, Mn, E

null : No logic integration

An : n-input AND (can be used for synchronous reset)

AOmn : AOI style input (can be used for synchronous set and reset with set dominant)

On : n-input OR (can be used for asynchronous set)

OAmn : OAI style input (can be used for synchronous reset and set with reset dominant)

Mn : n-input encoded mux

E : mux-hold flop (enable)

root : DFF, DRFF, SDFF, SDRFF

DFF : basic master slave flop

DRFF : basic master slave flop with retention

SDFF : mux-d flop

SDRFF : mux-d flop with retention

clock : null, N

null : positive edge clock and base setup verses clock->q relationship

N : negative edge clock and base setup verses clock->q relationship

async : null, S, R, RS, SR, P
null : no async inputs
S : async set
R : async reset
RS : async reset and set with reset dominant
SR : async set and reset with set dominant
P : active high

output : null, Q, QN
null : dual output flop
Q : non-inverting output flop (q)
QN : inverting output flop (qn)

ppa : null
null : base flop design point with regards to power, delay, and area

Integrated Clock Gate
[logic][test ovrd]ICG[clock][ppa];
logic : null
null : No logic integration

test ovrd : FR, POST, PRE
FR : free running version with no enable designed to match PRE and POST delay
POST : test over-ride input is asynchronous
PRE : test over-ride input is synchronous

clock : null
null : ICG produces and active high output

ppa : null
null : base flop design point with regards to power, delay, and area

Latches
The naming convention for latches is basically the same as the flops convention for consistency.
[logic][root][clock][async][scanout][output][ppa];
logic : null
null : No logic integration

root : LAT

LAT : basic transparent latch

clock : null, N
null : latch is transparent while clock is high
N : latch is transparent while clock is low

async : null, S, R, P
null : no async inputs
S : async set
R : async reset
P : active high

scanout : null
null : no dedicated SO pin

output : Q, QN
Q : non-inverting output flop (q)
QN : inverting output flop (qn)

ppa : null
null : base flop design point with regards to power, delay, and area

Reading the Datasheet

Please refer to the **sample** datasheet for DFF at the end of the introduction for the arrangement of each of the following datasheet sections. Datasheet titles reference standard Artisan cell names. Cell names for your specific library are reflected in the cell size table on each datasheet.

NOTE: This datasheet contains **sample** characterization values.

1. Base Cell Name

The cell name field contains the cell name. The datasheets are presented alphabetically by cell name. The cell name presented here is the base cell name. The Cell Size table displays cell names for your specific library.

2. Cell Description

The cell description gives the function of the cell. When applicable, the equation(s) for the output pins are provided.

3. Functions

The function table gives all possible combinations of input and output signals for the cell. Table 7 defines the symbols used in datasheet function tables.

Table 7. Functions Key

Symbol	Description
0	Logic Low
1	Logic High
‾_	High to Low Transition
_/‾	Low to High Transition
X	Don’t Care
IL	Illegal/Undefined
Z	High Impedance

4. Logic Symbol

The logic symbol is a graphical representation of the cell, similar to the view in the schematic editor when the cell is instantiated. The symbol shows the name and location of the input and output pins.

5. Cell Size

This cell size table gives the height and width (μm) for each drive strength of the cell.

6. Functional Schematic

The functional schematic provides a functional representation of the cell.

7. Drive Strength

The drive strength of each cell is indicated by an "X" followed by the unit strength.

8. AC Power

The AC power table shows the amount of energy consumed (μW/MHz) within the cell when the corresponding pin changes state. The energy data for each drive strength of the cell in the **sample** DFF datasheet are calculated at 25°C, 1.0V, typical process, input slew of 0.01055ns, and no external load at the output pins.

9. Delay

The delay table shows the intrinsic delay (ns) which is the delay through the cell when there is no load on the output, and the load multiplier for load dependent delay, K_{load} (ns/pF). The delays and load multiplier for each drive strength of the cell in the sample DFF datasheet are calculated at 25°C, 1.0V, typical process, and input slew of 0.01055ns.

10. Timing Constraints

The timing constraints table in the **sample** DFF datasheet shows the timing conditions (ns) required at 25°C, 1.0V, and typical process to maintain proper functionality. Setup constraint values are measured for 0.01055ns data slew and 0.01055ns clock slew. Hold constraint values are measured for 0.01055ns data slew and 0.01055ns clock slew. Minimum pulse width is defined to be 0.883028ns for all set/reset pins and 0.883028ns for all clock pins. These are the largest minimum pulse widths measured from all the cells in the library.

11. Pin Capacitance

The pin capacitance table shows the typical loading at the input pins of the cell (pF) for each drive strength of the cell.

▼ *This datasheet contains sample characterization values.* ▼

1

DFF

Process Technology:
CustomerName & Code

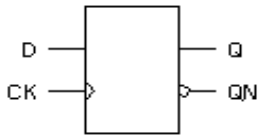
Cell Description

The DFF cell is a positive-edge triggered, static D-type flip-flop.

2

4

Logic Symbol



3

Function Table

D	CK	Q[n+1]	QN[n+1]
0	↑	0	1
1	↑	1	0
x	↓	Q[n]	QN[n]

5

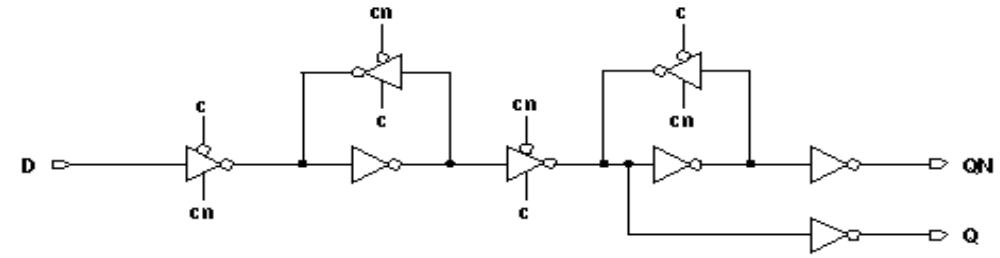
Cell Size

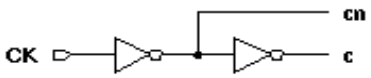
Drive Strength	Height (µm)	Width (µm)
DFFXL	1.000	1.000
DFFX1	2.000	2.000
DFFX2	3.000	3.000
DFFX4	4.000	4.000

6

Functional Schematic

7





ARM Sample Standard Cell Library Databook, p. **84**

▼ *This datasheet contains sample characterization values.* ▼

Process Technology:
CustomerName & Code

DFF

(8) **AC Power**

Pin	Power (µW/MHz)			
(7)	XL	X1	X2	X4
D	1.000	1.000	1.000	1.000
CK	2.000	2.000	2.000	2.000
Q	3.000	3.000	3.000	3.000

(11) **Pin Capacitance**

Pin	Capacitance (pF)			
	XL	X1	X2	X4
D	1.000	1.000	1.000	1.000
CK	2.000	2.000	2.000	2.000

(9) **Delays at TypTemp°C, TypVoltV, Typical Process**

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	XL	X1	X2	X4	XL	X1	X2	X4
CK → Q↑	1.000	1.000	1.000	1.000	1.000	1.000	1.000	1.000
CK → Q↓	2.000	2.000	2.000	2.000	2.000	2.000	2.000	2.000
CK → QN↑	3.000	3.000	3.000	3.000	3.000	3.000	3.000	3.000
CK → QN↓	4.000	4.000	4.000	4.000	4.000	4.000	4.000	4.000

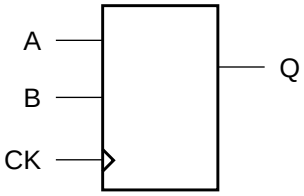
(10) **Timing Constraints at TypTemp°C, TypVoltV, Typical Process**

Pin	Requirement	Interval (ns)			
		XL	X1	X2	X4
D	setup↑ → CK	1.000	1.000	1.000	1.000
	setup↓ → CK	2.000	2.000	2.000	2.000
	hold↑ → CK	3.000	3.000	3.000	3.000
	hold↓ → CK	4.000	4.000	4.000	4.000
CK	minpwh	5.000	5.000	5.000	5.000
	minpwh	6.000	6.000	6.000	6.000

Cell Description

The A2DFFQ cell is a positive-edge triggered, static D-type flip-flop. It provides the logical AND of two inputs (A, B) and has a single output (Q). The cell supports integrated synchronous reset.

Logic Symbol



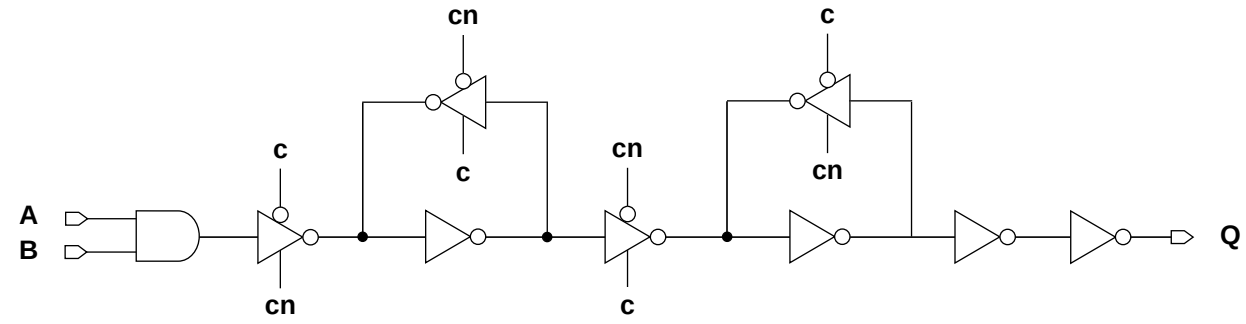
Function Table

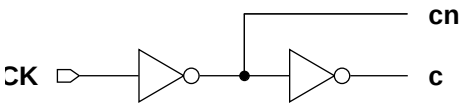
A	B	CK	Q[n+1]
0	0	⎍	0
0	1	⎍	0
1	0	⎍	0
1	1	⎍	1
x	x	⎎	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
A2DFFQX0P5MA10TR	2.00	4.40
A2DFFQX1MA10TR	2.00	4.40
A2DFFQX2MA10TR	2.00	4.60
A2DFFQX3MA10TR	2.00	5.00
A2DFFQX4MA10TR	2.00	5.60

Functional Schematic





AC Power

Pin	Power (uW/MHz)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
A	0.0041	0.0052	0.0065	0.0071	0.0074
CK	0.0037	0.0042	0.0048	0.0054	0.0058
B	0.0044	0.0056	0.0071	0.0077	0.0080
Q	0.0030	0.0040	0.0058	0.0079	0.0106

Pin Capacitance

Pin	Capacitance (pF)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
A	0.0012	0.0014	0.0018	0.0018	0.0018
CK	0.0010	0.0010	0.0011	0.0011	0.0012
B	0.0011	0.0013	0.0017	0.0017	0.0017

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
CK → Q ↑	0.0914	0.0795	0.0773	0.0757	0.0728
CK → Q ↓	0.1029	0.0862	0.0841	0.0825	0.0784

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
CK → Q ↑	4.1712	2.3340	1.1622	0.7832	0.5830
CK → Q ↓	2.4962	1.3334	0.6611	0.4571	0.3321

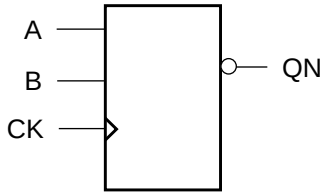
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)				
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
A	setup ↑ → CK	0.0273	0.0273	0.0234	0.0273	0.0312
	setup ↓ → CK	0.0273	0.0234	0.0156	0.0195	0.0234
	hold ↑ → CK	-0.0117	-0.0117	-0.0117	-0.0117	-0.0117
	hold ↓ → CK	-0.0039	0.0000	0.0039	0.0000	0.0000
CK	minpwh	0.8830	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830
B	setup ↑ → CK	0.0273	0.0273	0.0273	0.0273	0.0312
	setup ↓ → CK	0.0352	0.0273	0.0195	0.0234	0.0273
	hold ↑ → CK	-0.0117	-0.0156	-0.0117	-0.0156	-0.0156
	hold ↓ → CK	-0.0078	-0.0039	0.0000	-0.0039	-0.0039

Cell Description

The A2DFFQN cell is a positive-edge triggered, static D-type flip-flop. It provides the logical AND of two inputs (A, B) and has a single output (QN). The cell supports synchronous reset.

Logic Symbol



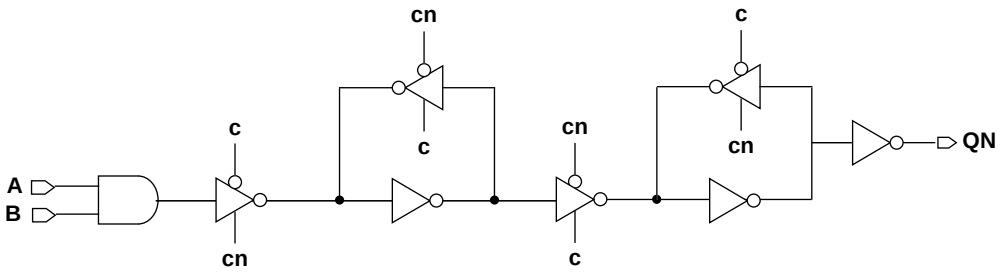
Function Table

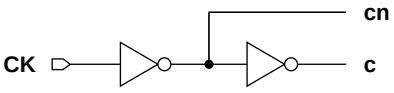
A	B	CK	QN[n+1]
0	0	⎍	1
0	1	⎍	1
1	0	⎍	1
1	1	⎍	0
x	x	⎎	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
A2DFFQNX0P5MA10TR	2.00	4.40
A2DFFQNX1MA10TR	2.00	4.40
A2DFFQNX2MA10TR	2.00	4.60
A2DFFQNX3MA10TR	2.00	5.00

Functional Schematic





AC Power

Pin	Power (uW/MHz)			
	X0P5M	X1P0M	X2P0M	X3P0M
A	0.0039	0.0053	0.0064	0.0072
CK	0.0036	0.0041	0.0047	0.0056
B	0.0041	0.0058	0.0069	0.0078
QN	0.0033	0.0038	0.0057	0.0078

Pin Capacitance

Pin	Capacitance (pF)			
	X0P5M	X1P0M	X2P0M	X3P0M
A	0.0011	0.0014	0.0017	0.0017
CK	0.0010	0.0010	0.0011	0.0012
B	0.0010	0.0013	0.0016	0.0016

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X0P5M	X1P0M	X2P0M	X3P0M	X0P5M	X1P0M	X2P0M	X3P0M
CK → QN ↑	0.0882	0.0746	0.0733	0.0660	4.2503	2.3523	1.1737	0.7974
CK → QN ↓	0.0870	0.0741	0.0772	0.0727	2.8914	1.5234	0.7653	0.5107

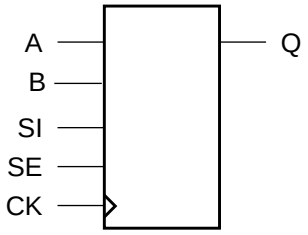
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X0P5M	X1P0M	X2P0M	X3P0M
A	setup ↑ → CK	0.0312	0.0273	0.0273	0.0312
	setup ↓ → CK	0.0273	0.0234	0.0234	0.0273
	hold ↑ → CK	-0.0156	-0.0117	-0.0117	-0.0117
	hold ↓ → CK	0.0000	0.0000	0.0000	-0.0039
CK	minpwh	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830
B	setup ↑ → CK	0.0352	0.0312	0.0273	0.0312
	setup ↓ → CK	0.0312	0.0312	0.0273	0.0352
	hold ↑ → CK	-0.0156	-0.0156	-0.0117	-0.0117
	hold ↓ → CK	-0.0039	-0.0039	-0.0039	-0.0078

Cell Description

The A2SDFFQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE). The cell performs a logical AND of two inputs (A, B) and produces a single output (Q). The cell supports integrated synchronous reset.

Logic Symbol



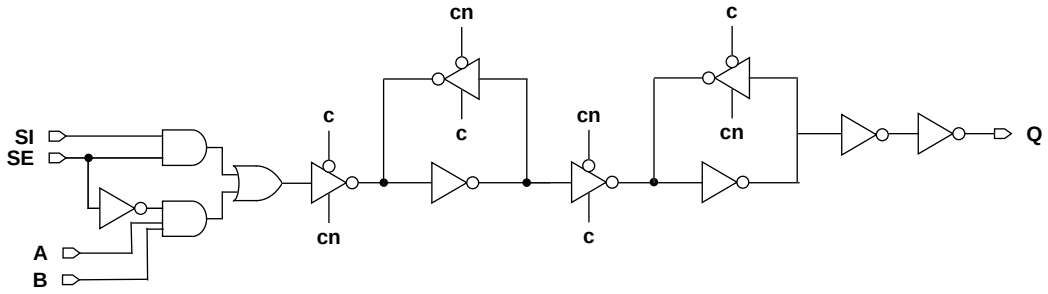
Function Table

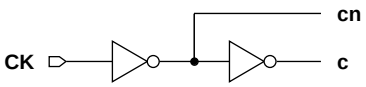
A	B	SI	SE	CK	Q[n+1]
0	0	x	0	⎍	0
0	1	x	0	⎍	0
1	0	x	0	⎍	0
1	1	x	0	⎍	1
x	x	x	x	⎎	Q[n]
x	x	0	1	⎍	0
x	x	1	1	⎍	1

Cell Size

Drive Strength	Height (um)	Width (um)
A2SDFFQX0P5MA10TR	2.00	5.40
A2SDFFQX1MA10TR	2.00	5.80
A2SDFFQX2MA10TR	2.00	6.00
A2SDFFQX3MA10TR	2.00	6.20
A2SDFFQX4MA10TR	2.00	7.00

Functional Schematic





AC Power

Pin	Power (uW/MHz)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
SI	0.0057	0.0074	0.0090	0.0102	0.0105
SE	0.0056	0.0068	0.0079	0.0087	0.0090
A	0.0048	0.0063	0.0075	0.0082	0.0086
CK	0.0036	0.0042	0.0048	0.0053	0.0056
B	0.0052	0.0070	0.0082	0.0089	0.0093
Q	0.0032	0.0042	0.0061	0.0081	0.0106

Pin Capacitance

Pin	Capacitance (pF)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
SI	0.0007	0.0007	0.0007	0.0007	0.0007
SE	0.0021	0.0023	0.0024	0.0024	0.0024
A	0.0008	0.0010	0.0011	0.0011	0.0011
CK	0.0009	0.0010	0.0011	0.0012	0.0012
B	0.0012	0.0016	0.0017	0.0017	0.0017

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
CK → Q ↑	0.0910	0.0786	0.0769	0.0755	0.0715
CK → Q ↓	0.1024	0.0859	0.0830	0.0842	0.0775

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
CK → Q ↑	4.1933	2.3366	1.1633	0.7840	0.5833
CK → Q ↓	2.4784	1.3393	0.6627	0.4585	0.3323

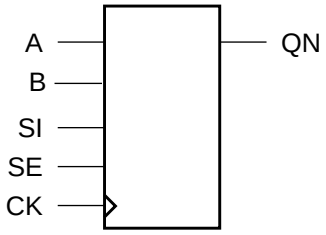
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)				
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
SI	setup ↑ → CK	0.0859	0.0938	0.1094	0.1133	0.1172
	setup ↓ → CK	0.1211	0.1172	0.1289	0.1445	0.1484
	hold ↑ → CK	-0.0547	-0.0664	-0.0742	-0.0781	-0.0742
	hold ↓ → CK	-0.0625	-0.0586	-0.0664	-0.0781	-0.0703
SE	setup ↑ → CK	0.1484	0.1523	0.1719	0.1836	0.1875
	setup ↓ → CK	0.0820	0.0586	0.0625	0.0625	0.0664
	hold ↑ → CK	-0.0547	-0.0625	-0.0742	-0.0742	-0.0742
	hold ↓ → CK	-0.0273	-0.0195	-0.0195	-0.0234	-0.0234
A	setup ↑ → CK	0.0586	0.0312	0.0312	0.0352	0.0391
	setup ↓ → CK	0.0586	0.0391	0.0391	0.0469	0.0508
	hold ↑ → CK	-0.0352	-0.0156	-0.0195	-0.0195	-0.0195
	hold ↓ → CK	-0.0273	-0.0156	-0.0156	-0.0195	-0.0195
CK	minpwh	0.8830	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830
B	setup ↑ → CK	0.0586	0.0352	0.0352	0.0391	0.0430
	setup ↓ → CK	0.0625	0.0469	0.0430	0.0508	0.0547
	hold ↑ → CK	-0.0352	-0.0195	-0.0195	-0.0234	-0.0234
	hold ↓ → CK	-0.0273	-0.0195	-0.0195	-0.0234	-0.0234

Cell Description

The A2SDFFQN cell is a positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE). The cell performs a logical AND of two inputs (A, B) and produces a single output (QN). The cell supports integrated synchronous reset.

Logic Symbol



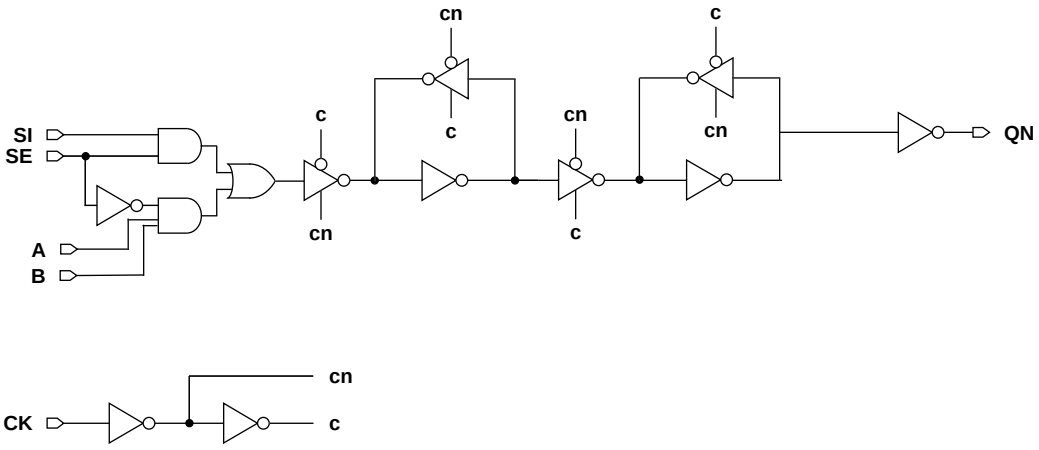
Function Table

A	B	SI	SE	CK
0	0	x	0	⎍
0	1	x	0	⎍
1	0	x	0	⎍
1	1	x	0	⎍
x	x	x	x	⎎
x	x	0	1	⎍
x	x	1	1	⎍

Cell Size

Drive Strength	Height (um)	Width (um)
A2SDFFQNX0P5MA10TR	2.00	5.40
A2SDFFQNX1MA10TR	2.00	5.80
A2SDFFQNX2MA10TR	2.00	6.00
A2SDFFQNX3MA10TR	2.00	6.20

Functional Schematic



AC Power

Pin	Power (uW/MHz)			
	X0P5M	X1P0M	X2P0M	X3P0M
SI	0.0057	0.0075	0.0089	0.0102
SE	0.0056	0.0067	0.0077	0.0084
A	0.0048	0.0063	0.0074	0.0083
CK	0.0035	0.0041	0.0047	0.0056
B	0.0052	0.0068	0.0081	0.0090
QN	0.0033	0.0040	0.0062	0.0079

Pin Capacitance

Pin	Capacitance (pF)			
	X0P5M	X1P0M	X2P0M	X3P0M
SI	0.0006	0.0007	0.0007	0.0007
SE	0.0021	0.0023	0.0024	0.0024
A	0.0008	0.0010	0.0012	0.0012
CK	0.0009	0.0010	0.0011	0.0012
B	0.0012	0.0015	0.0017	0.0017

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X0P5M	X1P0M	X2P0M	X3P0M	X0P5M	X1P0M	X2P0M	X3P0M
CK → QN ↑	0.0871	0.0737	0.0739	0.0678	4.2418	2.3515	1.1685	0.7929
CK → QN ↓	0.0877	0.0737	0.0786	0.0736	2.9282	1.5299	0.7666	0.5272

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**
SI	setup ↑ → CK	0.0859	0.0977	0.1094	0.1211
	setup ↓ → CK	0.1250	0.1172	0.1328	0.1484
	hold ↑ → CK	-0.0547	-0.0625	-0.0703	-0.0703
	hold ↓ → CK	-0.0586	-0.0547	-0.0625	-0.0625
SE	setup ↑ → CK	0.1523	0.1484	0.1719	0.1836
	setup ↓ → CK	0.0859	0.0625	0.0625	0.0664
	hold ↑ → CK	-0.0508	-0.0625	-0.0703	-0.0703
	hold ↓ → CK	-0.0234	-0.0156	-0.0156	-0.0195
A	setup ↑ → CK	0.0625	0.0352	0.0352	0.0391
	setup ↓ → CK	0.0625	0.0430	0.0391	0.0469
	hold ↑ → CK	-0.0352	-0.0195	-0.0156	-0.0195
	hold ↓ → CK	-0.0234	-0.0156	-0.0117	-0.0156
CK	minpwh	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830
B	setup ↑ → CK	0.0625	0.0391	0.0352	0.0430
	setup ↓ → CK	0.0664	0.0469	0.0469	0.0508
	hold ↑ → CK	-0.0391	-0.0234	-0.0195	-0.0195
	hold ↓ → CK	-0.0273	-0.0195	-0.0156	-0.0195

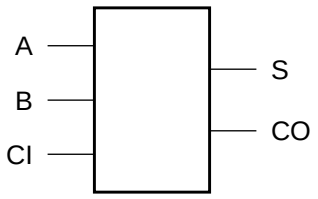
Cell Description

The ADDF cell provides the arithmetic sum (S) and carry out (CO) of two operands (A,B) with carry in (CI). The two outputs (S,CO) are represented by the logic equations:

$S = (A \oplus B \oplus CI)$

$CO = (A \oplus B) \bullet CI + (A \bullet B)$

Logic Symbol



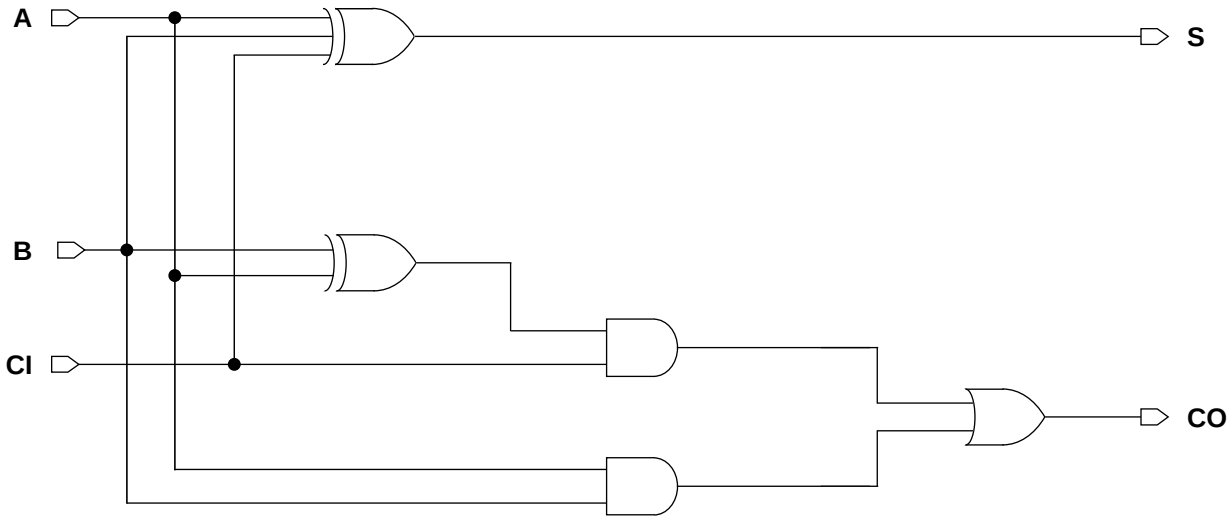
Function Table

CI	A	B	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
ADDFX1MA10TR	2.00	4.20
ADDFX1P4MA10TR	2.00	4.80
ADDFX2MA10TR	2.00	4.80

Functional Schematic



AC Power

Pin	Power (uW/MHz)		
	X1P0M	X1P4M	X2P0M
A	0.0113	0.0133	0.0154
B	0.0118	0.0138	0.0159
CI	0.0102	0.0123	0.0143

Pin Capacitance

Pin	Capacitance (pF)		
	X1P0M	X1P4M	X2P0M
A	0.0049	0.0049	0.0049
B	0.0052	0.0052	0.0052
CI	0.0038	0.0038	0.0038

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)			K_{load} (ns/pF)		
	X1P0M	X1P4M	X2P0M	X1P0M	X1P4M	X2P0M
A → S ↑	0.0872	0.1003	0.1097	2.3682	1.6215	1.1720
A → S ↓	0.0888	0.1010	0.1118	1.5232	1.0525	0.7557
B → S ↑	0.0876	0.1003	0.1100	2.3683	1.6221	1.1720
B → S ↓	0.0912	0.1013	0.1118	1.5573	1.0881	0.7816
CI → S ↑	0.0796	0.0933	0.1012	2.3681	1.6214	1.1709
CI → S ↓	0.0857	0.0974	0.1068	1.5516	1.0746	0.7775
A → CO ↑	0.0501	0.0543	0.0571	2.4289	1.6585	1.1950
A → CO ↓	0.0600	0.0646	0.0690	1.5991	1.0553	0.7692
B → CO ↑	0.0486	0.0527	0.0555	2.4284	1.6581	1.1948
B → CO ↓	0.0600	0.0646	0.0690	1.5985	1.0550	0.7690
CI → CO ↑	0.0421	0.0459	0.0486	2.4174	1.6494	1.1884
CI → CO ↓	0.0522	0.0570	0.0607	1.5981	1.0598	0.7669

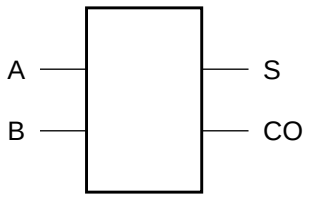
Cell Description

The ADDH cell provides the arithmetic sum (S) and carry out (CO) of two operands (A,B). The two outputs (S,CO) are represented by the logic equations:

$S = (\overline{A} \bullet B) + (A \bullet \overline{B})$

$CO = A \bullet B$

Logic Symbol



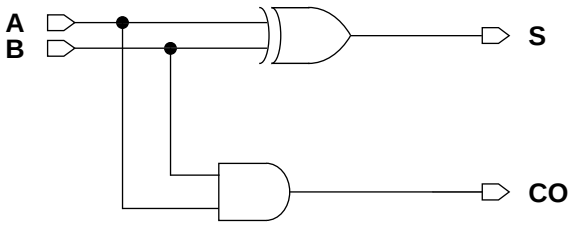
Function Table

A	B	S	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Cell Size

Drive Strength	Height (um)	Width (um)
ADDHX1MA10TR	2.00	2.60
ADDHX1P4MA10TR	2.00	3.20
ADDHX2MA10TR	2.00	3.20

Functional Schematic



AC Power

Pin	Power (uW/MHz)		
	X1P0M	X1P4M	X2P0M
A	0.0078	0.0105	0.0121
B	0.0082	0.0111	0.0128

Pin Capacitance

Pin	Capacitance (pF)		
	X1P0M	X1P4M	X2P0M
A	0.0024	0.0030	0.0030
B	0.0025	0.0031	0.0032

Delays at 25°C,1.0V, Typical Process

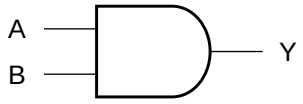
Description				Intrinsic Delay (ns)			K_{load} (ns/pF)		
				X1P0M	X1P4M	X2P0M	X1P0M	X1P4M	X2P0M
A	→	S	↑	0.0549	0.0528	0.0583	2.4100	1.6435	1.1762
A	→	S	↓	0.0620	0.0603	0.0676	1.4839	1.0280	0.7174
B	→	S	↑	0.0553	0.0548	0.0589	2.4086	1.6426	1.1756
B	→	S	↓	0.0634	0.0618	0.0690	1.4849	1.0290	0.7179
A	→	CO	↑	0.0356	0.0337	0.0362	2.4865	1.6397	1.1867
A	→	CO	↓	0.0329	0.0312	0.0335	1.4798	1.0034	0.7127
B	→	CO	↑	0.0369	0.0351	0.0377	2.4857	1.6396	1.1866
B	→	CO	↓	0.0350	0.0346	0.0356	1.4817	1.0067	0.7138

Cell Description

The AND2 cell provides the logical AND of two inputs (A,B). The output (Y) is represented by the logic equation:

$Y = (A \bullet B)$

Logic Symbol



Function Table

A	B	Y
0	x	0
x	0	0
1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
AND2X0P5MA10TR	2.00	1.20
AND2X0P7MA10TR	2.00	1.20
AND2X1MA10TR	2.00	1.20
AND2X1P4MA10TR	2.00	1.40
AND2X2MA10TR	2.00	1.40
AND2X3MA10TR	2.00	2.20
AND2X4MA10TR	2.00	2.40
AND2X6MA10TR	2.00	3.40
AND2X8MA10TR	2.00	4.60
AND2X11MA10TR	2.00	6.40

Functional Schematic

AC Power

Pin	Power (uW/MHz)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A	0.0005	0.0006	0.0007	0.0009	0.0012	0.0019	0.0024	0.0037
B	0.0005	0.0005	0.0006	0.0009	0.0011	0.0018	0.0023	0.0035

AC Power (Cont'd.)

Pin	Power (uW/MHz)	
	X8P0M	**X11P0M**
A	0.0049	0.0070
B	0.0047	0.0067

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A	0.0009	0.0010	0.0011	0.0014	0.0017	0.0028	0.0033	0.0052
B	0.0009	0.0010	0.0011	0.0014	0.0017	0.0028	0.0033	0.0049

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)	
	X8P0M	**X11P0M**
A	0.0067	0.0098
B	0.0066	0.0094

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A → Y ↑	0.0343	0.0321	0.0303	0.0296	0.0280	0.0276	0.0267	0.0270
A → Y ↓	0.0367	0.0353	0.0344	0.0347	0.0335	0.0324	0.0316	0.0318
B → Y ↑	0.0360	0.0338	0.0318	0.0310	0.0293	0.0288	0.0279	0.0281
B → Y ↓	0.0396	0.0377	0.0370	0.0372	0.0359	0.0350	0.0345	0.0344

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)	
	X8P0M	**X11P0M**
A → Y ↑	0.0264	0.0266
A → Y ↓	0.0309	0.0315
B → Y ↑	0.0276	0.0278
B → Y ↓	0.0339	0.0343

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A → Y ↑	4.6154	3.3732	2.4273	1.6527	1.1803	0.8009	0.5841	0.3888
A → Y ↓	2.8042	2.0497	1.4480	1.0154	0.7014	0.4856	0.3540	0.2368
B → Y ↑	4.6151	3.3728	2.4267	1.6524	1.1802	0.8009	0.5841	0.3888
B → Y ↓	2.8079	2.0518	1.4495	1.0166	0.7024	0.4863	0.3547	0.2372

Delays at 25°C,1.0V, Typical Process (Cont'd.)

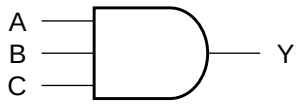
Description	K_{load} (ns/pF)	
	X8P0M	**X11P0M**
A → Y ↑	0.2895	0.2096
A → Y ↓	0.1778	0.1303
B → Y ↑	0.2895	0.2096
B → Y ↓	0.1781	0.1306

Cell Description

The AND3 cell provides the logical AND of three inputs (A,B,C). The output (Y) is represented by the logic equation:

$Y = (A \bullet B \bullet C)$

Logic Symbol



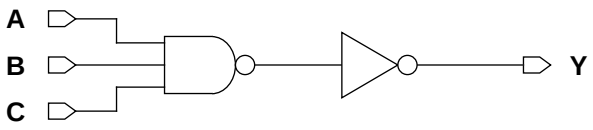
Function Table

A	B	C	Y
0	x	x	0
x	0	x	0
x	x	0	0
1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
AND3X0P5MA10TR	2.00	1.40
AND3X0P7MA10TR	2.00	1.40
AND3X1MA10TR	2.00	1.40
AND3X1P4MA10TR	2.00	1.80
AND3X2MA10TR	2.00	2.20
AND3X3MA10TR	2.00	3.00
AND3X4MA10TR	2.00	4.00
AND3X6MA10TR	2.00	6.00
AND3X8MA10TR	2.00	7.00
AND3X11MA10TR	2.00	9.40

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A	0.0006	0.0007	0.0008	0.0010	0.0014	0.0023	0.0029	0.0042
B	0.0005	0.0005	0.0007	0.0009	0.0011	0.0018	0.0024	0.0035
C	0.0004	0.0005	0.0007	0.0009	0.0013	0.0020	0.0024	0.0035

AC Power (Cont'd.)

Pin	Power (uW/MHz)	
	X8P0M	**X11P0M**
A	0.0055	0.0078
B	0.0047	0.0066
C	0.0047	0.0066

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A	0.0011	0.0013	0.0014	0.0018	0.0025	0.0040	0.0046	0.0065
B	0.0011	0.0012	0.0014	0.0017	0.0023	0.0036	0.0045	0.0063
C	0.0010	0.0011	0.0014	0.0018	0.0027	0.0038	0.0044	0.0064

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)	
	X8P0M	**X11P0M**
A	0.0084	0.0119
B	0.0082	0.0116
C	0.0082	0.0116

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A → Y ↑	0.0358	0.0350	0.0334	0.0327	0.0298	0.0323	0.0290	0.0279
A → Y ↓	0.0363	0.0368	0.0365	0.0361	0.0335	0.0346	0.0333	0.0324
B → Y ↑	0.0384	0.0374	0.0361	0.0355	0.0323	0.0345	0.0328	0.0319
B → Y ↓	0.0395	0.0399	0.0398	0.0397	0.0372	0.0380	0.0387	0.0382
C → Y ↑	0.0396	0.0385	0.0377	0.0369	0.0342	0.0363	0.0346	0.0339
C → Y ↓	0.0426	0.0428	0.0430	0.0429	0.0412	0.0419	0.0440	0.0433

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)	
	X8P0M	**X11P0M**
A → Y ↑	0.0279	0.0278
A → Y ↓	0.0326	0.0322
B → Y ↑	0.0315	0.0314
B → Y ↓	0.0380	0.0376
C → Y ↑	0.0333	0.0332
C → Y ↓	0.0431	0.0427

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A → Y ↑	4.5833	3.3428	2.5914	1.6630	1.1924	0.8033	0.5829	0.3876
A → Y ↓	2.7715	2.0225	1.4391	0.9875	0.6993	0.4894	0.3594	0.2403
B → Y ↑	4.5825	3.3421	2.5907	1.6630	1.1923	0.8033	0.5829	0.3876
B → Y ↓	2.7787	2.0277	1.4423	0.9899	0.7014	0.4907	0.3608	0.2413
C → Y ↑	4.5799	3.3403	2.5899	1.6627	1.1922	0.8032	0.5829	0.3876
C → Y ↓	2.7861	2.0330	1.4459	0.9928	0.7036	0.4922	0.3630	0.2427

Delays at 25°C,1.0V, Typical Process (Cont'd.)

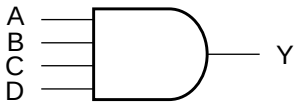
Description	K_{load} (ns/pF)	
	X8P0M	**X11P0M**
A → Y ↑	0.2895	0.2109
A → Y ↓	0.1804	0.1325
B → Y ↑	0.2895	0.2109
B → Y ↓	0.1812	0.1330
C → Y ↑	0.2895	0.2109
C → Y ↓	0.1821	0.1337

Cell Description

The AND4 cell provides the logical AND of four inputs (A,B,C,D). The output (Y) is represented by the logic equation:

$Y = (A \bullet B \bullet C \bullet D)$

Logic Symbol



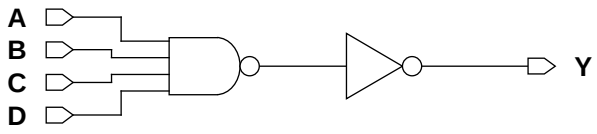
Function Table

A	B	C	D	Y
0	x	x	x	0
x	0	x	x	0
x	x	0	x	0
x	x	x	0	0
1	1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
AND4X0P5MA10TR	2.00	1.60
AND4X0P7MA10TR	2.00	1.60
AND4X1MA10TR	2.00	2.00
AND4X1P4MA10TR	2.00	3.00
AND4X2MA10TR	2.00	4.20
AND4X3MA10TR	2.00	4.80
AND4X4MA10TR	2.00	6.40
AND4X6MA10TR	2.00	7.80
AND4X8MA10TR	2.00	9.60

Functional Schematic



AC Power

Pin	Power (uW/MHz)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A	0.0006	0.0007	0.0009	0.0013	0.0020	0.0025	0.0034	0.0049	0.0065
B	0.0005	0.0006	0.0007	0.0010	0.0015	0.0020	0.0027	0.0039	0.0052
C	0.0005	0.0006	0.0007	0.0011	0.0014	0.0019	0.0027	0.0039	0.0052
D	0.0006	0.0006	0.0007	0.0013	0.0014	0.0019	0.0026	0.0039	0.0052

Pin Capacitance

Pin	Capacitance (pF)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A	0.0014	0.0015	0.0017	0.0026	0.0036	0.0045	0.0060	0.0084	0.0111
B	0.0013	0.0014	0.0016	0.0025	0.0035	0.0043	0.0058	0.0083	0.0109
C	0.0013	0.0014	0.0016	0.0028	0.0035	0.0043	0.0058	0.0082	0.0109
D	0.0014	0.0015	0.0017	0.0030	0.0034	0.0042	0.0060	0.0081	0.0108

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A → Y ↑	0.0386	0.0372	0.0349	0.0343	0.0318	0.0303	0.0306	0.0298	0.0299
A → Y ↓	0.0373	0.0370	0.0359	0.0342	0.0351	0.0341	0.0345	0.0332	0.0332
B → Y ↑	0.0430	0.0416	0.0392	0.0382	0.0377	0.0358	0.0367	0.0352	0.0357
B → Y ↓	0.0420	0.0418	0.0410	0.0388	0.0423	0.0411	0.0418	0.0400	0.0403
C → Y ↑	0.0460	0.0447	0.0422	0.0418	0.0414	0.0392	0.0402	0.0386	0.0390
C → Y ↓	0.0463	0.0462	0.0456	0.0442	0.0486	0.0470	0.0477	0.0458	0.0460
D → Y ↑	0.0477	0.0462	0.0438	0.0438	0.0432	0.0409	0.0420	0.0403	0.0408
D → Y ↓	0.0501	0.0500	0.0499	0.0486	0.0541	0.0521	0.0532	0.0508	0.0512

Delays at 25°C,1.0V, Typical Process (Cont'd.)

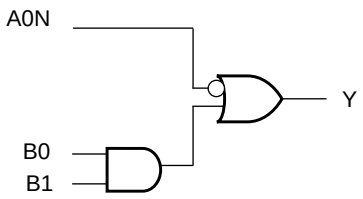
Description	K_{load} (ns/pF)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A → Y ↑	4.7670	3.5338	2.4777	1.6395	1.1834	0.7915	0.5879	0.3895	0.2921
A → Y ↓	2.7395	1.9977	1.4581	1.0001	0.7156	0.4874	0.3612	0.2411	0.1812
B → Y ↑	4.7660	3.5333	2.4777	1.6394	1.1834	0.7916	0.5879	0.3896	0.2921
B → Y ↓	2.7487	2.0044	1.4634	1.0036	0.7193	0.4898	0.3631	0.2422	0.1821
C → Y ↑	4.7656	3.5326	2.4777	1.6391	1.1834	0.7915	0.5879	0.3896	0.2921
C → Y ↓	2.7589	2.0119	1.4696	1.0085	0.7244	0.4929	0.3653	0.2437	0.1832
D → Y ↑	4.7648	3.5319	2.4777	1.6389	1.1834	0.7915	0.5879	0.3896	0.2921
D → Y ↓	2.7723	2.0213	1.4774	1.0137	0.7306	0.4965	0.3683	0.2455	0.1846

Cell Description

The AO1B2 cell provides the logical inverted OR of one AND group consisting of two inputs each: (A0N) and (B0, B1). The output (Y) is represented by the logic equation:

$Y = \overline{A0N} + (B0 \bullet B1)$

Logic Symbol



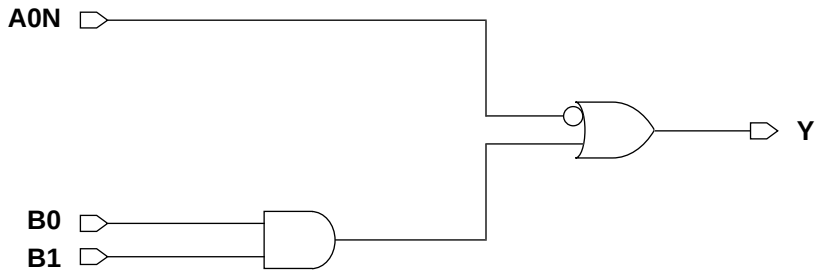
Function Table

B0	B1	A0N	Y
x	x	0	1
1	1	x	1
0	x	1	0
x	0	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
AO1B2X0P5MA10TR	2.00	1.40
AO1B2X0P7MA10TR	2.00	1.40
AO1B2X1MA10TR	2.00	1.40
AO1B2X1P4MA10TR	2.00	2.00
AO1B2X2MA10TR	2.00	2.00
AO1B2X3MA10TR	2.00	3.00
AO1B2X4MA10TR	2.00	3.40
AO1B2X6MA10TR	2.00	5.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
B0	0.0005	0.0006	0.0006	0.0009	0.0011	0.0018	0.0021	0.0033
B1	0.0004	0.0005	0.0006	0.0008	0.0010	0.0017	0.0021	0.0032
A0N	0.0006	0.0007	0.0010	0.0016	0.0021	0.0031	0.0043	0.0065

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
B0	0.0009	0.0009	0.0011	0.0014	0.0016	0.0027	0.0032	0.0050
B1	0.0008	0.0009	0.0010	0.0014	0.0016	0.0028	0.0033	0.0047
A0N	0.0012	0.0014	0.0018	0.0030	0.0037	0.0054	0.0074	0.0111

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
B0 → Y ↑	0.0423	0.0407	0.0375	0.0388	0.0353	0.0353	0.0339	0.0346
B0 → Y ↓	0.0378	0.0368	0.0355	0.0360	0.0330	0.0324	0.0314	0.0318
B1 → Y ↑	0.0429	0.0415	0.0384	0.0402	0.0367	0.0365	0.0351	0.0356
B1 → Y ↓	0.0385	0.0377	0.0364	0.0374	0.0345	0.0342	0.0331	0.0334
A0N → Y ↑	0.0115	0.0109	0.0103	0.0107	0.0101	0.0100	0.0100	0.0099
A0N → Y ↓	0.0125	0.0119	0.0117	0.0118	0.0113	0.0111	0.0111	0.0111

Delays at 25°C,1.0V, Typical Process (Cont'd.)

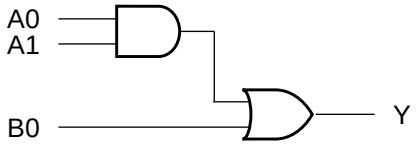
Description	K_{load} (ns/pF)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
B0 → Y ↑	4.5893	3.3576	2.4160	1.6203	1.1673	0.7727	0.5771	0.3825
B0 → Y ↓	4.8721	3.5209	2.5638	1.7865	1.2652	0.8395	0.6291	0.4191
B1 → Y ↑	4.5893	3.3571	2.4158	1.6201	1.1673	0.7727	0.5771	0.3825
B1 → Y ↓	4.8735	3.5222	2.5641	1.7867	1.2658	0.8399	0.6291	0.4191
A0N → Y ↑	4.4258	3.2339	2.3311	1.6022	1.1539	0.7634	0.5778	0.3808
A0N → Y ↓	4.8617	3.5143	2.5591	1.7825	1.2634	0.8383	0.6281	0.4184

Cell Description

The AO21 cell provides the logical OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$Y = (A0 \bullet A1) + \overline{B0}$

Logic Symbol



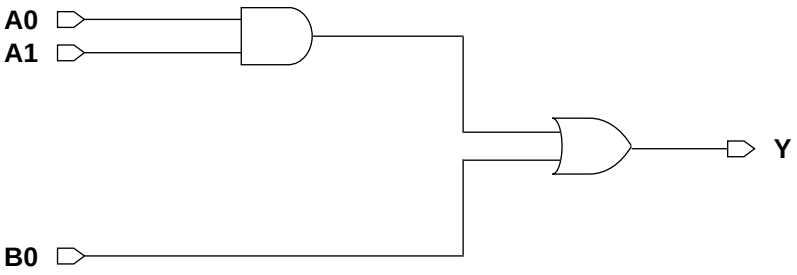
Function Table

A0	A1	B0	Y
0	x	0	0
x	0	0	0
x	x	1	1
1	1	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
AO21X0P5MA10TR	2.00	1.60
AO21X0P7MA10TR	2.00	1.60
AO21X1MA10TR	2.00	1.60
AO21X1P4MA10TR	2.00	2.60
AO21X2MA10TR	2.00	2.60
AO21X3MA10TR	2.00	3.60
AO21X4MA10TR	2.00	4.00
AO21X6MA10TR	2.00	5.60

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M
A0	0.0006	0.0007	0.0009	0.0012	0.0017	0.0026	0.0032	0.0049
A1	0.0006	0.0007	0.0009	0.0012	0.0017	0.0025	0.0033	0.0049
B0	0.0004	0.0005	0.0007	0.0010	0.0014	0.0019	0.0024	0.0037

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M
A0	0.0012	0.0013	0.0016	0.0022	0.0029	0.0044	0.0052	0.0071
A1	0.0011	0.0012	0.0015	0.0019	0.0029	0.0041	0.0048	0.0071
B0	0.0011	0.0013	0.0015	0.0019	0.0024	0.0035	0.0044	0.0064

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M
A0 → Y ↑	0.0380	0.0384	0.0354	0.0338	0.0316	0.0338	0.0322	0.0297
A0 → Y ↓	0.0451	0.0456	0.0428	0.0411	0.0404	0.0413	0.0396	0.0382
A1 → Y ↑	0.0388	0.0393	0.0363	0.0349	0.0328	0.0346	0.0331	0.0322
A1 → Y ↓	0.0487	0.0493	0.0464	0.0442	0.0439	0.0442	0.0427	0.0439
B0 → Y ↑	0.0281	0.0279	0.0263	0.0267	0.0262	0.0259	0.0256	0.0258
B0 → Y ↓	0.0434	0.0435	0.0408	0.0387	0.0372	0.0381	0.0375	0.0382

Delays at 25°C,1.0V, Typical Process (Cont'd.)

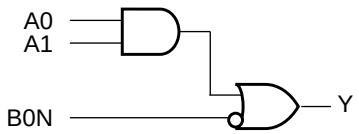
Description	K_{load} (ns/pF)							
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M
A0 → Y ↑	4.6290	3.3738	2.4158	1.6654	1.1868	0.7902	0.5854	0.3878
A0 → Y ↓	2.8746	2.0815	1.4604	1.0287	0.7251	0.4899	0.3616	0.2411
A1 → Y ↑	4.6288	3.3738	2.4158	1.6655	1.1868	0.7902	0.5854	0.3877
A1 → Y ↓	2.8845	2.0885	1.4652	1.0318	0.7270	0.4911	0.3626	0.2422
B0 → Y ↑	4.6013	3.3526	2.4034	1.6579	1.1821	0.7868	0.5830	0.3868
B0 → Y ↓	2.8846	2.0885	1.4651	1.0317	0.7269	0.4911	0.3626	0.2422

Cell Description

The AO21B cell provides the logical AND of two inputs (A0, A1) and the logical OR of one inverted signal (B0N). The output (Y) is represented by the logic equation:

$Y = (A0 + A1) \bullet \overline{B0N}$

Logic Symbol



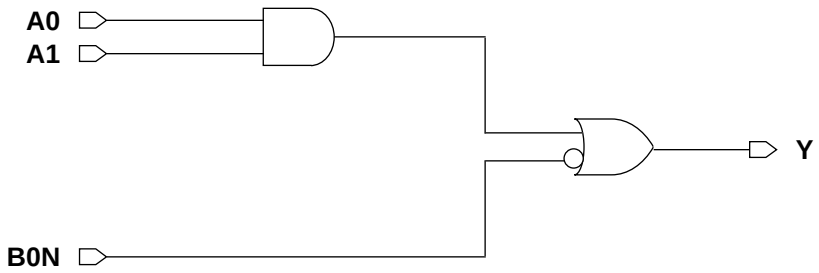
Function Table

A0	A1	B0N	Y
1	1	x	1
x	x	0	1
x	0	1	0
0	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
AO21BX0P5MA10TR	2.00	1.40
AO21BX0P7MA10TR	2.00	1.40
AO21BX1MA10TR	2.00	1.40
AO21BX1P4MA10TR	2.00	2.00
AO21BX2MA10TR	2.00	2.00
AO21BX3MA10TR	2.00	3.00
AO21BX4MA10TR	2.00	3.40
AO21BX6MA10TR	2.00	5.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A0	0.0005	0.0006	0.0007	0.0010	0.0013	0.0021	0.0026	0.0040
A1	0.0005	0.0006	0.0007	0.0010	0.0013	0.0021	0.0026	0.0038
B0N	0.0007	0.0009	0.0011	0.0017	0.0022	0.0034	0.0045	0.0068

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A0	0.0009	0.0010	0.0011	0.0014	0.0017	0.0027	0.0032	0.0050
A1	0.0009	0.0010	0.0011	0.0014	0.0016	0.0028	0.0033	0.0047
B0N	0.0013	0.0016	0.0020	0.0030	0.0037	0.0058	0.0075	0.0115

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A0 → Y ↑	0.0426	0.0411	0.0379	0.0411	0.0377	0.0362	0.0358	0.0364
A0 → Y ↓	0.0371	0.0368	0.0349	0.0362	0.0338	0.0321	0.0319	0.0322
A1 → Y ↑	0.0440	0.0425	0.0393	0.0425	0.0390	0.0374	0.0370	0.0374
A1 → Y ↓	0.0384	0.0380	0.0362	0.0376	0.0351	0.0339	0.0337	0.0337
B0N → Y ↑	0.0104	0.0100	0.0092	0.0092	0.0085	0.0086	0.0084	0.0084
B0N → Y ↓	0.0115	0.0111	0.0100	0.0096	0.0088	0.0090	0.0087	0.0088

Delays at 25°C,1.0V, Typical Process (Cont'd.)

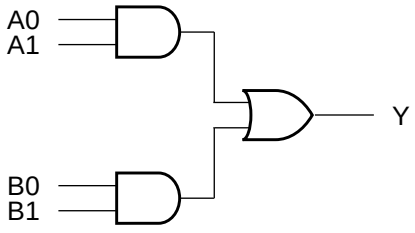
Description	K_{load} (ns/pF)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A0 → Y ↑	4.4568	3.2540	2.3388	1.6116	1.1596	0.7805	0.5799	0.3822
A0 → Y ↓	5.3365	3.8942	2.7685	1.7787	1.2587	0.8381	0.6282	0.4186
A1 → Y ↑	4.4563	3.2537	2.3386	1.6115	1.1596	0.7805	0.5799	0.3822
A1 → Y ↓	5.3361	3.8937	2.7683	1.7788	1.2586	0.8381	0.6282	0.4186
B0N → Y ↑	4.5351	3.3108	2.3788	1.6105	1.1617	0.7667	0.5740	0.3805
B0N → Y ↓	5.3274	3.8873	2.7639	1.7741	1.2555	0.8365	0.6269	0.4177

Cell Description

The AO22 cell provides the logical OR of two AND groups. The output (Y) is represented by the logic equation:

$Y = (A0 \bullet A1) + (B0 \bullet B1)$

Logic Symbol



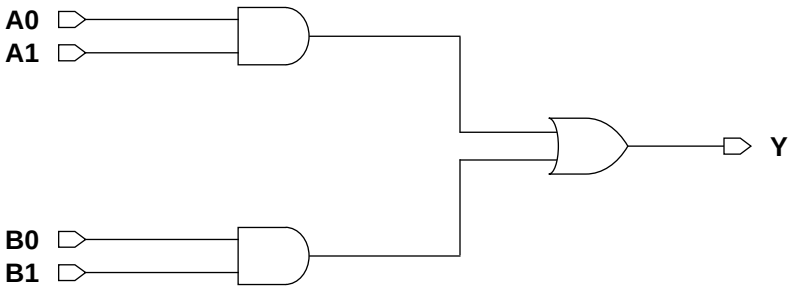
Function Table

A0	A1	B0	B1	Y
0	x	0	x	0
0	x	x	0	0
x	0	0	x	0
x	0	x	0	0
x	x	1	1	1
1	1	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
AO22X0P5MA10TR	2.00	2.00
AO22X0P7MA10TR	2.00	2.00
AO22X1MA10TR	2.00	2.00
AO22X1P4MA10TR	2.00	3.20
AO22X2MA10TR	2.00	3.20
AO22X3MA10TR	2.00	4.40
AO22X4MA10TR	2.00	4.80
AO22X6MA10TR	2.00	7.40

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A0	0.0006	0.0008	0.0010	0.0015	0.0020	0.0029	0.0037	0.0058
A1	0.0007	0.0008	0.0010	0.0015	0.0019	0.0029	0.0037	0.0059
B0	0.0002	0.0002	0.0003	0.0004	0.0006	0.0009	0.0012	0.0020
B1	0.0002	0.0002	0.0003	0.0005	0.0006	0.0009	0.0012	0.0020

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A0	0.0012	0.0014	0.0016	0.0024	0.0029	0.0043	0.0050	0.0080
A1	0.0011	0.0013	0.0015	0.0025	0.0030	0.0043	0.0051	0.0080
B0	0.0013	0.0014	0.0017	0.0023	0.0028	0.0043	0.0052	0.0082
B1	0.0012	0.0014	0.0016	0.0026	0.0031	0.0042	0.0052	0.0082

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A0 → Y ↑	0.0430	0.0412	0.0382	0.0417	0.0384	0.0390	0.0377	0.0377
A0 → Y ↓	0.0543	0.0529	0.0495	0.0510	0.0476	0.0510	0.0500	0.0492
A1 → Y ↑	0.0441	0.0424	0.0396	0.0428	0.0396	0.0412	0.0398	0.0399
A1 → Y ↓	0.0582	0.0569	0.0536	0.0544	0.0510	0.0549	0.0539	0.0532
B0 → Y ↑	0.0365	0.0353	0.0327	0.0330	0.0304	0.0321	0.0312	0.0312
B0 → Y ↓	0.0448	0.0442	0.0413	0.0426	0.0398	0.0431	0.0425	0.0419
B1 → Y ↑	0.0378	0.0367	0.0342	0.0347	0.0319	0.0344	0.0334	0.0334
B1 → Y ↓	0.0486	0.0480	0.0452	0.0464	0.0435	0.0475	0.0468	0.0463

Delays at 25°C,1.0V, Typical Process (Cont'd.)

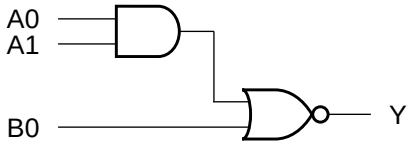
Description	K_{load} (ns/pF)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A0 → Y ↑	4.5919	3.3481	2.4128	1.6553	1.1860	0.7920	0.5875	0.3900
A0 → Y ↓	2.9034	2.0857	1.4650	1.0380	0.7295	0.4957	0.3659	0.2446
A1 → Y ↑	4.5916	3.3480	2.4127	1.6554	1.1860	0.7920	0.5875	0.3900
A1 → Y ↓	2.9139	2.0929	1.4699	1.0406	0.7314	0.4969	0.3669	0.2452
B0 → Y ↑	4.5720	3.3353	2.4046	1.6463	1.1803	0.7887	0.5852	0.3884
B0 → Y ↓	2.9055	2.0869	1.4658	1.0383	0.7297	0.4954	0.3657	0.2445
B1 → Y ↑	4.5723	3.3352	2.4047	1.6463	1.1803	0.7887	0.5853	0.3885
B1 → Y ↓	2.9138	2.0928	1.4699	1.0407	0.7314	0.4969	0.3669	0.2452

Cell Description

The AOI21 cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$Y = \overline{(A0 \bullet A1) + B0}$

Logic Symbol



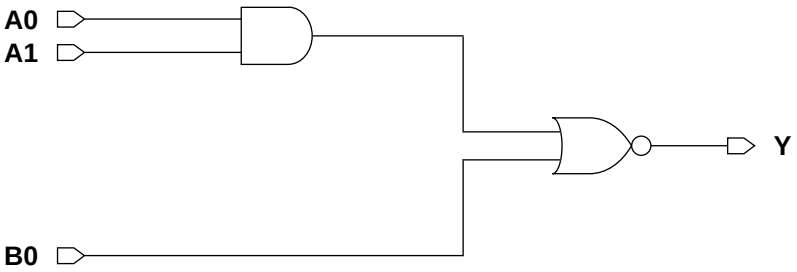
Function Table

A0	A1	B0	Y
0	x	0	1
x	0	0	1
x	x	1	0
1	1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI21X0P5MA10TR	2.00	1.20
AOI21X0P7MA10TR	2.00	1.20
AOI21X1MA10TR	2.00	1.20
AOI21X1P4MA10TR	2.00	2.00
AOI21X2MA10TR	2.00	2.00
AOI21X3MA10TR	2.00	2.60
AOI21X4MA10TR	2.00	3.40
AOI21X6MA10TR	2.00	5.00
AOI21X8MA10TR	2.00	6.60

Functional Schematic



AC Power

Pin	Power (uW/MHz)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0	0.0006	0.0007	0.0009	0.0014	0.0018	0.0027	0.0037	0.0055	0.0074
A1	0.0006	0.0007	0.0009	0.0015	0.0019	0.0027	0.0037	0.0055	0.0074
B0	0.0004	0.0005	0.0007	0.0011	0.0014	0.0019	0.0026	0.0039	0.0052

Pin Capacitance

Pin	Capacitance (pF)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0	0.0013	0.0014	0.0017	0.0027	0.0034	0.0049	0.0064	0.0096	0.0127
A1	0.0011	0.0014	0.0016	0.0029	0.0035	0.0049	0.0065	0.0097	0.0130
B0	0.0012	0.0015	0.0017	0.0024	0.0030	0.0045	0.0059	0.0086	0.0117

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0 → Y ↑	0.0231	0.0207	0.0189	0.0188	0.0177	0.0172	0.0166	0.0164	0.0164
A0 → Y ↓	0.0185	0.0166	0.0151	0.0151	0.0141	0.0132	0.0131	0.0129	0.0130
A1 → Y ↑	0.0254	0.0234	0.0218	0.0217	0.0205	0.0216	0.0212	0.0208	0.0208
A1 → Y ↓	0.0192	0.0177	0.0163	0.0165	0.0154	0.0154	0.0154	0.0152	0.0152
B0 → Y ↑	0.0196	0.0181	0.0165	0.0150	0.0145	0.0161	0.0153	0.0151	0.0153
B0 → Y ↓	0.0106	0.0099	0.0091	0.0085	0.0083	0.0088	0.0084	0.0084	0.0085

Delays at 25°C,1.0V, Typical Process (Cont'd.)

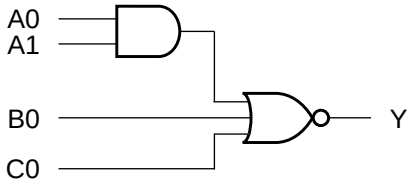
Description	K_{load} (ns/pF)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0 → Y ↑	8.7489	6.7387	4.8405	3.2760	2.3681	1.5688	1.1634	0.7718	0.5780
A0 → Y ↓	6.0713	4.6276	3.2714	2.2502	1.5870	1.0143	0.7715	0.5136	0.3861
A1 → Y ↑	8.7795	6.7719	4.8752	3.2743	2.3625	1.5896	1.1830	0.7836	0.5870
A1 → Y ↓	6.0711	4.6272	3.2712	2.2502	1.5869	1.0144	0.7714	0.5135	0.3862
B0 → Y ↑	8.7881	6.7774	4.8787	3.2760	2.3635	1.5903	1.1836	0.7840	0.5873
B0 → Y ↓	4.4454	3.4740	2.5350	1.7228	1.2566	0.8845	0.6521	0.4408	0.3345

Cell Description

The AOI211 cell provides the logical inverted OR of one AND group and two additional inputs. The output (Y) is represented by the logic equation:

$Y = \overline{(A0 \bullet A1) + B0 + C0}$

Logic Symbol



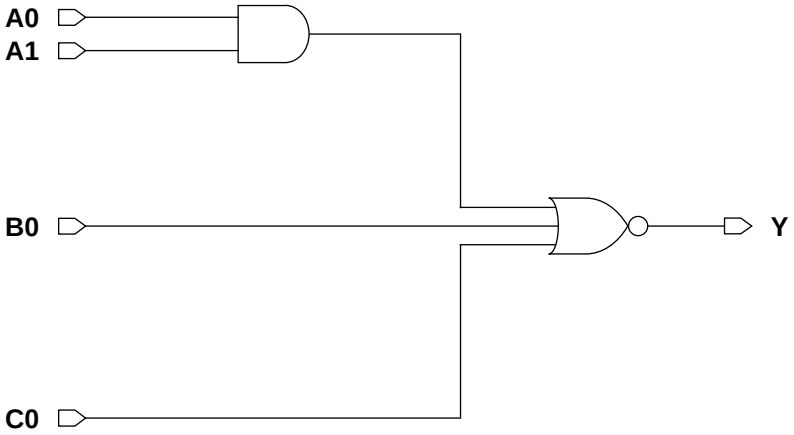
Function Table

A0	A1	B0	C0	Y
0	x	0	0	1
x	0	0	0	1
x	x	x	1	0
x	x	1	x	0
1	1	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI211X0P5MA10TR	2.00	1.40
AOI211X0P7MA10TR	2.00	1.40
AOI211X1MA10TR	2.00	1.40
AOI211X1P4MA10TR	2.00	2.40
AOI211X2MA10TR	2.00	2.40
AOI211X3MA10TR	2.00	3.40
AOI211X4MA10TR	2.00	4.20

Functional Schematic



AC Power

Pin	Power (uW/MHz)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A0	0.0005	0.0006	0.0008	0.0012	0.0015	0.0023	0.0031
A1	0.0004	0.0006	0.0008	0.0013	0.0017	0.0024	0.0033
B0	0.0002	0.0002	0.0003	0.0005	0.0006	0.0009	0.0012
C0	0.0001	0.0002	0.0003	0.0004	0.0006	0.0008	0.0011

Pin Capacitance

Pin	Capacitance (pF)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A0	0.0011	0.0014	0.0016	0.0024	0.0030	0.0046	0.0062
A1	0.0010	0.0012	0.0015	0.0026	0.0032	0.0045	0.0060
B0	0.0011	0.0012	0.0014	0.0021	0.0028	0.0040	0.0055
C0	0.0011	0.0013	0.0015	0.0021	0.0027	0.0043	0.0055

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A0 → Y ↑	0.0377	0.0332	0.0304	0.0291	0.0272	0.0266	0.0271
A0 → Y ↓	0.0268	0.0249	0.0232	0.0227	0.0213	0.0216	0.0216
A1 → Y ↑	0.0399	0.0358	0.0335	0.0319	0.0301	0.0293	0.0296
A1 → Y ↓	0.0270	0.0255	0.0241	0.0239	0.0225	0.0228	0.0226
B0 → Y ↑	0.0346	0.0300	0.0280	0.0257	0.0250	0.0242	0.0248
B0 → Y ↓	0.0123	0.0144	0.0138	0.0148	0.0144	0.0132	0.0138
C0 → Y ↑	0.0305	0.0258	0.0231	0.0198	0.0189	0.0192	0.0191
C0 → Y ↓	0.0114	0.0130	0.0120	0.0114	0.0109	0.0111	0.0113

Delays at 25°C,1.0V, Typical Process (Cont'd.)

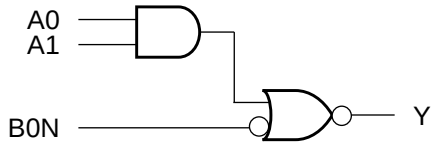
Description	K_{load} (ns/pF)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A0 → Y ↑	14.2989	10.0562	7.4713	5.0750	3.6674	2.4325	1.8154
A0 → Y ↓	8.1358	5.8851	4.4113	3.0594	2.1881	1.4983	1.1049
A1 → Y ↑	14.4234	10.1145	7.5398	5.0627	3.6538	2.4246	1.8130
A1 → Y ↓	8.1355	5.8857	4.4112	3.0594	2.1881	1.4982	1.1049
B0 → Y ↑	14.4303	10.1174	7.5415	5.0633	3.6547	2.4251	1.8134
B0 → Y ↓	4.3801	4.3386	3.3117	2.6203	1.8695	1.1575	0.8866
C0 → Y ↑	14.4380	10.1213	7.5434	5.0644	3.6551	2.4257	1.8138
C0 → Y ↓	4.5113	4.5111	3.4366	2.5066	1.7938	1.2166	0.9251

Cell Description

The AOI21B cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + \overline{B0N}}$$

Logic Symbol



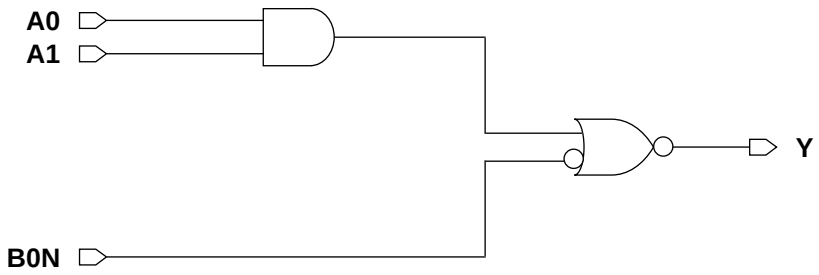
Function Table

A0	A1	B0N	Y
x	x	0	0
x	0	1	1
0	x	1	1
1	1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI21BX0P5MA10TR	2.00	1.60
AOI21BX0P7MA10TR	2.00	1.60
AOI21BX1MA10TR	2.00	1.60
AOI21BX1P4MA10TR	2.00	2.40
AOI21BX2MA10TR	2.00	2.40
AOI21BX3MA10TR	2.00	3.20
AOI21BX4MA10TR	2.00	4.00
AOI21BX6MA10TR	2.00	5.80
AOI21BX8MA10TR	2.00	7.40

Functional Schematic



AC Power

Pin	Power (uW/MHz)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A0	0.0007	0.0008	0.0011	0.0015	0.0020	0.0030	0.0040	0.0061	0.0081
A1	0.0006	0.0008	0.0010	0.0016	0.0021	0.0030	0.0040	0.0061	0.0081
B0N	0.0017	0.0017	0.0019	0.0024	0.0030	0.0041	0.0052	0.0077	0.0099

Pin Capacitance

Pin	Capacitance (pF)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A0	0.0013	0.0015	0.0018	0.0027	0.0034	0.0049	0.0064	0.0096	0.0127
A1	0.0011	0.0013	0.0016	0.0028	0.0035	0.0049	0.0065	0.0097	0.0129
B0N	0.0009	0.0009	0.0009	0.0011	0.0013	0.0016	0.0019	0.0031	0.0037

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A0 → Y ↑	0.0240	0.0219	0.0205	0.0202	0.0192	0.0187	0.0182	0.0179	0.0180
A0 → Y ↓	0.0188	0.0171	0.0154	0.0151	0.0140	0.0132	0.0131	0.0129	0.0129
A1 → Y ↑	0.0261	0.0243	0.0232	0.0229	0.0220	0.0230	0.0227	0.0223	0.0224
A1 → Y ↓	0.0192	0.0177	0.0163	0.0164	0.0153	0.0153	0.0153	0.0151	0.0152
B0N → Y ↑	0.0336	0.0328	0.0331	0.0306	0.0299	0.0306	0.0298	0.0284	0.0287
B0N → Y ↓	0.0347	0.0359	0.0386	0.0374	0.0364	0.0360	0.0360	0.0336	0.0342

Delays at 25°C,1.0V, Typical Process (Cont'd.)

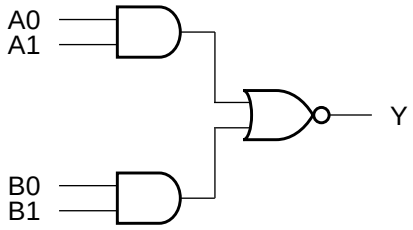
Description	K_{load} (ns/pF)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A0 → Y ↑	8.5350	6.5747	4.7234	3.2371	2.3437	1.5476	1.1515	0.7658	0.5749
A0 → Y ↓	6.0593	4.6432	3.2656	2.2505	1.5875	1.0128	0.7695	0.5136	0.3865
A1 → Y ↑	8.6353	6.6609	4.7961	3.2313	2.3385	1.5684	1.1704	0.7781	0.5842
A1 → Y ↓	6.0582	4.6430	3.2658	2.2494	1.5870	1.0128	0.7695	0.5136	0.3865
B0N → Y ↑	8.6451	6.6677	4.8007	3.2334	2.3399	1.5692	1.1709	0.7784	0.5845
B0N → Y ↓	4.4308	3.4633	2.5314	1.7250	1.2567	0.8854	0.6649	0.4412	0.3352

Cell Description

The AOI22 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + (B0 \bullet B1)}$$

Logic Symbol



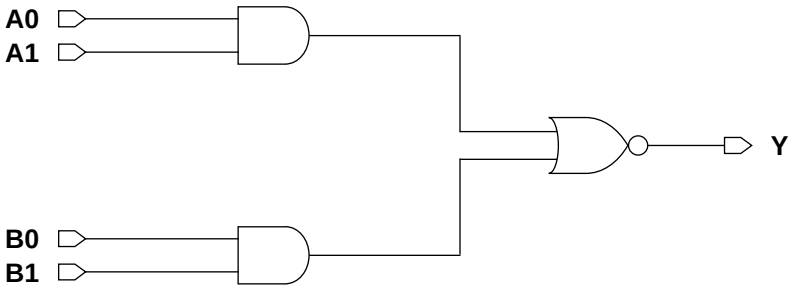
Function Table

A0	A1	B0	B1	Y
0	x	0	x	1
0	x	x	0	1
x	0	0	x	1
x	0	x	0	1
x	x	1	1	0
1	1	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI22X0P5MA10TR	2.00	1.40
AOI22X0P7MA10TR	2.00	1.40
AOI22X1MA10TR	2.00	1.40
AOI22X1P4MA10TR	2.00	2.40
AOI22X2MA10TR	2.00	2.40
AOI22X3MA10TR	2.00	3.40
AOI22X4MA10TR	2.00	4.80
AOI22X6MA10TR	2.00	6.80
AOI22X8MA10TR	2.00	9.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A0	0.0006	0.0007	0.0010	0.0015	0.0021	0.0031	0.0042	0.0063	0.0084
A1	0.0006	0.0007	0.0010	0.0015	0.0021	0.0031	0.0041	0.0063	0.0084
B0	0.0001	0.0002	0.0002	0.0003	0.0005	0.0007	0.0010	0.0015	0.0020
B1	0.0001	0.0002	0.0002	0.0003	0.0005	0.0007	0.0010	0.0015	0.0020

Pin Capacitance

Pin	Capacitance (pF)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A0	0.0012	0.0014	0.0018	0.0026	0.0034	0.0050	0.0066	0.0099	0.0132
A1	0.0011	0.0013	0.0016	0.0027	0.0034	0.0050	0.0066	0.0100	0.0133
B0	0.0012	0.0015	0.0018	0.0027	0.0034	0.0052	0.0069	0.0104	0.0138
B1	0.0012	0.0014	0.0017	0.0029	0.0036	0.0052	0.0069	0.0104	0.0139

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A0 → Y ↑	0.0303	0.0283	0.0261	0.0274	0.0253	0.0256	0.0249	0.0248	0.0247
A0 → Y ↓	0.0229	0.0212	0.0193	0.0208	0.0189	0.0181	0.0173	0.0175	0.0175
A1 → Y ↑	0.0326	0.0310	0.0289	0.0301	0.0279	0.0290	0.0297	0.0296	0.0295
A1 → Y ↓	0.0236	0.0220	0.0204	0.0219	0.0201	0.0202	0.0199	0.0199	0.0198
B0 → Y ↑	0.0203	0.0193	0.0177	0.0197	0.0180	0.0189	0.0193	0.0192	0.0192
B0 → Y ↓	0.0136	0.0128	0.0115	0.0133	0.0119	0.0116	0.0111	0.0112	0.0112
B1 → Y ↑	0.0238	0.0229	0.0213	0.0228	0.0210	0.0224	0.0233	0.0232	0.0233
B1 → Y ↓	0.0151	0.0143	0.0131	0.0147	0.0133	0.0138	0.0135	0.0136	0.0136

Delays at 25°C,1.0V, Typical Process (Cont'd.)

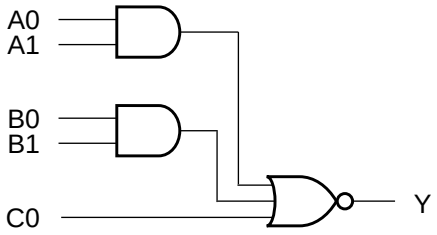
Description	K_{load} (ns/pF)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A0 → Y ↑	8.7012	6.7107	4.8192	3.2805	2.3591	1.5738	1.1617	0.7730	0.5797
A0 → Y ↓	5.9658	4.5443	3.2088	2.2441	1.5823	1.0130	0.7503	0.5020	0.3781
A1 → Y ↑	8.7487	6.7681	4.8630	3.2763	2.3555	1.5550	1.1734	0.7819	0.5867
A1 → Y ↓	5.9642	4.5436	3.2088	2.2439	1.5821	1.0129	0.7502	0.5020	0.3781
B0 → Y ↑	8.6395	6.6816	4.7978	3.2839	2.3689	1.5740	1.1819	0.7875	0.5910
B0 → Y ↓	5.7070	4.3721	3.0982	2.2404	1.5857	1.0123	0.7622	0.5085	0.3821
B1 → Y ↑	8.7524	6.7710	4.8639	3.2778	2.3530	1.5505	1.1680	0.7782	0.5844
B1 → Y ↓	5.7063	4.3716	3.0979	2.2402	1.5856	1.0122	0.7620	0.5083	0.3820

Cell Description

The AOI221 cell provides the logical inverted OR of two AND groups and a third input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + (B0 \bullet B1) + C0}$$

Logic Symbol



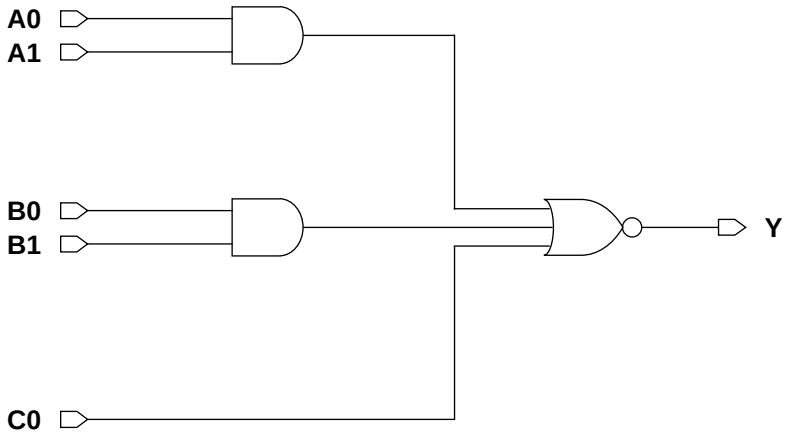
Function Table

A0	A1	B0	B1	C0	Y
0	x	0	x	0	1
0	x	x	0	0	1
x	0	0	x	0	1
x	0	x	0	0	1
x	x	x	x	1	0
x	x	1	1	x	0
1	1	x	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI221X0P5MA10TR	2.00	1.80
AOI221X0P7MA10TR	2.00	1.80
AOI221X1MA10TR	2.00	1.80
AOI221X1P4MA10TR	2.00	3.20
AOI221X2MA10TR	2.00	3.20
AOI221X3MA10TR	2.00	4.40
AOI221X4MA10TR	2.00	5.80

Functional Schematic



AC Power

Pin	Power (uW/MHz)						
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M
A0	0.0004	0.0006	0.0008	0.0013	0.0016	0.0025	0.0032
A1	0.0004	0.0006	0.0008	0.0012	0.0017	0.0024	0.0034
B0	0.0002	0.0002	0.0003	0.0005	0.0006	0.0009	0.0012
B1	0.0002	0.0002	0.0003	0.0004	0.0006	0.0009	0.0012
C0	0.0004	0.0005	0.0006	0.0009	0.0012	0.0016	0.0023

Pin Capacitance

Pin	Capacitance (pF)						
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M
A0	0.0011	0.0013	0.0016	0.0026	0.0031	0.0046	0.0064
A1	0.0010	0.0012	0.0015	0.0022	0.0031	0.0044	0.0062
B0	0.0011	0.0013	0.0016	0.0025	0.0031	0.0047	0.0064
B1	0.0010	0.0013	0.0015	0.0022	0.0031	0.0045	0.0062
C0	0.0011	0.0013	0.0015	0.0021	0.0028	0.0041	0.0054

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)						
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M
A0 → Y ↑	0.0491	0.0432	0.0408	0.0385	0.0390	0.0367	0.0373
A0 → Y ↓	0.0331	0.0298	0.0285	0.0288	0.0277	0.0264	0.0267
A1 → Y ↑	0.0515	0.0461	0.0440	0.0408	0.0415	0.0393	0.0395
A1 → Y ↓	0.0335	0.0308	0.0294	0.0293	0.0288	0.0273	0.0275
B0 → Y ↑	0.0419	0.0362	0.0338	0.0323	0.0325	0.0303	0.0310
B0 → Y ↓	0.0262	0.0230	0.0214	0.0218	0.0208	0.0199	0.0201
B1 → Y ↑	0.0456	0.0397	0.0373	0.0345	0.0354	0.0328	0.0335
B1 → Y ↓	0.0276	0.0245	0.0228	0.0226	0.0219	0.0209	0.0209
C0 → Y ↑	0.0322	0.0272	0.0258	0.0210	0.0228	0.0218	0.0219
C0 → Y ↓	0.0120	0.0135	0.0130	0.0118	0.0122	0.0117	0.0117

Delays at 25°C,1.0V, Typical Process (Cont'd.)

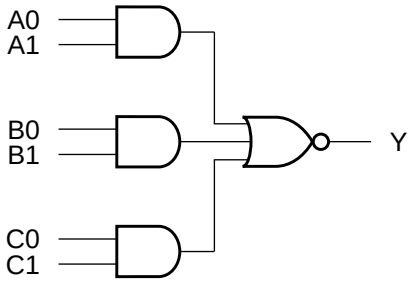
Description	K_{load} (ns/pF)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A0 → Y ↑	13.9374	9.8619	7.3653	4.9387	3.5741	2.3820	1.7688
A0 → Y ↓	8.3988	5.9992	4.4564	3.1672	2.2159	1.4585	1.0959
A1 → Y ↑	13.9996	9.8879	7.4157	4.9491	3.5659	2.3704	1.7663
A1 → Y ↓	8.3985	5.9992	4.4564	3.1671	2.2159	1.4585	1.0957
B0 → Y ↑	14.0043	9.8862	7.3911	4.9574	3.5745	2.3764	1.7694
B0 → Y ↓	8.2972	5.9280	4.4090	3.1412	2.1546	1.4531	1.0804
B1 → Y ↑	14.0018	9.8891	7.4164	4.9493	3.5660	2.3726	1.7662
B1 → Y ↓	8.2972	5.9279	4.4089	3.1410	2.1545	1.4531	1.0803
C0 → Y ↑	14.0112	9.8930	7.4190	4.9509	3.5672	2.3732	1.7668
C0 → Y ↓	4.6326	4.6318	3.5376	2.5754	1.7972	1.2061	0.8864

Cell Description

The AOI222 cell provides the logical inverted OR of three AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1) + (B0 \bullet B1) + (C0 \bullet C1)}$$

Logic Symbol



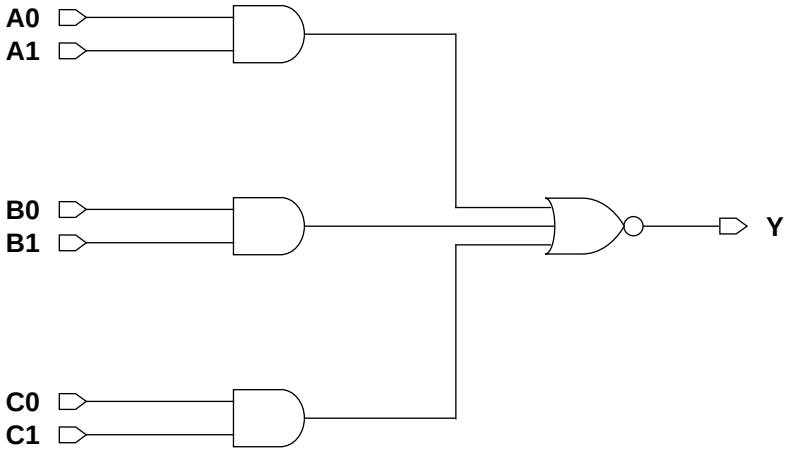
Function Table

A0	A1	B0	B1	C0	C1	Y
0	x	0	x	0	x	1
0	x	0	x	x	0	1
0	x	x	0	0	x	1
0	x	x	0	x	0	1
x	0	0	x	0	x	1
x	0	0	x	x	0	1
x	0	x	0	0	x	1
x	0	x	0	x	0	1
x	x	x	x	1	1	0
x	x	1	1	x	x	0
1	1	x	x	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI222X0P5MA10TR	2.00	2.20
AOI222X0P7MA10TR	2.00	2.20
AOI222X1MA10TR	2.00	2.20
AOI222X1P4MA10TR	2.00	3.60
AOI222X2MA10TR	2.00	3.60
AOI222X3MA10TR	2.00	5.20
AOI222X4MA10TR	2.00	6.80

Functional Schematic



AC Power

Pin	Power (uW/MHz)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A0	0.0004	0.0006	0.0008	0.0013	0.0016	0.0025	0.0032
A1	0.0004	0.0006	0.0008	0.0012	0.0017	0.0024	0.0034
B0	0.0002	0.0002	0.0003	0.0005	0.0006	0.0009	0.0012
B1	0.0002	0.0002	0.0003	0.0004	0.0006	0.0009	0.0012
C0	0.0001	0.0001	0.0001	0.0002	0.0003	0.0004	0.0005
C1	0.0001	0.0001	0.0001	0.0002	0.0003	0.0004	0.0005

Pin Capacitance

Pin	Capacitance (pF)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A0	0.0011	0.0013	0.0017	0.0025	0.0030	0.0046	0.0062
A1	0.0010	0.0012	0.0015	0.0022	0.0032	0.0044	0.0063
B0	0.0011	0.0013	0.0016	0.0025	0.0031	0.0045	0.0062
B1	0.0010	0.0012	0.0015	0.0022	0.0032	0.0044	0.0062
C0	0.0011	0.0013	0.0017	0.0025	0.0031	0.0048	0.0064
C1	0.0011	0.0013	0.0016	0.0022	0.0034	0.0046	0.0066

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A0 → Y ↑	0.0586	0.0541	0.0513	0.0491	0.0481	0.0461	0.0468
A0 → Y ↓	0.0412	0.0391	0.0368	0.0343	0.0341	0.0338	0.0340
A1 → Y ↑	0.0612	0.0569	0.0542	0.0516	0.0510	0.0486	0.0494
A1 → Y ↓	0.0417	0.0398	0.0375	0.0351	0.0353	0.0347	0.0351
B0 → Y ↑	0.0512	0.0465	0.0440	0.0419	0.0414	0.0396	0.0402
B0 → Y ↓	0.0323	0.0300	0.0280	0.0264	0.0265	0.0261	0.0261
B1 → Y ↑	0.0538	0.0493	0.0468	0.0448	0.0444	0.0422	0.0430
B1 → Y ↓	0.0332	0.0310	0.0290	0.0277	0.0277	0.0272	0.0271
C0 → Y ↑	0.0324	0.0288	0.0273	0.0260	0.0256	0.0247	0.0254
C0 → Y ↓	0.0205	0.0191	0.0176	0.0175	0.0163	0.0161	0.0162
C1 → Y ↑	0.0355	0.0319	0.0304	0.0274	0.0293	0.0273	0.0288

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
C1 → Y ↓	0.0215	0.0200	0.0186	0.0180	0.0177	0.0171	0.0176

Delays at 25°C,1.0V, Typical Process (Cont'd.)

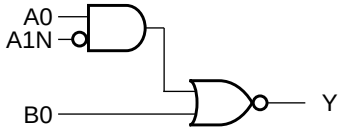
Description	K_{load} (ns/pF)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A0 → Y ↑	13.6955	10.0383	7.2746	4.9357	3.5777	2.3657	1.7629
A0 → Y ↓	8.3637	6.2127	4.4386	2.8971	2.1532	1.4556	1.0853
A1 → Y ↑	13.7555	10.0824	7.3222	4.9326	3.5699	2.3544	1.7595
A1 → Y ↓	8.3635	6.2125	4.4384	2.8972	2.1536	1.4554	1.0854
B0 → Y ↑	13.7725	10.0733	7.3058	4.9143	3.5814	2.3624	1.7636
B0 → Y ↓	8.2225	6.1098	4.3720	2.8785	2.1566	1.4525	1.0777
B1 → Y ↑	13.7546	10.0833	7.3222	4.9328	3.5700	2.3567	1.7596
B1 → Y ↓	8.2221	6.1097	4.3719	2.8784	2.1565	1.4524	1.0777
C0 → Y ↑	13.6511	10.0058	7.2475	4.9531	3.5495	2.3644	1.7573
C0 → Y ↓	8.0549	6.2674	4.4681	3.2062	2.1713	1.4693	1.0902
C1 → Y ↑	13.7589	10.0858	7.3236	4.9290	3.5709	2.3569	1.7599
C1 → Y ↓	8.0536	6.2666	4.4675	3.2055	2.1712	1.4691	1.0901

Cell Description

The AOI2XB1cell provides the logical inverted OR of two AND group consisting of three inputs: (A0, A1N) and (B0). The output (Y) is represented by the logic equation:

$Y = \overline{(A0 \bullet \overline{A1N}) + (B0)}$

Logic Symbol



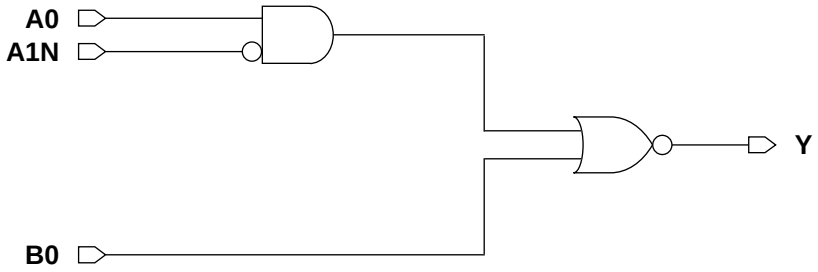
Function Table

A0	A1N	B0	Y
0	x	0	1
x	1	0	1
x	x	1	0
1	0	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI2XB1X0P5MA10TR	2.00	1.60
AOI2XB1X0P7MA10TR	2.00	1.60
AOI2XB1X1MA10TR	2.00	1.60
AOI2XB1X1P4MA10TR	2.00	2.40
AOI2XB1X2MA10TR	2.00	2.40
AOI2XB1X3MA10TR	2.00	3.20
AOI2XB1X4MA10TR	2.00	4.20
AOI2XB1X6MA10TR	2.00	5.80
AOI2XB1X8MA10TR	2.00	7.60

Functional Schematic



AC Power

Pin	Power (uW/MHz)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0	0.0006	0.0007	0.0009	0.0014	0.0018	0.0028	0.0038	0.0057	0.0076
A1N	0.0015	0.0016	0.0017	0.0025	0.0031	0.0042	0.0055	0.0080	0.0109
B0	0.0007	0.0008	0.0010	0.0016	0.0021	0.0028	0.0037	0.0056	0.0074

Pin Capacitance

Pin	Capacitance (pF)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0	0.0013	0.0015	0.0017	0.0027	0.0034	0.0049	0.0064	0.0096	0.0128
A1N	0.0009	0.0009	0.0009	0.0011	0.0013	0.0017	0.0025	0.0033	0.0045
B0	0.0012	0.0014	0.0017	0.0024	0.0031	0.0045	0.0059	0.0087	0.0117

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0 → Y ↑	0.0228	0.0209	0.0189	0.0187	0.0178	0.0173	0.0167	0.0164	0.0164
A0 → Y ↓	0.0182	0.0167	0.0150	0.0149	0.0141	0.0133	0.0131	0.0129	0.0130
A1N → Y ↑	0.0397	0.0394	0.0392	0.0407	0.0393	0.0377	0.0368	0.0359	0.0368
A1N → Y ↓	0.0407	0.0415	0.0427	0.0447	0.0435	0.0416	0.0405	0.0397	0.0404
B0 → Y ↑	0.0186	0.0175	0.0160	0.0149	0.0145	0.0160	0.0152	0.0150	0.0152
B0 → Y ↓	0.0102	0.0098	0.0090	0.0085	0.0084	0.0088	0.0084	0.0084	0.0086

Delays at 25°C,1.0V, Typical Process (Cont'd.)

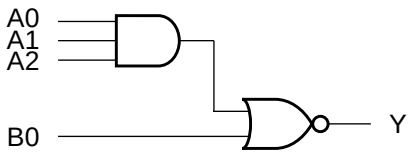
Description	K_{load} (ns/pF)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0 → Y ↑	8.6737	6.6784	4.7972	3.2650	2.3628	1.5632	1.1636	0.7713	0.5779
A0 → Y ↓	6.0476	4.6134	3.2593	2.2449	1.5836	1.0115	0.7705	0.5129	0.3856
A1N → Y ↑	8.6628	6.6803	4.8102	3.2546	2.3516	1.5728	1.1709	0.7788	0.5841
A1N → Y ↓	6.0503	4.6170	3.2624	2.2480	1.5857	1.0125	0.7712	0.5133	0.3860
B0 → Y ↑	8.6712	6.6849	4.8126	3.2561	2.3524	1.5732	1.1713	0.7790	0.5843
B0 → Y ↓	4.4381	3.4672	2.5342	1.7241	1.2555	0.8849	0.6514	0.4408	0.3346

Cell Description

The AOI31 cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1 \bullet A2) + B0}$$

Logic Symbol



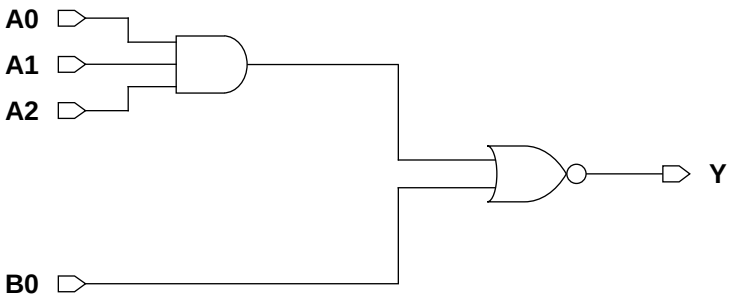
Function Table

A0	A1	A2	B0	Y
0	x	x	0	1
x	0	x	0	1
x	x	0	0	1
x	x	x	1	0
1	1	1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI31X0P5MA10TR	2.00	1.40
AOI31X0P7MA10TR	2.00	1.40
AOI31X1MA10TR	2.00	1.40
AOI31X1P4MA10TR	2.00	2.60
AOI31X2MA10TR	2.00	2.60
AOI31X3MA10TR	2.00	3.40
AOI31X4MA10TR	2.00	4.80
AOI31X6MA10TR	2.00	6.80

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A0	0.0005	0.0006	0.0008	0.0013	0.0017	0.0027	0.0035	0.0053
A1	0.0005	0.0006	0.0008	0.0013	0.0017	0.0027	0.0035	0.0054
A2	0.0006	0.0007	0.0009	0.0013	0.0017	0.0027	0.0035	0.0053
B0	0.0005	0.0006	0.0008	0.0013	0.0018	0.0024	0.0035	0.0051

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A0	0.0013	0.0016	0.0019	0.0027	0.0035	0.0053	0.0070	0.0107
A1	0.0012	0.0014	0.0017	0.0026	0.0034	0.0052	0.0068	0.0104
A2	0.0012	0.0014	0.0017	0.0027	0.0035	0.0052	0.0070	0.0105
B0	0.0012	0.0014	0.0017	0.0023	0.0029	0.0043	0.0056	0.0087

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A0 → Y ↑	0.0256	0.0239	0.0216	0.0225	0.0205	0.0196	0.0196	0.0198
A0 → Y ↓	0.0216	0.0199	0.0175	0.0175	0.0160	0.0151	0.0152	0.0154
A1 → Y ↑	0.0285	0.0271	0.0253	0.0277	0.0256	0.0252	0.0252	0.0251
A1 → Y ↓	0.0232	0.0217	0.0196	0.0212	0.0195	0.0189	0.0191	0.0191
A2 → Y ↑	0.0328	0.0314	0.0296	0.0338	0.0313	0.0303	0.0303	0.0304
A2 → Y ↓	0.0246	0.0232	0.0211	0.0237	0.0219	0.0208	0.0211	0.0211
B0 → Y ↑	0.0260	0.0246	0.0231	0.0248	0.0230	0.0230	0.0225	0.0229
B0 → Y ↓	0.0111	0.0104	0.0097	0.0098	0.0090	0.0093	0.0090	0.0092

Delays at 25°C,1.0V, Typical Process (Cont'd.)

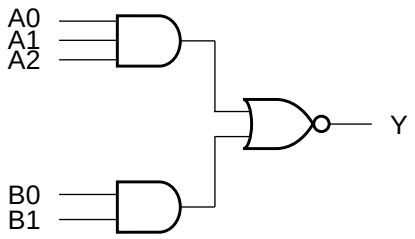
Description	K_{load} (ns/pF)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A0 → Y ↑	8.5637	6.9211	4.9714	3.4808	2.4847	1.6317	1.2198	0.8095
A0 → Y ↓	6.6249	5.2438	3.6398	2.5217	1.7931	1.1503	0.8734	0.5800
A1 → Y ↑	8.6357	6.9856	5.0289	3.4731	2.4865	1.6365	1.2219	0.8121
A1 → Y ↓	6.6237	5.2438	3.6395	2.5213	1.7932	1.1504	0.8732	0.5799
A2 → Y ↑	8.7181	7.0668	5.0898	3.5131	2.5195	1.6609	1.2354	0.8229
A2 → Y ↓	6.6235	5.2433	3.6393	2.5214	1.7932	1.1503	0.8732	0.5799
B0 → Y ↑	8.7269	7.0715	5.0929	3.5148	2.5204	1.6617	1.2360	0.8233
B0 → Y ↓	4.3572	3.5520	2.6149	1.9405	1.3585	0.9515	0.7054	0.4733

Cell Description

The AOI32 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 \bullet A1 \bullet A2) + (B0 \bullet B1)}$$

Logic Symbol



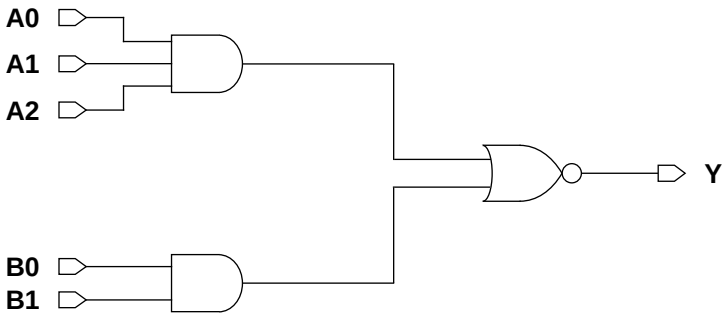
Function Table

A0	A1	A2	B0	B1	Y
0	x	x	0	x	1
0	x	x	x	0	1
x	0	x	0	x	1
x	0	x	x	0	1
x	x	0	0	x	1
x	x	0	x	0	1
x	x	x	1	1	0
1	1	1	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
AOI32X0P5MA10TR	2.00	1.60
AOI32X0P7MA10TR	2.00	1.60
AOI32X1MA10TR	2.00	1.60
AOI32X1P4MA10TR	2.00	3.00
AOI32X2MA10TR	2.00	3.00
AOI32X3MA10TR	2.00	4.20
AOI32X4MA10TR	2.00	6.00
AOI32X6MA10TR	2.00	8.60

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M
A0	0.0005	0.0007	0.0009	0.0014	0.0019	0.0030	0.0040	0.0060
A1	0.0005	0.0007	0.0009	0.0014	0.0018	0.0028	0.0038	0.0057
A2	0.0006	0.0007	0.0009	0.0015	0.0020	0.0029	0.0038	0.0058
B0	0.0001	0.0002	0.0003	0.0004	0.0006	0.0009	0.0012	0.0018
B1	0.0001	0.0002	0.0003	0.0004	0.0006	0.0009	0.0011	0.0018

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M
A0	0.0012	0.0015	0.0018	0.0028	0.0036	0.0053	0.0070	0.0105
A1	0.0012	0.0014	0.0017	0.0028	0.0035	0.0052	0.0069	0.0102
A2	0.0011	0.0014	0.0017	0.0031	0.0038	0.0052	0.0070	0.0105
B0	0.0012	0.0014	0.0017	0.0026	0.0033	0.0051	0.0068	0.0101
B1	0.0011	0.0013	0.0016	0.0027	0.0033	0.0049	0.0066	0.0099

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M
A0 → Y ↑	0.0330	0.0298	0.0278	0.0301	0.0280	0.0278	0.0291	0.0285
A0 → Y ↓	0.0271	0.0238	0.0216	0.0228	0.0206	0.0199	0.0208	0.0206
A1 → Y ↑	0.0364	0.0336	0.0317	0.0335	0.0316	0.0334	0.0347	0.0342
A1 → Y ↓	0.0294	0.0262	0.0241	0.0251	0.0230	0.0237	0.0247	0.0245
A2 → Y ↑	0.0405	0.0377	0.0359	0.0378	0.0357	0.0387	0.0403	0.0397
A2 → Y ↓	0.0307	0.0276	0.0255	0.0270	0.0249	0.0255	0.0267	0.0265
B0 → Y ↑	0.0265	0.0247	0.0234	0.0247	0.0237	0.0251	0.0263	0.0259
B0 → Y ↓	0.0144	0.0131	0.0119	0.0131	0.0120	0.0113	0.0121	0.0119
B1 → Y ↑	0.0301	0.0284	0.0270	0.0275	0.0263	0.0298	0.0315	0.0310
B1 → Y ↓	0.0160	0.0146	0.0134	0.0145	0.0133	0.0135	0.0146	0.0143

Delays at 25°C,1.0V, Typical Process (Cont'd.)

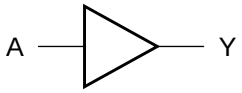
Description	K_{load} (ns/pF)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A0 → Y ↑	9.4995	7.0110	5.0645	3.4036	2.4599	1.6297	1.2321	0.8177
A0 → Y ↓	7.2848	5.2306	3.6652	2.4226	1.6964	1.1464	0.8744	0.5858
A1 → Y ↑	9.4650	7.0053	5.0488	3.3899	2.4406	1.6343	1.2347	0.8210
A1 → Y ↓	7.2839	5.2304	3.6652	2.4223	1.6962	1.1462	0.8743	0.5857
A2 → Y ↑	9.5177	7.0402	5.0701	3.3935	2.4459	1.6564	1.2504	0.8315
A2 → Y ↓	7.2840	5.2309	3.6651	2.4224	1.6963	1.1462	0.8743	0.5857
B0 → Y ↑	9.3663	6.9211	4.9773	3.4074	2.4595	1.6311	1.2252	0.8169
B0 → Y ↓	6.3522	4.7173	3.3291	2.3252	1.6380	1.0430	0.8041	0.5366
B1 → Y ↑	9.5222	7.0430	5.0717	3.3947	2.4418	1.6567	1.2508	0.8317
B1 → Y ↓	6.3518	4.7169	3.3287	2.3251	1.6379	1.0428	0.8040	0.5365

Cell Description

The BUF cell provides the logical buffer of a single input (A). The output (Y) is represented by the logic equation:

$Y = A$

Logic Symbol



Function Table

A	Y
0	0
1	1

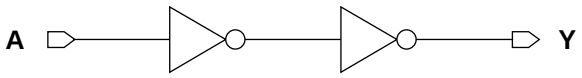
Cell Size

Drive Strength	Height (um)	Width (um)
BUFX0P7BA10TR	2.00	0.80
BUFX0P7MA10TR	2.00	0.80
BUFX0P8BA10TR	2.00	0.80
BUFX0P8MA10TR	2.00	0.80
BUFX1BA10TR	2.00	0.80
BUFX1MA10TR	2.00	0.80
BUFX1P2BA10TR	2.00	1.20
BUFX1P2MA10TR	2.00	1.20
BUFX1P4BA10TR	2.00	1.20
BUFX1P4MA10TR	2.00	1.20
BUFX1P7BA10TR	2.00	1.20
BUFX1P7MA10TR	2.00	1.20
BUFX2BA10TR	2.00	1.20
BUFX2MA10TR	2.00	1.20
BUFX2P5BA10TR	2.00	1.40
BUFX2P5MA10TR	2.00	1.40
BUFX3BA10TR	2.00	1.40
BUFX3MA10TR	2.00	1.40
BUFX3P5BA10TR	2.00	2.00
BUFX3P5MA10TR	2.00	2.00

Cell Size (Cont'd.)

Drive Strength	Height (um)	Width (um)
BUFX4BA10TR	2.00	2.00
BUFX4MA10TR	2.00	2.00
BUFX5BA10TR	2.00	2.20
BUFX5MA10TR	2.00	2.20
BUFX6BA10TR	2.00	2.40
BUFX6MA10TR	2.00	2.40
BUFX7P5BA10TR	2.00	3.20
BUFX7P5MA10TR	2.00	3.20
BUFX9BA10TR	2.00	3.40
BUFX9MA10TR	2.00	3.40
BUFX11BA10TR	2.00	4.20
BUFX11MA10TR	2.00	4.20
BUFX13BA10TR	2.00	4.80
BUFX13MA10TR	2.00	4.80
BUFX16BA10TR	2.00	5.80
BUFX16MA10TR	2.00	5.80

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P7B	**X0P7M**	**X0P8B**	**X0P8M**	**X1P0B**	**X1P0M**	**X1P2B**	**X1P2M**
A	0.0024	0.0025	0.0025	0.0026	0.0026	0.0028	0.0032	0.0035

AC Power (Cont'd.)

Pin	Power (uW/MHz)							
	X1P4B	**X1P4M**	**X1P7B**	**X1P7M**	**X2P0B**	**X2P0M**	**X2P5B**	**X2P5M**
A	0.0035	0.0039	0.0039	0.0045	0.0044	0.0049	0.0055	0.0065

AC Power (Cont'd.)

Pin	Power (uW/MHz)							
	X3P0B	**X3P0M**	**X3P5B**	**X3P5M**	**X4P0B**	**X4P0M**	**X5P0B**	**X5P0M**
A	0.0064	0.0073	0.0074	0.0086	0.0082	0.0094	0.0102	0.0119

AC Power (Cont'd.)

Pin	Power (uW/MHz)							
	X6P0B	**X6P0M**	**X7P5B**	**X7P5M**	**X9P0B**	**X9P0M**	**X11P0B**	**X11P0M**
A	0.0120	0.0139	0.0158	0.0183	0.0183	0.0215	0.0226	0.0263

AC Power (Cont'd.)

Pin	Power (uW/MHz)			
	X13P0B	**X13P0M**	**X16P0B**	**X16P0M**
A	0.0267	0.0307	0.0325	0.0376

Pin Capacitance

Pin	Capacitance (pF)							
	X0P7B	**X0P7M**	**X0P8B**	**X0P8M**	**X1P0B**	**X1P0M**	**X1P2B**	**X1P2M**
A	0.0011	0.0010	0.0011	0.0010	0.0010	0.0009	0.0010	0.0011

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)							
	X1P4B	**X1P4M**	**X1P7B**	**X1P7M**	**X2P0B**	**X2P0M**	**X2P5B**	**X2P5M**
A	0.0011	0.0012	0.0012	0.0013	0.0013	0.0014	0.0015	0.0017

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)							
	X3P0B	**X3P0M**	**X3P5B**	**X3P5M**	**X4P0B**	**X4P0M**	**X5P0B**	**X5P0M**
A	0.0017	0.0018	0.0022	0.0024	0.0024	0.0025	0.0027	0.0031

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)							
	X6P0B	**X6P0M**	**X7P5B**	**X7P5M**	**X9P0B**	**X9P0M**	**X11P0B**	**X11P0M**
A	0.0030	0.0034	0.0040	0.0045	0.0045	0.0051	0.0057	0.0065

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)			
	X13P0B	**X13P0M**	**X16P0B**	**X16P0M**
A	0.0065	0.0072	0.0077	0.0087

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P7B	**X0P7M**	**X0P8B**	**X0P8M**	**X1P0B**	**X1P0M**	**X1P2B**	**X1P2M**
A → Y ↑	0.0245	0.0255	0.0246	0.0259	0.0253	0.0248	0.0285	0.0249
A → Y ↓	0.0281	0.0340	0.0287	0.0353	0.0306	0.0341	0.0333	0.0342

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)							
	X1P4B	**X1P4M**	**X1P7B**	**X1P7M**	**X2P0B**	**X2P0M**	**X2P5B**	**X2P5M**
A → Y ↑	0.0287	0.0246	0.0274	0.0245	0.0274	0.0235	0.0272	0.0241
A → Y ↓	0.0331	0.0341	0.0321	0.0343	0.0316	0.0330	0.0309	0.0333

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)							
	X3P0B	**X3P0M**	**X3P5B**	**X3P5M**	**X4P0B**	**X4P0M**	**X5P0B**	**X5P0M**
A → Y ↑	0.0272	0.0234	0.0252	0.0227	0.0255	0.0224	0.0255	0.0223
A → Y ↓	0.0312	0.0327	0.0291	0.0312	0.0290	0.0305	0.0289	0.0306

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)							
	X6P0B	**X6P0M**	**X7P5B**	**X7P5M**	**X9P0B**	**X9P0M**	**X11P0B**	**X11P0M**
A → Y ↑	0.0255	0.0221	0.0265	0.0232	0.0265	0.0231	0.0260	0.0225
A → Y ↓	0.0289	0.0306	0.0296	0.0313	0.0291	0.0311	0.0289	0.0306

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)			
	X13P0B	**X13P0M**	**X16P0B**	**X16P0M**
A → Y ↑	0.0261	0.0224	0.0262	0.0227
A → Y ↓	0.0292	0.0305	0.0293	0.0308

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X0P7B	**X0P7M**	**X0P8B**	**X0P8M**	**X1P0B**	**X1P0M**	**X1P2B**	**X1P2M**
A → Y ↑	3.4444	3.4970	3.0413	3.0818	2.5067	2.5254	1.9133	1.9134
A → Y ↓	3.0310	2.1942	2.7217	1.9099	2.2322	1.5443	1.6896	1.1960

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X1P4B	**X1P4M**	**X1P7B**	**X1P7M**	**X2P0B**	**X2P0M**	**X2P5B**	**X2P5M**
A → Y ↑	1.6547	1.6550	1.3780	1.3784	1.1896	1.1895	0.9320	0.9315
A → Y ↓	1.4603	1.0331	1.2377	0.8462	1.0524	0.7210	0.8442	0.5772

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X3P0B	**X3P0M**	**X3P5B**	**X3P5M**	**X4P0B**	**X4P0M**	**X5P0B**	**X5P0M**
A → Y ↑	0.7890	0.7885	0.6575	0.6575	0.5843	0.5842	0.4666	0.4663
A → Y ↓	0.7085	0.4846	0.6003	0.4087	0.5253	0.3613	0.4243	0.2898

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X6P0B	**X6P0M**	**X7P5B**	**X7P5M**	**X9P0B**	**X9P0M**	**X11P0B**	**X11P0M**
A → Y ↑	0.3865	0.3862	0.3049	0.3046	0.2569	0.2568	0.2092	0.2091
A → Y ↓	0.3485	0.2389	0.2781	0.1906	0.2340	0.1606	0.1920	0.1307

Delays at 25°C,1.0V, Typical Process (Cont'd.)

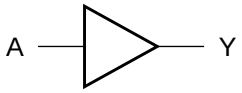
Description	K_{load} (ns/pF)			
	X13P0B	**X13P0M**	**X16P0B**	**X16P0M**
A → Y ↑	0.1766	0.1764	0.1431	0.1430
A → Y ↓	0.1617	0.1103	0.1307	0.0915

Cell Description

The BUFH cell is a high-speed buffer of a single input (A). The output (Y) is represented by the logic equation:

$Y = A$

Logic Symbol



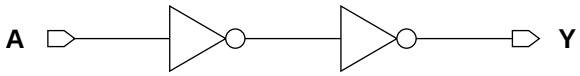
Function Table

A	Y
0	0
1	1

Cell Size

Drive Strength	Height (um)	Width (um)
BUFHX0P7MA10TR	2.00	0.80
BUFHX0P8MA10TR	2.00	0.80
BUFHX1MA10TR	2.00	0.80
BUFHX1P2MA10TR	2.00	1.20
BUFHX1P4MA10TR	2.00	1.20
BUFHX1P7MA10TR	2.00	1.20
BUFHX2MA10TR	2.00	1.40
BUFHX2P5MA10TR	2.00	1.60
BUFHX3MA10TR	2.00	1.60
BUFHX3P5MA10TR	2.00	2.20
BUFHX4MA10TR	2.00	2.20
BUFHX5MA10TR	2.00	2.40
BUFHX6MA10TR	2.00	3.00
BUFHX7P5MA10TR	2.00	3.80
BUFHX9MA10TR	2.00	4.20
BUFHX11MA10TR	2.00	5.00
BUFHX13MA10TR	2.00	5.80
BUFHX16MA10TR	2.00	7.20

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P7M	X0P8M	X1P0M	X1P2M	X1P4M	X1P7M	X2P0M	X2P5M
A	0.0028	0.0030	0.0033	0.0041	0.0045	0.0050	0.0057	0.0075

AC Power (Cont'd.)

Pin	Power (uW/MHz)							
	X3P0M	X3P5M	X4P0M	X5P0M	X6P0M	X7P5M	X9P0M	X11P0M
A	0.0084	0.0104	0.0113	0.0141	0.0166	0.0213	0.0252	0.0309

AC Power (Cont'd.)

Pin	Power (uW/MHz)	
	X13P0M	X16P0M
A	0.0362	0.0441

Pin Capacitance

Pin	Capacitance (pF)							
	X0P7M	X0P8M	X1P0M	X1P2M	X1P4M	X1P7M	X2P0M	X2P5M
A	0.0013	0.0014	0.0015	0.0017	0.0018	0.0019	0.0025	0.0031

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)							
	X3P0M	X3P5M	X4P0M	X5P0M	X6P0M	X7P5M	X9P0M	X11P0M
A	0.0035	0.0043	0.0047	0.0055	0.0067	0.0084	0.0101	0.0121

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)	
	X13P0M	X16P0M
A	0.0143	0.0175

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P7M	**X0P8M**	**X1P0M**	**X1P2M**	**X1P4M**	**X1P7M**	**X2P0M**	**X2P5M**
A → Y ↑	0.0209	0.0202	0.0193	0.0194	0.0191	0.0185	0.0170	0.0174
A → Y ↓	0.0267	0.0260	0.0248	0.0245	0.0244	0.0240	0.0218	0.0222

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)							
	X3P0M	**X3P5M**	**X4P0M**	**X5P0M**	**X6P0M**	**X7P5M**	**X9P0M**	**X11P0M**
A → Y ↑	0.0169	0.0176	0.0172	0.0172	0.0165	0.0172	0.0169	0.0171
A → Y ↓	0.0218	0.0224	0.0219	0.0219	0.0212	0.0216	0.0213	0.0215

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)	
	X13P0M	**X16P0M**
A → Y ↑	0.0167	0.0167
A → Y ↓	0.0212	0.0212

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X0P7M	**X0P8M**	**X1P0M**	**X1P2M**	**X1P4M**	**X1P7M**	**X2P0M**	**X2P5M**
A → Y ↑	3.4453	3.0763	2.5227	1.9035	1.6451	1.3694	1.1808	0.9266
A → Y ↓	2.1563	1.8859	1.5091	1.1576	1.0031	0.8295	0.7163	0.5716

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X3P0M	**X3P5M**	**X4P0M**	**X5P0M**	**X6P0M**	**X7P5M**	**X9P0M**	**X11P0M**
A → Y ↑	0.7830	0.6536	0.5807	0.4642	0.3842	0.3034	0.2559	0.2084
A → Y ↓	0.4820	0.4035	0.3550	0.2846	0.2364	0.1881	0.1589	0.1292

Delays at 25°C,1.0V, Typical Process (Cont'd.)

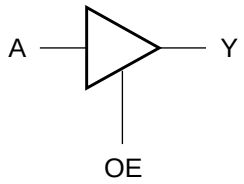
Description	K_{load} (ns/pF)	
	X13P0M	**X16P0M**
A → Y ↑	0.1761	0.1428
A → Y ↓	0.1093	0.0908

Cell Description

The BUFZ cell provides the logical buffer of a single input (A) with an active-high output enable (OE). The output (Y) is tristated when the enable is low. When the enable is high, the output is represented by the logic equation:

$Y = A$

Logic Symbol



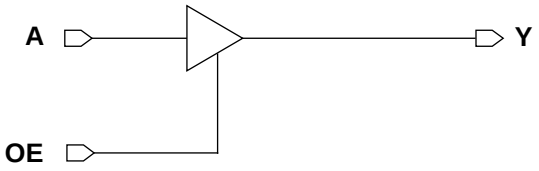
Function Table

OE	A	Y
0	x	Z
1	0	0
1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
BUFZX1MA10TR	2.00	2.20
BUFZX1P4MA10TR	2.00	2.20
BUFZX2MA10TR	2.00	3.00
BUFZX3MA10TR	2.00	3.20
BUFZX4MA10TR	2.00	3.80
BUFZX6MA10TR	2.00	5.40
BUFZX8MA10TR	2.00	7.00
BUFZX11MA10TR	2.00	8.80
BUFZX16MA10TR	2.00	12.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)								
	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M	X11P0M	X16P0M
A	0.0008	0.0010	0.0015	0.0019	0.0025	0.0035	0.0046	0.0061	0.0087
OE	0.0034	0.0044	0.0061	0.0083	0.0111	0.0153	0.0202	0.0269	0.0384

Pin Capacitance

Pin	Capacitance (pF)								
	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M	X11P0M	X16P0M
A	0.0016	0.0019	0.0029	0.0037	0.0047	0.0064	0.0082	0.0106	0.0150
OE	0.0018	0.0019	0.0022	0.0030	0.0036	0.0051	0.0066	0.0084	0.0109
Y	0.0013	0.0016	0.0026	0.0033	0.0042	0.0063	0.0085	0.0114	0.0166

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)								
	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M	X11P0M	X16P0M
A → Y ↑	0.0379	0.0353	0.0346	0.0332	0.0321	0.0342	0.0336	0.0343	0.0346
A → Y ↓	0.0459	0.0436	0.0421	0.0427	0.0411	0.0418	0.0415	0.0416	0.0414
OE → Y ↑	0.0299	0.0282	0.0283	0.0262	0.0252	0.0278	0.0272	0.0280	0.0284
OE → Y ↓	0.0410	0.0404	0.0401	0.0378	0.0381	0.0369	0.0366	0.0362	0.0359

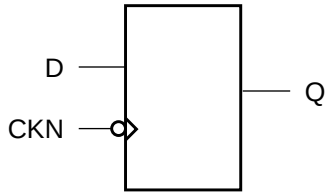
Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)								
	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M	X11P0M	X16P0M
A → Y ↑	2.2380	1.6300	1.1336	0.7554	0.5686	0.3746	0.2799	0.2043	0.1411
A → Y ↓	1.3663	0.9874	0.7043	0.4787	0.3528	0.2338	0.1756	0.1287	0.0887
OE → Y ↑	2.2353	1.6282	1.1321	0.7546	0.5680	0.3743	0.2796	0.2041	0.1409
OE → Y ↓	1.3661	0.9873	0.7044	0.4787	0.3529	0.2338	0.1756	0.1286	0.0887

Cell Description

The DFFNQ cell is a negative-edge triggered, static D-type flip-flop.

Logic Symbol



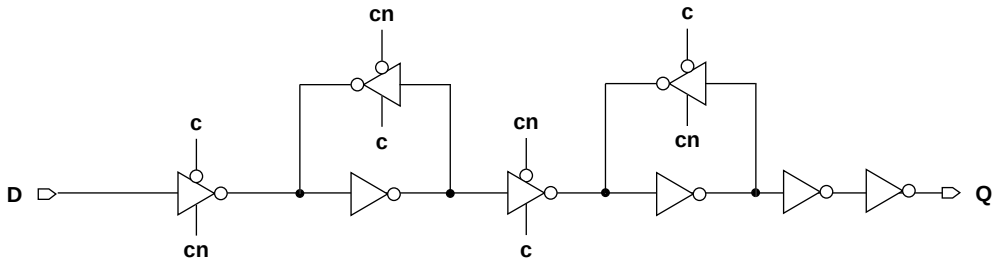
Function Table

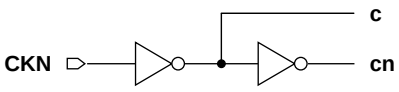
D	CKN	Q[n+1]
0	↓	0
1	↓	1
x	↑	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFNQX1MA10TR	2.00	4.20
DFFNQX2MA10TR	2.00	4.40
DFFNQX3MA10TR	2.00	4.80

Functional Schematic





AC Power

Pin	Power (uW/MHz)		
	X1P0M	X2P0M	X3P0M
D	0.0048	0.0059	0.0063
CKN	0.0047	0.0053	0.0059
Q	0.0047	0.0066	0.0083

Pin Capacitance

Pin	Capacitance (pF)		
	X1P0M	X2P0M	X3P0M
D	0.0013	0.0016	0.0016
CKN	0.0010	0.0010	0.0011

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)			K_{load} (ns/pF)		
	X1P0M	X2P0M	X3P0M	X1P0M	X2P0M	X3P0M
CKN → Q ↑	0.0906	0.0882	0.0878	2.3372	1.1657	0.7822
CKN → Q ↓	0.0847	0.0842	0.0862	1.4526	0.7226	0.4589

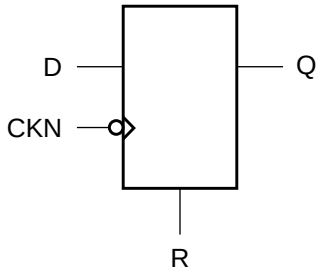
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)		
		X1P0M	X2P0M	X3P0M
D	setup ↑ → CKN	0.0039	0.0000	0.0000
	setup ↓ → CKN	0.0195	0.0195	0.0195
	hold ↑ → CKN	0.0156	0.0195	0.0156
	hold ↓ → CKN	-0.0078	-0.0078	-0.0078
CKN	minpwl	0.8830	0.8830	0.8830
	minpwh	0.8830	0.8830	0.8830

Cell Description

The DFFNRPQ cell is a negative-edge triggered, static D-type flip-flop with asynchronous active-high reset (R).

Logic Symbol



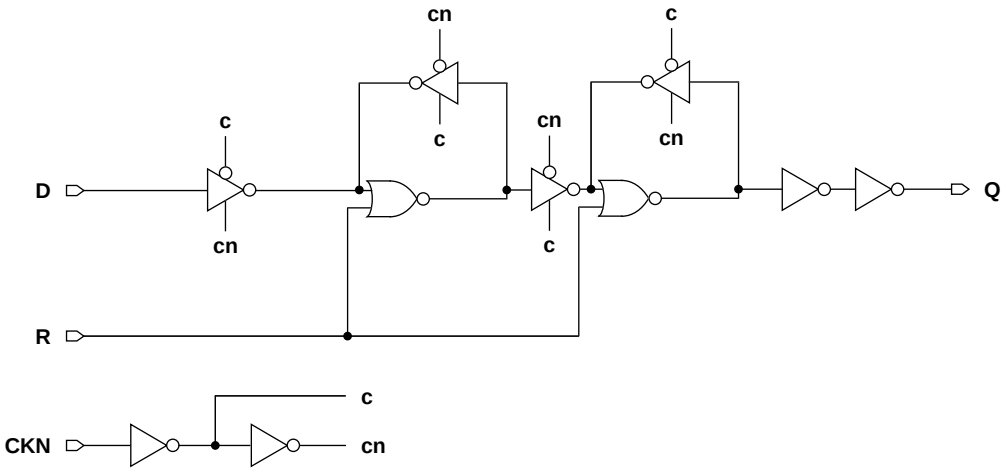
Function Table

R	D	CKN	Q[n+1]
1	x	x	0
0	0	⎺_	0
0	1	⎺_	1
0	x	_/⎺	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFNRPQX1MA10TR	2.00	4.80
DFFNRPQX2MA10TR	2.00	5.20
DFFNRPQX3MA10TR	2.00	5.40

Functional Schematic



AC Power

Pin	Power (uW/MHz)		
	X1P0M	X2P0M	X3P0M
D	0.0050	0.0063	0.0065
CKN	0.0049	0.0055	0.0060
R	0.0014	0.0019	0.0022
Q	0.0054	0.0070	0.0089

Pin Capacitance

Pin	Capacitance (pF)		
	X1P0M	X2P0M	X3P0M
D	0.0013	0.0016	0.0016
CKN	0.0010	0.0010	0.0011
R	0.0021	0.0024	0.0024

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)			K_{load} (ns/pF)		
	X1P0M	X2P0M	X3P0M	X1P0M	X2P0M	X3P0M
CKN → Q ↑	0.1041	0.0964	0.0993	2.3369	1.1508	0.7850
CKN → Q ↓	0.0990	0.0948	0.0972	1.4577	0.7100	0.4615
R → Q ↓	0.0564	0.0590	0.0663	1.4551	0.7092	0.4610

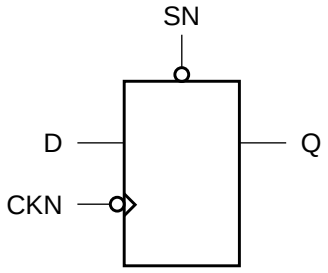
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)		
		X1P0M	X2P0M	X3P0M
D	setup ↑ → CKN	0.0117	0.0078	0.0078
	setup ↓ → CKN	0.0234	0.0195	0.0195
	hold ↑ → CKN	0.0156	0.0195	0.0195
	hold ↓ → CKN	-0.0117	-0.0078	-0.0078
CKN	minpwl	0.8830	0.8830	0.8830
	minpwh	0.8830	0.8830	0.8830
R	minpwh	0.8830	0.8830	0.8830
	recovery	-0.0273	-0.0273	-0.0273
	removal	0.0664	0.0742	0.0703

Cell Description

The DFFNSQ cell is a negative-edge triggered, static D-type flip-flop with asynchronous active-low set (SN).

Logic Symbol



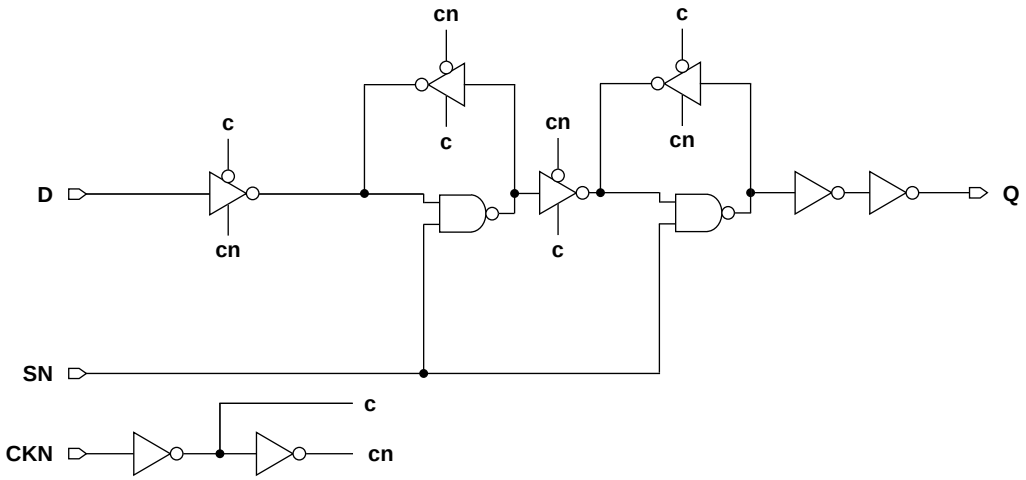
Function Table

SN	D	CKN	Q[n+1]
0	x	x	1
1	0	↓	0
1	1	↓	1
1	x	↑	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFNSQX1MA10TR	2.00	4.80
DFFNSQX2MA10TR	2.00	5.20
DFFNSQX3MA10TR	2.00	5.80

Functional Schematic



AC Power

Pin	Power (uW/MHz)		
	X1P0M	X2P0M	X3P0M
D	0.0054	0.0064	0.0068
CKN	0.0049	0.0056	0.0062
SN	0.0016	0.0019	0.0022
Q	0.0052	0.0067	0.0090

Pin Capacitance

Pin	Capacitance (pF)		
	X1P0M	X2P0M	X3P0M
D	0.0013	0.0016	0.0016
CKN	0.0010	0.0010	0.0011
SN	0.0017	0.0018	0.0018

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)			K_{load} (ns/pF)		
	X1P0M	X2P0M	X3P0M	X1P0M	X2P0M	X3P0M
CKN → Q ↑	0.0939	0.0929	0.0956	2.3793	1.1635	0.7819
CKN → Q ↓	0.0931	0.0934	0.0974	1.4677	0.7263	0.4612
SN → Q ↑	0.0580	0.0620	0.0698	2.3771	1.1631	0.7816

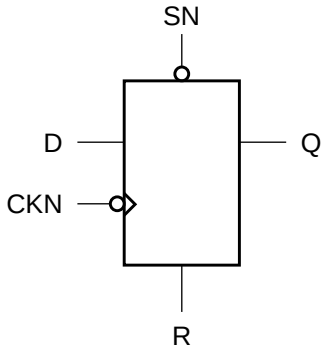
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)		
		X1P0M	X2P0M	X3P0M
D	setup ↑ → CKN	0.0078	0.0039	0.0078
	setup ↓ → CKN	0.0195	0.0156	0.0156
	hold ↑ → CKN	0.0117	0.0195	0.0156
	hold ↓ → CKN	-0.0078	-0.0039	-0.0039
CKN	minpwl	0.8830	0.8830	0.8830
	minpwh	0.8830	0.8830	0.8830
SN	minpwl	0.8830	0.8830	0.8830
	recovery	-0.0195	-0.0234	-0.0195
	removal	0.0469	0.0508	0.0469

Cell Description

The DFFNSRPQ cell is a negative-edge triggered, static D-type flip-flop with asynchronous active-high reset (R) and asynchronous active-low set (SN). Set is dominant over reset if both are asserted.

Logic Symbol



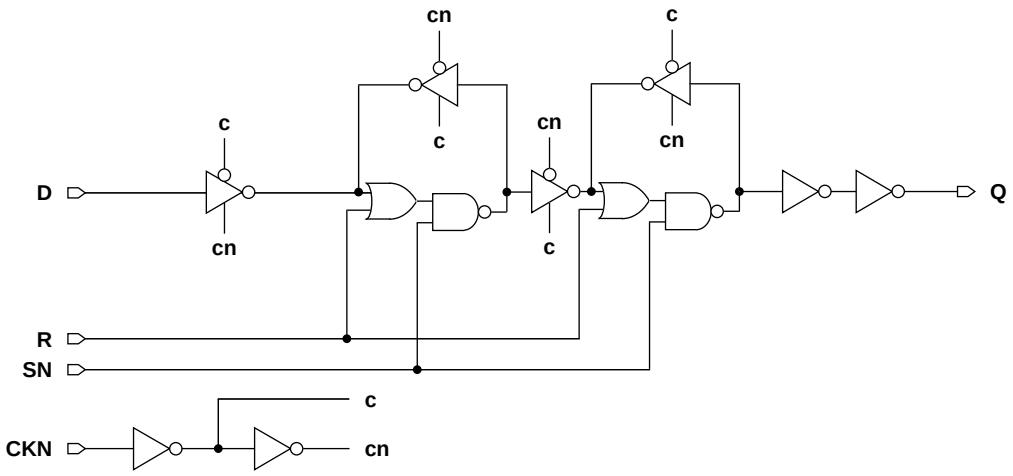
Function Table

R	SN	D	CKN	Q
1	1	x	x	0
0	0	x	x	1
1	0	x	x	1
0	1	0	↓	0
0	1	1	↓	1
0	1	x	↑	Q

Cell Size

Drive Strength	Height (um)	Width (um)
DFFNSRPQX1MA10TR	2.00	6.00
DFFNSRPQX2MA10TR	2.00	6.20
DFFNSRPQX3MA10TR	2.00	6.40

Functional Schematic



AC Power

Pin	Power (uW/MHz)		
	X1P0M	X2P0M	X3P0M
D	0.0052	0.0065	0.0067
CKN	0.0047	0.0054	0.0059
SN	0.0017	0.0021	0.0023
R	0.0018	0.0024	0.0026
Q	0.0053	0.0069	0.0090

Pin Capacitance

Pin	Capacitance (pF)		
	X1P0M	X2P0M	X3P0M
D	0.0013	0.0016	0.0016
CKN	0.0010	0.0010	0.0011
SN	0.0026	0.0030	0.0029
R	0.0021	0.0025	0.0024

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)			K_{load} (ns/pF)		
	X1P0M	X2P0M	X3P0M	X1P0M	X2P0M	X3P0M
CKN → Q ↑	0.1136	0.1154	0.1102	2.3368	1.1549	0.7861
CKN → Q ↓	0.1100	0.1145	0.1088	1.4593	0.7215	0.4638
SN → Q ↑	0.0645	0.0688	0.0745	2.3336	1.1542	0.7857
SN → Q ↓	0.0774	0.0835	0.0897	1.4577	0.7212	0.4637
R → Q ↓	0.0755	0.0819	0.0881	1.4577	0.7212	0.4636

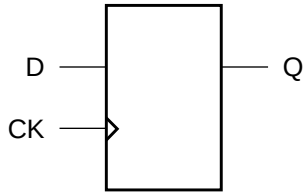
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)		
		X1P0M	X2P0M	X3P0M
D	setup ↑ → CKN	0.0195	0.0039	0.0156
	setup ↓ → CKN	0.0273	0.0195	0.0234
	hold ↑ → CKN	0.0156	0.0273	0.0195
	hold ↓ → CKN	-0.0078	-0.0039	-0.0039
CKN	minpwl	0.8830	0.8830	0.8830
	minpwh	0.8830	0.8830	0.8830
SN	minpwl	0.8830	0.8830	0.8830
	recovery	0.0000	-0.0078	-0.0039
	removal	0.0195	0.0312	0.0234
R	minpwh	0.8830	0.8830	0.8830
	recovery	-0.0078	-0.0273	-0.0117
	removal	0.0430	0.0586	0.0430

Cell Description

The DFFQ cell is a positive-edge triggered, static D-type flip-flop. The cell has a single output (Q) .

Logic Symbol



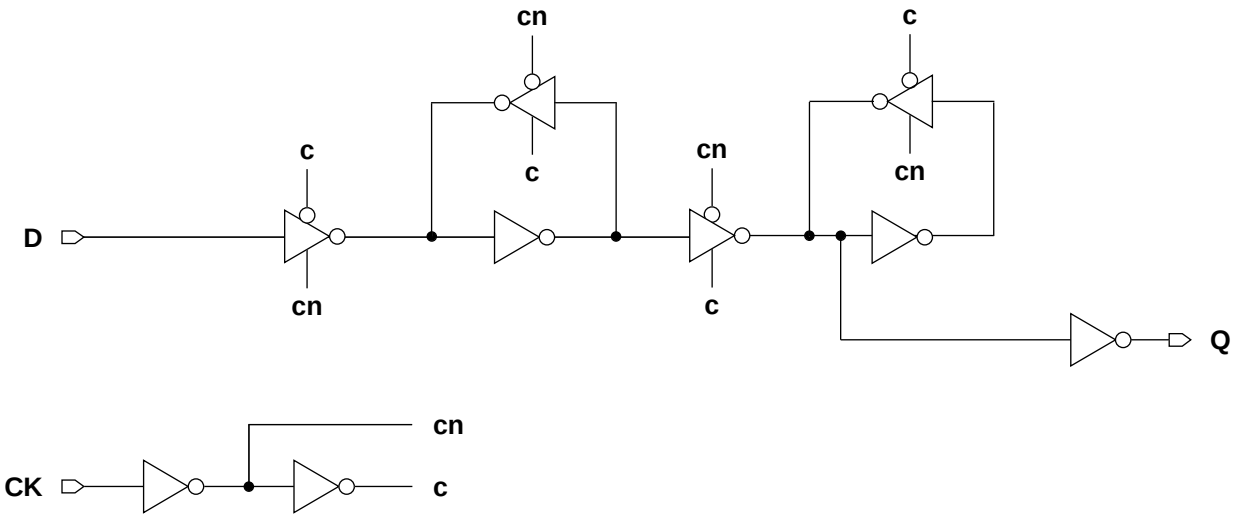
Function Table

D	CK	Q[n+1]
0	⎍	0
1	⎍	1
x	⎎	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFQX0P5MA10TR	2.00	4.00
DFFQX1MA10TR	2.00	4.20
DFFQX2MA10TR	2.00	4.40
DFFQX3MA10TR	2.00	4.80
DFFQX4MA10TR	2.00	5.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D	0.0037	0.0048	0.0060	0.0065	0.0066
CK	0.0036	0.0041	0.0047	0.0053	0.0055
Q	0.0031	0.0040	0.0057	0.0080	0.0106

Pin Capacitance

Pin	Capacitance (pF)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D	0.0011	0.0014	0.0017	0.0018	0.0017
CK	0.0009	0.0009	0.0010	0.0011	0.0012

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
CK → Q ↑	0.0925	0.0784	0.0752	0.0754	0.0736
CK → Q ↓	0.1016	0.0854	0.0821	0.0825	0.0767

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
CK → Q ↑	4.1883	2.3336	1.1633	0.7833	0.5862
CK → Q ↓	2.4669	1.3332	0.6623	0.4568	0.3342

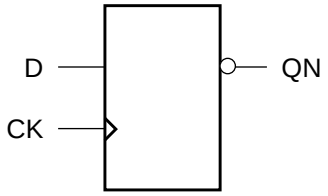
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)				
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D	setup ↑ → CK	0.0195	0.0156	0.0117	0.0156	0.0156
	setup ↓ → CK	0.0156	0.0117	0.0117	0.0156	0.0156
	hold ↑ → CK	-0.0078	-0.0039	0.0000	-0.0039	-0.0039
	hold ↓ → CK	0.0039	0.0039	0.0039	0.0000	0.0039
CK	minpwh	0.8830	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830

Cell Description

The DFFQN cell is a positive-edge triggered, static D-type flip-flop. The cell has a single output (QN).

Logic Symbol



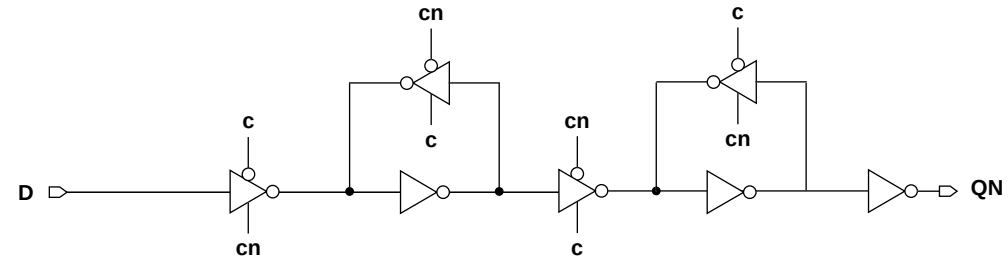
Function Table

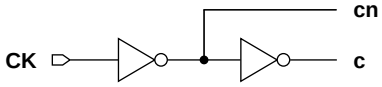
D	CK	QN[n+1]
0	⎍	1
1	⎍	0
x	⎏	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFQNX0P5MA10TR	2.00	4.00
DFFQNX1MA10TR	2.00	4.20
DFFQNX2MA10TR	2.00	4.40
DFFQNX3MA10TR	2.00	4.80

Functional Schematic





AC Power

Pin	Power (uW/MHz)			
	X0P5M	X1P0M	X2P0M	X3P0M
D	0.0037	0.0049	0.0060	0.0067
CK	0.0036	0.0040	0.0046	0.0055
QN	0.0032	0.0038	0.0056	0.0080

Pin Capacitance

Pin	Capacitance (pF)			
	X0P5M	X1P0M	X2P0M	X3P0M
D	0.0011	0.0014	0.0017	0.0018
CK	0.0009	0.0009	0.0010	0.0012

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X0P5M	X1P0M	X2P0M	X3P0M	X0P5M	X1P0M	X2P0M	X3P0M
CK → QN ↑	0.0886	0.0734	0.0720	0.0660	4.2553	2.3600	1.1728	0.7875
CK → QN ↓	0.0867	0.0733	0.0758	0.0736	2.9083	1.5358	0.7639	0.5181

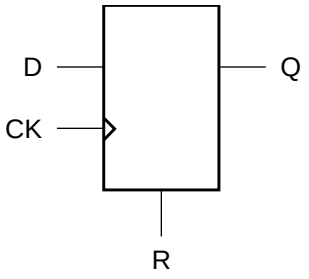
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X0P5M	X1P0M	X2P0M	X3P0M
D	setup ↑ → CK	0.0195	0.0156	0.0156	0.0156
	setup ↓ → CK	0.0156	0.0156	0.0156	0.0195
	hold ↑ → CK	-0.0039	-0.0039	0.0000	0.0000
	hold ↓ → CK	0.0078	0.0078	0.0039	0.0039
CK	minpwh	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830

Cell Description

The DFFRPQ cell is a positive-edge triggered, static D-type flip-flop with asynchronous active-high reset (R). The cell has a single output (Q).

Logic Symbol



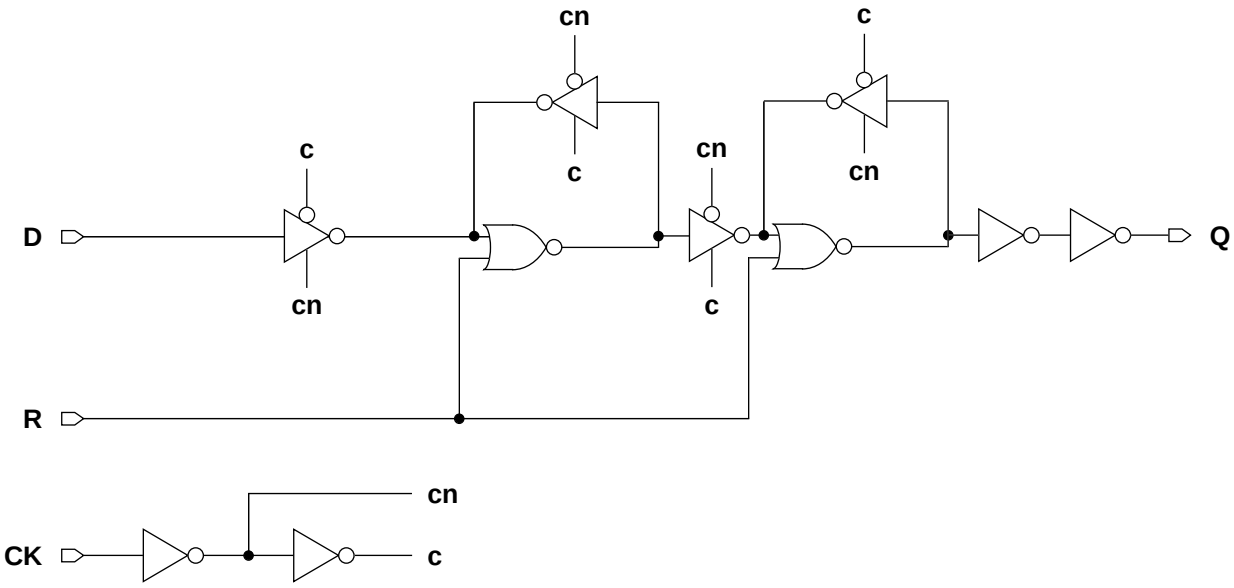
Function Table

R	D	CK	Q[n+1]
1	x	x	0
0	0	⎍	0
0	1	⎍	1
0	x	⎎	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFRPQX0P5MA10TR	2.00	4.80
DFFRPQX1MA10TR	2.00	4.80
DFFRPQX2MA10TR	2.00	5.20
DFFRPQX3MA10TR	2.00	5.60
DFFRPQX4MA10TR	2.00	6.20

Functional Schematic



AC Power

Pin	Power (uW/MHz)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
D	0.0041	0.0052	0.0064	0.0069	0.0070
CK	0.0039	0.0043	0.0050	0.0055	0.0060
R	0.0014	0.0015	0.0019	0.0023	0.0026
Q	0.0035	0.0048	0.0061	0.0082	0.0112

Pin Capacitance

Pin	Capacitance (pF)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
D	0.0011	0.0014	0.0018	0.0018	0.0016
CK	0.0009	0.0010	0.0010	0.0011	0.0012
R	0.0018	0.0023	0.0026	0.0026	0.0027

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
CK → Q ↑	0.1050	0.0908	0.0815	0.0813	0.0838
CK → Q ↓	0.1122	0.0930	0.0881	0.0878	0.0861
R → Q ↓	0.0566	0.0525	0.0567	0.0629	0.0706

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
CK → Q ↑	4.2125	2.3987	1.1527	0.7794	0.5803
CK → Q ↓	2.6008	1.3218	0.7210	0.4596	0.3341
R → Q ↓	2.5891	1.3204	0.7207	0.4595	0.3342

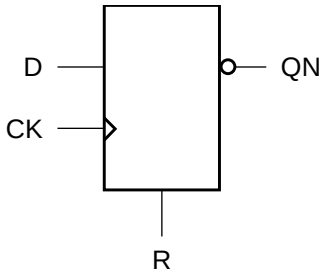
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)				
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D	setup ↑ → CK	0.0352	0.0195	0.0195	0.0195	0.0195
	setup ↓ → CK	0.0195	0.0156	0.0156	0.0195	0.0195
	hold ↑ → CK	-0.0078	-0.0039	-0.0039	-0.0039	0.0000
	hold ↓ → CK	0.0039	0.0039	0.0039	0.0000	0.0000
CK	minpwh	0.8830	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830
R	minpwh	0.8830	0.8830	0.8830	0.8830	0.8830
	recovery	0.0156	0.0000	0.0039	0.0039	0.0000
	removal	0.0117	0.0391	0.0430	0.0430	0.0352

Cell Description

The DFFRPQN cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-high reset (R). The cell has a single inverted output (QN).

Logic Symbol



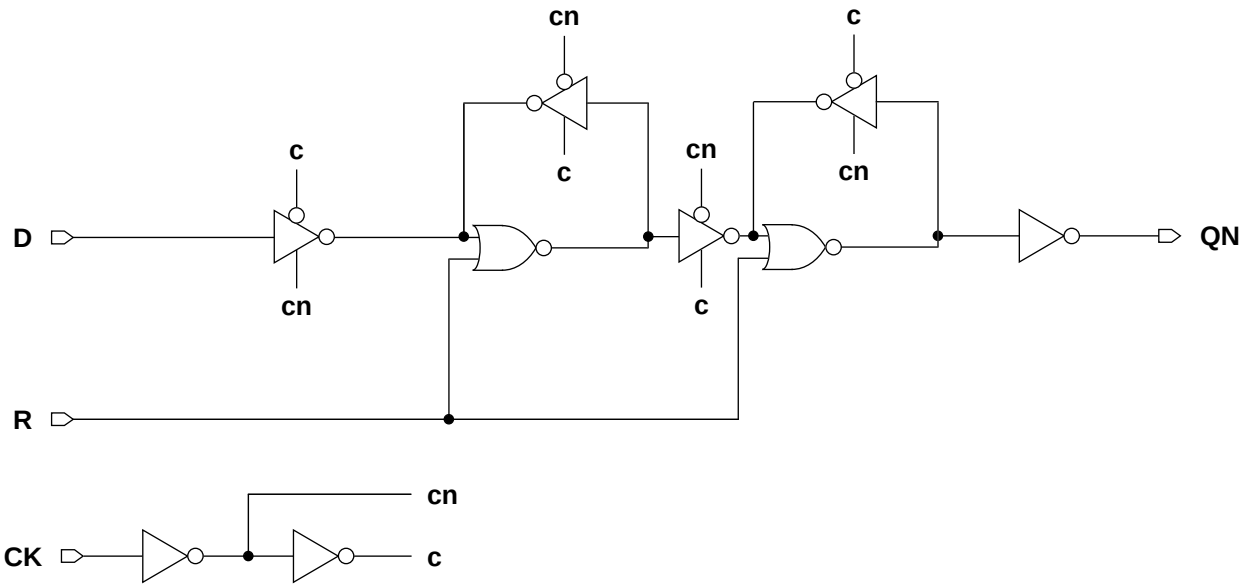
Function Table

R	D	CK	QN[n+1]
1	x	x	1
0	0	⎍	1
0	1	⎍	0
0	x	⎎	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFRPQNX0P5MA10TR	2.00	4.80
DFFRPQNX1MA10TR	2.00	4.80
DFFRPQNX2MA10TR	2.00	5.20
DFFRPQNX3MA10TR	2.00	5.60

Functional Schematic



AC Power

Pin	Power (uW/MHz)			
	X0P5M	X1P0M	X2P0M	X3P0M
D	0.0042	0.0053	0.0066	0.0069
CK	0.0038	0.0044	0.0048	0.0057
R	0.0015	0.0014	0.0018	0.0020
QN	0.0035	0.0044	0.0066	0.0096

Pin Capacitance

Pin	Capacitance (pF)			
	X0P5M	X1P0M	X2P0M	X3P0M
D	0.0011	0.0014	0.0019	0.0018
CK	0.0009	0.0009	0.0010	0.0012
R	0.0019	0.0024	0.0026	0.0026

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X0P5M	X1P0M	X2P0M	X3P0M	X0P5M	X1P0M	X2P0M	X3P0M
CK → QN ↑	0.0927	0.0801	0.0755	0.0747	4.3042	2.3596	1.1874	0.8001
CK → QN ↓	0.0930	0.0847	0.0842	0.0887	3.1235	1.5824	0.7592	0.5240
R → QN ↑	0.0349	0.0382	0.0494	0.0607	4.2418	2.3539	1.1861	0.7991

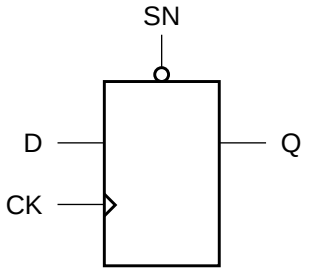
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X0P5M	X1P0M	X2P0M	X3P0M
D	setup ↑ → CK	0.0312	0.0234	0.0195	0.0195
	setup ↓ → CK	0.0234	0.0156	0.0156	0.0234
	hold ↑ → CK	-0.0078	-0.0039	-0.0039	0.0000
	hold ↓ → CK	0.0039	0.0039	0.0039	0.0000
CK	minpwh	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830
R	minpwh	0.8830	0.8830	0.8830	0.8830
	recovery	0.0117	0.0039	0.0000	0.0039
	removal	0.0156	0.0391	0.0352	0.0312

Cell Description

The DFFSQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low set (SN). The cell has a single output (Q).

Logic Symbol



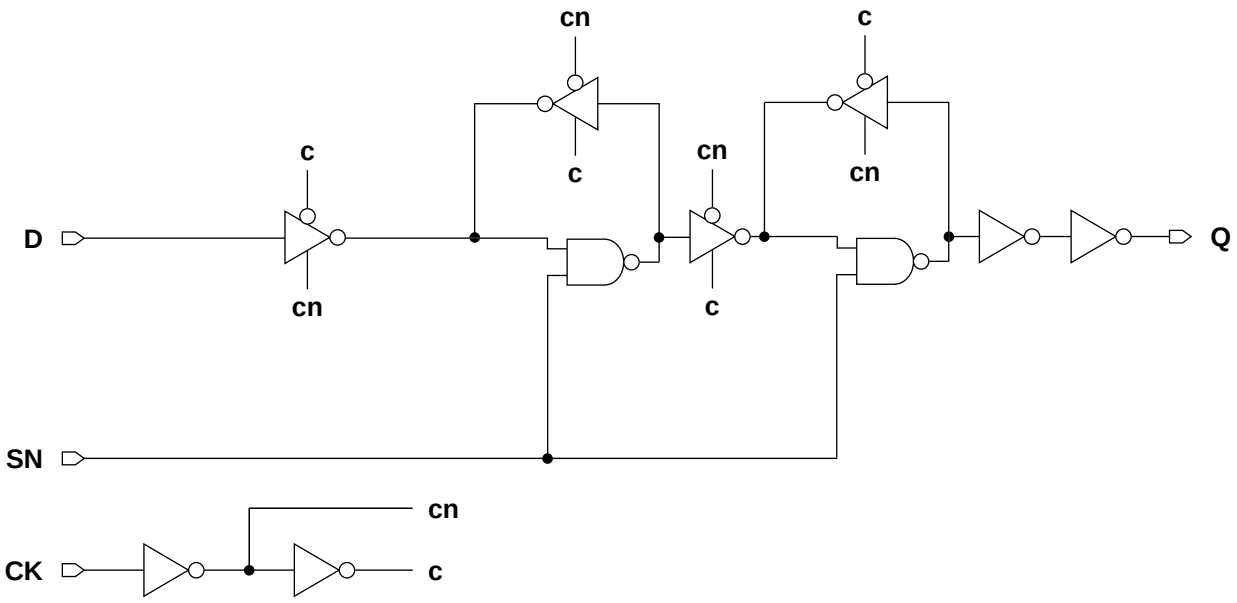
Function Table

SN	D	CK	Q[n+1]
0	x	x	1
1	0	↑	0
1	1	↑	1
1	x	↓	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFSQX0P5MA10TR	2.00	5.00
DFFSQX1MA10TR	2.00	5.00
DFFSQX2MA10TR	2.00	5.40
DFFSQX3MA10TR	2.00	5.60
DFFSQX4MA10TR	2.00	5.80

Functional Schematic



AC Power

Pin	Power (uW/MHz)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D	0.0042	0.0052	0.0066	0.0068	0.0070
CK	0.0037	0.0043	0.0050	0.0054	0.0058
SN	0.0014	0.0018	0.0022	0.0024	0.0027
Q	0.0033	0.0045	0.0063	0.0081	0.0112

Pin Capacitance

Pin	Capacitance (pF)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D	0.0012	0.0013	0.0018	0.0018	0.0017
CK	0.0009	0.0010	0.0010	0.0011	0.0012
SN	0.0018	0.0022	0.0027	0.0027	0.0027

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
CK → Q ↑	0.0967	0.0859	0.0793	0.0796	0.0779
CK → Q ↓	0.1109	0.0946	0.0887	0.0908	0.0872
SN → Q ↑	0.0665	0.0640	0.0687	0.0731	0.0795

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
CK → Q ↑	4.1893	2.3343	1.1600	0.7831	0.5838
CK → Q ↓	2.4784	1.3350	0.6619	0.4584	0.3323
SN → Q ↑	4.1924	2.3355	1.1603	0.7834	0.5837

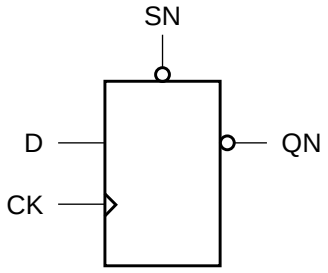
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)				
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D	setup ↑ → CK	0.0234	0.0156	0.0156	0.0156	0.0195
	setup ↓ → CK	0.0195	0.0117	0.0117	0.0156	0.0156
	hold ↑ → CK	-0.0078	-0.0039	-0.0039	-0.0039	-0.0039
	hold ↓ → CK	0.0039	0.0078	0.0039	0.0039	0.0039
CK	minpwh	0.8830	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830
SN	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830
	recovery	-0.0273	-0.0312	-0.0312	-0.0312	-0.0234
	removal	0.0508	0.0625	0.0625	0.0625	0.0508

Cell Description

The DFFSQN cell is a positive-edge triggered, static D-type flip-flop with asynchronous active-low set (SN). The cell has a single inverted output (QN).

Logic Symbol



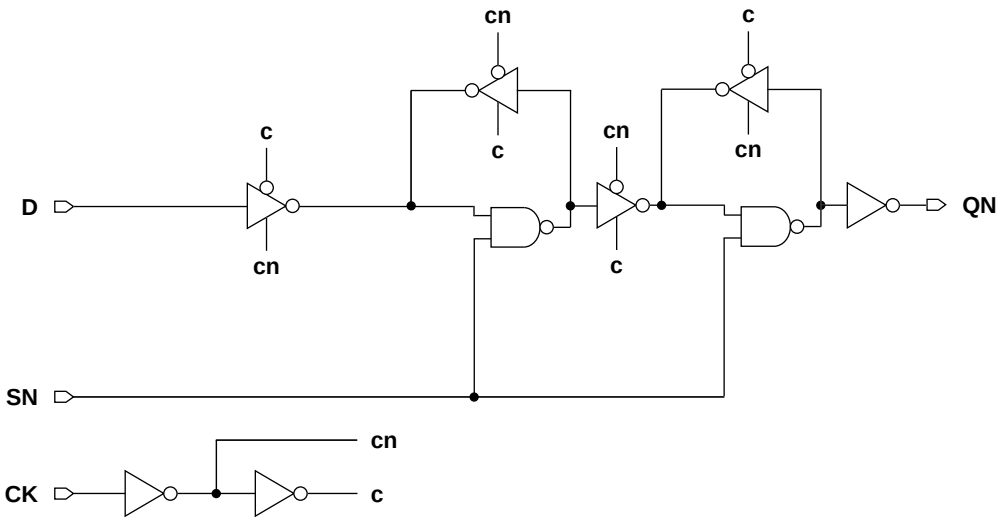
Function Table

SN	D	CK	QN
0	x	x	0
1	0	↑	1
1	1	↑	0
1	x	↓	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFSQNX0P5MA10TR	2.00	5.00
DFFSQNX1MA10TR	2.00	5.00
DFFSQNX2MA10TR	2.00	5.40
DFFSQNX3MA10TR	2.00	5.60

Functional Schematic



AC Power

Pin	Power (uW/MHz)			
	X0P5M	X1P0M	X2P0M	X3P0M
D	0.0043	0.0054	0.0066	0.0068
CK	0.0036	0.0041	0.0048	0.0055
SN	0.0014	0.0018	0.0022	0.0024
QN	0.0035	0.0044	0.0062	0.0089

Pin Capacitance

Pin	Capacitance (pF)			
	X0P5M	X1P0M	X2P0M	X3P0M
D	0.0012	0.0013	0.0018	0.0018
CK	0.0009	0.0009	0.0010	0.0012
SN	0.0019	0.0024	0.0026	0.0025

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X0P5M	X1P0M	X2P0M	X3P0M	X0P5M	X1P0M	X2P0M	X3P0M
CK → QN ↑	0.0961	0.0807	0.0790	0.0776	4.2816	2.3581	1.1748	0.7956
CK → QN ↓	0.0869	0.0797	0.0788	0.0824	2.9117	1.5399	0.7923	0.5319
SN → QN ↓	0.0539	0.0560	0.0699	0.0850	2.7502	1.4958	0.7802	0.5241

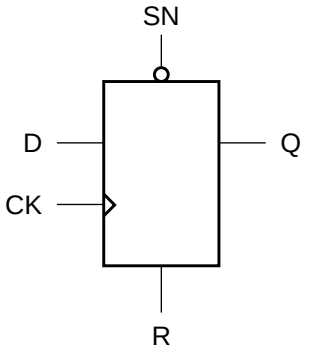
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X0P5M	X1P0M	X2P0M	X3P0M
D	setup ↑ → CK	0.0234	0.0234	0.0156	0.0195
	setup ↓ → CK	0.0195	0.0117	0.0156	0.0195
	hold ↑ → CK	-0.0078	-0.0078	-0.0039	-0.0039
	hold ↓ → CK	0.0078	0.0078	0.0078	0.0039
CK	minpwh	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830
SN	minpwl	0.8830	0.8830	0.8830	0.8830
	recovery	-0.0312	-0.0352	-0.0312	-0.0234
	removal	0.0508	0.0664	0.0625	0.0547

Cell Description

The DFFSRPQ cell is a positive-edge triggered, static D-type flip-flop with asynchronous active-low reset (R) and set (SN), and set dominating reset.

Logic Symbol



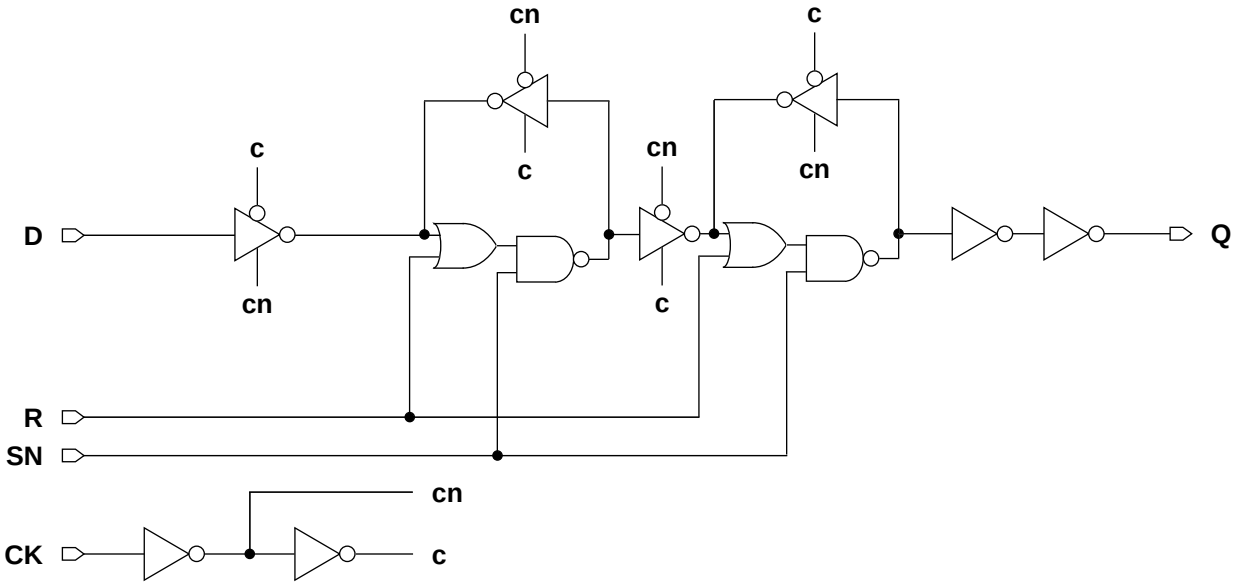
Function Table

R	SN	D	CK	Q[n+1]
1	1	x	x	0
1	0	x	x	1
0	0	x	x	1
0	1	0	⎍	0
0	1	1	⎍	1
0	1	x	⎎	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFSRPQX0P5MA10TR	2.00	6.00
DFFSRPQX1MA10TR	2.00	6.00
DFFSRPQX2MA10TR	2.00	6.20
DFFSRPQX3MA10TR	2.00	6.40
DFFSRPQX4MA10TR	2.00	7.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
D	0.0041	0.0053	0.0065	0.0068	0.0070
CK	0.0050	0.0055	0.0064	0.0067	0.0072
SN	0.0014	0.0019	0.0022	0.0024	0.0027
R	0.0014	0.0020	0.0024	0.0027	0.0030
Q	0.0040	0.0052	0.0071	0.0090	0.0118

Pin Capacitance

Pin	Capacitance (pF)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
D	0.0011	0.0013	0.0017	0.0017	0.0017
CK	0.0009	0.0009	0.0010	0.0011	0.0012
SN	0.0025	0.0029	0.0031	0.0031	0.0031
R	0.0016	0.0020	0.0021	0.0022	0.0022

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
CK → Q ↑	0.1170	0.0964	0.0933	0.0937	0.0953
CK → Q ↓	0.1280	0.1018	0.0989	0.1024	0.1003
SN → Q ↑	0.0707	0.0692	0.0765	0.0781	0.0804
SN → Q ↓	0.0735	0.0667	0.0760	0.0835	0.0904
R → Q ↓	0.0718	0.0648	0.0743	0.0817	0.0884

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
CK → Q ↑	4.2057	2.3338	1.1539	0.7790	0.5857
CK → Q ↓	2.6228	1.3346	0.6711	0.4628	0.3345
SN → Q ↑	4.2036	2.3345	1.1538	0.7791	0.5855
SN → Q ↓	2.6062	1.3322	0.6710	0.4627	0.3346
R → Q ↓	2.6062	1.3321	0.6710	0.4626	0.3346

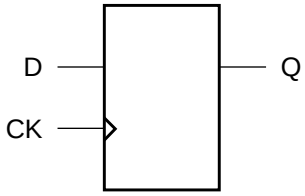
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)				
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D	setup ↑ → CK	0.0391	0.0273	0.0234	0.0234	0.0234
	setup ↓ → CK	0.0234	0.0234	0.0195	0.0234	0.0273
	hold ↑ → CK	-0.0078	-0.0039	0.0000	0.0000	0.0000
	hold ↓ → CK	0.0039	0.0039	0.0039	0.0039	0.0000
CK	minpwh	0.8830	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830
SN	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830
	recovery	-0.0156	-0.0156	-0.0156	-0.0117	-0.0039
	removal	0.0352	0.0352	0.0352	0.0312	0.0273
R	minpwh	0.8830	0.8830	0.8830	0.8830	0.8830
	recovery	0.0195	0.0117	0.0156	0.0156	0.0117
	removal	0.0156	0.0234	0.0195	0.0195	0.0156

Cell Description

The DFFYQ cell is a positive-edge triggered, static D-type flip-flop to be used in synchronizing circuitry between asynchronous systems. The cell has a single output (Q) and overdriven feedback loops to increase MTBF due to metastability.

Logic Symbol



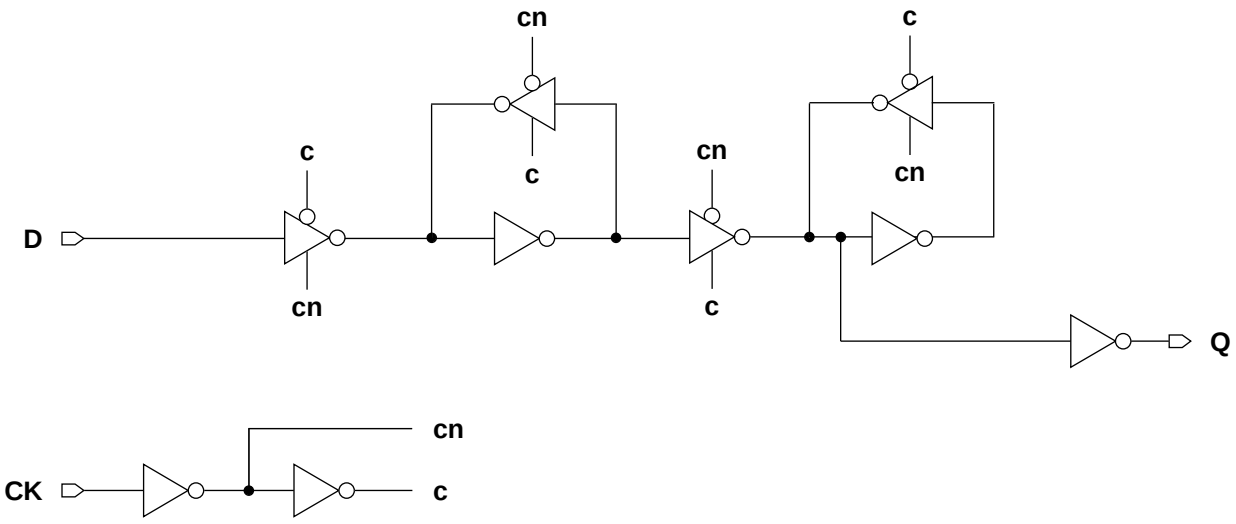
Function Table

D	CK	Q[n+1]
0	⎍	0
1	⎍	1
x	⎎	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
DFFYQX1MA10TR	2.00	4.20
DFFYQX2MA10TR	2.00	4.60
DFFYQX3MA10TR	2.00	4.80
DFFYQX4MA10TR	2.00	5.40

Functional Schematic



AC Power

Pin	Power (uW/MHz)			
	X1P0M	X2P0M	X3P0M	X4P0M
D	0.0055	0.0068	0.0067	0.0073
CK	0.0055	0.0065	0.0062	0.0074
Q	0.0047	0.0063	0.0091	0.0120

Pin Capacitance

Pin	Capacitance (pF)			
	X1P0M	X2P0M	X3P0M	X4P0M
D	0.0014	0.0017	0.0017	0.0018
CK	0.0013	0.0016	0.0012	0.0015

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1P0M	X2P0M	X3P0M	X4P0M	X1P0M	X2P0M	X3P0M	X4P0M
CK → Q ↑	0.0751	0.0676	0.0763	0.0711	2.3326	1.1637	0.7847	0.5869
CK → Q ↓	0.0802	0.0734	0.0852	0.0760	1.4505	0.7216	0.4591	0.3341

Timing Constraints at 25°C,1.0V, Typical Process

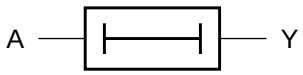
Pin	Requirement	Interval (ns)			
		X1P0M	X2P0M	X3P0M	X4P0M
D	setup ↑ → CK	0.0195	0.0156	0.0156	0.0156
	setup ↓ → CK	0.0234	0.0234	0.0195	0.0273
	hold ↑ → CK	-0.0078	-0.0039	-0.0039	-0.0039
	hold ↓ → CK	-0.0039	-0.0039	0.0000	-0.0039
CK	minpwh	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830

Cell Description

The DLY2 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$Y = A$

Logic Symbol



Function Table

A	Y
0	0
1	1

Cell Size

Drive Strength	Height (um)	Width (um)
DLY2X0P5MA10TR	2.00	1.20

Functional Schematic

AC Power

Pin	Power (uW/MHz)
	X0P5M
A	0.0028

Pin Capacitance

Pin	Capacitance (pF)
	X0P5M
A	0.0014

Delays at 25°C,1.0V, Typical Process

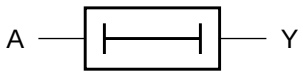
Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X0P5M	X0P5M
A → Y ↑	0.0450	4.7442
A → Y ↓	0.0634	2.9678

Cell Description

The DLY4 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$Y = A$

Logic Symbol



Function Table

A	Y
0	0
1	1

Cell Size

Drive Strength	Height (um)	Width (um)
DLY4X0P5MA10TR	2.00	2.20

Functional Schematic

AC Power

Pin	Power (uW/MHz)
	X0P5M
A	0.0053

Pin Capacitance

Pin	Capacitance (pF)
	X0P5M
A	0.0014

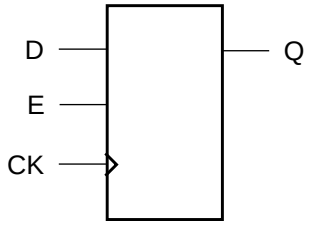
Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)	K_{load} (ns/pF)
	X0P5M	X0P5M
A → Y ↑	0.1308	4.7047
A → Y ↓	0.1481	2.9586

Cell Description

The EDFFQ cell is a positive-edge triggered, static D-type flip-flop with a synchronous, active-high enable (E). The cell has a single output (Q).

Logic Symbol



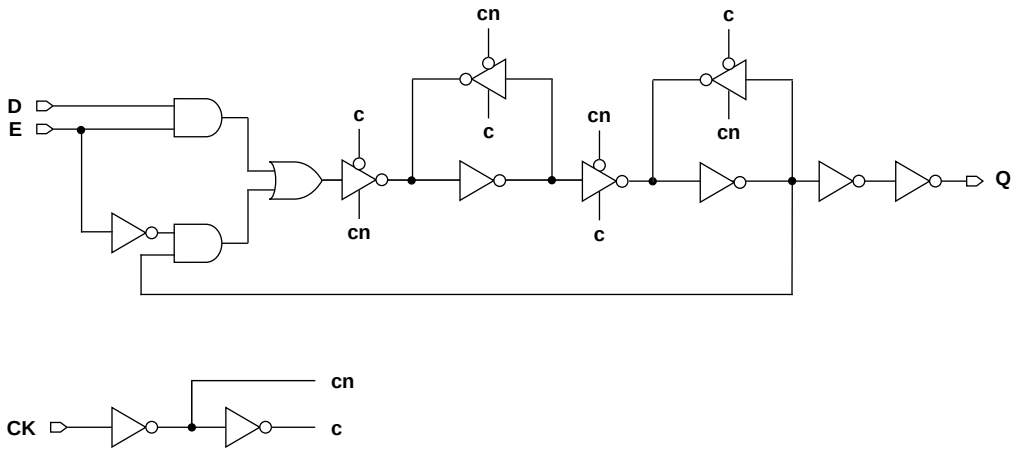
Function Table

E	D	CK	Q[n+1]
0	x	x	Q[n]
1	0	↑	0
1	1	↑	1
x	x	↓	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
EDFFQX0P5MA10TR	2.00	6.20
EDFFQX1MA10TR	2.00	6.20
EDFFQX2MA10TR	2.00	6.60
EDFFQX3MA10TR	2.00	6.60

Functional Schematic



AC Power

Pin	Power (uW/MHz)			
	X0P5M	X1P0M	X2P0M	X3P0M
D	0.0061	0.0069	0.0086	0.0095
CK	0.0038	0.0044	0.0050	0.0058
E	0.0060	0.0070	0.0086	0.0094
Q	0.0052	0.0060	0.0082	0.0107

Pin Capacitance

Pin	Capacitance (pF)			
	X0P5M	X1P0M	X2P0M	X3P0M
D	0.0012	0.0011	0.0013	0.0014
CK	0.0009	0.0010	0.0010	0.0012
E	0.0022	0.0023	0.0028	0.0028

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X0P5M	X1P0M	X2P0M	X3P0M	X0P5M	X1P0M	X2P0M	X3P0M
CK → Q ↑	0.0935	0.0783	0.0739	0.0711	4.2855	2.3344	1.1614	0.7855
CK → Q ↓	0.0860	0.0724	0.0728	0.0739	3.0069	1.5219	0.7553	0.5148

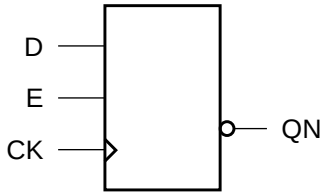
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X0P5M	X1P0M	X2P0M	X3P0M
D	setup ↑ → CK	0.0469	0.0430	0.0391	0.0430
	setup ↓ → CK	0.0586	0.0508	0.0508	0.0508
	hold ↑ → CK	-0.0195	-0.0195	-0.0156	-0.0195
	hold ↓ → CK	-0.0391	-0.0352	-0.0352	-0.0312
CK	minpwh	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830
E	setup ↑ → CK	0.0625	0.0547	0.0508	0.0508
	setup ↓ → CK	0.0469	0.0391	0.0391	0.0391
	hold ↑ → CK	-0.0312	-0.0273	-0.0234	-0.0273
	hold ↓ → CK	-0.0312	-0.0273	-0.0234	-0.0273

Cell Description

The EDFFQN cell is a positive-edge triggered, static D-type flip-flop with synchronous active-high enable (E). The cell has a single inverted output (QN).

Logic Symbol



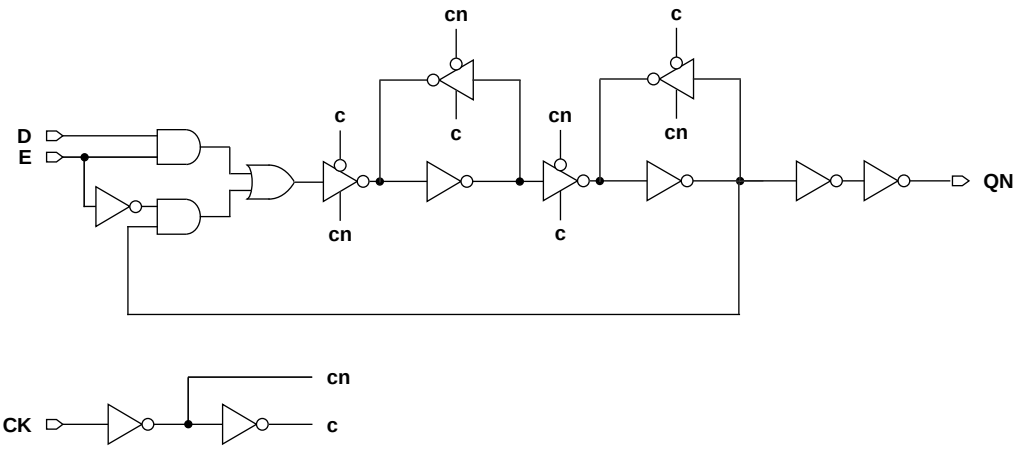
Function Table

E	D	CK	QN[n+1]
0	x	x	QN[n]
1	0	⎍	1
1	1	⎍	0
x	x	⎎	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
EDFFQNX0P5MA10TR	2.00	6.20
EDFFQNX1MA10TR	2.00	6.20
EDFFQNX2MA10TR	2.00	6.60
EDFFQNX3MA10TR	2.00	7.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)			
	X0P5M	X1P0M	X2P0M	X3P0M
D	0.0056	0.0068	0.0086	0.0097
CK	0.0038	0.0043	0.0050	0.0057
E	0.0056	0.0067	0.0082	0.0087
QN	0.0061	0.0068	0.0087	0.0108

Pin Capacitance

Pin	Capacitance (pF)			
	X0P5M	X1P0M	X2P0M	X3P0M
D	0.0011	0.0012	0.0015	0.0015
CK	0.0009	0.0010	0.0010	0.0011
E	0.0022	0.0025	0.0030	0.0034

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X0P5M	X1P0M	X2P0M	X3P0M	X0P5M	X1P0M	X2P0M	X3P0M
CK → QN ↑	0.0941	0.0788	0.0741	0.0699	4.2978	2.3352	1.1654	0.7854
CK → QN ↓	0.0868	0.0731	0.0729	0.0728	3.0219	1.6301	0.7613	0.5196

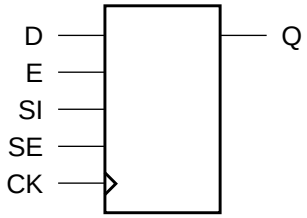
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X0P5M	X1P0M	X2P0M	X3P0M
D	setup ↑ → CK	0.0469	0.0430	0.0391	0.0430
	setup ↓ → CK	0.0508	0.0469	0.0430	0.0469
	hold ↑ → CK	-0.0234	-0.0234	-0.0195	-0.0195
	hold ↓ → CK	-0.0117	-0.0117	-0.0078	-0.0117
CK	minpwh	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830
E	setup ↑ → CK	0.0469	0.0469	0.0391	0.0430
	setup ↓ → CK	0.0391	0.0352	0.0312	0.0352
	hold ↑ → CK	-0.0234	-0.0234	-0.0234	-0.0234
	hold ↓ → CK	-0.0078	-0.0117	-0.0078	-0.0078

Cell Description

The ESDFFQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and synchronous active-high enable (E). The cell has a single output (Q).

Logic Symbol



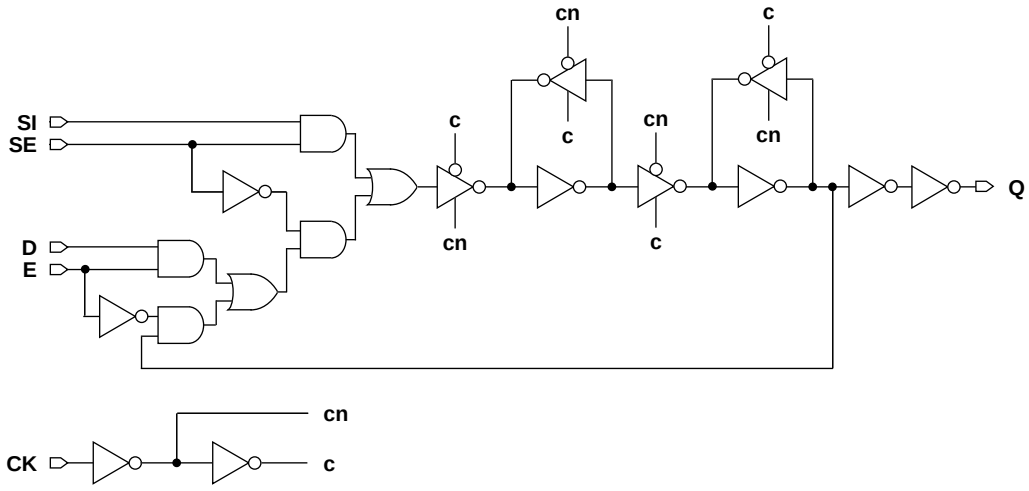
Function Table

D	E	SI	SE	CK	Q[n+1]
x	x	1	1	⎍	1
x	x	0	1	⎍	0
x	0	x	0	⎍	Q[n]
0	1	x	0	⎍	0
1	1	x	0	⎍	1
x	x	x	x	⎎	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
ESDFFQX0P5MA10TR	2.00	7.60
ESDFFQX1MA10TR	2.00	7.60
ESDFFQX2MA10TR	2.00	7.80
ESDFFQX3MA10TR	2.00	8.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)			
	X0P5M	X1P0M	X2P0M	X3P0M
SI	0.0053	0.0064	0.0075	0.0082
SE	0.0058	0.0069	0.0081	0.0087
D	0.0072	0.0085	0.0103	0.0109
CK	0.0039	0.0044	0.0052	0.0059
E	0.0070	0.0086	0.0099	0.0106
Q	0.0052	0.0061	0.0086	0.0106

Pin Capacitance

Pin	Capacitance (pF)			
	X0P5M	X1P0M	X2P0M	X3P0M
SI	0.0008	0.0007	0.0007	0.0007
SE	0.0017	0.0017	0.0019	0.0018
D	0.0012	0.0012	0.0014	0.0014
CK	0.0009	0.0009	0.0011	0.0012
E	0.0015	0.0019	0.0019	0.0019

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X0P5M	X1P0M	X2P0M	X3P0M	X0P5M	X1P0M	X2P0M	X3P0M
CK → Q ↑	0.0933	0.0770	0.0769	0.0714	4.2777	2.3242	1.1619	0.7861
CK → Q ↓	0.0851	0.0713	0.0752	0.0731	2.8651	1.5005	0.7514	0.5221

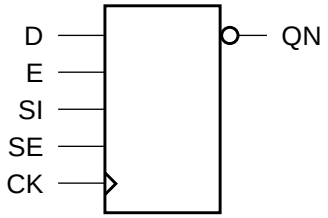
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**
SI	setup ↑ → CK	0.0586	0.0586	0.0586	0.0625
	setup ↓ → CK	0.0781	0.0820	0.0820	0.0898
	hold ↑ → CK	-0.0273	-0.0312	-0.0312	-0.0391
	hold ↓ → CK	-0.0547	-0.0625	-0.0664	-0.0703
SE	setup ↑ → CK	0.0898	0.0977	0.0977	0.1055
	setup ↓ → CK	0.0664	0.0625	0.0547	0.0625
	hold ↑ → CK	-0.0234	-0.0234	-0.0273	-0.0312
	hold ↓ → CK	-0.0352	-0.0391	-0.0273	-0.0312
D	setup ↑ → CK	0.0742	0.0703	0.0625	0.0664
	setup ↓ → CK	0.0938	0.0820	0.0742	0.0742
	hold ↑ → CK	-0.0430	-0.0430	-0.0352	-0.0391
	hold ↓ → CK	-0.0703	-0.0664	-0.0547	-0.0586
CK	minpwh	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830
E	setup ↑ → CK	0.0938	0.0820	0.0742	0.0781
	setup ↓ → CK	0.0742	0.0664	0.0586	0.0625
	hold ↑ → CK	-0.0547	-0.0547	-0.0430	-0.0508
	hold ↓ → CK	-0.0508	-0.0508	-0.0469	-0.0508

Cell Description

The ESDFFQN cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and synchronous active-high enable (E). The cell has a single output (QN).

Logic Symbol



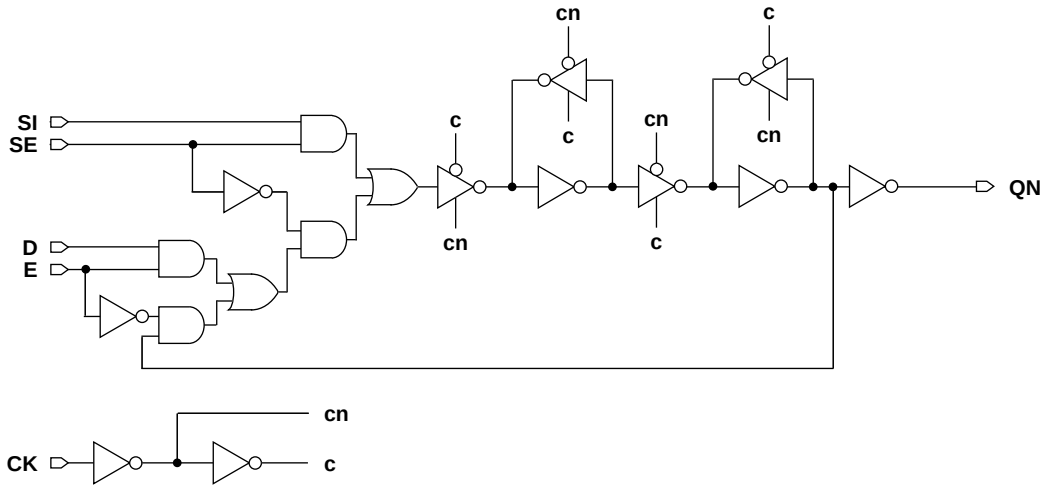
Function Table

D	E	SI	SE	CK	QN[n+1]
x	x	1	1	⎍	0
x	x	0	1	⎍	1
x	0	x	0	⎍	QN[n]
0	1	x	0	⎍	1
1	1	x	0	⎍	0
x	x	x	x	⎎	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
ESDFFQNX0P5MA10TR	2.00	7.60
ESDFFQNX1MA10TR	2.00	7.60
ESDFFQNX2MA10TR	2.00	7.80
ESDFFQNX3MA10TR	2.00	8.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)			
	X0P5M	X1P0M	X2P0M	X3P0M
SI	0.0051	0.0065	0.0077	0.0085
SE	0.0057	0.0070	0.0081	0.0088
D	0.0071	0.0085	0.0105	0.0113
CK	0.0039	0.0044	0.0052	0.0057
E	0.0068	0.0085	0.0101	0.0108
QN	0.0052	0.0066	0.0086	0.0102

Pin Capacitance

Pin	Capacitance (pF)			
	X0P5M	X1P0M	X2P0M	X3P0M
SI	0.0007	0.0007	0.0007	0.0007
SE	0.0018	0.0017	0.0019	0.0019
D	0.0012	0.0011	0.0014	0.0014
CK	0.0009	0.0010	0.0011	0.0011
E	0.0014	0.0018	0.0020	0.0020

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X0P5M	X1P0M	X2P0M	X3P0M	X0P5M	X1P0M	X2P0M	X3P0M
CK → QN ↑	0.0973	0.0837	0.0847	0.0796	4.2429	2.3204	1.1585	0.7814
CK → QN ↓	0.1075	0.0907	0.0883	0.0903	2.4469	1.3327	0.7205	0.4603

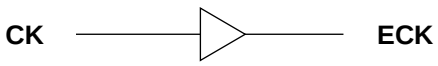
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**
SI	setup ↑ → CK	0.0625	0.0508	0.0547	0.0586
	setup ↓ → CK	0.0859	0.0781	0.0820	0.0859
	hold ↑ → CK	-0.0312	-0.0312	-0.0352	-0.0391
	hold ↓ → CK	-0.0625	-0.0625	-0.0664	-0.0703
SE	setup ↑ → CK	0.0977	0.0938	0.0938	0.1016
	setup ↓ → CK	0.0703	0.0586	0.0508	0.0547
	hold ↑ → CK	-0.0273	-0.0234	-0.0312	-0.0312
	hold ↓ → CK	-0.0391	-0.0391	-0.0312	-0.0352
D	setup ↑ → CK	0.0781	0.0703	0.0586	0.0625
	setup ↓ → CK	0.0938	0.0820	0.0703	0.0742
	hold ↑ → CK	-0.0469	-0.0469	-0.0391	-0.0430
	hold ↓ → CK	-0.0703	-0.0703	-0.0547	-0.0586
CK	minpwh	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830
E	setup ↑ → CK	0.0938	0.0820	0.0703	0.0742
	setup ↓ → CK	0.0781	0.0703	0.0586	0.0586
	hold ↑ → CK	-0.0586	-0.0547	-0.0430	-0.0469
	hold ↓ → CK	-0.0625	-0.0547	-0.0469	-0.0508

Cell Description

The FRICG cell is a free running integrated latch clock gate, There are no enable signals since the ECK always reflects the value of (CK). The purpose of this cell is to match the delay of the POSTICG and PREICG cells across PVT.

Logic Symbol



Function Table

CK	ECK
1	1
0	0

Cell Size

Drive Strength	Height (um)	Width (um)
FRICGX0P5BA10TR	2.00	1.60
FRICGX0P6BA10TR	2.00	1.60
FRICGX0P7BA10TR	2.00	1.60
FRICGX0P8BA10TR	2.00	1.60
FRICGX1BA10TR	2.00	1.60
FRICGX1P2BA10TR	2.00	2.00
FRICGX1P4BA10TR	2.00	2.00
FRICGX1P7BA10TR	2.00	2.00
FRICGX2BA10TR	2.00	2.00
FRICGX2P5BA10TR	2.00	2.20
FRICGX3BA10TR	2.00	2.20
FRICGX3P5BA10TR	2.00	3.00
FRICGX4BA10TR	2.00	3.00
FRICGX5BA10TR	2.00	3.20
FRICGX6BA10TR	2.00	3.40
FRICGX7P5BA10TR	2.00	4.00
FRICGX9BA10TR	2.00	4.40
FRICGX11BA10TR	2.00	5.20
FRICGX13BA10TR	2.00	5.60
FRICGX16BA10TR	2.00	6.80

Functional Schematic

AC Power

Pin	Power (uW/MHz)							
	X0P5B	**X0P6B**	**X0P7B**	**X0P8B**	**X1P0B**	**X1P2B**	**X1P4B**	**X1P7B**
CK	0.0021	0.0022	0.0023	0.0024	0.0027	0.0035	0.0037	0.0041

AC Power (Cont'd.)

Pin	Power (uW/MHz)							
	X2P0B	**X2P5B**	**X3P0B**	**X3P5B**	**X4P0B**	**X5P0B**	**X6P0B**	**X7P5B**
CK	0.0047	0.0058	0.0065	0.0080	0.0088	0.0110	0.0128	0.0166

AC Power (Cont'd.)

Pin	Power (uW/MHz)			
	X9P0B	**X11P0B**	**X13P0B**	**X16P0B**
CK	0.0195	0.0240	0.0274	0.0337

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5B	**X0P6B**	**X0P7B**	**X0P8B**	**X1P0B**	**X1P2B**	**X1P4B**	**X1P7B**
CK	0.0009	0.0009	0.0010	0.0010	0.0010	0.0011	0.0012	0.0013

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)							
	X2P0B	**X2P5B**	**X3P0B**	**X3P5B**	**X4P0B**	**X5P0B**	**X6P0B**	**X7P5B**
CK	0.0014	0.0017	0.0018	0.0023	0.0026	0.0030	0.0034	0.0048

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)			
	X9P0B	**X11P0B**	**X13P0B**	**X16P0B**
CK	0.0053	0.0066	0.0074	0.0092

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5B	**X0P6B**	**X0P7B**	**X0P8B**	**X1P0B**	**X1P2B**	**X1P4B**	**X1P7B**
CK → ECK ↑	0.0366	0.0375	0.0389	0.0393	0.0383	0.0382	0.0374	0.0360
CK → ECK ↓	0.0328	0.0335	0.0347	0.0352	0.0341	0.0348	0.0341	0.0333

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)							
	X2P0B	**X2P5B**	**X3P0B**	**X3P5B**	**X4P0B**	**X5P0B**	**X6P0B**	**X7P5B**
CK → ECK ↑	0.0361	0.0341	0.0325	0.0339	0.0334	0.0330	0.0326	0.0322
CK → ECK ↓	0.0339	0.0321	0.0318	0.0322	0.0325	0.0319	0.0318	0.0307

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)			
	X9P0B	**X11P0B**	**X13P0B**	**X16P0B**
CK → ECK ↑	0.0315	0.0316	0.0304	0.0308
CK → ECK ↓	0.0308	0.0308	0.0305	0.0301

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X0P5B	**X0P6B**	**X0P7B**	**X0P8B**	**X1P0B**	**X1P2B**	**X1P4B**	**X1P7B**
CK → ECK ↑	4.7835	4.0971	3.5531	3.0632	2.4902	1.9016	1.6491	1.3828
CK → ECK ↓	3.9687	3.3981	2.9286	2.6127	2.1270	1.6806	1.4446	1.2294

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X2P0B	**X2P5B**	**X3P0B**	**X3P5B**	**X4P0B**	**X5P0B**	**X6P0B**	**X7P5B**
CK → ECK ↑	1.1887	0.9308	0.7844	0.6624	0.5848	0.4679	0.3882	0.3099
CK → ECK ↓	1.0461	0.8342	0.7002	0.6024	0.5294	0.4169	0.3505	0.2795

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)			
	X9P0B	**X11P0B**	**X13P0B**	**X16P0B**
CK → ECK ↑	0.2581	0.2101	0.1788	0.1446
CK → ECK ↓	0.2322	0.1882	0.1642	0.1345

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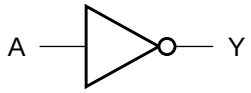
Cell Description

The INV cell provides the logical inversion of a single input (A). The output (Y) is represented by the logic equation:

$Y = \overline{A}$

Logic Symbol



Function Table

A	Y
0	1
1	0

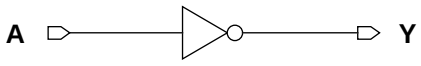
Cell Size

Drive Strength	Height (um)	Width (um)
INVX0P5BA10TR	2.00	0.60
INVX0P5MA10TR	2.00	0.60
INVX0P6BA10TR	2.00	0.60
INVX0P6MA10TR	2.00	0.60
INVX0P7BA10TR	2.00	0.60
INVX0P7MA10TR	2.00	0.60
INVX0P8BA10TR	2.00	0.60
INVX0P8MA10TR	2.00	0.60
INVX1BA10TR	2.00	0.60
INVX1MA10TR	2.00	0.60
INVX1P2BA10TR	2.00	0.80
INVX1P2MA10TR	2.00	0.80
INVX1P4BA10TR	2.00	0.80
INVX1P4MA10TR	2.00	0.80
INVX1P7BA10TR	2.00	0.80
INVX1P7MA10TR	2.00	0.80
INVX2BA10TR	2.00	0.80
INVX2MA10TR	2.00	0.80
INVX2P5BA10TR	2.00	1.20
INVX2P5MA10TR	2.00	1.20

Cell Size (Cont'd.)

Drive Strength	Height (um)	Width (um)
INVX3BA10TR	2.00	1.20
INVX3MA10TR	2.00	1.20
INVX3P5BA10TR	2.00	1.40
INVX3P5MA10TR	2.00	1.40
INVX4BA10TR	2.00	1.40
INVX4MA10TR	2.00	1.40
INVX5BA10TR	2.00	1.60
INVX5MA10TR	2.00	1.60
INVX6BA10TR	2.00	2.00
INVX6MA10TR	2.00	2.00
INVX7P5BA10TR	2.00	2.40
INVX7P5MA10TR	2.00	2.40
INVX9BA10TR	2.00	2.60
INVX9MA10TR	2.00	2.60
INVX11BA10TR	2.00	3.20
INVX11MA10TR	2.00	3.20
INVX13BA10TR	2.00	3.80
INVX13MA10TR	2.00	3.80
INVX16BA10TR	2.00	4.60
INVX16MA10TR	2.00	4.60

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P5B	**X0P5M**	**X0P6B**	**X0P6M**	**X0P7B**	**X0P7M**	**X0P8B**	**X0P8M**
A	0.0011	0.0012	0.0012	0.0014	0.0014	0.0015	0.0015	0.0017

AC Power (Cont'd.)

Pin	Power (uW/MHz)							
	X1P0B	**X1P0M**	**X1P2B**	**X1P2M**	**X1P4B**	**X1P4M**	**X1P7B**	**X1P7M**
A	0.0017	0.0019	0.0021	0.0023	0.0024	0.0027	0.0027	0.0030

AC Power (Cont'd.)

Pin	Power (uW/MHz)							
	X2P0B	**X2P0M**	**X2P5B**	**X2P5M**	**X3P0B**	**X3P0M**	**X3P5B**	**X3P5M**
A	0.0031	0.0034	0.0041	0.0046	0.0048	0.0052	0.0054	0.0062

AC Power (Cont'd.)

Pin	Power (uW/MHz)							
	X4P0B	**X4P0M**	**X5P0B**	**X5P0M**	**X6P0B**	**X6P0M**	**X7P5B**	**X7P5M**
A	0.0062	0.0068	0.0079	0.0087	0.0094	0.0102	0.0114	0.0130

AC Power (Cont'd.)

Pin	Power (uW/MHz)							
	X9P0B	**X9P0M**	**X11P0B**	**X11P0M**	**X13P0B**	**X13P0M**	**X16P0B**	**X16P0M**
A	0.0143	0.0157	0.0175	0.0192	0.0207	0.0227	0.0252	0.0277

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5B	**X0P5M**	**X0P6B**	**X0P6M**	**X0P7B**	**X0P7M**	**X0P8B**	**X0P8M**
A	0.0012	0.0012	0.0013	0.0015	0.0014	0.0016	0.0015	0.0017

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)							
	X1P0B	**X1P0M**	**X1P2B**	**X1P2M**	**X1P4B**	**X1P4M**	**X1P7B**	**X1P7M**
A	0.0017	0.0019	0.0023	0.0026	0.0026	0.0030	0.0029	0.0033

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)							
	X2P0B	**X2P0M**	**X2P5B**	**X2P5M**	**X3P0B**	**X3P0M**	**X3P5B**	**X3P5M**
A	0.0033	0.0037	0.0042	0.0048	0.0049	0.0055	0.0058	0.0067

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)							
	X4P0B	**X4P0M**	**X5P0B**	**X5P0M**	**X6P0B**	**X6P0M**	**X7P5B**	**X7P5M**
A	0.0066	0.0073	0.0082	0.0092	0.0099	0.0111	0.0122	0.0140

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)							
	X9P0B	**X9P0M**	**X11P0B**	**X11P0M**	**X13P0B**	**X13P0M**	**X16P0B**	**X16P0M**
A	0.0150	0.0168	0.0183	0.0205	0.0216	0.0242	0.0266	0.0295

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5B	**X0P5M**	**X0P6B**	**X0P6M**	**X0P7B**	**X0P7M**	**X0P8B**	**X0P8M**
A → Y ↑	0.0091	0.0096	0.0086	0.0095	0.0083	0.0090	0.0080	0.0087
A → Y ↓	0.0084	0.0071	0.0080	0.0070	0.0077	0.0068	0.0075	0.0065

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)							
	X1P0B	**X1P0M**	**X1P2B**	**X1P2M**	**X1P4B**	**X1P4M**	**X1P7B**	**X1P7M**
A → Y ↑	0.0079	0.0083	0.0075	0.0079	0.0073	0.0079	0.0069	0.0076
A → Y ↓	0.0074	0.0063	0.0073	0.0061	0.0068	0.0061	0.0066	0.0059

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)							
	X2P0B	**X2P0M**	**X2P5B**	**X2P5M**	**X3P0B**	**X3P0M**	**X3P5B**	**X3P5M**
A → Y ↑	0.0070	0.0073	0.0071	0.0077	0.0070	0.0075	0.0068	0.0073
A → Y ↓	0.0066	0.0057	0.0069	0.0061	0.0068	0.0059	0.0066	0.0058

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)							
	X4P0B	**X4P0M**	**X5P0B**	**X5P0M**	**X6P0B**	**X6P0M**	**X7P5B**	**X7P5M**
A → Y ↑	0.0068	0.0072	0.0069	0.0073	0.0068	0.0071	0.0066	0.0072
A → Y ↓	0.0066	0.0057	0.0067	0.0058	0.0066	0.0057	0.0065	0.0058

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)							
	X9P0B	**X9P0M**	**X11P0B**	**X11P0M**	**X13P0B**	**X13P0M**	**X16P0B**	**X16P0M**
A → Y ↑	0.0069	0.0072	0.0068	0.0072	0.0068	0.0072	0.0068	0.0072
A → Y ↓	0.0067	0.0057	0.0067	0.0057	0.0066	0.0057	0.0066	0.0058

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X0P5B	**X0P5M**	**X0P6B**	**X0P6M**	**X0P7B**	**X0P7M**	**X0P8B**	**X0P8M**
A → Y ↑	4.7642	4.7662	4.0146	4.0166	3.4643	3.4595	3.0494	3.0509
A → Y ↓	3.9911	2.8360	3.4175	2.3580	2.9347	2.0468	2.6170	1.7864

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X1P0B	**X1P0M**	**X1P2B**	**X1P2M**	**X1P4B**	**X1P4M**	**X1P7B**	**X1P7M**
A → Y ↑	2.4858	2.4868	1.9550	1.9545	1.6898	1.6905	1.4106	1.4112
A → Y ↓	2.1023	1.4401	1.7599	1.1725	1.4465	1.0129	1.2290	0.8359

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X2P0B	**X2P0M**	**X2P5B**	**X2P5M**	**X3P0B**	**X3P0M**	**X3P5B**	**X3P5M**
A → Y ↑	1.2176	1.2180	0.9444	0.9449	0.7973	0.7976	0.6687	0.6687
A → Y ↓	1.0394	0.7077	0.8471	0.5816	0.7092	0.4797	0.5976	0.4043

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X4P0B	**X4P0M**	**X5P0B**	**X5P0M**	**X6P0B**	**X6P0M**	**X7P5B**	**X7P5M**
A → Y ↑	0.5916	0.5919	0.4725	0.4726	0.3892	0.3893	0.3078	0.3080
A → Y ↓	0.5232	0.3545	0.4236	0.2864	0.3489	0.2359	0.2808	0.1920

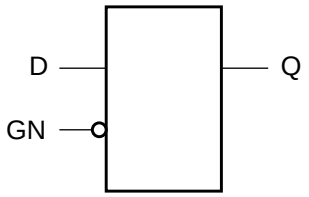
Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X9P0B	**X9P0M**	**X11P0B**	**X11P0M**	**X13P0B**	**X13P0M**	**X16P0B**	**X16P0M**
A → Y ↑	0.2587	0.2588	0.2104	0.2105	0.1773	0.1774	0.1435	0.1436
A → Y ↓	0.2343	0.1582	0.1911	0.1291	0.1615	0.1091	0.1305	0.0904

Cell Description

The LATNQ cell is a D-type active-low transparent latch. When the enable (GN) is low, data is transferred to the output (Q).

Logic Symbol



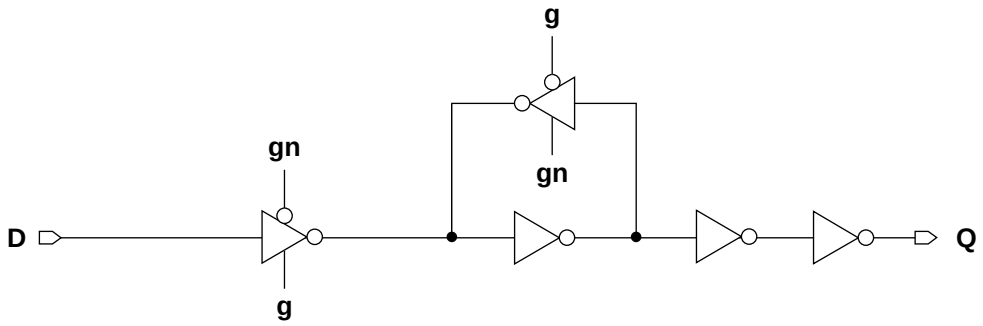
Function Table

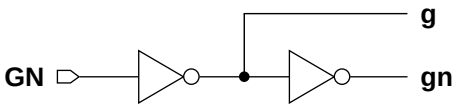
GN	D	Q[n+1]
0	0	0
0	1	1
1	x	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
LATNQX0P5MA10TR	2.00	2.40
LATNQX1MA10TR	2.00	2.40
LATNQX2MA10TR	2.00	2.60
LATNQX3MA10TR	2.00	3.00

Functional Schematic





AC Power

Pin	Power (uW/MHz)			
	X0P5M	X1P0M	X2P0M	X3P0M
D	0.0014	0.0019	0.0025	0.0030
GN	0.0016	0.0018	0.0021	0.0025
Q	0.0032	0.0040	0.0060	0.0084

Pin Capacitance

Pin	Capacitance (pF)			
	X0P5M	X1P0M	X2P0M	X3P0M
D	0.0010	0.0014	0.0018	0.0019
GN	0.0018	0.0018	0.0019	0.0021

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X0P5M	X1P0M	X2P0M	X3P0M	X0P5M	X1P0M	X2P0M	X3P0M
D → Q ↑	0.0505	0.0393	0.0387	0.0406	4.7285	2.4563	1.2028	0.7973
D → Q ↓	0.0608	0.0502	0.0496	0.0555	2.8750	1.4938	0.7170	0.4826
GN → Q ↑	0.0550	0.0475	0.0478	0.0480	4.7279	2.4561	1.2026	0.7972
GN → Q ↓	0.0608	0.0525	0.0534	0.0566	2.8746	1.4933	0.7168	0.4825

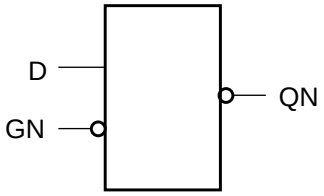
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X0P5M	X1P0M	X2P0M	X3P0M
D	setup ↑ → GN	0.0508	0.0352	0.0352	0.0352
	setup ↓ → GN	0.0547	0.0469	0.0469	0.0508
	hold ↑ → GN	-0.0352	-0.0234	-0.0234	-0.0234
	hold ↓ → GN	-0.0469	-0.0352	-0.0352	-0.0430
GN	minpwl	0.8830	0.8830	0.8830	0.8830

Cell Description

The LATNQN cell is a D-type active-low transparent latch. When the enable (GN) is low, data is transferred to the output (QN).

Logic Symbol



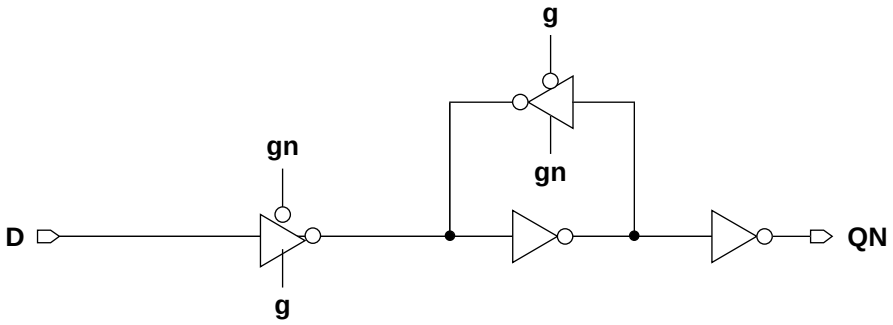
Function Table

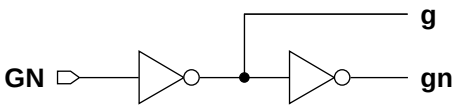
GN	D	QN[n+1]
0	0	1
0	1	0
1	x	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
LATNQNX0P5MA10TR	2.00	2.60
LATNQNX1MA10TR	2.00	2.60
LATNQNX2MA10TR	2.00	2.80
LATNQNX3MA10TR	2.00	3.00
LATNQNX4MA10TR	2.00	3.40

Functional Schematic





AC Power

Pin	Power (uW/MHz)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
D	0.0013	0.0019	0.0024	0.0027	0.0031
GN	0.0015	0.0018	0.0021	0.0024	0.0028
QN	0.0032	0.0042	0.0061	0.0082	0.0098

Pin Capacitance

Pin	Capacitance (pF)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
D	0.0010	0.0014	0.0016	0.0017	0.0019
GN	0.0017	0.0018	0.0019	0.0019	0.0021

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
D → QN ↑	0.0675	0.0572	0.0539	0.0558	0.0591
D → QN ↓	0.0639	0.0537	0.0521	0.0559	0.0568
GN → QN ↑	0.0663	0.0560	0.0525	0.0544	0.0555
GN → QN ↓	0.0688	0.0621	0.0609	0.0644	0.0652

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
D → QN ↑	4.6193	2.3825	1.1767	0.7859	0.5817
D → QN ↓	2.8247	1.4441	0.7131	0.4885	0.3622
GN → QN ↑	4.6196	2.3824	1.1766	0.7860	0.5817
GN → QN ↓	2.8248	1.4443	0.7130	0.4885	0.3622

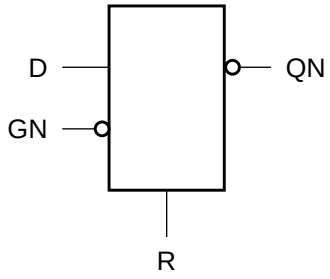
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)				
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D	setup ↑ → GN	0.0430	0.0273	0.0273	0.0273	0.0234
	setup ↓ → GN	0.0469	0.0391	0.0391	0.0391	0.0391
	hold ↑ → GN	-0.0273	-0.0156	-0.0156	-0.0156	-0.0156
	hold ↓ → GN	-0.0430	-0.0312	-0.0312	-0.0312	-0.0312
GN	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830

Cell Description

The LATNRPQN cell is a D-type active-low transparent latch with asynchronous active-high reset (R). When the enable (GN) is low, data is transferred to the output (QN).

Logic Symbol



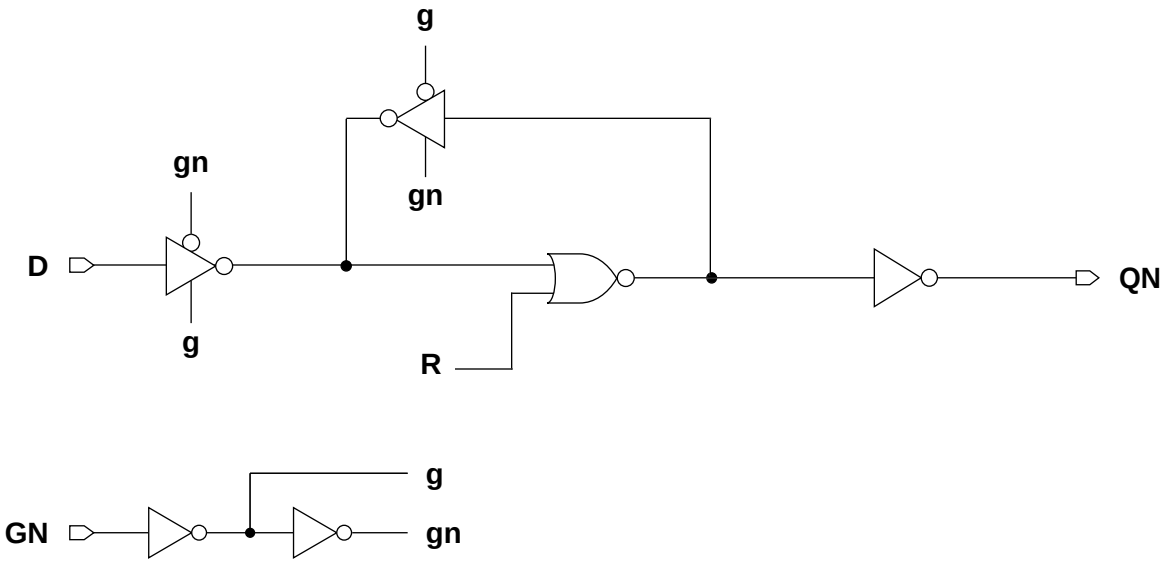
Function Table

R	GN	D	QN[n+1]
1	x	x	1
0	0	0	1
0	0	1	0
0	1	x	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
LATNRPQNX0P5MA10TR	2.00	2.80
LATNRPQNX1MA10TR	2.00	2.80
LATNRPQNX2MA10TR	2.00	3.00
LATNRPQNX3MA10TR	2.00	3.20
LATNRPQNX4MA10TR	2.00	3.60

Functional Schematic



AC Power

Pin	Power (uW/MHz)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
D	0.0014	0.0021	0.0026	0.0028	0.0032
GN	0.0016	0.0019	0.0023	0.0025	0.0029
R	0.0009	0.0012	0.0015	0.0016	0.0018
QN	0.0035	0.0047	0.0065	0.0089	0.0118

Pin Capacitance

Pin	Capacitance (pF)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
D	0.0010	0.0014	0.0017	0.0017	0.0019
GN	0.0017	0.0018	0.0019	0.0019	0.0021
R	0.0012	0.0016	0.0017	0.0016	0.0016

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
D → QN ↑	0.0717	0.0568	0.0572	0.0647	0.0698
D → QN ↓	0.0735	0.0625	0.0663	0.0770	0.0834
GN → QN ↑	0.0710	0.0566	0.0552	0.0627	0.0659
GN → QN ↓	0.0783	0.0701	0.0752	0.0850	0.0918
R → QN ↑	0.0294	0.0251	0.0294	0.0395	0.0436
R → QN ↓	0.0455	0.0428	0.0505	0.0603	0.0692

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
D → QN ↑	4.6441	2.3803	1.1765	0.7873	0.5840
D → QN ↓	2.7768	1.3110	0.6643	0.4638	0.3503
GN → QN ↑	4.6440	2.3803	1.1765	0.7873	0.5840
GN → QN ↓	2.7772	1.3111	0.6644	0.4638	0.3504
R → QN ↑	4.6576	2.3861	1.1794	0.7890	0.5850
R → QN ↓	2.7751	1.3105	0.6642	0.4637	0.3503

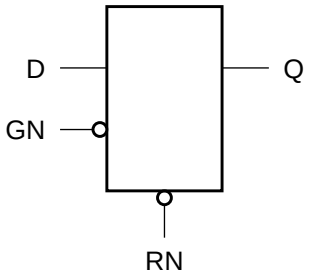
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)				
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D	setup ↑ → GN	0.0430	0.0312	0.0273	0.0273	0.0273
	setup ↓ → GN	0.0508	0.0430	0.0391	0.0430	0.0430
	hold ↑ → GN	-0.0273	-0.0195	-0.0156	-0.0156	-0.0156
	hold ↓ → GN	-0.0430	-0.0352	-0.0312	-0.0352	-0.0352
GN	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830
R	minpwh	0.8830	0.8830	0.8830	0.8830	0.8830
	recovery	-0.0039	-0.0156	-0.0156	-0.0117	-0.0078
	removal	0.0078	0.0195	0.0195	0.0156	0.0117

Cell Description

The LATNRQ cell is a D-type active-low transparent latch with asynchronous active-low reset (RN). When the enable (GN) is low, data is transferred to the output (Q).

Logic Symbol



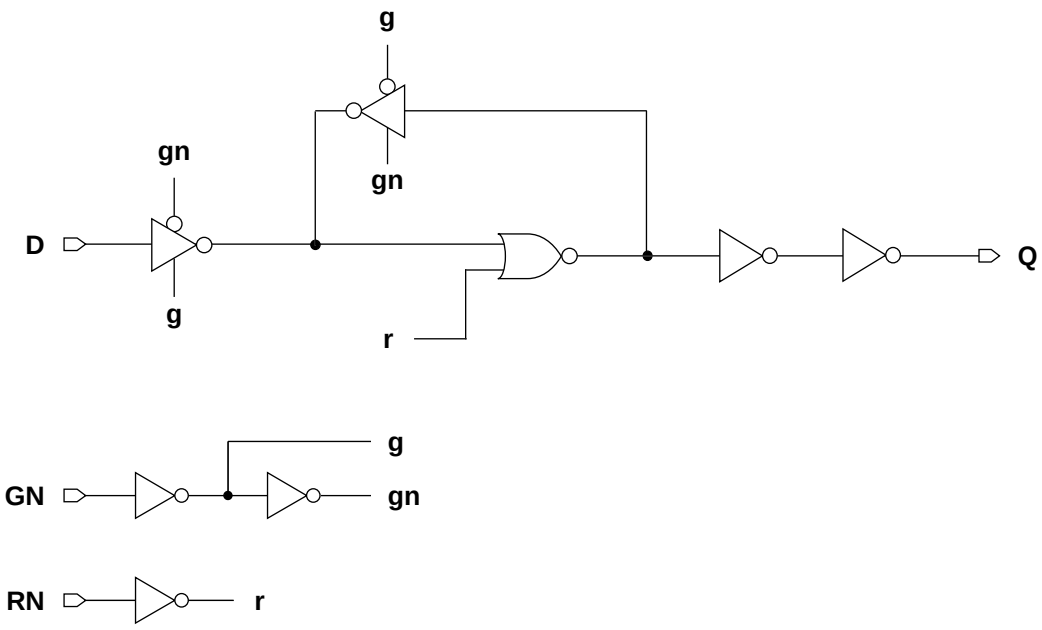
Function Table

RN	GN	D	Q[n+1]
0	x	x	0
1	0	0	0
1	0	1	1
1	1	x	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
LATNRQX0P5MA10TR	2.00	3.00
LATNRQX1MA10TR	2.00	3.00
LATNRQX2MA10TR	2.00	3.20
LATNRQX3MA10TR	2.00	3.40

Functional Schematic



AC Power

Pin	Power (uW/MHz)			
	X0P5M	X1P0M	X2P0M	X3P0M
D	0.0016	0.0022	0.0027	0.0030
GN	0.0017	0.0019	0.0022	0.0026
RN	0.0011	0.0013	0.0015	0.0017
Q	0.0034	0.0042	0.0063	0.0087

Pin Capacitance

Pin	Capacitance (pF)			
	X0P5M	X1P0M	X2P0M	X3P0M
D	0.0011	0.0015	0.0017	0.0017
GN	0.0017	0.0019	0.0020	0.0022
RN	0.0020	0.0023	0.0024	0.0024

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X0P5M	X1P0M	X2P0M	X3P0M	X0P5M	X1P0M	X2P0M	X3P0M
D → Q ↑	0.0542	0.0464	0.0491	0.0553	4.8346	2.4719	1.2058	0.8088
D → Q ↓	0.0641	0.0547	0.0563	0.0618	3.0481	1.6518	0.7898	0.5349
GN → Q ↑	0.0578	0.0517	0.0540	0.0572	4.8339	2.4718	1.2056	0.8086
GN → Q ↓	0.0649	0.0564	0.0587	0.0621	3.0482	1.6515	0.7896	0.5348
RN → Q ↑	0.0573	0.0491	0.0515	0.0577	4.8340	2.4717	1.2059	0.8088
RN → Q ↓	0.0307	0.0405	0.0490	0.0585	2.8101	1.6025	0.7693	0.5244

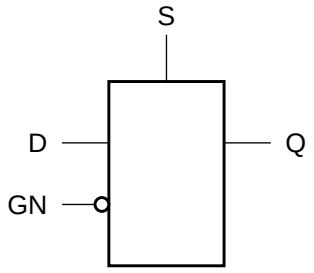
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X0P5M	X1P0M	X2P0M	X3P0M
D	setup ↑ → GN	0.0508	0.0430	0.0430	0.0508
	setup ↓ → GN	0.0586	0.0508	0.0547	0.0586
	hold ↑ → GN	-0.0352	-0.0273	-0.0312	-0.0352
	hold ↓ → GN	-0.0508	-0.0430	-0.0430	-0.0469
GN	minpwl	0.8830	0.8830	0.8830	0.8830
RN	minpwl	0.8830	0.8830	0.8830	0.8830
	recovery	0.0469	0.0391	0.0391	0.0430
	removal	-0.0430	-0.0352	-0.0352	-0.0391

Cell Description

The LATNSPQ cell is a D-type active-low transparent latch with asynchronous active-high set (S). When the enable (GN) is low, data is transferred to the output (Q).

Logic Symbol



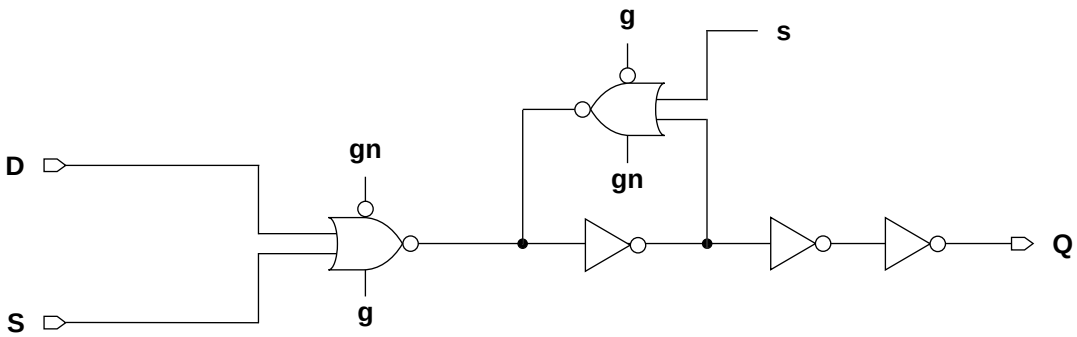
Function Table

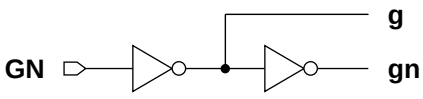
S	GN	D	Q[n+1]
1	x	x	1
0	0	0	0
0	0	1	1
0	1	x	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
LATNSPQX0P5MA10TR	2.00	3.00
LATNSPQX1MA10TR	2.00	3.00
LATNSPQX2MA10TR	2.00	3.20
LATNSPQX3MA10TR	2.00	4.20

Functional Schematic





AC Power

Pin	Power (uW/MHz)			
	X0P5M	X1P0M	X2P0M	X3P0M
D	0.0016	0.0022	0.0025	0.0045
GN	0.0017	0.0020	0.0022	0.0030
S	0.0012	0.0016	0.0017	0.0028
Q	0.0036	0.0045	0.0071	0.0086

Pin Capacitance

Pin	Capacitance (pF)			
	X0P5M	X1P0M	X2P0M	X3P0M
D	0.0011	0.0015	0.0016	0.0029
GN	0.0017	0.0018	0.0019	0.0021
S	0.0015	0.0018	0.0018	0.0027

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X0P5M	X1P0M	X2P0M	X3P0M	X0P5M	X1P0M	X2P0M	X3P0M
D → Q ↑	0.0529	0.0426	0.0470	0.0438	4.7242	2.4277	1.2066	0.7973
D → Q ↓	0.0749	0.0659	0.0766	0.0634	2.9747	1.5360	0.7620	0.4931
GN → Q ↑	0.0565	0.0493	0.0529	0.0542	4.7240	2.4274	1.2063	0.7971
GN → Q ↓	0.0693	0.0611	0.0704	0.0588	2.9739	1.5349	0.7615	0.4920
S → Q ↑	0.0357	0.0440	0.0537	0.0703	4.6960	2.4397	1.2156	0.8138
S → Q ↓	0.0778	0.0686	0.0792	0.0662	2.9747	1.5360	0.7620	0.4931

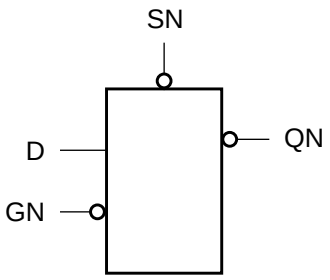
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X0P5M	X1P0M	X2P0M	X3P0M
D	setup ↑ → GN	0.0508	0.0391	0.0430	0.0352
	setup ↓ → GN	0.0703	0.0625	0.0703	0.0586
	hold ↑ → GN	-0.0352	-0.0273	-0.0273	-0.0234
	hold ↓ → GN	-0.0625	-0.0547	-0.0625	-0.0508
GN	minpwl	0.8830	0.8830	0.8830	0.8830
S	minpwh	0.8830	0.8830	0.8830	0.8830
	recovery	0.0703	0.0625	0.0703	0.0586
	removal	-0.0664	-0.0586	-0.0664	-0.0547

Cell Description

The LATNSQN cell is a D-type active-low transparent latch with asynchronous active-low set (SN). When the enable (GN) is low, data is transferred to the output (QN).

Logic Symbol



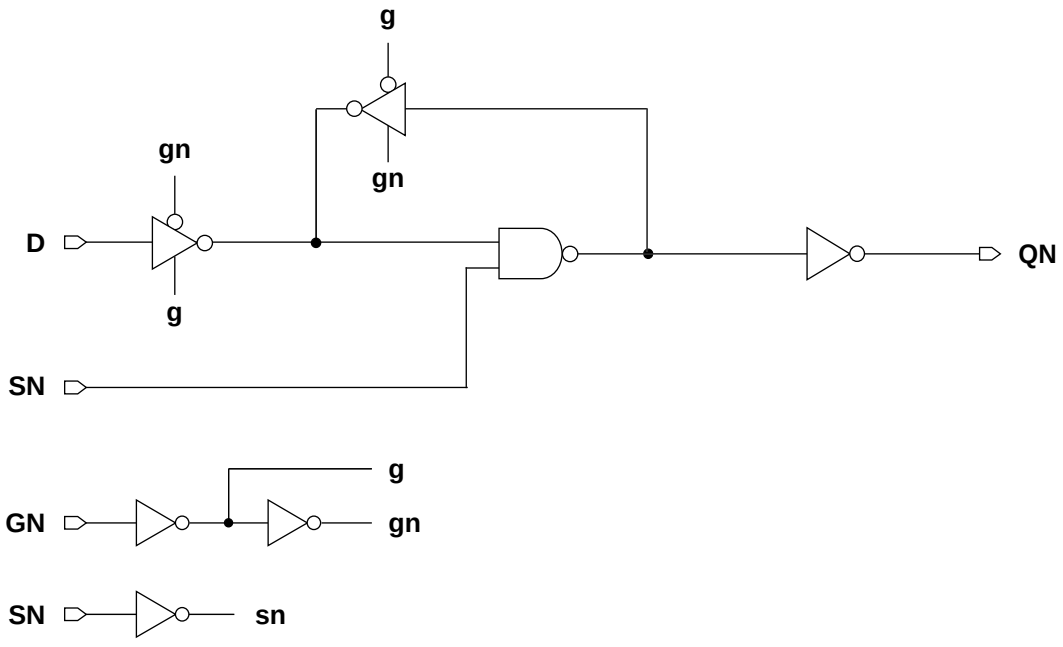
Function Table

SN	GN	D	QN[n+1]
0	x	x	0
1	0	0	1
1	0	1	0
1	1	x	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
LATNSQNX0P5MA10TR	2.00	2.80
LATNSQNX1MA10TR	2.00	2.80
LATNSQNX2MA10TR	2.00	3.00
LATNSQNX3MA10TR	2.00	3.20
LATNSQNX4MA10TR	2.00	3.40

Functional Schematic



AC Power

Pin	Power (uW/MHz)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D	0.0014	0.0020	0.0026	0.0028	0.0031
GN	0.0015	0.0018	0.0022	0.0024	0.0028
SN	0.0007	0.0009	0.0014	0.0016	0.0018
QN	0.0034	0.0044	0.0063	0.0082	0.0102

Pin Capacitance

Pin	Capacitance (pF)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D	0.0010	0.0014	0.0017	0.0017	0.0019
GN	0.0020	0.0022	0.0023	0.0024	0.0026
SN	0.0011	0.0013	0.0017	0.0017	0.0017

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D → QN ↑	0.0766	0.0645	0.0609	0.0674	0.0737
D → QN ↓	0.0672	0.0568	0.0564	0.0616	0.0653
GN → QN ↑	0.0754	0.0634	0.0603	0.0658	0.0702
GN → QN ↓	0.0718	0.0646	0.0644	0.0701	0.0737
SN → QN ↑	0.0355	0.0350	0.0353	0.0416	0.0472
SN → QN ↓	0.0371	0.0376	0.0370	0.0435	0.0497

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D → QN ↑	4.5741	2.3658	1.1666	0.7847	0.5861
D → QN ↓	2.8072	1.4490	0.7162	0.4920	0.3696
GN → QN ↑	4.5740	2.3658	1.1666	0.7847	0.5861
GN → QN ↓	2.8078	1.4492	0.7163	0.4921	0.3696
SN → QN ↑	4.5699	2.3649	1.1663	0.7847	0.5861
SN → QN ↓	2.8215	1.4582	0.7192	0.4928	0.3699

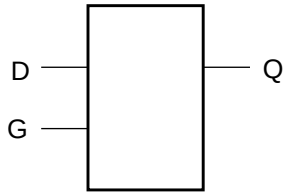
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)				
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D	setup ↑ → GN	0.0430	0.0312	0.0273	0.0273	0.0234
	setup ↓ → GN	0.0547	0.0430	0.0391	0.0430	0.0430
	hold ↑ → GN	-0.0273	-0.0156	-0.0156	-0.0156	-0.0156
	hold ↓ → GN	-0.0469	-0.0352	-0.0312	-0.0352	-0.0352
GN	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830
SN	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830
	recovery	0.0039	0.0039	0.0039	0.0078	0.0078
	removal	0.0000	0.0000	0.0000	-0.0039	-0.0039

Cell Description

The LATQ cell is a D-type active-high transparent latch. When the enable (G) is high, data is transferred to the output (Q).

Logic Symbol



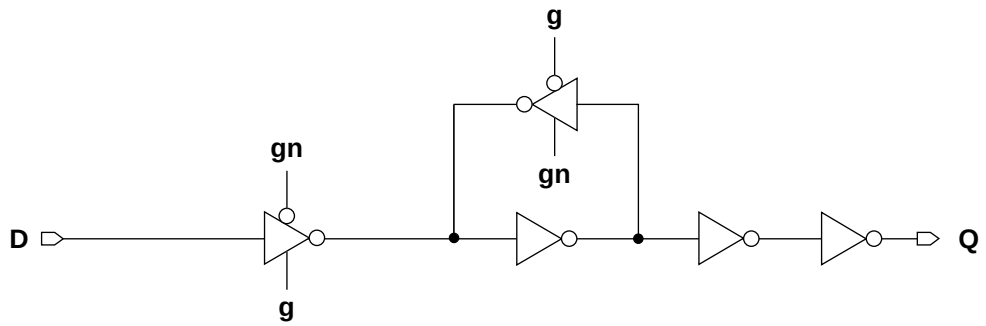
Function Table

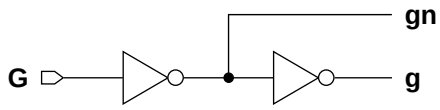
G	D	Q[n+1]
1	0	0
1	1	1
0	x	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
LATQX0P5MA10TR	2.00	2.40
LATQX1MA10TR	2.00	2.40
LATQX2MA10TR	2.00	2.60
LATQX3MA10TR	2.00	3.00

Functional Schematic





AC Power

Pin	Power (uW/MHz)			
	X0P5M	X1P0M	X2P0M	X3P0M
D	0.0012	0.0018	0.0024	0.0028
G	0.0020	0.0022	0.0025	0.0028
Q	0.0036	0.0047	0.0068	0.0092

Pin Capacitance

Pin	Capacitance (pF)			
	X0P5M	X1P0M	X2P0M	X3P0M
D	0.0010	0.0014	0.0018	0.0019
G	0.0014	0.0017	0.0016	0.0017

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X0P5M	X1P0M	X2P0M	X3P0M	X0P5M	X1P0M	X2P0M	X3P0M
D → Q ↑	0.0488	0.0375	0.0367	0.0383	4.7257	2.4486	1.1995	0.7963
D → Q ↓	0.0618	0.0519	0.0519	0.0574	2.8491	1.4841	0.7164	0.4849
G → Q ↑	0.0400	0.0312	0.0317	0.0334	4.7260	2.4484	1.1995	0.7964
G → Q ↓	0.0607	0.0520	0.0516	0.0539	2.8489	1.4841	0.7164	0.4848

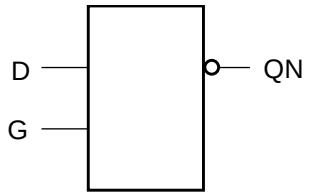
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X0P5M	X1P0M	X2P0M	X3P0M
D	setup ↑ → G	0.0508	0.0391	0.0391	0.0391
	setup ↓ → G	0.0508	0.0430	0.0391	0.0469
	hold ↑ → G	-0.0391	-0.0312	-0.0312	-0.0312
	hold ↓ → G	-0.0391	-0.0273	-0.0273	-0.0312
G	minpwh	0.8830	0.8830	0.8830	0.8830

Cell Description

The LATQN cell is a D-type active-high transparent latch. When the enable (G) is high, data is transferred to the outputs (QN).

Logic Symbol



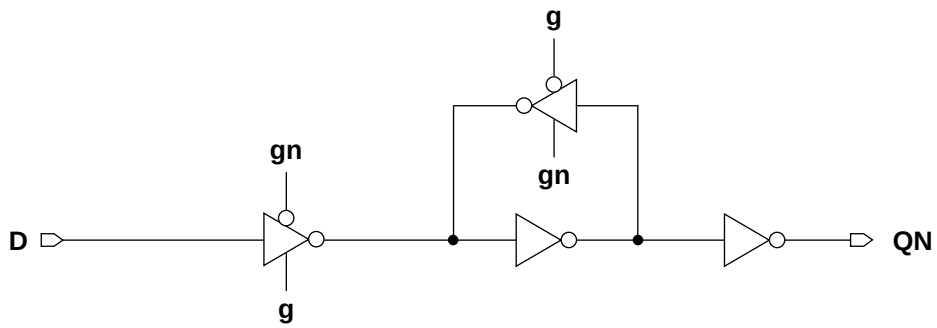
Function Table

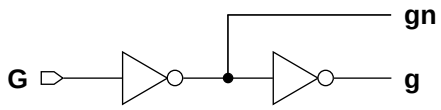
G	D	QN[n+1]
1	0	1
1	1	0
0	x	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
LATQNX0P5MA10TR	2.00	2.40
LATQNX1MA10TR	2.00	2.40
LATQNX2MA10TR	2.00	2.80
LATQNX3MA10TR	2.00	3.00
LATQNX4MA10TR	2.00	3.40

Functional Schematic





AC Power

Pin	Power (uW/MHz)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D	0.0012	0.0017	0.0022	0.0026	0.0029
G	0.0020	0.0022	0.0025	0.0026	0.0029
QN	0.0037	0.0049	0.0069	0.0090	0.0106

Pin Capacitance

Pin	Capacitance (pF)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D	0.0009	0.0013	0.0016	0.0017	0.0019
G	0.0014	0.0015	0.0015	0.0015	0.0016

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D → QN ↑	0.0692	0.0591	0.0552	0.0582	0.0599
D → QN ↓	0.0638	0.0532	0.0507	0.0546	0.0548
G → QN ↑	0.0689	0.0603	0.0563	0.0592	0.0591
G → QN ↓	0.0557	0.0472	0.0447	0.0486	0.0494

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D → QN ↑	4.6752	2.4076	1.1801	0.7856	0.5834
D → QN ↓	2.8543	1.4639	0.7147	0.4893	0.3625
G → QN ↑	4.6753	2.4077	1.1801	0.7856	0.5834
G → QN ↓	2.8542	1.4637	0.7147	0.4893	0.3625

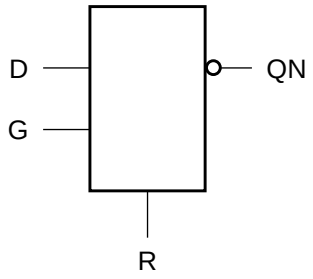
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)				
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D	setup ↑ → G	0.0430	0.0312	0.0312	0.0312	0.0273
	setup ↓ → G	0.0430	0.0352	0.0312	0.0312	0.0312
	hold ↑ → G	-0.0312	-0.0234	-0.0234	-0.0234	-0.0195
	hold ↓ → G	-0.0312	-0.0234	-0.0234	-0.0234	-0.0234
G	minpwh	0.8830	0.8830	0.8830	0.8830	0.8830

Cell Description

The LATRPQN cell is a D-type active-high transparent latch with asynchronous active-high reset (R). When the enable (G) is high, data is transferred to the output (QN).

Logic Symbol



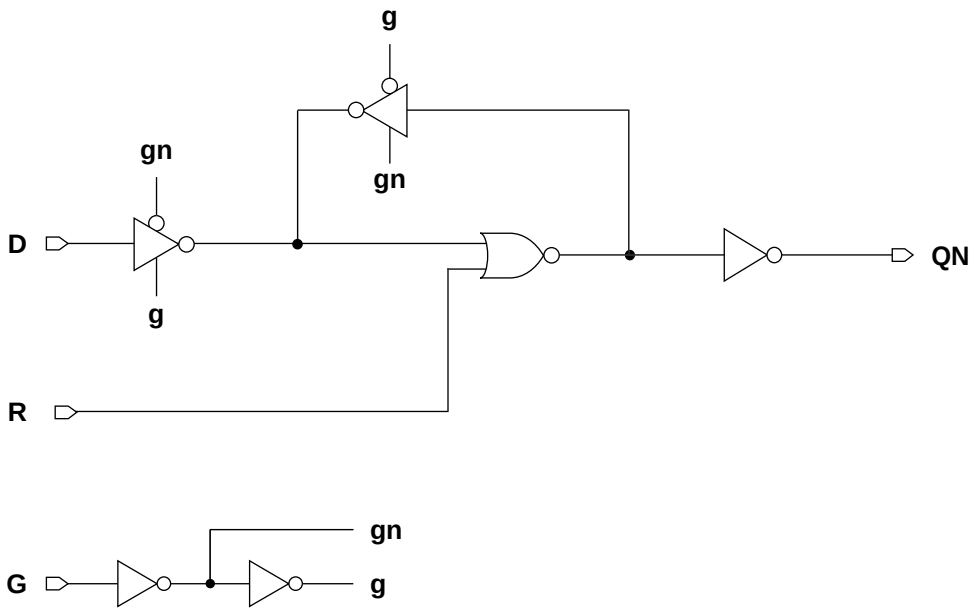
Function Table

R	G	D	QN[n+1]
1	x	x	1
0	1	0	1
0	1	1	0
0	0	x	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
LATRPQNX0P5MA10TR	2.00	2.60
LATRPQNX1MA10TR	2.00	2.60
LATRPQNX2MA10TR	2.00	3.00
LATRPQNX3MA10TR	2.00	3.20
LATRPQNX4MA10TR	2.00	3.60

Functional Schematic



AC Power

Pin	Power (uW/MHz)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
D	0.0013	0.0019	0.0024	0.0026	0.0030
G	0.0021	0.0023	0.0026	0.0027	0.0030
R	0.0009	0.0012	0.0014	0.0016	0.0018
QN	0.0041	0.0054	0.0071	0.0091	0.0113

Pin Capacitance

Pin	Capacitance (pF)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
D	0.0009	0.0014	0.0017	0.0017	0.0019
G	0.0014	0.0014	0.0015	0.0014	0.0016
R	0.0013	0.0016	0.0017	0.0016	0.0016

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
D → QN ↑	0.0735	0.0584	0.0590	0.0672	0.0719
D → QN ↓	0.0721	0.0610	0.0649	0.0764	0.0823
G → QN ↑	0.0731	0.0593	0.0600	0.0692	0.0713
G → QN ↓	0.0638	0.0551	0.0601	0.0706	0.0775
R → QN ↑	0.0292	0.0242	0.0283	0.0395	0.0438
R → QN ↓	0.0452	0.0427	0.0508	0.0614	0.0695

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
D → QN ↑	4.7041	2.4154	1.1799	0.7880	0.5841
D → QN ↓	2.7505	1.3462	0.6665	0.4645	0.3506
G → QN ↑	4.7039	2.4154	1.1799	0.7880	0.5841
G → QN ↓	2.7506	1.3463	0.6665	0.4645	0.3505
R → QN ↑	4.7178	2.4216	1.1824	0.7896	0.5852
R → QN ↓	2.7488	1.3459	0.6664	0.4644	0.3505

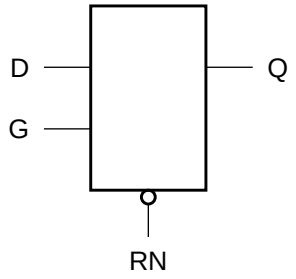
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)				
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D	setup ↑ → G	0.0430	0.0352	0.0312	0.0352	0.0391
	setup ↓ → G	0.0469	0.0352	0.0312	0.0352	0.0352
	hold ↑ → G	-0.0352	-0.0273	-0.0234	-0.0234	-0.0234
	hold ↓ → G	-0.0352	-0.0234	-0.0234	-0.0234	-0.0234
G	minpwh	0.8830	0.8830	0.8830	0.8830	0.8830
R	minpwh	0.8830	0.8830	0.8830	0.8830	0.8830
	recovery	0.0078	0.0078	0.0078	0.0117	0.0117
	removal	-0.0039	-0.0039	-0.0039	-0.0078	-0.0078

Cell Description

The LATRQ cell is a D-type active-high transparent latch with asynchronous active-low reset (RN). When the enable (G) is high, data is transferred to the output (Q).

Logic Symbol



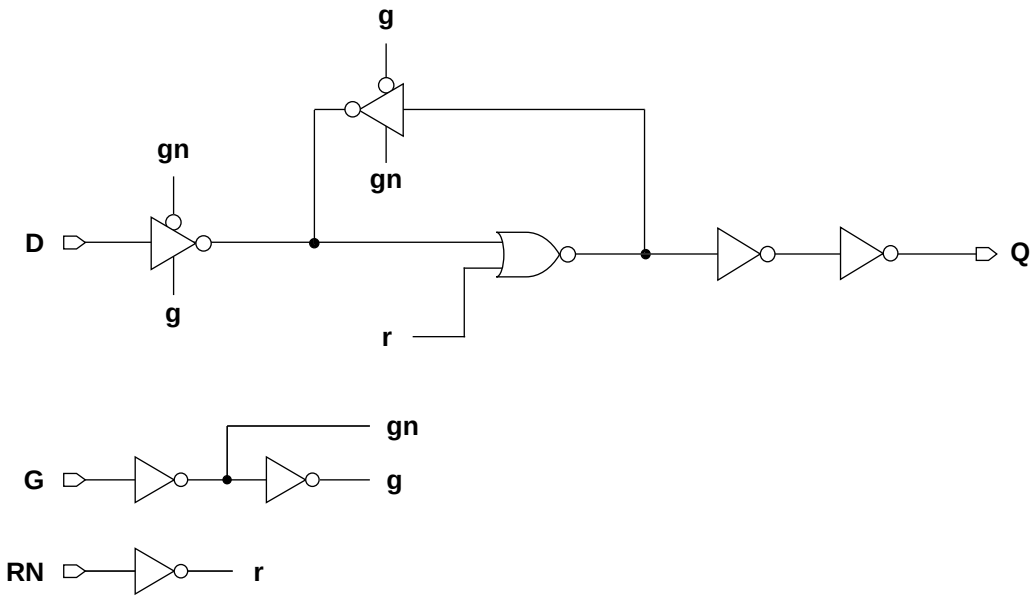
Function Table

RN	G	D	Q[n+1]
0	x	x	0
1	1	0	0
1	1	1	1
1	0	x	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
LATRQX0P5MA10TR	2.00	3.00
LATRQX1MA10TR	2.00	3.00
LATRQX2MA10TR	2.00	3.20
LATRQX3MA10TR	2.00	3.40

Functional Schematic



AC Power

Pin	Power (uW/MHz)			
	X0P5M	X1P0M	X2P0M	X3P0M
D	0.0015	0.0020	0.0025	0.0028
G	0.0021	0.0024	0.0026	0.0030
RN	0.0008	0.0010	0.0012	0.0015
Q	0.0039	0.0048	0.0069	0.0095

Pin Capacitance

Pin	Capacitance (pF)			
	X0P5M	X1P0M	X2P0M	X3P0M
D	0.0011	0.0015	0.0017	0.0018
G	0.0016	0.0017	0.0018	0.0019
RN	0.0018	0.0020	0.0021	0.0022

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X0P5M	X1P0M	X2P0M	X3P0M	X0P5M	X1P0M	X2P0M	X3P0M
D → Q ↑	0.0530	0.0430	0.0461	0.0524	4.8272	2.4822	1.2235	0.8113
D → Q ↓	0.0641	0.0544	0.0568	0.0627	3.0304	1.5246	0.7732	0.5292
G → Q ↑	0.0432	0.0343	0.0373	0.0422	4.8284	2.4824	1.2237	0.8115
G → Q ↓	0.0617	0.0529	0.0545	0.0575	3.0297	1.5243	0.7730	0.5290
RN → Q ↑	0.0556	0.0451	0.0480	0.0546	4.8277	2.4823	1.2234	0.8114
RN → Q ↓	0.0437	0.0544	0.0679	0.0821	2.8740	1.5153	0.7813	0.5427

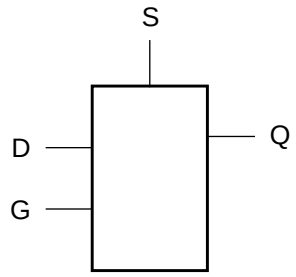
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X0P5M	X1P0M	X2P0M	X3P0M
D	setup ↑ → G	0.0547	0.0430	0.0469	0.0508
	setup ↓ → G	0.0547	0.0430	0.0430	0.0508
	hold ↑ → G	-0.0430	-0.0352	-0.0391	-0.0430
	hold ↓ → G	-0.0391	-0.0312	-0.0312	-0.0352
G	minpwh	0.8830	0.8830	0.8830	0.8830
RN	minpwl	0.8830	0.8830	0.8830	0.8830
	recovery	0.0508	0.0430	0.0430	0.0508
	removal	-0.0469	-0.0391	-0.0391	-0.0469

Cell Description

The LATSPQ cell is a D-type active-high transparent latch with asynchronous active-high set (S). When the enable (G) is high, data is transferred to the output (Q).

Logic Symbol



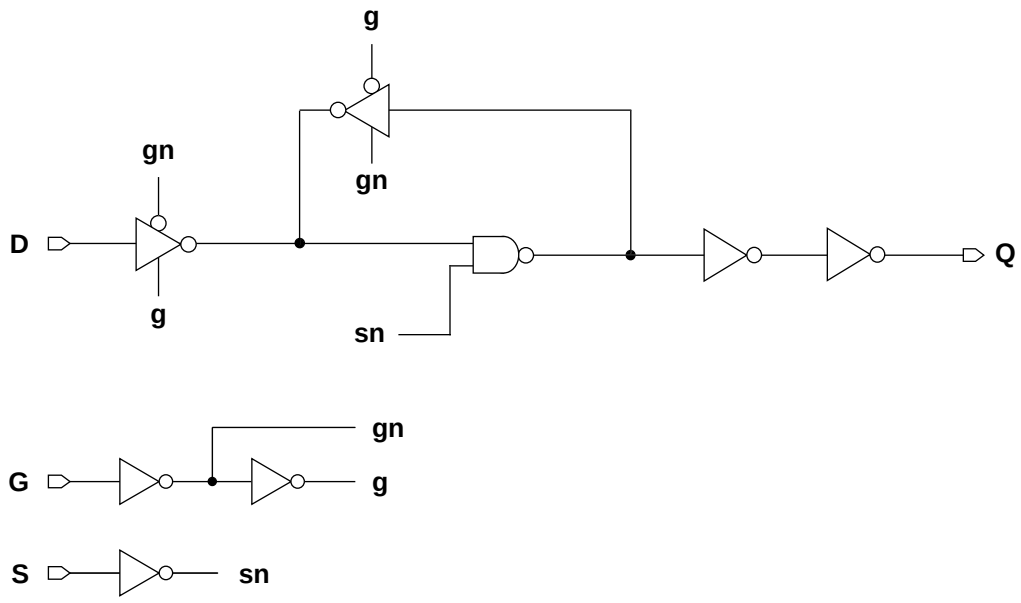
Function Table

S	G	D	Q[n+1]
1	x	x	1
0	1	0	0
0	1	1	1
0	0	x	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
LATSPQX0P5MA10TR	2.00	3.00
LATSPQX1MA10TR	2.00	3.00
LATSPQX2MA10TR	2.00	3.20
LATSPQX3MA10TR	2.00	4.20

Functional Schematic



AC Power

Pin	Power (uW/MHz)			
	X0P5M	X1P0M	X2P0M	X3P0M
D	0.0015	0.0021	0.0024	0.0043
G	0.0021	0.0024	0.0026	0.0031
S	0.0010	0.0014	0.0015	0.0025
Q	0.0042	0.0052	0.0080	0.0096

Pin Capacitance

Pin	Capacitance (pF)			
	X0P5M	X1P0M	X2P0M	X3P0M
D	0.0007	0.0009	0.0009	0.0017
G	0.0014	0.0014	0.0015	0.0018
S	0.0015	0.0017	0.0017	0.0027

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X0P5M	X1P0M	X2P0M	X3P0M	X0P5M	X1P0M	X2P0M	X3P0M
D → Q ↑	0.0516	0.0412	0.0456	0.0416	4.7200	2.3922	1.1937	0.7974
D → Q ↓	0.0762	0.0673	0.0779	0.0657	2.9785	1.4841	0.7587	0.4930
G → Q ↑	0.0420	0.0336	0.0376	0.0347	4.7203	2.3922	1.1937	0.7974
G → Q ↓	0.0686	0.0595	0.0672	0.0561	2.9780	1.4835	0.7584	0.4928
S → Q ↑	0.0364	0.0450	0.0547	0.0709	4.6923	2.4046	1.2026	0.8126
S → Q ↓	0.0791	0.0701	0.0806	0.0683	2.9783	1.4840	0.7587	0.4930

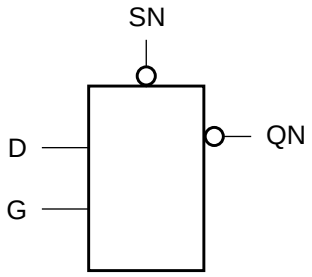
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X0P5M	X1P0M	X2P0M	X3P0M
D	setup ↑ → G	0.0508	0.0430	0.0469	0.0430
	setup ↓ → G	0.0664	0.0547	0.0664	0.0547
	hold ↑ → G	-0.0430	-0.0352	-0.0391	-0.0312
	hold ↓ → G	-0.0508	-0.0430	-0.0547	-0.0430
G	minpwh	0.8830	0.8830	0.8830	0.8830
S	minpwh	0.8830	0.8830	0.8830	0.8830
	recovery	0.0625	0.0508	0.0625	0.0508
	removal	-0.0586	-0.0469	-0.0586	-0.0469

Cell Description

The LATSQN cell is a D-type active-high transparent latch with asynchronous active-low set (SN). When the enable (G) is high, data is transferred to the output (QN).

Logic Symbol



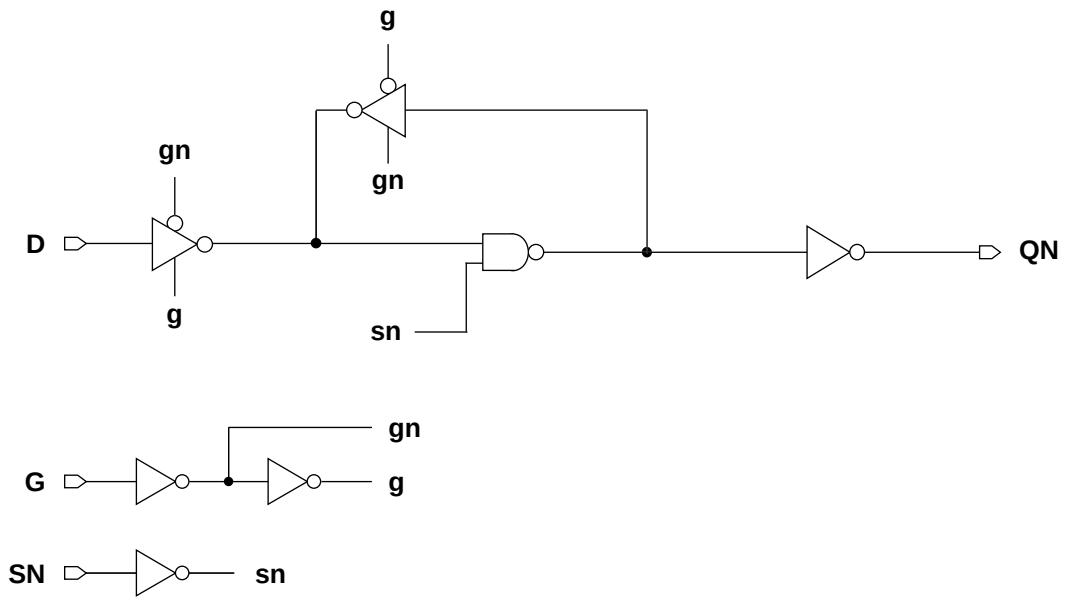
Function Table

SN	G	D	QN[n+1]
0	x	x	0
1	1	0	1
1	1	1	0
1	0	x	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
LATSQNX0P5MA10TR	2.00	2.80
LATSQNX1MA10TR	2.00	2.80
LATSQNX2MA10TR	2.00	3.00
LATSQNX3MA10TR	2.00	3.20
LATSQNX4MA10TR	2.00	3.40

Functional Schematic



AC Power

Pin	Power (uW/MHz)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D	0.0013	0.0018	0.0024	0.0026	0.0030
G	0.0020	0.0022	0.0025	0.0027	0.0030
SN	0.0006	0.0009	0.0013	0.0015	0.0017
QN	0.0040	0.0052	0.0071	0.0092	0.0111

Pin Capacitance

Pin	Capacitance (pF)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D	0.0009	0.0013	0.0016	0.0017	0.0019
G	0.0012	0.0013	0.0013	0.0013	0.0014
SN	0.0011	0.0013	0.0017	0.0017	0.0016

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D → QN ↑	0.0783	0.0667	0.0626	0.0700	0.0757
D → QN ↓	0.0660	0.0556	0.0544	0.0601	0.0643
G → QN ↑	0.0776	0.0676	0.0643	0.0714	0.0749
G → QN ↓	0.0579	0.0496	0.0481	0.0543	0.0586
SN → QN ↑	0.0355	0.0351	0.0351	0.0421	0.0475
SN → QN ↓	0.0372	0.0377	0.0386	0.0458	0.0522

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D → QN ↑	4.5746	2.3575	1.1676	0.7841	0.5860
D → QN ↓	2.8081	1.4497	0.7161	0.4928	0.3701
G → QN ↑	4.5745	2.3576	1.1675	0.7841	0.5860
G → QN ↓	2.8078	1.4497	0.7162	0.4928	0.3701
SN → QN ↑	4.5701	2.3567	1.1674	0.7840	0.5860
SN → QN ↓	2.8233	1.4600	0.7209	0.4946	0.3716

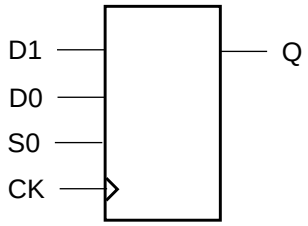
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)				
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D	setup ↑ → G	0.0430	0.0312	0.0312	0.0312	0.0312
	setup ↓ → G	0.0469	0.0352	0.0312	0.0352	0.0352
	hold ↑ → G	-0.0352	-0.0234	-0.0234	-0.0234	-0.0234
	hold ↓ → G	-0.0352	-0.0234	-0.0195	-0.0234	-0.0234
G	minpwh	0.8830	0.8830	0.8830	0.8830	0.8830
SN	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830
	recovery	-0.0117	-0.0156	-0.0195	-0.0156	-0.0156
	removal	0.0156	0.0195	0.0234	0.0195	0.0195

Cell Description

The M2DFFQ cell is a positive-edge triggered, static D-type flip-flop with a 2-to-1 data select control (S0) for the data inputs (D1, D0). The cell has a single output (Q).

Logic Symbol



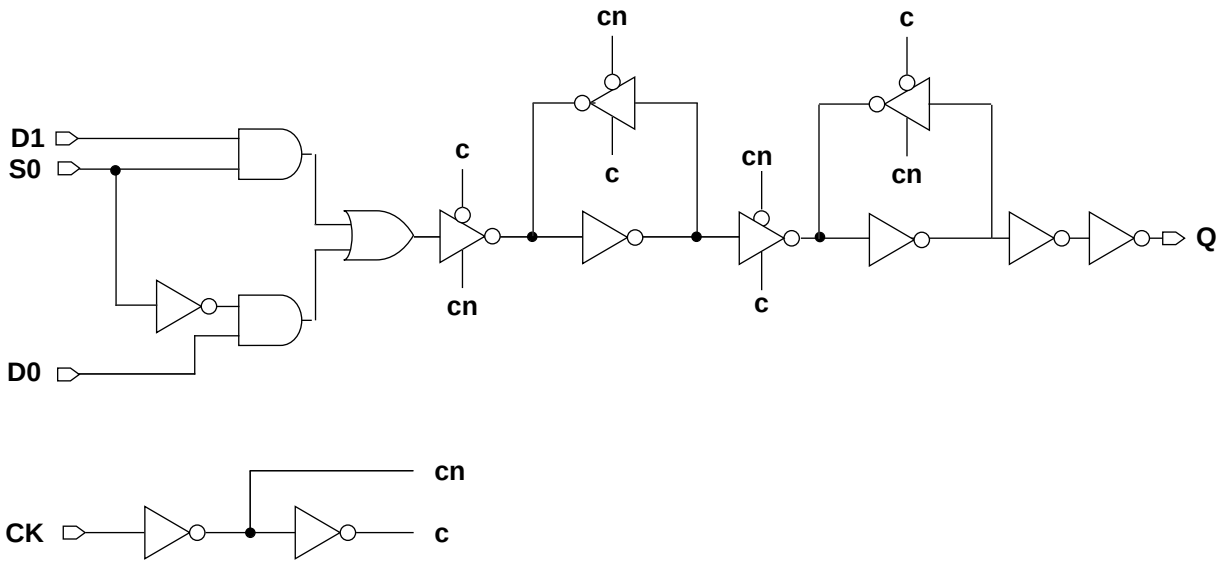
Function Table

S0	D1	D0	CK	Q[n+1]
0	x	0	⎍	0
0	x	1	⎍	1
1	0	x	⎍	0
1	1	x	⎍	1
x	x	x	⎎	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
M2DFFQX0P5MA10TR	2.00	5.80
M2DFFQX1MA10TR	2.00	5.80
M2DFFQX2MA10TR	2.00	6.20
M2DFFQX3MA10TR	2.00	6.40
M2DFFQX4MA10TR	2.00	7.20

Functional Schematic



AC Power

Pin	Power (uW/MHz)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D0	0.0051	0.0065	0.0081	0.0088	0.0094
D1	0.0055	0.0068	0.0086	0.0093	0.0099
S0	0.0056	0.0072	0.0086	0.0093	0.0088
CK	0.0038	0.0043	0.0051	0.0060	0.0059
Q	0.0033	0.0039	0.0056	0.0082	0.0103

Pin Capacitance

Pin	Capacitance (pF)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D0	0.0012	0.0012	0.0015	0.0015	0.0019
D1	0.0012	0.0011	0.0014	0.0014	0.0018
S0	0.0018	0.0021	0.0022	0.0022	0.0026
CK	0.0009	0.0010	0.0010	0.0012	0.0011

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
CK → Q ↑	0.0895	0.0733	0.0708	0.0664	0.0727
CK → Q ↓	0.0866	0.0740	0.0732	0.0750	0.0766

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
CK → Q ↑	4.3141	2.3951	1.1691	0.7864	0.5836
CK → Q ↓	2.9337	1.5901	0.7652	0.5023	0.3611

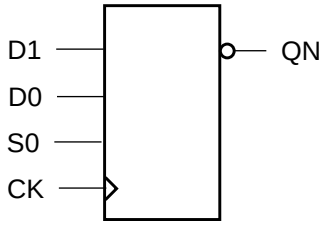
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)				
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
D0	setup ↑ → CK	0.0508	0.0430	0.0430	0.0469	0.0352
	setup ↓ → CK	0.0625	0.0547	0.0469	0.0508	0.0430
	hold ↑ → CK	-0.0195	-0.0195	-0.0195	-0.0195	-0.0195
	hold ↓ → CK	-0.0391	-0.0391	-0.0312	-0.0312	-0.0117
D1	setup ↑ → CK	0.0508	0.0430	0.0391	0.0430	0.0352
	setup ↓ → CK	0.0664	0.0547	0.0508	0.0508	0.0430
	hold ↑ → CK	-0.0195	-0.0195	-0.0156	-0.0195	-0.0195
	hold ↓ → CK	-0.0430	-0.0391	-0.0352	-0.0352	-0.0117
S0	setup ↑ → CK	0.0664	0.0547	0.0508	0.0547	0.0430
	setup ↓ → CK	0.0625	0.0508	0.0508	0.0508	0.0469
	hold ↑ → CK	-0.0117	-0.0117	-0.0117	-0.0117	-0.0117
	hold ↓ → CK	-0.0312	-0.0273	-0.0273	-0.0273	-0.0117
CK	minpwh	0.8830	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830

Cell Description

The M2DFFQN cell is a positive-edge triggered, static D-type flip-flop with a 2-to-1 data select control (S0) for the data inputs (D1, D0). The cell has a single output (QN).

Logic Symbol



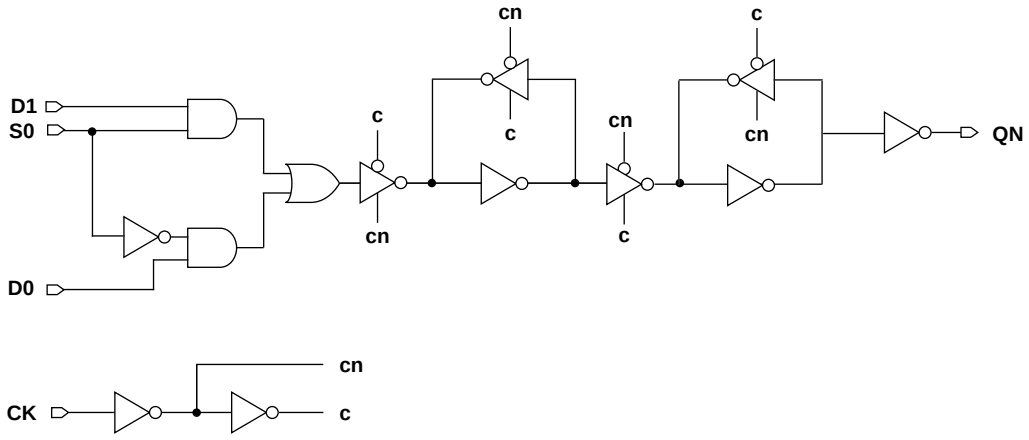
Function Table

S0	D1	D0	CK	QN[n+1]
0	x	0	⎍	1
0	x	1	⎍	0
1	0	x	⎍	1
1	1	x	⎍	0
x	x	x	⎎	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
M2DFFQNX0P5MA10TR	2.00	5.60
M2DFFQNX1MA10TR	2.00	5.80
M2DFFQNX2MA10TR	2.00	6.20
M2DFFQNX3MA10TR	2.00	6.60

Functional Schematic



AC Power

Pin	Power (uW/MHz)			
	X0P5M	X1P0M	X2P0M	X3P0M
D0	0.0051	0.0064	0.0078	0.0091
D1	0.0057	0.0068	0.0083	0.0096
S0	0.0057	0.0067	0.0080	0.0087
CK	0.0038	0.0043	0.0050	0.0059
QN	0.0035	0.0040	0.0058	0.0084

Pin Capacitance

Pin	Capacitance (pF)			
	X0P5M	X1P0M	X2P0M	X3P0M
D0	0.0012	0.0014	0.0016	0.0018
D1	0.0012	0.0013	0.0014	0.0017
S0	0.0020	0.0022	0.0023	0.0028
CK	0.0009	0.0010	0.0010	0.0012

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X0P5M	X1P0M	X2P0M	X3P0M	X0P5M	X1P0M	X2P0M	X3P0M
CK → QN ↑	0.0888	0.0733	0.0708	0.0667	4.2721	2.3951	1.1692	0.7872
CK → QN ↓	0.0870	0.0739	0.0731	0.0745	2.9512	1.5901	0.7653	0.5032

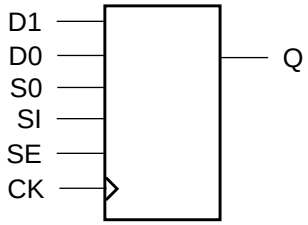
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X0P5M	X1P0M	X2P0M	X3P0M
D0	setup ↑ → CK	0.0469	0.0430	0.0391	0.0391
	setup ↓ → CK	0.0469	0.0391	0.0469	0.0430
	hold ↑ → CK	-0.0234	-0.0234	-0.0195	-0.0195
	hold ↓ → CK	-0.0117	-0.0078	-0.0117	-0.0078
D1	setup ↑ → CK	0.0469	0.0430	0.0391	0.0391
	setup ↓ → CK	0.0508	0.0430	0.0469	0.0469
	hold ↑ → CK	-0.0234	-0.0234	-0.0195	-0.0156
	hold ↓ → CK	-0.0117	-0.0078	-0.0117	-0.0117
S0	setup ↑ → CK	0.0469	0.0391	0.0469	0.0430
	setup ↓ → CK	0.0547	0.0508	0.0508	0.0469
	hold ↑ → CK	-0.0078	-0.0078	-0.0078	-0.0078
	hold ↓ → CK	-0.0039	-0.0078	-0.0078	-0.0078
CK	minpwh	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830

Cell Description

The M2SDFFQ cell is a positive-edge triggered, static D-type flip-flop with a 2-to-1 data select control (S0) for the data inputs (D1, D0), scan input (SI), and active-high scan enable (SE). The cell has a single output (Q).

Logic Symbol



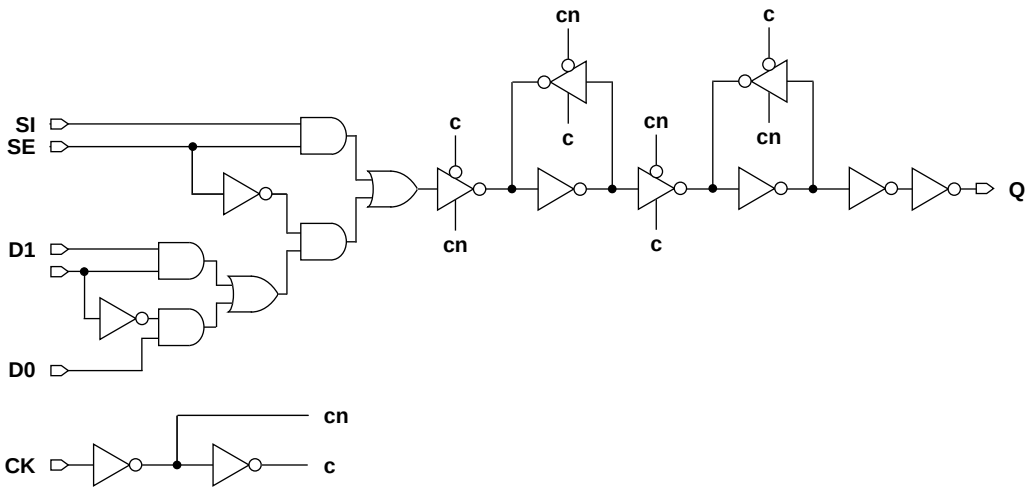
Function Table

SE	SI	S0	D1	D0	CK	Q[n+1]
0	x	0	x	0	⎍	0
0	x	0	x	1	⎍	1
0	x	1	0	x	⎍	0
0	x	1	1	x	⎍	1
1	0	x	x	x	⎍	0
1	1	x	x	x	⎍	1
x	x	x	x	x	⎎	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
M2SDFFQX0P5MA10TR	2.00	7.60
M2SDFFQX1MA10TR	2.00	7.60
M2SDFFQX2MA10TR	2.00	8.00
M2SDFFQX3MA10TR	2.00	8.00
M2SDFFQX4MA10TR	2.00	8.60

Functional Schematic



AC Power

Pin	Power (uW/MHz)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
SI	0.0049	0.0062	0.0073	0.0080	0.0082
SE	0.0056	0.0068	0.0080	0.0086	0.0088
D0	0.0064	0.0079	0.0096	0.0102	0.0104
D1	0.0068	0.0084	0.0101	0.0107	0.0109
S0	0.0069	0.0087	0.0102	0.0108	0.0110
CK	0.0038	0.0044	0.0051	0.0060	0.0060
Q	0.0033	0.0038	0.0056	0.0081	0.0116

Pin Capacitance

Pin	Capacitance (pF)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
SI	0.0007	0.0007	0.0007	0.0007	0.0007
SE	0.0017	0.0017	0.0018	0.0018	0.0018
D0	0.0012	0.0012	0.0015	0.0015	0.0015
D1	0.0011	0.0012	0.0014	0.0014	0.0014
S0	0.0018	0.0022	0.0023	0.0023	0.0023
CK	0.0009	0.0009	0.0010	0.0012	0.0011

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
CK → Q ↑	0.0885	0.0734	0.0708	0.0699	0.0702
CK → Q ↓	0.0846	0.0705	0.0722	0.0781	0.0850

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
CK → Q ↑	4.3073	2.3532	1.1646	0.7887	0.5870
CK → Q ↓	2.9232	1.5243	0.7584	0.5313	0.3932

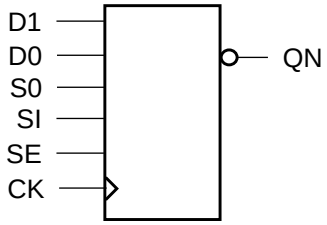
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)				
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
SI	setup ↑ → CK	0.0625	0.0586	0.0586	0.0664	0.0664
	setup ↓ → CK	0.0859	0.0820	0.0859	0.0859	0.0859
	hold ↑ → CK	-0.0312	-0.0312	-0.0352	-0.0391	-0.0391
	hold ↓ → CK	-0.0625	-0.0625	-0.0664	-0.0664	-0.0664
SE	setup ↑ → CK	0.0977	0.0938	0.0977	0.1016	0.1016
	setup ↓ → CK	0.0703	0.0625	0.0547	0.0625	0.0625
	hold ↑ → CK	-0.0234	-0.0273	-0.0273	-0.0352	-0.0352
	hold ↓ → CK	-0.0352	-0.0352	-0.0312	-0.0352	-0.0352
D0	setup ↑ → CK	0.0820	0.0742	0.0664	0.0703	0.0742
	setup ↓ → CK	0.0938	0.0820	0.0742	0.0742	0.0742
	hold ↑ → CK	-0.0469	-0.0469	-0.0430	-0.0469	-0.0469
	hold ↓ → CK	-0.0703	-0.0625	-0.0547	-0.0586	-0.0547
D1	setup ↑ → CK	0.0781	0.0703	0.0625	0.0703	0.0703
	setup ↓ → CK	0.0977	0.0820	0.0742	0.0742	0.0742
	hold ↑ → CK	-0.0469	-0.0430	-0.0391	-0.0430	-0.0430
	hold ↓ → CK	-0.0703	-0.0625	-0.0586	-0.0586	-0.0586
S0	setup ↑ → CK	0.0977	0.0820	0.0742	0.0781	0.0781
	setup ↓ → CK	0.0938	0.0781	0.0742	0.0781	0.0781
	hold ↑ → CK	-0.0391	-0.0391	-0.0312	-0.0391	-0.0391
	hold ↓ → CK	-0.0547	-0.0508	-0.0469	-0.0508	-0.0547
CK	minpwh	0.8830	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830

Cell Description

The M2SDFFQN cell is a positive-edge triggered, static D-type flip-flop with a 2-to-1 data select control (S0) for the data inputs (D1,D0), scan input (SI), and active-high scan enable (SE). The cell has a single output (QN).

Logic Symbol



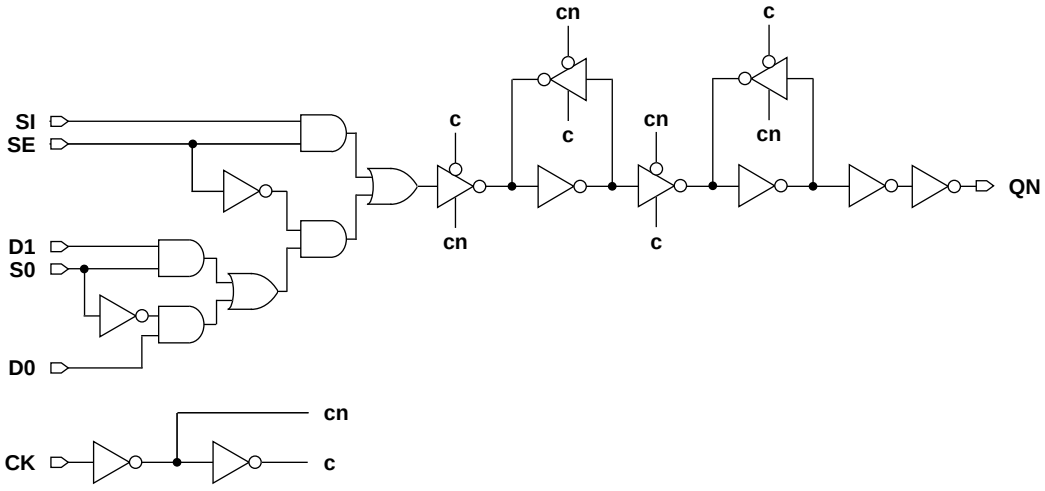
Function Table

SE	SI	S0	D1	D0	CK	QN[n+1]
0	x	0	x	0	↑	1
0	x	0	x	1	↑	0
0	x	1	0	x	↑	1
0	x	1	1	x	↑	0
1	0	x	x	x	↑	1
1	1	x	x	x	↑	0
x	x	x	x	x	↓	QN[n]

Cell Size

Drive Strength	Height (um)	Width (um)
M2SDFFQNX0P5MA10TR	2.00	7.60
M2SDFFQNX1MA10TR	2.00	7.60
M2SDFFQNX2MA10TR	2.00	8.00
M2SDFFQNX3MA10TR	2.00	8.20

Functional Schematic



AC Power

Pin	Power (uW/MHz)			
	X0P5M	X1P0M	X2P0M	X3P0M
SI	0.0050	0.0063	0.0076	0.0082
SE	0.0056	0.0069	0.0083	0.0088
D0	0.0064	0.0079	0.0099	0.0104
D1	0.0068	0.0083	0.0104	0.0109
S0	0.0070	0.0087	0.0105	0.0110
CK	0.0039	0.0045	0.0051	0.0057
QN	0.0033	0.0041	0.0062	0.0079

Pin Capacitance

Pin	Capacitance (pF)			
	X0P5M	X1P0M	X2P0M	X3P0M
SI	0.0007	0.0007	0.0007	0.0007
SE	0.0017	0.0017	0.0018	0.0018
D0	0.0012	0.0012	0.0015	0.0016
D1	0.0011	0.0011	0.0014	0.0014
S0	0.0018	0.0021	0.0023	0.0023
CK	0.0009	0.0009	0.0010	0.0011

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X0P5M	X1P0M	X2P0M	X3P0M	X0P5M	X1P0M	X2P0M	X3P0M
CK → QN ↑	0.0902	0.0788	0.0731	0.0732	4.2468	2.3426	1.1555	0.7823
CK → QN ↓	0.1001	0.0876	0.0814	0.0813	2.4649	1.3648	0.6584	0.4563

Timing Constraints at 25°C,1.0V, Typical Process

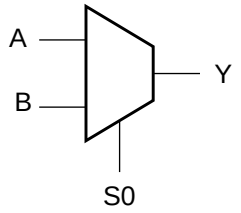
Pin	Requirement	Interval (ns)			
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**
SI	setup ↑ → CK	0.0586	0.0547	0.0586	0.0586
	setup ↓ → CK	0.0859	0.0781	0.0859	0.0859
	hold ↑ → CK	-0.0312	-0.0312	-0.0391	-0.0391
	hold ↓ → CK	-0.0625	-0.0625	-0.0703	-0.0703
SE	setup ↑ → CK	0.0977	0.0898	0.0977	0.0977
	setup ↓ → CK	0.0703	0.0625	0.0547	0.0547
	hold ↑ → CK	-0.0273	-0.0273	-0.0312	-0.0352
	hold ↓ → CK	-0.0391	-0.0391	-0.0352	-0.0352
D0	setup ↑ → CK	0.0781	0.0742	0.0664	0.0664
	setup ↓ → CK	0.0938	0.0820	0.0742	0.0742
	hold ↑ → CK	-0.0508	-0.0508	-0.0469	-0.0469
	hold ↓ → CK	-0.0703	-0.0664	-0.0586	-0.0586
D1	setup ↑ → CK	0.0781	0.0703	0.0625	0.0625
	setup ↓ → CK	0.0938	0.0820	0.0742	0.0742
	hold ↑ → CK	-0.0469	-0.0469	-0.0430	-0.0430
	hold ↓ → CK	-0.0703	-0.0664	-0.0586	-0.0586
S0	setup ↑ → CK	0.0938	0.0820	0.0742	0.0742
	setup ↓ → CK	0.0898	0.0781	0.0742	0.0703
	hold ↑ → CK	-0.0430	-0.0430	-0.0352	-0.0391
	hold ↓ → CK	-0.0586	-0.0547	-0.0508	-0.0508
CK	minpwh	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830

Cell Description

The MX2 cell is a 2-to-1 multiplexer. The state of the select input (S0) determines which data input (A, B) is presented to the output (Y). The output (Y) is represented by the logic equation:

$Y = (\overline{S0} \bullet A) + (S0 \bullet B)$

Logic Symbol



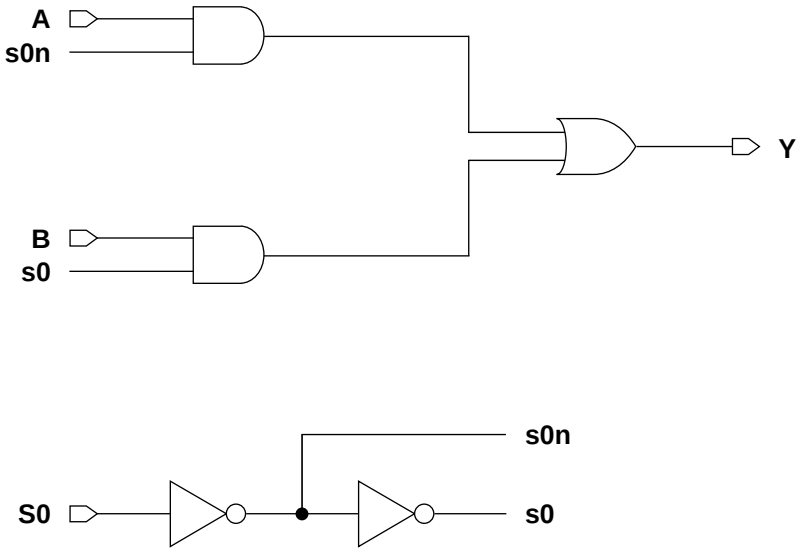
Function Table

S0	A	B	Y
0	0	x	0
0	1	x	1
1	x	0	0
1	x	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
MX2X0P5BA10TR	2.00	2.60
MX2X0P5MA10TR	2.00	2.40
MX2X0P7BA10TR	2.00	2.60
MX2X0P7MA10TR	2.00	2.40
MX2X1BA10TR	2.00	2.60
MX2X1MA10TR	2.00	2.40
MX2X1P4BA10TR	2.00	3.20
MX2X1P4MA10TR	2.00	3.80
MX2X2BA10TR	2.00	3.20
MX2X2MA10TR	2.00	4.00
MX2X3BA10TR	2.00	4.60
MX2X3MA10TR	2.00	5.60
MX2X4BA10TR	2.00	5.00
MX2X4MA10TR	2.00	5.60
MX2X6BA10TR	2.00	7.80
MX2X6MA10TR	2.00	8.40
MX2X8BA10TR	2.00	9.80

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P5B	**X0P5M**	**X0P7B**	**X0P7M**	**X1P0B**	**X1P0M**	**X1P4B**	**X1P4M**
S0	0.0024	0.0025	0.0026	0.0028	0.0030	0.0032	0.0035	0.0048
B	0.0007	0.0008	0.0008	0.0009	0.0010	0.0012	0.0013	0.0017
A	0.0006	0.0002	0.0007	0.0003	0.0008	0.0004	0.0012	0.0005

AC Power (Cont'd.)

Pin	Power (uW/MHz)								
	X2P0B	**X2P0M**	**X3P0B**	**X3P0M**	**X4P0B**	**X4P0M**	**X6P0B**	**X6P0M**	**X8P0B**
S0	0.0042	0.0060	0.0066	0.0081	0.0081	0.0097	0.0121	0.0153	0.0161
B	0.0016	0.0023	0.0025	0.0033	0.0033	0.0042	0.0050	0.0066	0.0067
A	0.0014	0.0007	0.0022	0.0011	0.0028	0.0015	0.0042	0.0023	0.0056

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5B	**X0P5M**	**X0P7B**	**X0P7M**	**X1P0B**	**X1P0M**	**X1P4B**	**X1P4M**
S0	0.0026	0.0023	0.0027	0.0025	0.0029	0.0028	0.0029	0.0044
B	0.0009	0.0012	0.0009	0.0013	0.0011	0.0016	0.0014	0.0024
A	0.0010	0.0013	0.0010	0.0014	0.0012	0.0016	0.0015	0.0024

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)								
	X2P0B	**X2P0M**	**X3P0B**	**X3P0M**	**X4P0B**	**X4P0M**	**X6P0B**	**X6P0M**	**X8P0B**
S0	0.0033	0.0058	0.0055	0.0076	0.0066	0.0088	0.0096	0.0137	0.0129
B	0.0017	0.0030	0.0025	0.0042	0.0031	0.0051	0.0049	0.0080	0.0064
A	0.0018	0.0031	0.0027	0.0043	0.0032	0.0053	0.0050	0.0083	0.0065

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5B	**X0P5M**	**X0P7B**	**X0P7M**	**X1P0B**	**X1P0M**	**X1P4B**	**X1P4M**
S0 → Y ↑	0.0559	0.0532	0.0533	0.0511	0.0514	0.0478	0.0535	0.0490
S0 → Y ↓	0.0474	0.0565	0.0452	0.0550	0.0437	0.0525	0.0464	0.0527
B → Y ↑	0.0422	0.0457	0.0400	0.0436	0.0377	0.0404	0.0384	0.0418
B → Y ↓	0.0371	0.0557	0.0355	0.0540	0.0344	0.0508	0.0340	0.0519
A → Y ↑	0.0414	0.0371	0.0387	0.0353	0.0364	0.0325	0.0394	0.0342
A → Y ↓	0.0368	0.0450	0.0346	0.0437	0.0327	0.0409	0.0361	0.0429

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)								
	X2P0B	**X2P0M**	**X3P0B**	**X3P0M**	**X4P0B**	**X4P0M**	**X6P0B**	**X6P0M**	**X8P0B**
S0 → Y ↑	0.0511	0.0458	0.0487	0.0480	0.0466	0.0455	0.0476	0.0462	0.0461
S0 → Y ↓	0.0438	0.0497	0.0422	0.0537	0.0404	0.0514	0.0419	0.0513	0.0405
B → Y ↑	0.0365	0.0396	0.0337	0.0404	0.0338	0.0373	0.0342	0.0372	0.0338
B → Y ↓	0.0327	0.0495	0.0307	0.0528	0.0315	0.0505	0.0317	0.0495	0.0316
A → Y ↑	0.0369	0.0323	0.0360	0.0345	0.0342	0.0316	0.0351	0.0316	0.0341
A → Y ↓	0.0335	0.0407	0.0331	0.0454	0.0319	0.0430	0.0324	0.0422	0.0318

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X0P5B	**X0P5M**	**X0P7B**	**X0P7M**	**X1P0B**	**X1P0M**	**X1P4B**	**X1P4M**
S0 → Y ↑	4.3852	4.5878	3.2055	3.3499	2.3036	2.3983	1.6411	1.6479
S0 → Y ↓	5.0343	2.8996	3.6418	2.0929	2.5346	1.4695	1.8029	1.0377
B → Y ↑	4.3863	4.6218	3.2351	3.3732	2.3088	2.4132	1.6139	1.6593
B → Y ↓	5.0272	2.8995	3.6390	2.0928	2.5338	1.4694	1.8009	1.0377
A → Y ↑	4.3809	4.5955	3.2033	3.3557	2.3024	2.4021	1.6411	1.6512
A → Y ↓	5.0255	2.8988	3.6372	2.0922	2.5322	1.4693	1.8020	1.0377

Delays at 25°C,1.0V, Typical Process (Cont'd.)

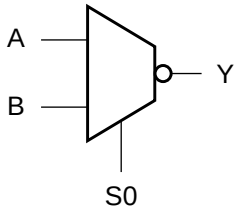
Description	K_{load} (ns/pF)								
	X2P0B	**X2P0M**	**X3P0B**	**X3P0M**	**X4P0B**	**X4P0M**	**X6P0B**	**X6P0M**	**X8P0B**
S0 → Y ↑	1.1642	1.1747	0.7731	0.7846	0.5762	0.5821	0.3829	0.3876	0.2878
S0 → Y ↓	1.2670	0.7238	0.8434	0.4945	0.6267	0.3655	0.4195	0.2448	0.3146
B → Y ↑	1.1569	1.1823	0.7686	0.7896	0.5740	0.5856	0.3816	0.3900	0.2870
B → Y ↓	1.2663	0.7239	0.8429	0.4945	0.6266	0.3655	0.4194	0.2448	0.3145
A → Y ↑	1.1642	1.1771	0.7730	0.7869	0.5762	0.5836	0.3829	0.3887	0.2879
A → Y ↓	1.2665	0.7237	0.8428	0.4949	0.6265	0.3657	0.4193	0.2449	0.3144

Cell Description

The MXIT2 cell is a 2-to-1 multiplexer with inverted output. The state of the select input (S0) determines which data input (A, B) is presented to the output (Y). The output (Y) is represented by the logic equation:

$Y = \overline{(\overline{S0} \bullet A) + (S0 \bullet B)}$

Logic Symbol



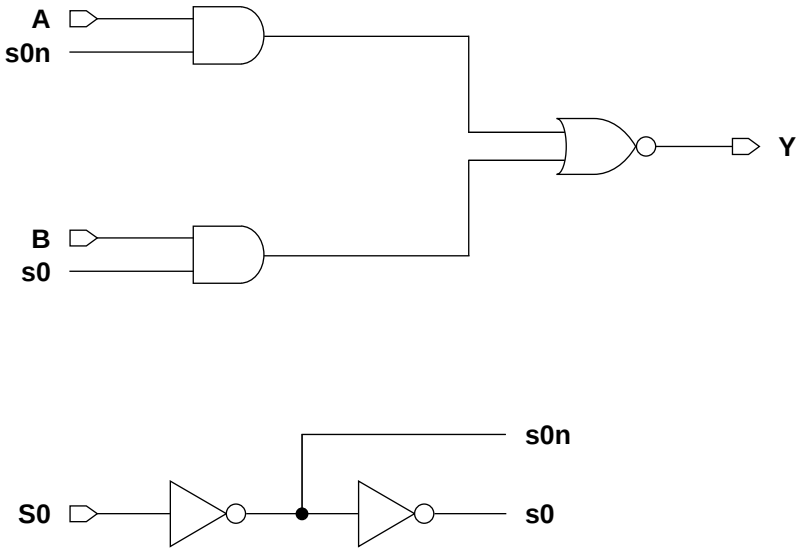
Function Table

S0	A	B	Y
0	0	x	1
0	1	x	0
1	x	0	1
1	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
MXIT2X0P5MA10TR	2.00	2.00
MXIT2X0P7MA10TR	2.00	2.00
MXIT2X1MA10TR	2.00	2.00
MXIT2X1P4MA10TR	2.00	3.40
MXIT2X2MA10TR	2.00	3.60
MXIT2X3MA10TR	2.00	4.00
MXIT2X4MA10TR	2.00	6.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)						
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M
S0	0.0022	0.0024	0.0029	0.0041	0.0055	0.0073	0.0101
B	0.0015	0.0018	0.0023	0.0035	0.0045	0.0067	0.0095
A	0.0015	0.0020	0.0025	0.0037	0.0047	0.0069	0.0097

Pin Capacitance

Pin	Capacitance (pF)						
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M
S0	0.0028	0.0032	0.0036	0.0044	0.0061	0.0080	0.0110
B	0.0012	0.0014	0.0018	0.0027	0.0035	0.0052	0.0070
A	0.0011	0.0014	0.0018	0.0026	0.0033	0.0049	0.0064

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)						
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M
S0 → Y ↑	0.0180	0.0171	0.0163	0.0185	0.0165	0.0147	0.0153
S0 → Y ↓	0.0178	0.0171	0.0169	0.0203	0.0177	0.0164	0.0173
B → Y ↑	0.0203	0.0186	0.0171	0.0192	0.0177	0.0161	0.0168
B → Y ↓	0.0149	0.0136	0.0124	0.0144	0.0132	0.0121	0.0127
A → Y ↑	0.0193	0.0183	0.0165	0.0170	0.0160	0.0142	0.0150
A → Y ↓	0.0154	0.0148	0.0136	0.0150	0.0140	0.0128	0.0136

Delays at 25°C,1.0V, Typical Process (Cont'd.)

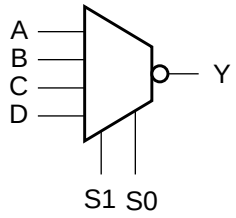
Description	K_{load} (ns/pF)						
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M
S0 → Y ↑	6.7057	4.9530	3.5696	2.4856	1.8189	1.1901	0.8987
S0 → Y ↓	4.5335	3.3086	2.3439	1.7486	1.2926	0.8371	0.6361
B → Y ↑	6.5864	4.8783	3.5313	2.5084	1.8086	1.1933	0.9013
B → Y ↓	4.5373	3.3270	2.3674	1.7938	1.2658	0.8251	0.6228
A → Y ↑	6.6910	4.9445	3.5644	2.4850	1.8183	1.1897	0.8986
A → Y ↓	4.6001	3.3528	2.3745	1.7696	1.3052	0.8455	0.6429

Cell Description

The MXIT4 cell is a 4-to-1 multiplexer with inverted output. The state of the select inputs (S1, S0) determines which data input (A, B, C, D) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = \overline{(\overline{S0} \bullet \overline{S1} \bullet A) + (S0 \bullet \overline{S1} \bullet B) + (\overline{S0} \bullet S1 \bullet C) + (S0 \bullet S1 \bullet D)}$$

Logic Symbol



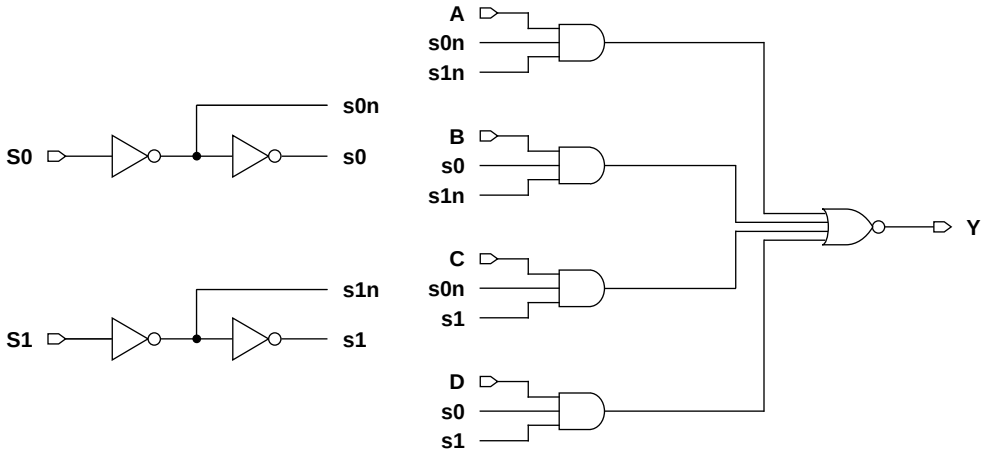
Function Table

S1	S0	A	B	C	D	Y
0	0	0	x	x	x	1
0	0	1	x	x	x	0
0	1	x	0	x	x	1
0	1	x	1	x	x	0
1	0	x	x	0	x	1
1	0	x	x	1	x	0
1	1	x	x	x	0	1
1	1	x	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
MXIT4X0P5MA10TR	2.00	5.60
MXIT4X0P7MA10TR	2.00	5.60
MXIT4X1MA10TR	2.00	6.00
MXIT4X1P4MA10TR	2.00	6.20
MXIT4X2MA10TR	2.00	6.20
MXIT4X3MA10TR	2.00	6.60

Functional Schematic



AC Power

Pin	Power (uW/MHz)					
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**
S1	0.0022	0.0024	0.0027	0.0032	0.0036	0.0044
S0	0.0036	0.0040	0.0044	0.0050	0.0054	0.0062
D	0.0015	0.0017	0.0020	0.0025	0.0028	0.0033
C	0.0015	0.0018	0.0021	0.0026	0.0030	0.0035
B	0.0014	0.0017	0.0020	0.0025	0.0028	0.0032
A	0.0016	0.0019	0.0022	0.0027	0.0031	0.0036

Pin Capacitance

Pin	Capacitance (pF)					
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**
S1	0.0015	0.0015	0.0017	0.0019	0.0021	0.0024
S0	0.0036	0.0039	0.0043	0.0051	0.0054	0.0061
D	0.0009	0.0010	0.0012	0.0014	0.0015	0.0017
C	0.0010	0.0011	0.0012	0.0014	0.0016	0.0018
B	0.0009	0.0011	0.0012	0.0014	0.0016	0.0017
A	0.0009	0.0011	0.0012	0.0014	0.0016	0.0018

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)					
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**
S1 → Y ↑	0.0473	0.0461	0.0443	0.0444	0.0449	0.0462
S1 → Y ↓	0.0518	0.0516	0.0508	0.0526	0.0548	0.0589
S0 → Y ↑	0.0948	0.0874	0.0830	0.0786	0.0792	0.0792
S0 → Y ↓	0.0989	0.0940	0.0899	0.0866	0.0888	0.0901
D → Y ↑	0.0835	0.0788	0.0735	0.0714	0.0715	0.0734
D → Y ↓	0.0876	0.0838	0.0796	0.0795	0.0808	0.0843
C → Y ↑	0.0816	0.0771	0.0720	0.0702	0.0708	0.0729
C → Y ↓	0.0857	0.0828	0.0789	0.0788	0.0805	0.0839
B → Y ↑	0.0905	0.0836	0.0790	0.0765	0.0771	0.0783
B → Y ↓	0.0930	0.0874	0.0832	0.0817	0.0837	0.0868
A → Y ↑	0.0931	0.0859	0.0810	0.0780	0.0788	0.0800

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)					
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**
A → Y ↓	0.0937	0.0886	0.0843	0.0826	0.0848	0.0877

Delays at 25°C,1.0V, Typical Process (Cont'd.)

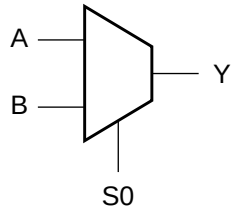
Description	K_{load} (ns/pF)					
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**
S1 → Y ↑	4.5925	3.3552	2.3839	1.6919	1.2018	0.7873
S1 → Y ↓	2.9114	2.0204	1.3907	1.0406	0.7269	0.4808
S0 → Y ↑	4.5959	3.3575	2.3852	1.6926	1.2023	0.7876
S0 → Y ↓	2.9132	2.0176	1.3896	1.0392	0.7261	0.4801
D → Y ↑	4.5951	3.3575	2.3853	1.6924	1.2024	0.7877
D → Y ↓	2.9133	2.0214	1.3912	1.0409	0.7271	0.4809
C → Y ↑	4.5948	3.3572	2.3853	1.6926	1.2024	0.7877
C → Y ↓	2.9130	2.0213	1.3911	1.0409	0.7270	0.4809
B → Y ↑	4.5952	3.3573	2.3852	1.6927	1.2023	0.7876
B → Y ↓	2.9131	2.0174	1.3896	1.0393	0.7261	0.4802
A → Y ↑	4.5961	3.3574	2.3853	1.6927	1.2023	0.7876
A → Y ↓	2.9127	2.0174	1.3895	1.0392	0.7261	0.4802

Cell Description

The MXT2 cell is a 2-to-1multiplexer. The state of the select input (S0) determines which data input (A, B) is presented to the output (Y). The output (Y) is represented by the logic equation:

$Y = (\overline{S0} \bullet A) + (S0 \bullet B)$

Logic Symbol



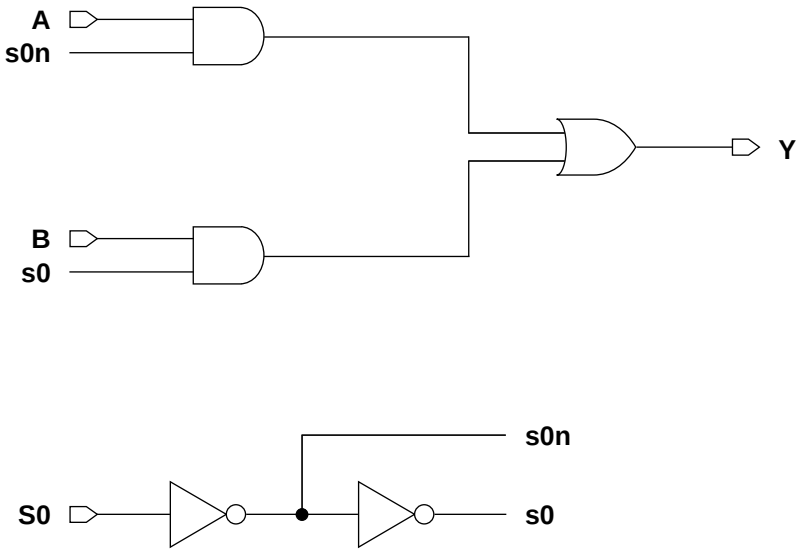
Function Table

S0	A	B	Y
0	0	x	0
0	1	x	1
1	x	0	0
1	x	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
MXT2X0P5MA10TR	2.00	2.20
MXT2X0P7MA10TR	2.00	2.20
MXT2X1MA10TR	2.00	2.20
MXT2X1P4MA10TR	2.00	2.60
MXT2X2MA10TR	2.00	2.60
MXT2X3MA10TR	2.00	4.40
MXT2X4MA10TR	2.00	4.60
MXT2X6MA10TR	2.00	5.60

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
S0	0.0020	0.0023	0.0025	0.0027	0.0032	0.0052	0.0060	0.0085
B	0.0014	0.0016	0.0019	0.0022	0.0027	0.0043	0.0052	0.0077
A	0.0015	0.0017	0.0021	0.0024	0.0029	0.0045	0.0054	0.0081

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
S0	0.0026	0.0029	0.0031	0.0032	0.0037	0.0052	0.0059	0.0082
B	0.0010	0.0012	0.0014	0.0015	0.0017	0.0030	0.0035	0.0050
A	0.0011	0.0012	0.0014	0.0015	0.0019	0.0027	0.0032	0.0048

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
S0 → Y ↑	0.0427	0.0412	0.0390	0.0418	0.0395	0.0431	0.0410	0.0387
S0 → Y ↓	0.0468	0.0460	0.0443	0.0463	0.0439	0.0465	0.0459	0.0425
B → Y ↑	0.0382	0.0364	0.0339	0.0356	0.0333	0.0351	0.0343	0.0324
B → Y ↓	0.0503	0.0490	0.0465	0.0488	0.0461	0.0481	0.0474	0.0445
A → Y ↑	0.0383	0.0362	0.0340	0.0359	0.0340	0.0380	0.0370	0.0346
A → Y ↓	0.0485	0.0472	0.0446	0.0470	0.0447	0.0478	0.0471	0.0436

Delays at 25°C,1.0V, Typical Process (Cont'd.)

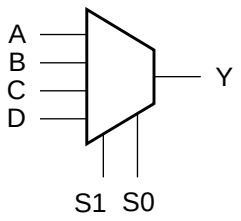
Description	K_{load} (ns/pF)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
S0 → Y ↑	4.5143	3.3146	2.3778	1.6089	1.1649	0.7955	0.5860	0.3878
S0 → Y ↓	2.6748	1.9349	1.3781	0.9448	0.6646	0.4770	0.3487	0.2281
B → Y ↑	4.5164	3.3162	2.3787	1.6096	1.1653	0.7945	0.5854	0.3875
B → Y ↓	2.6746	1.9350	1.3780	0.9448	0.6649	0.4764	0.3483	0.2281
A → Y ↑	4.5109	3.3119	2.3757	1.6086	1.1647	0.7956	0.5861	0.3878
A → Y ↓	2.6685	1.9306	1.3753	0.9430	0.6641	0.4774	0.3489	0.2282

Cell Description

The MXT4 cell is a 4-to-1 multiplexer. The state of the select inputs (S1, S0) determines which data input (A, B, C, D) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = (\overline{S0} \bullet \overline{S1} \bullet A) + (S0 \bullet \overline{S1} \bullet B) + (\overline{S0} \bullet S1 \bullet C) + (S0 \bullet S1 \bullet D)$$

Logic Symbol



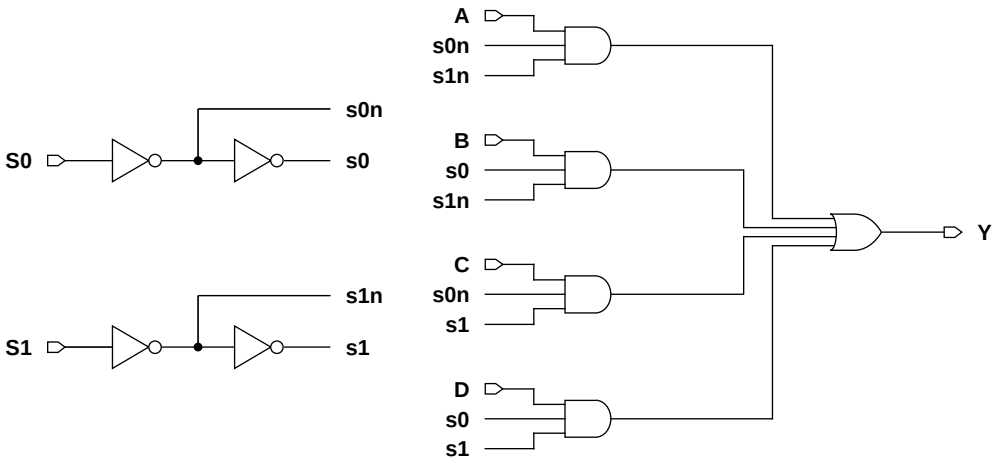
Function Table

S1	S0	A	B	C	D	Y
0	0	0	x	x	x	0
0	0	1	x	x	x	1
0	1	x	0	x	x	0
0	1	x	1	x	x	1
1	0	x	x	0	x	0
1	0	x	x	1	x	1
1	1	x	x	x	0	0
1	1	x	x	x	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
MXT4X0P5MA10TR	2.00	5.60
MXT4X0P7MA10TR	2.00	5.60
MXT4X1MA10TR	2.00	5.60
MXT4X1P4MA10TR	2.00	5.80
MXT4X2MA10TR	2.00	5.80
MXT4X3MA10TR	2.00	11.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)					
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**
S1	0.0023	0.0026	0.0029	0.0034	0.0038	0.0060
S0	0.0039	0.0044	0.0048	0.0053	0.0056	0.0117
D	0.0016	0.0019	0.0023	0.0025	0.0030	0.0055
C	0.0017	0.0020	0.0023	0.0025	0.0030	0.0061
B	0.0016	0.0019	0.0022	0.0025	0.0029	0.0055
A	0.0017	0.0020	0.0024	0.0027	0.0031	0.0059

Pin Capacitance

Pin	Capacitance (pF)					
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**
S1	0.0020	0.0022	0.0024	0.0028	0.0030	0.0053
S0	0.0039	0.0044	0.0050	0.0054	0.0056	0.0116
D	0.0010	0.0012	0.0014	0.0015	0.0017	0.0031
C	0.0011	0.0013	0.0015	0.0015	0.0018	0.0033
B	0.0011	0.0013	0.0014	0.0015	0.0017	0.0031
A	0.0010	0.0012	0.0014	0.0015	0.0017	0.0033

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)					
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**
S1 → Y ↑	0.0499	0.0470	0.0472	0.0480	0.0488	0.0443
S1 → Y ↓	0.0601	0.0578	0.0582	0.0624	0.0635	0.0546
S0 → Y ↑	0.0705	0.0655	0.0633	0.0641	0.0648	0.0619
S0 → Y ↓	0.0884	0.0824	0.0799	0.0847	0.0842	0.0766
D → Y ↑	0.0633	0.0586	0.0561	0.0569	0.0576	0.0553
D → Y ↓	0.0816	0.0767	0.0754	0.0798	0.0793	0.0726
C → Y ↑	0.0634	0.0587	0.0579	0.0584	0.0593	0.0566
C → Y ↓	0.0797	0.0744	0.0742	0.0786	0.0779	0.0732
B → Y ↑	0.0655	0.0603	0.0585	0.0596	0.0606	0.0564
B → Y ↓	0.0826	0.0771	0.0758	0.0811	0.0804	0.0719
A → Y ↑	0.0659	0.0607	0.0588	0.0601	0.0605	0.0573

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)					
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**
A → Y ↓	0.0842	0.0780	0.0766	0.0827	0.0810	0.0725

Delays at 25°C,1.0V, Typical Process (Cont'd.)

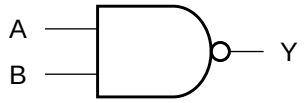
Description	K_{load} (ns/pF)					
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**
S1 → Y ↑	4.6043	3.3414	2.4118	1.6695	1.1920	0.7821
S1 → Y ↓	2.9317	2.0769	1.4555	1.0437	0.7321	0.4915
S0 → Y ↑	4.6092	3.3434	2.4135	1.6699	1.1919	0.7821
S0 → Y ↓	2.9699	2.0928	1.4652	1.0523	0.7361	0.4922
D → Y ↑	4.6025	3.3404	2.4099	1.6674	1.1903	0.7817
D → Y ↓	2.9412	2.0812	1.4586	1.0447	0.7330	0.4915
C → Y ↑	4.6046	3.3415	2.4124	1.6695	1.1917	0.7821
C → Y ↓	2.9348	2.0728	1.4568	1.0446	0.7322	0.4922
B → Y ↑	4.6074	3.3431	2.4123	1.6696	1.1921	0.7821
B → Y ↓	2.9599	2.0895	1.4634	1.0499	0.7354	0.4919
A → Y ↑	4.6024	3.3403	2.4101	1.6678	1.1904	0.7819
A → Y ↓	2.9703	2.0931	1.4654	1.0523	0.7361	0.4926

Cell Description

The NAND2 cell provides the logical NAND of two inputs (A,B). The output (Y) is represented by the logic equation:

$Y = \overline{(A \bullet B)}$

Logic Symbol



Function Table

A	B	Y
0	x	1
x	0	1
1	1	0

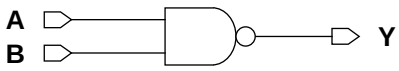
Cell Size

Drive Strength	Height (um)	Width (um)
NAND2X0P5AA10TR	2.00	0.80
NAND2X0P5BA10TR	2.00	0.80
NAND2X0P5MA10TR	2.00	0.80
NAND2X0P7AA10TR	2.00	0.80
NAND2X0P7BA10TR	2.00	0.80
NAND2X0P7MA10TR	2.00	0.80
NAND2X1AA10TR	2.00	0.80
NAND2X1BA10TR	2.00	0.80
NAND2X1MA10TR	2.00	0.80
NAND2X1P4AA10TR	2.00	1.40
NAND2X1P4BA10TR	2.00	1.40
NAND2X1P4MA10TR	2.00	1.40
NAND2X2AA10TR	2.00	1.40
NAND2X2BA10TR	2.00	1.40
NAND2X2MA10TR	2.00	1.40
NAND2X3AA10TR	2.00	2.00
NAND2X3BA10TR	2.00	2.00
NAND2X3MA10TR	2.00	2.00
NAND2X4AA10TR	2.00	2.40
NAND2X4BA10TR	2.00	2.40

Cell Size (Cont'd.)

Drive Strength	Height (um)	Width (um)
NAND2X4MA10TR	2.00	2.40
NAND2X6AA10TR	2.00	3.40
NAND2X6BA10TR	2.00	3.40
NAND2X6MA10TR	2.00	3.40
NAND2X8AA10TR	2.00	4.60
NAND2X8BA10TR	2.00	4.60
NAND2X8MA10TR	2.00	4.60

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P5A	**X0P5B**	**X0P5M**	**X0P7A**	**X0P7B**	**X0P7M**	**X1P0A**	**X1P0B**
A	0.0006	0.0006	0.0005	0.0008	0.0008	0.0007	0.0009	0.0011
B	0.0005	0.0006	0.0004	0.0007	0.0007	0.0006	0.0008	0.0009

AC Power (Cont'd.)

Pin	Power (uW/MHz)							
	X1P0M	**X1P4A**	**X1P4B**	**X1P4M**	**X2P0A**	**X2P0B**	**X2P0M**	**X3P0A**
A	0.0008	0.0014	0.0016	0.0013	0.0018	0.0020	0.0017	0.0029
B	0.0007	0.0014	0.0015	0.0012	0.0018	0.0020	0.0016	0.0026

AC Power (Cont'd.)

Pin	Power (uW/MHz)							
	X3P0B	**X3P0M**	**X4P0A**	**X4P0B**	**X4P0M**	**X6P0A**	**X6P0B**	**X6P0M**
A	0.0032	0.0026	0.0037	0.0041	0.0034	0.0057	0.0063	0.0051
B	0.0029	0.0023	0.0036	0.0040	0.0032	0.0054	0.0060	0.0048

AC Power (Cont'd.)

Pin	Power (uW/MHz)		
	X8P0A	**X8P0B**	**X8P0M**
A	0.0076	0.0084	0.0068
B	0.0073	0.0080	0.0064

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5A	**X0P5B**	**X0P5M**	**X0P7A**	**X0P7B**	**X0P7M**	**X1P0A**	**X1P0B**
A	0.0012	0.0013	0.0012	0.0015	0.0016	0.0015	0.0019	0.0020
B	0.0011	0.0012	0.0010	0.0014	0.0015	0.0013	0.0017	0.0018

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)							
	X1P0M	**X1P4A**	**X1P4B**	**X1P4M**	**X2P0A**	**X2P0B**	**X2P0M**	**X3P0A**
A	0.0018	0.0028	0.0029	0.0027	0.0035	0.0037	0.0033	0.0056
B	0.0016	0.0028	0.0029	0.0026	0.0035	0.0038	0.0033	0.0051

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)							
	X3P0B	**X3P0M**	**X4P0A**	**X4P0B**	**X4P0M**	**X6P0A**	**X6P0B**	**X6P0M**
A	0.0058	0.0052	0.0071	0.0075	0.0068	0.0108	0.0115	0.0103
B	0.0054	0.0049	0.0070	0.0075	0.0067	0.0106	0.0112	0.0099

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)		
	X8P0A	**X8P0B**	**X8P0M**
A	0.0146	0.0154	0.0138
B	0.0141	0.0149	0.0132

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5A	**X0P5B**	**X0P5M**	**X0P7A**	**X0P7B**	**X0P7M**	**X1P0A**	**X1P0B**
A → Y ↑	0.0115	0.0111	0.0129	0.0111	0.0103	0.0124	0.0101	0.0095
A → Y ↓	0.0108	0.0119	0.0106	0.0104	0.0108	0.0100	0.0093	0.0097
B → Y ↑	0.0129	0.0122	0.0144	0.0124	0.0114	0.0141	0.0117	0.0108
B → Y ↓	0.0113	0.0123	0.0109	0.0109	0.0113	0.0105	0.0101	0.0105

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)							
	X1P0M	**X1P4A**	**X1P4B**	**X1P4M**	**X2P0A**	**X2P0B**	**X2P0M**	**X3P0A**
A → Y ↑	0.0112	0.0100	0.0093	0.0111	0.0092	0.0086	0.0101	0.0093
A → Y ↓	0.0088	0.0094	0.0098	0.0090	0.0085	0.0089	0.0081	0.0087
B → Y ↑	0.0132	0.0120	0.0110	0.0135	0.0113	0.0104	0.0127	0.0112
B → Y ↓	0.0097	0.0105	0.0110	0.0101	0.0097	0.0103	0.0093	0.0098

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)							
	X3P0B	**X3P0M**	**X4P0A**	**X4P0B**	**X4P0M**	**X6P0A**	**X6P0B**	**X6P0M**
A → Y ↑	0.0088	0.0102	0.0092	0.0086	0.0100	0.0091	0.0086	0.0100
A → Y ↓	0.0091	0.0083	0.0084	0.0088	0.0080	0.0083	0.0089	0.0080
B → Y ↑	0.0103	0.0125	0.0112	0.0103	0.0125	0.0111	0.0102	0.0124
B → Y ↓	0.0102	0.0094	0.0097	0.0101	0.0093	0.0096	0.0101	0.0092

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)		
	X8P0A	**X8P0B**	**X8P0M**
A → Y ↑	0.0091	0.0085	0.0100
A → Y ↓	0.0084	0.0088	0.0079
B → Y ↑	0.0110	0.0102	0.0123
B → Y ↓	0.0096	0.0100	0.0091

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X0P5A	**X0P5B**	**X0P5M**	**X0P7A**	**X0P7B**	**X0P7M**	**X1P0A**	**X1P0B**
A → Y ↑	5.4422	4.6623	6.4523	3.9669	3.4073	4.7620	2.8594	2.4550
A → Y ↓	5.1410	5.1488	5.1441	3.6920	3.6922	3.6468	2.5926	2.5930
B → Y ↑	5.4388	4.6363	6.4472	3.9415	3.3822	4.7356	2.8349	2.4310
B → Y ↓	5.1389	5.1464	5.1420	3.6908	3.6912	3.6463	2.5914	2.5920

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X1P0M	**X1P4A**	**X1P4B**	**X1P4M**	**X2P0A**	**X2P0B**	**X2P0M**	**X3P0A**
A → Y ↑	3.4673	1.9361	1.6579	2.3220	1.3956	1.1779	1.6725	0.9081
A → Y ↓	2.5923	1.8087	1.8090	1.7864	1.2677	1.2671	1.2615	0.8496
B → Y ↑	3.4424	1.9315	1.6509	2.3206	1.3861	1.1824	1.6812	0.9060
B → Y ↓	2.5911	1.8084	1.8085	1.7860	1.2674	1.2669	1.2614	0.8494

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X3P0B	**X3P0M**	**X4P0A**	**X4P0B**	**X4P0M**	**X6P0A**	**X6P0B**	**X6P0M**
A → Y ↑	0.7769	1.1015	0.6757	0.5791	0.8186	0.4475	0.3838	0.5411
A → Y ↓	0.8440	0.8476	0.6201	0.6204	0.6294	0.4085	0.4180	0.4085
B → Y ↑	0.7765	1.0988	0.6777	0.5810	0.8208	0.4485	0.3844	0.5425
B → Y ↓	0.8438	0.8474	0.6199	0.6202	0.6291	0.4085	0.4178	0.4084

Delays at 25°C,1.0V, Typical Process (Cont'd.)

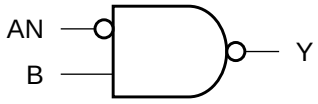
Description	K_{load} (ns/pF)		
	X8P0A	**X8P0B**	**X8P0M**
A → Y ↑	0.3339	0.2860	0.4031
A → Y ↓	0.3064	0.3103	0.3057
B → Y ↑	0.3341	0.2862	0.4035
B → Y ↓	0.3065	0.3102	0.3057

Cell Description

The NAND2B cell provides the logical NAND of one inverted input (AN) and one non-inverted input (B). The output (Y) is represented by the logic equation:

$Y = (\overline{\overline{AN} \bullet B})$

Logic Symbol



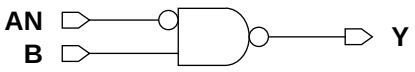
Function Table

AN	B	Y
1	x	1
x	0	1
0	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND2BX0P5MA10TR	2.00	1.20
NAND2BX0P7MA10TR	2.00	1.20
NAND2BX1MA10TR	2.00	1.20
NAND2BX1P4MA10TR	2.00	1.60
NAND2BX2MA10TR	2.00	1.60
NAND2BX3MA10TR	2.00	2.20
NAND2BX4MA10TR	2.00	2.60
NAND2BX6MA10TR	2.00	4.00
NAND2BX8MA10TR	2.00	5.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
AN	0.0014	0.0015	0.0016	0.0021	0.0026	0.0039	0.0048	0.0072	0.0091
B	0.0004	0.0005	0.0007	0.0012	0.0016	0.0023	0.0032	0.0049	0.0066

Pin Capacitance

Pin	Capacitance (pF)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
AN	0.0009	0.0009	0.0008	0.0011	0.0013	0.0017	0.0019	0.0031	0.0036
B	0.0010	0.0012	0.0016	0.0026	0.0034	0.0048	0.0066	0.0099	0.0133

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
AN → Y ↑	0.0280	0.0277	0.0289	0.0291	0.0274	0.0273	0.0272	0.0261	0.0265
AN → Y ↓	0.0342	0.0344	0.0364	0.0366	0.0350	0.0352	0.0371	0.0329	0.0344
B → Y ↑	0.0137	0.0129	0.0123	0.0130	0.0122	0.0121	0.0120	0.0119	0.0118
B → Y ↓	0.0113	0.0108	0.0108	0.0114	0.0108	0.0109	0.0110	0.0108	0.0109

Delays at 25°C,1.0V, Typical Process (Cont'd.)

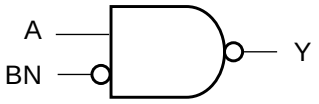
Description	K_{load} (ns/pF)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
AN → Y ↑	6.3300	4.6870	3.4098	2.3055	1.6582	1.0936	0.8154	0.5378	0.4021
AN → Y ↓	5.0856	3.6891	2.6628	1.7816	1.2585	0.8395	0.6289	0.4080	0.3060
B → Y ↑	6.2137	4.6096	3.3352	2.2988	1.6588	1.0858	0.8147	0.5367	0.4014
B → Y ↓	5.0763	3.6820	2.6582	1.7781	1.2560	0.8379	0.6275	0.4074	0.3055

Cell Description

The NAND2XB cell provides the logical NAND of one non-inverted input (A) and one inverted input (BN). The output (Y) is represented by the logic equation:

$Y = \overline{(A \bullet \overline{BN})}$

Logic Symbol



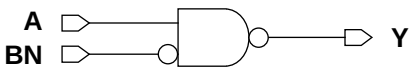
Function Table

A	BN	Y
0	x	1
x	1	1
1	0	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND2XBX0P5MA10TR	2.00	1.20
NAND2XBX0P7MA10TR	2.00	1.20
NAND2XBX1MA10TR	2.00	1.20
NAND2XBX1P4MA10TR	2.00	1.60
NAND2XBX2MA10TR	2.00	1.60
NAND2XBX3MA10TR	2.00	2.20
NAND2XBX4MA10TR	2.00	2.80
NAND2XBX6MA10TR	2.00	4.00
NAND2XBX8MA10TR	2.00	5.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A	0.0006	0.0007	0.0009	0.0013	0.0017	0.0027	0.0035	0.0052	0.0070
BN	0.0016	0.0017	0.0019	0.0025	0.0032	0.0046	0.0058	0.0085	0.0109

Pin Capacitance

Pin	Capacitance (pF)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A	0.0012	0.0015	0.0017	0.0026	0.0033	0.0052	0.0068	0.0103	0.0139
BN	0.0010	0.0010	0.0009	0.0011	0.0013	0.0017	0.0019	0.0031	0.0036

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A → Y ↑	0.0128	0.0119	0.0108	0.0110	0.0100	0.0102	0.0098	0.0099	0.0100
A → Y ↓	0.0104	0.0095	0.0085	0.0088	0.0078	0.0081	0.0078	0.0078	0.0078
BN → Y ↑	0.0284	0.0287	0.0300	0.0318	0.0305	0.0291	0.0296	0.0284	0.0286
BN → Y ↓	0.0322	0.0332	0.0357	0.0375	0.0367	0.0350	0.0361	0.0336	0.0349

Delays at 25°C,1.0V, Typical Process (Cont'd.)

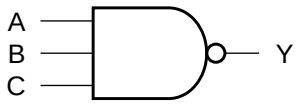
Description	K_{load} (ns/pF)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A → Y ↑	6.3259	4.6891	3.4070	2.3034	1.6572	1.0931	0.8127	0.5370	0.4019
A → Y ↓	5.0682	3.6736	2.6223	1.7864	1.2449	0.8408	0.6246	0.4067	0.3048
BN → Y ↑	6.2102	4.6121	3.3339	2.2981	1.6674	1.0866	0.8110	0.5363	0.4014
BN → Y ↓	5.0729	3.6789	2.6282	1.7913	1.2488	0.8432	0.6266	0.4078	0.3059

Cell Description

The NAND3 cell provides the logical NAND of three inputs (A,B,C). The output (Y) is represented by the logic equation:

$Y = \overline{(A \bullet B \bullet C)}$

Logic Symbol



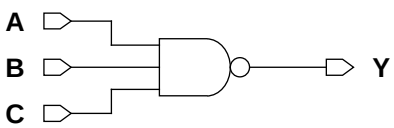
Function Table

A	B	C	Y
0	x	x	1
x	0	x	1
x	x	0	1
1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND3X0P5MA10TR	2.00	1.20
NAND3X0P5AA10TR	2.00	1.20
NAND3X0P7MA10TR	2.00	1.20
NAND3X0P7AA10TR	2.00	1.20
NAND3X1MA10TR	2.00	1.20
NAND3X1AA10TR	2.00	1.20
NAND3X1P4MA10TR	2.00	1.80
NAND3X1P4AA10TR	2.00	2.00
NAND3X2MA10TR	2.00	2.00
NAND3X2AA10TR	2.00	2.00
NAND3X3MA10TR	2.00	2.60
NAND3X3AA10TR	2.00	2.60
NAND3X4MA10TR	2.00	3.80
NAND3X4AA10TR	2.00	3.80
NAND3X6MA10TR	2.00	4.80
NAND3X6AA10TR	2.00	5.20

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P5M	**X0P5A**	**X0P7M**	**X0P7A**	**X1P0M**	**X1P0A**	**X1P4M**	**X1P4A**
A	0.0005	0.0005	0.0006	0.0007	0.0007	0.0009	0.0009	0.0014
B	0.0003	0.0004	0.0004	0.0005	0.0005	0.0007	0.0007	0.0012
C	0.0003	0.0004	0.0004	0.0006	0.0006	0.0007	0.0008	0.0013

AC Power (Cont'd.)

Pin	Power (uW/MHz)							
	X2P0M	**X2P0A**	**X3P0M**	**X3P0A**	**X4P0M**	**X4P0A**	**X6P0M**	**X6P0A**
A	0.0013	0.0017	0.0021	0.0027	0.0029	0.0036	0.0041	0.0054
B	0.0011	0.0015	0.0016	0.0022	0.0022	0.0030	0.0032	0.0045
C	0.0012	0.0015	0.0017	0.0023	0.0022	0.0030	0.0032	0.0045

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5M	**X0P5A**	**X0P7M**	**X0P7A**	**X1P0M**	**X1P0A**	**X1P4M**	**X1P4A**
A	0.0011	0.0012	0.0013	0.0015	0.0017	0.0018	0.0023	0.0028
B	0.0010	0.0010	0.0012	0.0013	0.0015	0.0017	0.0022	0.0028
C	0.0009	0.0010	0.0012	0.0014	0.0015	0.0017	0.0024	0.0029

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)							
	X2P0M	**X2P0A**	**X3P0M**	**X3P0A**	**X4P0M**	**X4P0A**	**X6P0M**	**X6P0A**
A	0.0030	0.0034	0.0046	0.0052	0.0061	0.0069	0.0087	0.0103
B	0.0030	0.0034	0.0045	0.0051	0.0059	0.0067	0.0083	0.0100
C	0.0032	0.0035	0.0045	0.0050	0.0060	0.0068	0.0083	0.0099

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5M	**X0P5A**	**X0P7M**	**X0P7A**	**X1P0M**	**X1P0A**	**X1P4M**	**X1P4A**
A → Y ↑	0.0167	0.0134	0.0158	0.0133	0.0148	0.0120	0.0140	0.0117
A → Y ↓	0.0147	0.0155	0.0129	0.0151	0.0118	0.0132	0.0107	0.0135
B → Y ↑	0.0189	0.0152	0.0183	0.0150	0.0178	0.0139	0.0176	0.0142
B → Y ↓	0.0167	0.0178	0.0150	0.0172	0.0143	0.0156	0.0135	0.0164
C → Y ↑	0.0220	0.0173	0.0217	0.0171	0.0210	0.0160	0.0219	0.0166
C → Y ↓	0.0178	0.0189	0.0162	0.0184	0.0154	0.0168	0.0151	0.0178

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)							
	X2P0M	**X2P0A**	**X3P0M**	**X3P0A**	**X4P0M**	**X4P0A**	**X6P0M**	**X6P0A**
A → Y ↑	0.0130	0.0107	0.0134	0.0110	0.0131	0.0107	0.0126	0.0106
A → Y ↓	0.0105	0.0118	0.0099	0.0112	0.0097	0.0109	0.0092	0.0108
B → Y ↑	0.0165	0.0130	0.0179	0.0139	0.0178	0.0138	0.0171	0.0136
B → Y ↓	0.0134	0.0147	0.0136	0.0149	0.0137	0.0150	0.0127	0.0149
C → Y ↑	0.0202	0.0155	0.0223	0.0167	0.0223	0.0167	0.0212	0.0163
C → Y ↓	0.0149	0.0162	0.0155	0.0168	0.0157	0.0170	0.0145	0.0167

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X0P5M	**X0P5A**	**X0P7M**	**X0P7A**	**X1P0M**	**X1P0A**	**X1P4M**	**X1P4A**
A → Y ↑	7.9308	5.7165	6.1062	4.2068	4.4168	3.0395	3.2014	2.0222
A → Y ↓	7.4579	7.3300	5.2805	5.2816	3.7410	3.7417	2.6435	2.6418
B → Y ↑	7.7737	5.6311	5.9834	4.1438	4.3507	2.9779	3.2128	2.0390
B → Y ↓	7.4557	7.3280	5.2794	5.2804	3.7411	3.7417	2.6432	2.6412
C → Y ↑	7.9140	5.7237	6.0931	4.1777	4.3863	3.0137	3.2628	2.0673
C → Y ↓	7.4570	7.3288	5.2797	5.2806	3.7411	3.7408	2.6439	2.6416

Delays at 25°C,1.0V, Typical Process (Cont'd.)

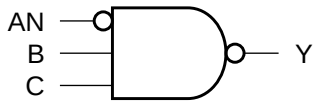
Description	K_{load} (ns/pF)							
	X2P0M	**X2P0A**	**X3P0M**	**X3P0A**	**X4P0M**	**X4P0A**	**X6P0M**	**X6P0A**
A → Y ↑	2.1357	1.4709	1.4576	0.9893	1.0841	0.7371	0.7314	0.4859
A → Y ↓	1.8748	1.8753	1.1467	1.1470	0.8648	0.8650	0.5724	0.5793
B → Y ↑	2.1533	1.4788	1.4215	0.9679	1.0599	0.7223	0.7221	0.4773
B → Y ↓	1.8746	1.8751	1.1466	1.1470	0.8647	0.8649	0.5723	0.5793
C → Y ↑	2.1770	1.5011	1.4555	0.9904	1.0756	0.7328	0.7304	0.4871
C → Y ↓	1.8751	1.8754	1.1466	1.1470	0.8648	0.8651	0.5725	0.5794

Cell Description

The NAND3B cell provides the logical NAND of one inverted input (AN) and two non-inverted inputs (B,C). The output (Y) is represented by the logic equation:

$Y = (\overline{\overline{AN} \bullet B \bullet C})$

Logic Symbol



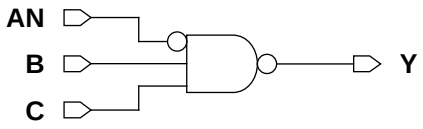
Function Table

AN	B	C	Y
1	x	x	1
x	0	x	1
x	x	0	1
0	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND3BX0P5MA10TR	2.00	1.40
NAND3BX0P7MA10TR	2.00	1.40
NAND3BX1MA10TR	2.00	1.40
NAND3BX1P4MA10TR	2.00	2.20
NAND3BX2MA10TR	2.00	2.20
NAND3BX3MA10TR	2.00	3.00
NAND3BX4MA10TR	2.00	4.20
NAND3BX6MA10TR	2.00	5.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M
AN	0.0015	0.0016	0.0017	0.0023	0.0027	0.0040	0.0055	0.0074
B	0.0004	0.0004	0.0006	0.0009	0.0012	0.0017	0.0023	0.0033
C	0.0004	0.0004	0.0006	0.0009	0.0012	0.0017	0.0023	0.0033

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M
AN	0.0009	0.0010	0.0009	0.0010	0.0012	0.0015	0.0018	0.0029
B	0.0010	0.0012	0.0015	0.0024	0.0031	0.0045	0.0060	0.0084
C	0.0010	0.0012	0.0015	0.0025	0.0032	0.0045	0.0060	0.0083

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M
AN → Y ↑	0.0313	0.0305	0.0317	0.0327	0.0311	0.0312	0.0320	0.0289
AN → Y ↓	0.0367	0.0358	0.0370	0.0398	0.0376	0.0371	0.0380	0.0339
B → Y ↑	0.0189	0.0178	0.0175	0.0167	0.0161	0.0174	0.0175	0.0167
B → Y ↓	0.0173	0.0156	0.0157	0.0151	0.0147	0.0160	0.0162	0.0151
C → Y ↑	0.0215	0.0210	0.0208	0.0203	0.0198	0.0217	0.0220	0.0210
C → Y ↓	0.0188	0.0172	0.0175	0.0168	0.0164	0.0182	0.0187	0.0172

Delays at 25°C,1.0V, Typical Process (Cont'd.)

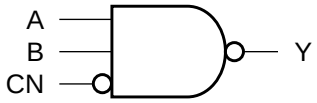
Description	K_{load} (ns/pF)							
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M
AN → Y ↑	7.9799	6.1306	4.4556	2.9365	2.1305	1.4557	1.0847	0.7317
AN → Y ↓	7.4282	5.3489	3.8740	2.6335	1.8643	1.1573	0.8663	0.5788
B → Y ↑	7.8301	6.0173	4.3738	2.9538	2.1443	1.4175	1.0592	0.7220
B → Y ↓	7.4246	5.3468	3.8736	2.6321	1.8636	1.1569	0.8660	0.5787
C → Y ↑	7.6993	6.0172	4.3593	2.9727	2.1607	1.4215	1.0650	0.7257
C → Y ↓	7.4249	5.3481	3.8732	2.6323	1.8638	1.1571	0.8661	0.5788

Cell Description

The NAND3XXB cell provides the logical NAND of two non-inverted inputs (A, B) and one inverted input (CN). The output (Y) is represented by the logic equation:

$Y = \overline{(A \bullet B \bullet \overline{CN})}$

Logic Symbol



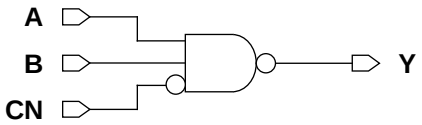
Function Table

A	B	CN	Y
x	x	1	1
x	0	x	1
0	x	x	1
1	1	0	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND3XXBX0P5MA10TR	2.00	1.40
NAND3XXBX0P7MA10TR	2.00	1.40
NAND3XXBX1MA10TR	2.00	1.40
NAND3XXBX1P4MA10TR	2.00	2.20
NAND3XXBX2MA10TR	2.00	2.20
NAND3XXBX3MA10TR	2.00	3.00
NAND3XXBX4MA10TR	2.00	4.20
NAND3XXBX6MA10TR	2.00	5.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M
A	0.0005	0.0006	0.0008	0.0011	0.0014	0.0022	0.0030	0.0042
B	0.0004	0.0004	0.0006	0.0008	0.0012	0.0017	0.0023	0.0033
CN	0.0015	0.0017	0.0018	0.0026	0.0030	0.0042	0.0053	0.0076

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M
A	0.0011	0.0013	0.0016	0.0024	0.0031	0.0046	0.0061	0.0087
B	0.0010	0.0012	0.0015	0.0024	0.0030	0.0045	0.0059	0.0083
CN	0.0010	0.0010	0.0009	0.0011	0.0012	0.0016	0.0019	0.0030

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M
A → Y ↑	0.0170	0.0155	0.0149	0.0134	0.0129	0.0134	0.0131	0.0126
A → Y ↓	0.0149	0.0127	0.0119	0.0111	0.0105	0.0100	0.0097	0.0092
B → Y ↑	0.0189	0.0181	0.0177	0.0168	0.0165	0.0178	0.0178	0.0170
B → Y ↓	0.0165	0.0147	0.0140	0.0137	0.0133	0.0136	0.0136	0.0128
CN → Y ↑	0.0344	0.0354	0.0377	0.0406	0.0386	0.0386	0.0395	0.0364
CN → Y ↓	0.0366	0.0369	0.0388	0.0437	0.0413	0.0415	0.0424	0.0381

Delays at 25°C,1.0V, Typical Process (Cont'd.)

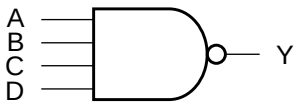
Description	K_{load} (ns/pF)							
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M
A → Y ↑	8.0380	6.1476	4.4546	2.9368	2.1282	1.4548	1.0859	0.7312
A → Y ↓	7.4057	5.3338	3.7409	2.6299	1.8680	1.1556	0.8652	0.5769
B → Y ↑	7.7941	5.9945	4.3722	2.9539	2.1420	1.4166	1.0586	0.7215
B → Y ↓	7.4037	5.3321	3.7410	2.6293	1.8678	1.1556	0.8652	0.5769
CN → Y ↑	7.6824	6.0202	4.4223	2.9751	2.1598	1.4218	1.0647	0.7258
CN → Y ↓	7.4054	5.3341	3.7422	2.6329	1.8704	1.1569	0.8660	0.5774

Cell Description

The NAND4 cell provides a logical NAND of four inputs (A,B,C,D). The output (Y) is represented by the logic equation:

$Y = \overline{(A \bullet B \bullet C \bullet D)}$

Logic Symbol



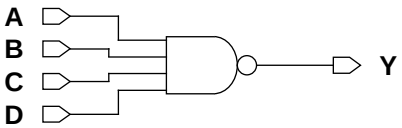
Function Table

A	B	C	D	Y
0	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
1	1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND4X0P5MA10TR	2.00	1.40
NAND4X0P5AA10TR	2.00	1.40
NAND4X0P7MA10TR	2.00	1.40
NAND4X0P7AA10TR	2.00	1.40
NAND4X1MA10TR	2.00	1.40
NAND4X1AA10TR	2.00	1.40
NAND4X1P4MA10TR	2.00	2.40
NAND4X1P4AA10TR	2.00	2.40
NAND4X2MA10TR	2.00	2.40
NAND4X2AA10TR	2.00	2.40
NAND4X3MA10TR	2.00	3.40
NAND4X3AA10TR	2.00	3.40
NAND4X4MA10TR	2.00	4.40
NAND4X4AA10TR	2.00	5.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P5M	**X0P5A**	**X0P7M**	**X0P7A**	**X1P0M**	**X1P0A**	**X1P4M**	**X1P4A**
A	0.0005	0.0005	0.0005	0.0007	0.0007	0.0009	0.0009	0.0012
B	0.0003	0.0004	0.0003	0.0005	0.0004	0.0006	0.0007	0.0009
C	0.0003	0.0004	0.0003	0.0005	0.0004	0.0007	0.0007	0.0010
D	0.0003	0.0004	0.0003	0.0005	0.0004	0.0007	0.0009	0.0011

AC Power (Cont'd.)

Pin	Power (uW/MHz)					
	X2P0M	**X2P0A**	**X3P0M**	**X3P0A**	**X4P0M**	**X4P0A**
A	0.0011	0.0015	0.0019	0.0025	0.0025	0.0033
B	0.0008	0.0012	0.0013	0.0020	0.0017	0.0026
C	0.0009	0.0013	0.0013	0.0020	0.0017	0.0026
D	0.0010	0.0015	0.0013	0.0020	0.0017	0.0026

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5M	**X0P5A**	**X0P7M**	**X0P7A**	**X1P0M**	**X1P0A**	**X1P4M**	**X1P4A**
A	0.0011	0.0012	0.0013	0.0015	0.0016	0.0018	0.0023	0.0026
B	0.0010	0.0010	0.0011	0.0013	0.0014	0.0016	0.0022	0.0025
C	0.0010	0.0011	0.0012	0.0013	0.0014	0.0017	0.0025	0.0027
D	0.0010	0.0010	0.0011	0.0013	0.0014	0.0016	0.0027	0.0029

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)					
	X2P0M	**X2P0A**	**X3P0M**	**X3P0A**	**X4P0M**	**X4P0A**
A	0.0028	0.0032	0.0042	0.0050	0.0056	0.0066
B	0.0028	0.0031	0.0041	0.0049	0.0051	0.0064
C	0.0030	0.0033	0.0041	0.0049	0.0051	0.0064
D	0.0031	0.0036	0.0041	0.0049	0.0051	0.0064

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5M	**X0P5A**	**X0P7M**	**X0P7A**	**X1P0M**	**X1P0A**	**X1P4M**	**X1P4A**
A → Y ↑	0.0208	0.0161	0.0193	0.0153	0.0174	0.0137	0.0167	0.0130
A → Y ↓	0.0183	0.0213	0.0159	0.0193	0.0134	0.0166	0.0131	0.0152
B → Y ↑	0.0235	0.0177	0.0223	0.0171	0.0209	0.0157	0.0207	0.0155
B → Y ↓	0.0211	0.0240	0.0188	0.0223	0.0166	0.0198	0.0167	0.0188
C → Y ↑	0.0281	0.0206	0.0271	0.0201	0.0259	0.0187	0.0257	0.0186
C → Y ↓	0.0245	0.0274	0.0221	0.0256	0.0199	0.0232	0.0200	0.0221
D → Y ↑	0.0315	0.0226	0.0309	0.0222	0.0297	0.0208	0.0308	0.0217
D → Y ↓	0.0254	0.0283	0.0233	0.0267	0.0211	0.0243	0.0223	0.0245

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)					
	X2P0M	**X2P0A**	**X3P0M**	**X3P0A**	**X4P0M**	**X4P0A**
A → Y ↑	0.0151	0.0117	0.0156	0.0127	0.0165	0.0126
A → Y ↓	0.0111	0.0133	0.0107	0.0138	0.0110	0.0136
B → Y ↑	0.0194	0.0143	0.0214	0.0160	0.0228	0.0162
B → Y ↓	0.0148	0.0170	0.0162	0.0194	0.0164	0.0196
C → Y ↑	0.0245	0.0173	0.0266	0.0190	0.0283	0.0195
C → Y ↓	0.0179	0.0201	0.0197	0.0228	0.0199	0.0235
D → Y ↑	0.0294	0.0201	0.0318	0.0220	0.0339	0.0224
D → Y ↓	0.0200	0.0223	0.0215	0.0246	0.0219	0.0254

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X0P5M	**X0P5A**	**X0P7M**	**X0P7A**	**X1P0M**	**X1P0A**	**X1P4M**	**X1P4A**
A → Y ↑	9.0125	6.2432	7.2388	4.6253	5.4297	3.3376	3.5183	2.2818
A → Y ↓	9.0459	9.6357	6.8377	6.8404	4.8467	4.8467	3.2031	3.2033
B → Y ↑	8.9233	6.1746	7.1614	4.5706	5.3669	3.2969	3.5127	2.2710
B → Y ↓	9.0433	9.6321	6.8378	6.8385	4.8452	4.8456	3.2019	3.2023
C → Y ↑	8.9917	6.2219	7.2147	4.6048	5.4054	3.3217	3.5622	2.3037
C → Y ↓	9.0444	9.6330	6.8381	6.8390	4.8463	4.8465	3.2035	3.2031
D → Y ↑	9.1118	6.3160	7.3173	4.6500	5.4807	3.3725	3.6244	2.3481
D → Y ↓	9.0464	9.6327	6.8369	6.8388	4.8462	4.8462	3.2034	3.2034

Delays at 25°C,1.0V, Typical Process (Cont'd.)

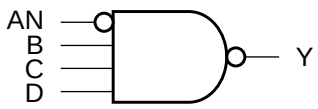
Description	K_{load} (ns/pF)					
	X2P0M	**X2P0A**	**X3P0M**	**X3P0A**	**X4P0M**	**X4P0A**
A → Y ↑	2.6379	1.6410	1.7852	1.0981	1.3774	0.8301
A → Y ↓	2.2713	2.2717	1.4954	1.4958	1.1245	1.1340
B → Y ↑	2.6287	1.6277	1.7474	1.0710	1.3895	0.8118
B → Y ↓	2.2706	2.2709	1.4952	1.4953	1.1245	1.1340
C → Y ↑	2.6654	1.6510	1.7498	1.0732	1.3910	0.8137
C → Y ↓	2.2706	2.2709	1.4953	1.4957	1.1247	1.1344
D → Y ↑	2.7145	1.6787	1.7918	1.1040	1.4150	0.8342
D → Y ↓	2.2712	2.2716	1.4954	1.4960	1.1249	1.1340

Cell Description

The NAND4B cell provides a logical NAND of one inverted input (AN) and three non-inverted inputs (B,C,D). The output (Y) is represented by the logic equation:

$Y = (\overline{\overline{AN} \bullet B \bullet C \bullet D})$

Logic Symbol



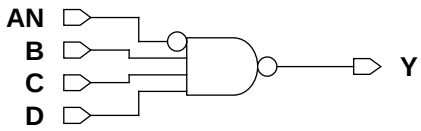
Function Table

AN	B	C	D	Y
1	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
0	1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND4BX0P5MA10TR	2.00	1.60
NAND4BX0P7MA10TR	2.00	1.60
NAND4BX1MA10TR	2.00	1.60
NAND4BX1P4MA10TR	2.00	2.60
NAND4BX2MA10TR	2.00	2.60
NAND4BX3MA10TR	2.00	3.80
NAND4BX4MA10TR	2.00	4.80

Functional Schematic



AC Power

Pin	Power (uW/MHz)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
AN	0.0015	0.0016	0.0016	0.0022	0.0027	0.0039	0.0051
B	0.0003	0.0004	0.0005	0.0006	0.0009	0.0014	0.0018
C	0.0003	0.0004	0.0005	0.0006	0.0009	0.0014	0.0018
D	0.0003	0.0003	0.0004	0.0007	0.0011	0.0013	0.0017

Pin Capacitance

Pin	Capacitance (pF)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
AN	0.0010	0.0010	0.0009	0.0011	0.0012	0.0015	0.0018
B	0.0010	0.0012	0.0014	0.0020	0.0027	0.0041	0.0051
C	0.0010	0.0011	0.0014	0.0022	0.0030	0.0041	0.0051
D	0.0010	0.0011	0.0014	0.0023	0.0032	0.0041	0.0051

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
AN → Y ↑	0.0345	0.0343	0.0335	0.0328	0.0323	0.0328	0.0343
AN → Y ↓	0.0406	0.0394	0.0375	0.0368	0.0373	0.0363	0.0363
B → Y ↑	0.0228	0.0216	0.0204	0.0198	0.0192	0.0210	0.0221
B → Y ↓	0.0219	0.0199	0.0184	0.0155	0.0161	0.0181	0.0185
C → Y ↑	0.0270	0.0260	0.0249	0.0257	0.0245	0.0265	0.0278
C → Y ↓	0.0253	0.0235	0.0218	0.0194	0.0198	0.0219	0.0222
D → Y ↑	0.0296	0.0296	0.0297	0.0306	0.0293	0.0313	0.0333
D → Y ↓	0.0262	0.0245	0.0230	0.0211	0.0218	0.0238	0.0244

Delays at 25°C,1.0V, Typical Process (Cont'd.)

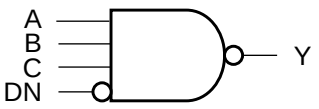
Description	K_{load} (ns/pF)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
AN → Y ↑	9.0757	7.2671	5.4285	3.8423	2.6329	1.7875	1.3800
AN → Y ↓	9.3605	7.1764	5.1383	3.1954	2.2771	1.4922	1.1286
B → Y ↑	8.9340	7.1820	5.3638	3.8665	2.6212	1.7485	1.3734
B → Y ↓	9.3581	7.1754	5.1381	3.1958	2.2765	1.4922	1.1287
C → Y ↑	8.9339	7.1439	5.3382	3.9149	2.6494	1.7460	1.3726
C → Y ↓	9.3576	7.1749	5.1387	3.1954	2.2772	1.4921	1.1287
D → Y ↑	8.8069	7.2163	5.5750	3.9715	2.6771	1.7524	1.3868
D → Y ↓	9.3585	7.1745	5.1376	3.1952	2.2772	1.4920	1.1290

Cell Description

The NAND4XXXB cell provides a logical NAND of three non-inverted inputs (A, B, C) and one inverted input (DN). The output (Y) is represented by the logic equation:

$Y = \overline{(A \bullet B \bullet C \bullet \overline{DN})}$

Logic Symbol



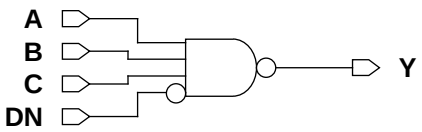
Function Table

A	B	C	DN	Y
x	x	x	1	1
x	x	0	x	1
x	0	x	x	1
0	x	x	x	1
1	1	1	0	0

Cell Size

Drive Strength	Height (um)	Width (um)
NAND4XXXBX0P5MA10TR	2.00	1.60
NAND4XXXBX0P7MA10TR	2.00	1.60
NAND4XXXBX1MA10TR	2.00	1.60
NAND4XXXBX1P4MA10TR	2.00	2.60
NAND4XXXBX2MA10TR	2.00	2.60
NAND4XXXBX3MA10TR	2.00	3.80
NAND4XXXBX4MA10TR	2.00	4.80

Functional Schematic



AC Power

Pin	Power (uW/MHz)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A	0.0005	0.0006	0.0007	0.0008	0.0012	0.0019	0.0025
B	0.0003	0.0004	0.0005	0.0006	0.0009	0.0013	0.0018
C	0.0003	0.0004	0.0004	0.0006	0.0009	0.0013	0.0017
DN	0.0016	0.0018	0.0019	0.0026	0.0030	0.0043	0.0050

Pin Capacitance

Pin	Capacitance (pF)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A	0.0012	0.0013	0.0016	0.0021	0.0028	0.0042	0.0056
B	0.0010	0.0011	0.0014	0.0020	0.0028	0.0041	0.0051
C	0.0010	0.0011	0.0014	0.0022	0.0030	0.0041	0.0051
DN	0.0010	0.0010	0.0010	0.0011	0.0012	0.0016	0.0018

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A → Y ↑	0.0206	0.0185	0.0175	0.0157	0.0152	0.0153	0.0165
A → Y ↓	0.0187	0.0157	0.0137	0.0110	0.0112	0.0103	0.0110
B → Y ↑	0.0231	0.0217	0.0212	0.0200	0.0195	0.0209	0.0225
B → Y ↓	0.0214	0.0191	0.0174	0.0144	0.0149	0.0158	0.0164
C → Y ↑	0.0270	0.0259	0.0255	0.0259	0.0245	0.0261	0.0279
C → Y ↓	0.0243	0.0219	0.0202	0.0178	0.0179	0.0192	0.0198
DN → Y ↑	0.0431	0.0436	0.0458	0.0487	0.0468	0.0462	0.0486
DN → Y ↓	0.0450	0.0439	0.0435	0.0460	0.0465	0.0451	0.0446

Delays at 25°C,1.0V, Typical Process (Cont'd.)

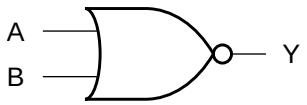
Description	K_{load} (ns/pF)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A → Y ↑	9.1022	7.2758	5.5121	3.8417	2.6321	1.7858	1.3821
A → Y ↓	9.3965	7.1550	5.1000	3.1669	2.2665	1.4911	1.1256
B → Y ↑	8.9673	7.1552	5.4522	3.8661	2.6203	1.7411	1.3729
B → Y ↓	9.3942	7.1541	5.0995	3.1671	2.2666	1.4911	1.1256
C → Y ↑	8.9084	7.1564	5.4195	3.9180	2.6492	1.7393	1.3724
C → Y ↓	9.3948	7.1566	5.1002	3.1668	2.2664	1.4910	1.1257
DN → Y ↑	8.8281	7.1932	5.6908	3.9834	2.6773	1.7511	1.3863
DN → Y ↓	9.3963	7.1565	5.1012	3.1690	2.2684	1.4915	1.1264

Cell Description

The NOR2 cell provides a logical NOR of two inputs (A,B). The output (Y) is represented by the logic equation:

$Y = \overline{(A + B)}$

Logic Symbol



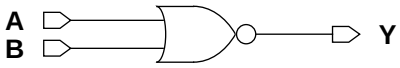
Function Table

A	B	Y
0	0	1
x	1	0
1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
NOR2X0P5MA10TR	2.00	0.80
NOR2X0P5AA10TR	2.00	0.80
NOR2X0P7MA10TR	2.00	0.80
NOR2X0P7AA10TR	2.00	0.80
NOR2X1MA10TR	2.00	0.80
NOR2X1AA10TR	2.00	0.80
NOR2X1P4MA10TR	2.00	1.40
NOR2X1P4AA10TR	2.00	1.40
NOR2X2MA10TR	2.00	1.40
NOR2X2AA10TR	2.00	1.40
NOR2X3MA10TR	2.00	2.00
NOR2X3AA10TR	2.00	2.00
NOR2X4MA10TR	2.00	2.40
NOR2X4AA10TR	2.00	2.40
NOR2X6MA10TR	2.00	3.40
NOR2X6AA10TR	2.00	3.40
NOR2X8MA10TR	2.00	4.60
NOR2X8AA10TR	2.00	4.60

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P5M	**X0P5A**	**X0P7M**	**X0P7A**	**X1P0M**	**X1P0A**	**X1P4M**	**X1P4A**
A	0.0002	0.0002	0.0002	0.0002	0.0003	0.0003	0.0005	0.0005
B	0.0005	0.0005	0.0006	0.0006	0.0008	0.0008	0.0012	0.0012

AC Power (Cont'd.)

Pin	Power (uW/MHz)							
	X2P0M	**X2P0A**	**X3P0M**	**X3P0A**	**X4P0M**	**X4P0A**	**X6P0M**	**X6P0A**
A	0.0007	0.0007	0.0010	0.0010	0.0014	0.0014	0.0021	0.0021
B	0.0016	0.0016	0.0025	0.0025	0.0033	0.0032	0.0049	0.0049

AC Power (Cont'd.)

Pin	Power (uW/MHz)	
	X8P0M	**X8P0A**
A	0.0028	0.0028
B	0.0065	0.0065

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5M	**X0P5A**	**X0P7M**	**X0P7A**	**X1P0M**	**X1P0A**	**X1P4M**	**X1P4A**
A	0.0012	0.0013	0.0014	0.0015	0.0016	0.0019	0.0025	0.0028
B	0.0010	0.0011	0.0012	0.0014	0.0014	0.0017	0.0024	0.0028

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)							
	X2P0M	**X2P0A**	**X3P0M**	**X3P0A**	**X4P0M**	**X4P0A**	**X6P0M**	**X6P0A**
A	0.0030	0.0035	0.0047	0.0055	0.0062	0.0071	0.0094	0.0108
B	0.0031	0.0036	0.0044	0.0051	0.0060	0.0070	0.0090	0.0105

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)	
	X8P0M	**X8P0A**
A	0.0126	0.0145
B	0.0119	0.0139

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5M	**X0P5A**	**X0P7M**	**X0P7A**	**X1P0M**	**X1P0A**	**X1P4M**	**X1P4A**
A → Y ↑	0.0170	0.0182	0.0151	0.0175	0.0134	0.0156	0.0131	0.0154
A → Y ↓	0.0104	0.0082	0.0096	0.0077	0.0088	0.0071	0.0089	0.0072
B → Y ↑	0.0178	0.0192	0.0164	0.0188	0.0151	0.0174	0.0152	0.0175
B → Y ↓	0.0113	0.0087	0.0107	0.0082	0.0102	0.0078	0.0103	0.0080

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)							
	X2P0M	**X2P0A**	**X3P0M**	**X3P0A**	**X4P0M**	**X4P0A**	**X6P0M**	**X6P0A**
A → Y ↑	0.0115	0.0137	0.0119	0.0139	0.0114	0.0134	0.0114	0.0134
A → Y ↓	0.0081	0.0066	0.0083	0.0068	0.0082	0.0068	0.0082	0.0067
B → Y ↑	0.0141	0.0164	0.0138	0.0159	0.0138	0.0159	0.0136	0.0157
B → Y ↓	0.0098	0.0076	0.0099	0.0076	0.0099	0.0076	0.0099	0.0076

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)	
	X8P0M	**X8P0A**
A → Y ↑	0.0113	0.0133
A → Y ↓	0.0082	0.0067
B → Y ↑	0.0135	0.0156
B → Y ↓	0.0098	0.0076

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X0P5M	**X0P5A**	**X0P7M**	**X0P7A**	**X1P0M**	**X1P0A**	**X1P4M**	**X1P4A**
A → Y ↑	9.5176	9.5228	7.3027	7.3075	5.2675	5.2704	3.5163	3.5183
A → Y ↓	4.5836	2.9842	3.5694	2.1726	2.6058	1.5237	1.8248	1.1151
B → Y ↑	9.5107	9.5136	7.2986	7.3018	5.2652	5.2675	3.5150	3.5166
B → Y ↓	4.5861	2.9874	3.5713	2.1528	2.6071	1.5254	1.7646	1.0695

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X2P0M	**X2P0A**	**X3P0M**	**X3P0A**	**X4P0M**	**X4P0A**	**X6P0M**	**X6P0A**
A → Y ↑	2.5203	2.5216	1.6617	1.6634	1.2215	1.2220	0.8097	0.8102
A → Y ↓	1.3328	0.7755	0.8705	0.5190	0.6579	0.3943	0.4365	0.2614
B → Y ↑	2.5197	2.5206	1.6611	1.6626	1.2212	1.2217	0.8095	0.8099
B → Y ↓	1.2874	0.7515	0.8695	0.5166	0.6467	0.3847	0.4318	0.2574

Delays at 25°C,1.0V, Typical Process (Cont'd.)

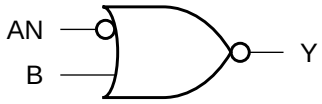
Description	K_{load} (ns/pF)	
	X8P0M	**X8P0A**
A → Y ↑	0.6034	0.6037
A → Y ↓	0.3264	0.1959
B → Y ↑	0.6032	0.6035
B → Y ↓	0.3238	0.1936

Cell Description

The NOR2B cell provides a logical NOR of one inverted input (AN) and one non-inverted input (B). The output (Y) is represented by the logic equation:

$Y = (\overline{\overline{AN} + B})$

Logic Symbol



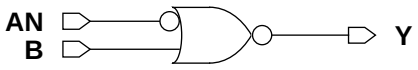
Function Table

AN	B	Y
1	0	1
x	1	0
0	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
NOR2BX0P5MA10TR	2.00	1.20
NOR2BX0P7MA10TR	2.00	1.20
NOR2BX1MA10TR	2.00	1.20
NOR2BX1P4MA10TR	2.00	1.60
NOR2BX2MA10TR	2.00	1.60
NOR2BX3MA10TR	2.00	2.20
NOR2BX4MA10TR	2.00	2.60
NOR2BX6MA10TR	2.00	4.00
NOR2BX8MA10TR	2.00	5.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
AN	0.0017	0.0018	0.0019	0.0025	0.0029	0.0044	0.0056	0.0080	0.0105
B	0.0006	0.0008	0.0010	0.0015	0.0020	0.0030	0.0041	0.0061	0.0081

Pin Capacitance

Pin	Capacitance (pF)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
AN	0.0009	0.0009	0.0009	0.0010	0.0012	0.0016	0.0019	0.0030	0.0035
B	0.0010	0.0012	0.0015	0.0024	0.0030	0.0043	0.0060	0.0090	0.0121

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
AN → Y ↑	0.0310	0.0299	0.0291	0.0297	0.0271	0.0279	0.0289	0.0262	0.0266
AN → Y ↓	0.0348	0.0356	0.0375	0.0391	0.0372	0.0370	0.0369	0.0345	0.0350
B → Y ↑	0.0182	0.0169	0.0158	0.0161	0.0149	0.0149	0.0149	0.0148	0.0149
B → Y ↓	0.0110	0.0104	0.0099	0.0099	0.0095	0.0096	0.0095	0.0095	0.0095

Delays at 25°C,1.0V, Typical Process (Cont'd.)

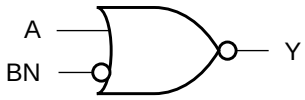
Description	K_{load} (ns/pF)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
AN → Y ↑	9.2557	7.1268	5.1346	3.4937	2.4968	1.6421	1.2241	0.8085	0.6038
AN → Y ↓	4.5632	3.5564	2.5977	1.8244	1.3311	0.8716	0.6599	0.4370	0.3279
B → Y ↑	9.2477	7.1220	5.1322	3.4922	2.4958	1.6415	1.2237	0.8082	0.6036
B → Y ↓	4.4623	3.4841	2.5516	1.7409	1.2759	0.8620	0.6405	0.4283	0.3225

Cell Description

The NOR2XB cell provides a logical NOR of one non-inverted input (A) and one inverted input (BN). The output (Y) is represented by the logic equation:

$Y = \overline{(A + \overline{BN})}$

Logic Symbol



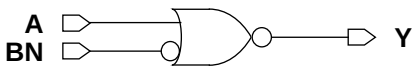
Function Table

A	BN	Y
0	1	1
x	0	0
1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
NOR2XBX0P5MA10TR	2.00	1.20
NOR2XBX0P7MA10TR	2.00	1.20
NOR2XBX1MA10TR	2.00	1.20
NOR2XBX1P4MA10TR	2.00	1.60
NOR2XBX2MA10TR	2.00	1.60
NOR2XBX3MA10TR	2.00	2.20
NOR2XBX4MA10TR	2.00	2.60
NOR2XBX6MA10TR	2.00	4.00
NOR2XBX8MA10TR	2.00	5.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A	0.0004	0.0005	0.0006	0.0009	0.0013	0.0019	0.0026	0.0039	0.0053
BN	0.0016	0.0017	0.0018	0.0024	0.0028	0.0039	0.0051	0.0075	0.0098

Pin Capacitance

Pin	Capacitance (pF)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A	0.0012	0.0014	0.0016	0.0024	0.0030	0.0048	0.0063	0.0092	0.0126
BN	0.0010	0.0010	0.0010	0.0011	0.0012	0.0016	0.0019	0.0030	0.0036

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A → Y ↑	0.0169	0.0149	0.0131	0.0128	0.0113	0.0116	0.0112	0.0109	0.0111
A → Y ↓	0.0105	0.0096	0.0088	0.0088	0.0082	0.0083	0.0081	0.0081	0.0082
BN → Y ↑	0.0313	0.0306	0.0308	0.0328	0.0306	0.0294	0.0316	0.0290	0.0293
BN → Y ↓	0.0347	0.0358	0.0383	0.0416	0.0396	0.0377	0.0387	0.0365	0.0367

Delays at 25°C,1.0V, Typical Process (Cont'd.)

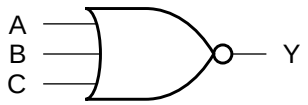
Description	K_{load} (ns/pF)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A → Y ↑	9.2530	7.1158	5.1337	3.4812	2.5001	1.6415	1.2178	0.8033	0.6011
A → Y ↓	4.5434	3.5417	2.5848	1.8133	1.3240	0.8671	0.6561	0.4348	0.3257
BN → Y ↑	9.2448	7.1107	5.1312	3.4805	2.4997	1.6410	1.2176	0.8032	0.6010
BN → Y ↓	4.4713	3.4956	2.5594	1.7520	1.2766	0.8632	0.6428	0.4297	0.3232

Cell Description

The NOR3 cell provides a logical NOR of three inputs (A,B,C). The output (Y) is represented by the logic equation:

$Y = \overline{(A + B + C)}$

Logic Symbol



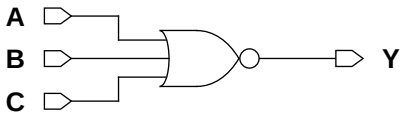
Function Table

A	B	C	Y
0	0	0	1
x	x	1	0
x	1	x	0
1	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
NOR3X0P5MA10TR	2.00	1.20
NOR3X0P5AA10TR	2.00	1.20
NOR3X0P7MA10TR	2.00	1.20
NOR3X0P7AA10TR	2.00	1.20
NOR3X1MA10TR	2.00	1.20
NOR3X1AA10TR	2.00	1.20
NOR3X1P4MA10TR	2.00	1.80
NOR3X1P4AA10TR	2.00	2.00
NOR3X2MA10TR	2.00	2.00
NOR3X2AA10TR	2.00	2.00
NOR3X3MA10TR	2.00	2.60
NOR3X3AA10TR	2.00	2.60
NOR3X4MA10TR	2.00	3.80
NOR3X4AA10TR	2.00	3.80

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P5M	**X0P5A**	**X0P7M**	**X0P7A**	**X1P0M**	**X1P0A**	**X1P4M**	**X1P4A**
A	0.0001	0.0001	0.0002	0.0002	0.0003	0.0003	0.0004	0.0004
B	0.0001	0.0001	0.0002	0.0002	0.0003	0.0003	0.0004	0.0004
C	0.0004	0.0004	0.0005	0.0005	0.0007	0.0007	0.0010	0.0010

AC Power (Cont'd.)

Pin	Power (uW/MHz)					
	X2P0M	**X2P0A**	**X3P0M**	**X3P0A**	**X4P0M**	**X4P0A**
A	0.0005	0.0005	0.0010	0.0010	0.0016	0.0016
B	0.0005	0.0005	0.0009	0.0009	0.0013	0.0013
C	0.0014	0.0014	0.0023	0.0023	0.0031	0.0031

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5M	**X0P5A**	**X0P7M**	**X0P7A**	**X1P0M**	**X1P0A**	**X1P4M**	**X1P4A**
A	0.0012	0.0012	0.0013	0.0014	0.0016	0.0018	0.0021	0.0026
B	0.0010	0.0010	0.0011	0.0013	0.0014	0.0016	0.0021	0.0025
C	0.0010	0.0011	0.0012	0.0013	0.0014	0.0016	0.0022	0.0027

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)					
	X2P0M	**X2P0A**	**X3P0M**	**X3P0A**	**X4P0M**	**X4P0A**
A	0.0029	0.0032	0.0043	0.0050	0.0058	0.0067
B	0.0028	0.0032	0.0042	0.0048	0.0055	0.0064
C	0.0030	0.0033	0.0041	0.0048	0.0055	0.0064

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5M	**X0P5A**	**X0P7M**	**X0P7A**	**X1P0M**	**X1P0A**	**X1P4M**	**X1P4A**
A → Y ↑	0.0288	0.0300	0.0228	0.0255	0.0193	0.0234	0.0165	0.0211
A → Y ↓	0.0119	0.0105	0.0128	0.0094	0.0118	0.0089	0.0112	0.0084
B → Y ↑	0.0317	0.0330	0.0266	0.0294	0.0238	0.0280	0.0220	0.0269
B → Y ↓	0.0127	0.0111	0.0144	0.0102	0.0139	0.0099	0.0139	0.0099
C → Y ↑	0.0344	0.0357	0.0292	0.0320	0.0265	0.0307	0.0247	0.0294
C → Y ↓	0.0142	0.0122	0.0165	0.0113	0.0161	0.0110	0.0161	0.0107

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)					
	X2P0M	**X2P0A**	**X3P0M**	**X3P0A**	**X4P0M**	**X4P0A**
A → Y ↑	0.0158	0.0186	0.0151	0.0190	0.0144	0.0181
A → Y ↓	0.0103	0.0077	0.0108	0.0084	0.0105	0.0081
B → Y ↑	0.0217	0.0246	0.0225	0.0265	0.0225	0.0262
B → Y ↓	0.0132	0.0092	0.0143	0.0102	0.0142	0.0099
C → Y ↑	0.0242	0.0271	0.0256	0.0295	0.0259	0.0296
C → Y ↓	0.0151	0.0101	0.0168	0.0112	0.0169	0.0110

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X0P5M	**X0P5A**	**X0P7M**	**X0P7A**	**X1P0M**	**X1P0A**	**X1P4M**	**X1P4A**
A → Y ↑	14.6818	14.6849	10.7376	10.7413	7.7385	7.7411	5.3817	5.3510
A → Y ↓	4.5448	3.6979	4.5441	2.7095	3.4612	1.9567	2.6063	1.3862
B → Y ↑	14.6726	14.6737	10.7331	10.7359	7.7352	7.7376	5.3797	5.3497
B → Y ↓	4.5103	3.6674	4.5091	2.6794	3.4265	1.9344	2.5920	1.3921
C → Y ↑	14.6728	14.6748	10.7330	10.7357	7.7357	7.7383	5.3804	5.3499
C → Y ↓	4.5572	3.7105	4.5533	2.7175	3.4677	1.9613	2.5421	1.3701

Delays at 25°C,1.0V, Typical Process (Cont'd.)

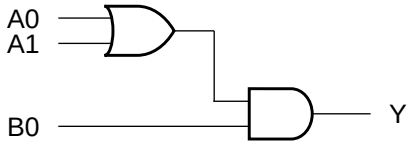
Description	K_{load} (ns/pF)					
	X2P0M	**X2P0A**	**X3P0M**	**X3P0A**	**X4P0M**	**X4P0A**
A → Y ↑	3.8309	3.8323	2.3905	2.3916	1.7847	1.7855
A → Y ↓	1.7453	0.9852	1.1817	0.6710	0.8736	0.4878
B → Y ↑	3.8301	3.8313	2.3896	2.3904	1.7841	1.7847
B → Y ↓	1.7524	0.9886	1.1659	0.6619	0.8696	0.4851
C → Y ↑	3.8299	3.8311	2.3896	2.3903	1.7842	1.7846
C → Y ↓	1.7200	0.9752	1.1735	0.6659	0.8766	0.4900

Cell Description

The OA21 cell provides the logical AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$Y = (A0 + A1) \bullet B0$

Logic Symbol



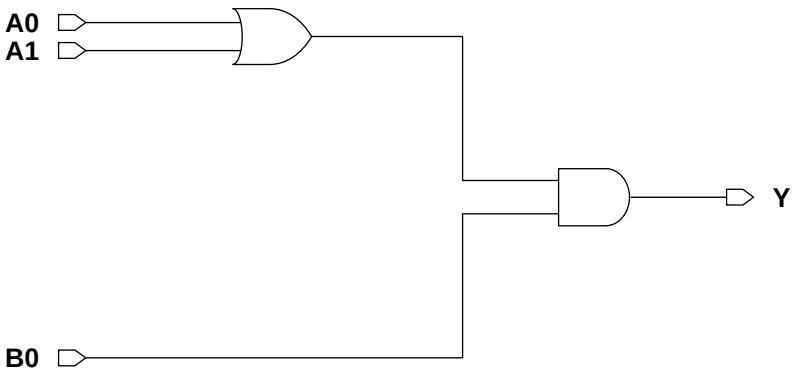
Function Table

A0	A1	B0	Y
x	x	0	0
0	0	x	0
x	1	1	1
1	x	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
OA21X0P5MA10TR	2.00	1.60
OA21X0P7MA10TR	2.00	1.60
OA21X1MA10TR	2.00	1.60
OA21X1P4MA10TR	2.00	2.60
OA21X2MA10TR	2.00	2.60
OA21X3MA10TR	2.00	3.40
OA21X4MA10TR	2.00	4.00
OA21X6MA10TR	2.00	5.60
OA21X8MA10TR	2.00	7.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0	0.0002	0.0003	0.0004	0.0006	0.0008	0.0013	0.0017	0.0031	0.0040
A1	0.0005	0.0007	0.0008	0.0012	0.0016	0.0023	0.0031	0.0050	0.0068
B0	0.0006	0.0007	0.0008	0.0011	0.0014	0.0021	0.0028	0.0042	0.0055

Pin Capacitance

Pin	Capacitance (pF)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0	0.0012	0.0013	0.0016	0.0022	0.0027	0.0041	0.0050	0.0073	0.0100
A1	0.0011	0.0012	0.0015	0.0024	0.0028	0.0039	0.0048	0.0070	0.0096
B0	0.0011	0.0012	0.0014	0.0017	0.0021	0.0029	0.0037	0.0054	0.0069

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0 → Y ↑	0.0358	0.0346	0.0327	0.0336	0.0310	0.0312	0.0306	0.0300	0.0301
A0 → Y ↓	0.0491	0.0472	0.0456	0.0459	0.0420	0.0421	0.0415	0.0388	0.0391
A1 → Y ↑	0.0383	0.0375	0.0356	0.0361	0.0335	0.0336	0.0333	0.0343	0.0345
A1 → Y ↓	0.0510	0.0494	0.0479	0.0481	0.0444	0.0442	0.0436	0.0425	0.0428
B0 → Y ↑	0.0348	0.0339	0.0318	0.0317	0.0295	0.0296	0.0299	0.0301	0.0304
B0 → Y ↓	0.0380	0.0376	0.0370	0.0391	0.0361	0.0350	0.0353	0.0352	0.0358

Delays at 25°C,1.0V, Typical Process (Cont'd.)

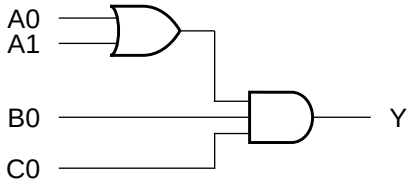
Description	K_{load} (ns/pF)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0 → Y ↑	4.6981	3.3651	2.4062	1.6539	1.1790	0.7855	0.5837	0.3855	0.2871
A0 → Y ↓	2.9121	2.0965	1.4716	1.0381	0.7236	0.4912	0.3637	0.2421	0.1824
A1 → Y ↑	4.7044	3.3697	2.4091	1.6558	1.1804	0.7864	0.5845	0.3864	0.2878
A1 → Y ↓	2.9121	2.0965	1.4717	1.0381	0.7236	0.4912	0.3637	0.2421	0.1824
B0 → Y ↑	4.7042	3.3697	2.4091	1.6558	1.1804	0.7864	0.5845	0.3864	0.2878
B0 → Y ↓	2.8888	2.0843	1.4658	1.0382	0.7244	0.4909	0.3638	0.2440	0.1840

Cell Description

The OA211 cell provides the logical OR of one OR group and two additional inputs. The output (Y) is represented by the logic equation:

$Y = (A0 + A1) \bullet B0 \bullet C0$

Logic Symbol



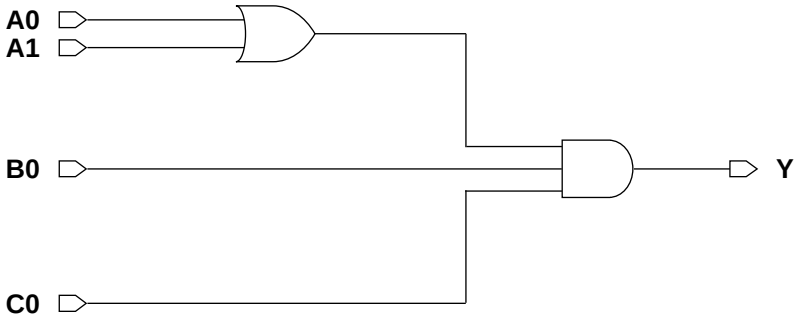
Function Table

A0	A1	B0	C0	Y
0	0	x	x	0
x	x	0	x	0
x	x	x	0	0
x	1	1	1	1
1	x	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
OA211X0P5MA10TR	2.00	1.80
OA211X0P7MA10TR	2.00	1.80
OA211X1MA10TR	2.00	2.40
OA211X1P4MA10TR	2.00	3.00
OA211X2MA10TR	2.00	3.20
OA211X3MA10TR	2.00	4.40
OA211X4MA10TR	2.00	5.60
OA211X6MA10TR	2.00	8.20

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A0	0.0004	0.0004	0.0006	0.0009	0.0011	0.0016	0.0021	0.0032
A1	0.0007	0.0008	0.0011	0.0015	0.0018	0.0026	0.0034	0.0051
B0	0.0006	0.0007	0.0008	0.0012	0.0016	0.0022	0.0030	0.0044
C0	0.0007	0.0008	0.0010	0.0012	0.0016	0.0023	0.0031	0.0046

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A0	0.0015	0.0017	0.0023	0.0030	0.0033	0.0050	0.0066	0.0102
A1	0.0014	0.0016	0.0024	0.0030	0.0034	0.0048	0.0064	0.0097
B0	0.0013	0.0014	0.0016	0.0024	0.0029	0.0038	0.0054	0.0078
C0	0.0013	0.0015	0.0018	0.0023	0.0028	0.0040	0.0053	0.0079

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A0 → Y ↑	0.0405	0.0388	0.0377	0.0368	0.0369	0.0378	0.0367	0.0369
A0 → Y ↓	0.0520	0.0503	0.0483	0.0465	0.0480	0.0480	0.0466	0.0472
A1 → Y ↑	0.0441	0.0426	0.0401	0.0394	0.0393	0.0407	0.0393	0.0397
A1 → Y ↓	0.0542	0.0526	0.0503	0.0487	0.0504	0.0500	0.0487	0.0492
B0 → Y ↑	0.0407	0.0392	0.0361	0.0358	0.0360	0.0373	0.0361	0.0362
B0 → Y ↓	0.0429	0.0422	0.0421	0.0407	0.0402	0.0419	0.0408	0.0415
C0 → Y ↑	0.0384	0.0367	0.0339	0.0329	0.0333	0.0347	0.0333	0.0335
C0 → Y ↓	0.0396	0.0387	0.0385	0.0364	0.0365	0.0381	0.0365	0.0373

Delays at 25°C,1.0V, Typical Process (Cont'd.)

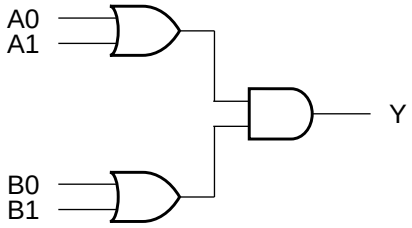
Description	K_{load} (ns/pF)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A0 → Y ↑	4.5836	3.3532	2.4006	1.6535	1.1807	0.7874	0.5853	0.3885
A0 → Y ↓	2.9097	2.1237	1.4986	1.0372	0.7282	0.5041	0.3728	0.2456
A1 → Y ↑	4.5917	3.3593	2.4037	1.6559	1.1821	0.7886	0.5862	0.3892
A1 → Y ↓	2.9099	2.1237	1.4985	1.0371	0.7282	0.5041	0.3728	0.2456
B0 → Y ↑	4.5917	3.3593	2.4036	1.6558	1.1821	0.7886	0.5862	0.3892
B0 → Y ↓	2.8914	2.1133	1.4976	1.0366	0.7255	0.5037	0.3726	0.2456
C0 → Y ↑	4.5917	3.3594	2.4036	1.6559	1.1821	0.7887	0.5862	0.3892
C0 → Y ↓	2.8848	2.1089	1.4936	1.0337	0.7239	0.5025	0.3715	0.2449

Cell Description

The OA22 cell provides the logical AND of two OR groups. The output (Y) is represented by the logic equation:

$Y = (A0 + A1) \bullet (B0 + B1)$

Logic Symbol



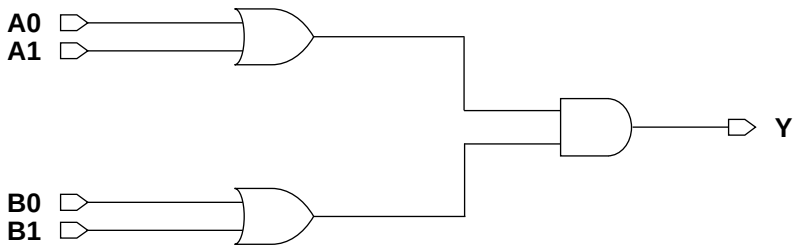
Function Table

A0	A1	B0	B1	Y
x	x	0	0	0
0	0	x	x	0
x	1	x	1	1
x	1	1	x	1
1	x	x	1	1
1	x	1	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
OA22X0P5MA10TR	2.00	2.00
OA22X0P7MA10TR	2.00	2.00
OA22X1MA10TR	2.00	2.00
OA22X1P4MA10TR	2.00	3.20
OA22X2MA10TR	2.00	3.20
OA22X3MA10TR	2.00	4.40
OA22X4MA10TR	2.00	4.80
OA22X6MA10TR	2.00	7.40
OA22X8MA10TR	2.00	9.20

Functional Schematic



AC Power

Pin	Power (uW/MHz)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0	0.0002	0.0003	0.0004	0.0006	0.0008	0.0013	0.0018	0.0027	0.0038
A1	0.0005	0.0006	0.0008	0.0012	0.0016	0.0025	0.0033	0.0051	0.0068
B0	0.0002	0.0003	0.0004	0.0006	0.0008	0.0014	0.0018	0.0027	0.0039
B1	0.0005	0.0006	0.0008	0.0011	0.0016	0.0026	0.0033	0.0051	0.0068

Pin Capacitance

Pin	Capacitance (pF)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0	0.0012	0.0013	0.0016	0.0024	0.0030	0.0043	0.0052	0.0080	0.0106
A1	0.0011	0.0012	0.0015	0.0023	0.0029	0.0042	0.0051	0.0078	0.0101
B0	0.0012	0.0014	0.0016	0.0024	0.0030	0.0043	0.0051	0.0079	0.0104
B1	0.0012	0.0013	0.0015	0.0024	0.0030	0.0041	0.0050	0.0078	0.0101

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0 → Y ↑	0.0410	0.0396	0.0373	0.0391	0.0362	0.0390	0.0369	0.0375	0.0361
A0 → Y ↓	0.0596	0.0574	0.0553	0.0573	0.0537	0.0539	0.0511	0.0511	0.0501
A1 → Y ↑	0.0430	0.0418	0.0396	0.0410	0.0382	0.0421	0.0399	0.0406	0.0399
A1 → Y ↓	0.0614	0.0593	0.0573	0.0591	0.0556	0.0572	0.0543	0.0543	0.0537
B0 → Y ↑	0.0355	0.0344	0.0319	0.0343	0.0314	0.0340	0.0325	0.0330	0.0323
B0 → Y ↓	0.0469	0.0455	0.0431	0.0462	0.0425	0.0433	0.0415	0.0415	0.0409
B1 → Y ↑	0.0378	0.0370	0.0346	0.0362	0.0335	0.0373	0.0356	0.0362	0.0358
B1 → Y ↓	0.0493	0.0482	0.0458	0.0482	0.0448	0.0468	0.0448	0.0449	0.0445

Delays at 25°C,1.0V, Typical Process (Cont'd.)

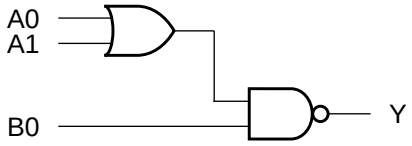
Description	K_{load} (ns/pF)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A0 → Y ↑	4.6940	3.3624	2.4041	1.6460	1.1800	0.7887	0.5851	0.3885	0.2906
A0 → Y ↓	2.9788	2.1413	1.5015	1.0628	0.7401	0.5068	0.3732	0.2497	0.1880
A1 → Y ↑	4.6984	3.3655	2.4063	1.6474	1.1810	0.7900	0.5861	0.3891	0.2912
A1 → Y ↓	2.9784	2.1413	1.5013	1.0627	0.7400	0.5068	0.3731	0.2497	0.1879
B0 → Y ↑	4.6937	3.3621	2.4039	1.6459	1.1799	0.7887	0.5851	0.3884	0.2907
B0 → Y ↓	2.9436	2.1181	1.4848	1.0526	0.7328	0.5025	0.3702	0.2477	0.1865
B1 → Y ↑	4.6982	3.3654	2.4063	1.6474	1.1810	0.7900	0.5860	0.3890	0.2912
B1 → Y ↓	2.9435	2.1180	1.4848	1.0526	0.7328	0.5024	0.3702	0.2477	0.1865

Cell Description

The OAI21 cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$Y = \overline{(A0 + A1) \bullet B0}$

Logic Symbol



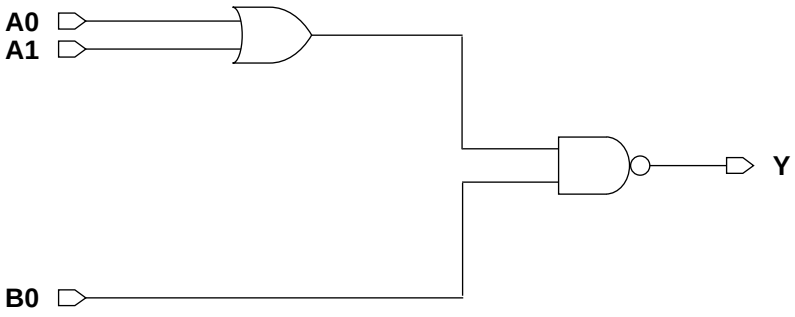
Function Table

A0	A1	B0	Y
0	0	x	1
x	x	0	1
x	1	1	0
1	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI21X0P5MA10TR	2.00	1.20
OAI21X0P7MA10TR	2.00	1.20
OAI21X1MA10TR	2.00	1.20
OAI21X1P4MA10TR	2.00	2.00
OAI21X2MA10TR	2.00	2.00
OAI21X3MA10TR	2.00	2.60
OAI21X4MA10TR	2.00	3.40
OAI21X6MA10TR	2.00	5.00
OAI21X8MA10TR	2.00	6.60

Functional Schematic



AC Power

Pin	Power (uW/MHz)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0	0.0002	0.0003	0.0004	0.0005	0.0007	0.0011	0.0020	0.0030	0.0040
A1	0.0005	0.0006	0.0008	0.0012	0.0016	0.0024	0.0035	0.0052	0.0070
B0	0.0005	0.0006	0.0008	0.0011	0.0015	0.0022	0.0029	0.0043	0.0058

Pin Capacitance

Pin	Capacitance (pF)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0	0.0012	0.0014	0.0018	0.0027	0.0034	0.0053	0.0069	0.0103	0.0138
A1	0.0011	0.0013	0.0016	0.0027	0.0034	0.0050	0.0065	0.0098	0.0131
B0	0.0011	0.0013	0.0016	0.0021	0.0027	0.0039	0.0052	0.0077	0.0102

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0 → Y ↑	0.0250	0.0222	0.0217	0.0210	0.0193	0.0196	0.0180	0.0177	0.0178
A0 → Y ↓	0.0153	0.0139	0.0135	0.0135	0.0125	0.0127	0.0125	0.0123	0.0123
A1 → Y ↑	0.0267	0.0241	0.0237	0.0233	0.0217	0.0216	0.0216	0.0212	0.0212
A1 → Y ↓	0.0171	0.0159	0.0155	0.0155	0.0146	0.0147	0.0156	0.0154	0.0155
B0 → Y ↑	0.0147	0.0136	0.0131	0.0123	0.0116	0.0118	0.0115	0.0110	0.0111
B0 → Y ↓	0.0138	0.0128	0.0122	0.0112	0.0105	0.0112	0.0116	0.0114	0.0115

Delays at 25°C,1.0V, Typical Process (Cont'd.)

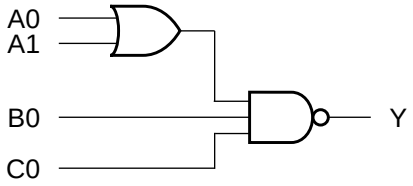
Description	K_{load} (ns/pF)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0 → Y ↑	9.7774	7.1445	5.1387	3.4458	2.4717	1.6398	1.1698	0.7755	0.5805
A0 → Y ↓	5.8418	4.3169	3.0550	2.1345	1.5197	1.0170	0.7626	0.5098	0.3833
A1 → Y ↑	9.7744	7.1427	5.1374	3.4452	2.4710	1.6395	1.1695	0.7753	0.5804
A1 → Y ↓	5.8421	4.3363	3.0582	2.1116	1.4989	1.0160	0.7690	0.5155	0.3890
B0 → Y ↑	7.5334	5.7589	4.1868	2.8996	2.0837	1.3809	1.0611	0.6958	0.5226
B0 → Y ↓	5.8446	4.3385	3.0591	2.1213	1.5104	1.0161	0.7692	0.5156	0.3891

Cell Description

The OAI211 cell provides the logical inverted OR of one OR group and two additional inputs. The output (Y) is represented by the logic equation:

$Y = \overline{(A0 + A1) \bullet B0 \bullet C0}$

Logic Symbol



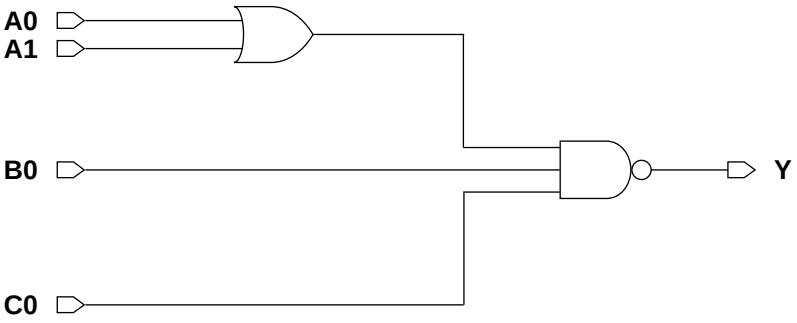
Function Table

A0	A1	B0	C0	Y
0	0	x	x	1
x	x	0	x	1
x	x	x	0	1
x	1	1	1	0
1	x	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI211X0P5MA10TR	2.00	1.40
OAI211X0P7MA10TR	2.00	1.40
OAI211X1MA10TR	2.00	1.40
OAI211X1P4MA10TR	2.00	2.40
OAI211X2MA10TR	2.00	2.40
OAI211X3MA10TR	2.00	3.40
OAI211X4MA10TR	2.00	4.40

Functional Schematic



AC Power

Pin	Power (uW/MHz)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A0	0.0002	0.0003	0.0004	0.0006	0.0008	0.0013	0.0017
A1	0.0004	0.0006	0.0007	0.0011	0.0014	0.0021	0.0028
B0	0.0004	0.0005	0.0006	0.0009	0.0013	0.0018	0.0026
C0	0.0005	0.0006	0.0007	0.0010	0.0014	0.0021	0.0028

Pin Capacitance

Pin	Capacitance (pF)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A0	0.0011	0.0014	0.0018	0.0029	0.0035	0.0054	0.0072
A1	0.0011	0.0014	0.0017	0.0028	0.0035	0.0052	0.0069
B0	0.0010	0.0012	0.0015	0.0023	0.0031	0.0042	0.0059
C0	0.0011	0.0014	0.0017	0.0022	0.0030	0.0045	0.0061

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A0 → Y ↑	0.0342	0.0328	0.0304	0.0298	0.0289	0.0281	0.0277
A0 → Y ↓	0.0214	0.0199	0.0182	0.0184	0.0175	0.0175	0.0171
A1 → Y ↑	0.0359	0.0348	0.0326	0.0315	0.0312	0.0299	0.0296
A1 → Y ↓	0.0236	0.0222	0.0206	0.0202	0.0195	0.0194	0.0191
B0 → Y ↑	0.0199	0.0194	0.0182	0.0184	0.0177	0.0177	0.0175
B0 → Y ↓	0.0199	0.0182	0.0169	0.0161	0.0155	0.0162	0.0158
C0 → Y ↑	0.0180	0.0173	0.0156	0.0147	0.0142	0.0146	0.0139
C0 → Y ↓	0.0182	0.0164	0.0147	0.0132	0.0128	0.0138	0.0131

Delays at 25°C,1.0V, Typical Process (Cont'd.)

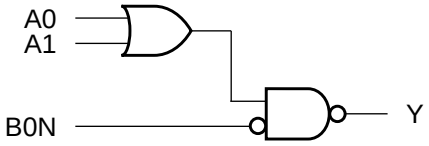
Description	K_{load} (ns/pF)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A0 → Y ↑	10.1188	7.3870	5.3594	3.6008	2.6269	1.7066	1.2736
A0 → Y ↓	7.1755	5.1065	3.6008	2.5215	1.7802	1.1829	0.8820
A1 → Y ↑	10.1173	7.3857	5.3591	3.5998	2.6265	1.7063	1.2733
A1 → Y ↓	7.1851	5.0985	3.6084	2.4918	1.7483	1.1816	0.8751
B0 → Y ↑	7.7525	5.9581	4.3208	3.0837	2.1441	1.4332	1.0644
B0 → Y ↓	7.1850	5.0991	3.6094	2.5060	1.7705	1.1818	0.8768
C0 → Y ↑	8.0195	6.1724	4.4777	3.1265	2.1693	1.4531	1.0716
C0 → Y ↓	7.1866	5.1000	3.6093	2.5059	1.7702	1.1819	0.8768

Cell Description

The OAI21B cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet \overline{B0N}}$$

Logic Symbol



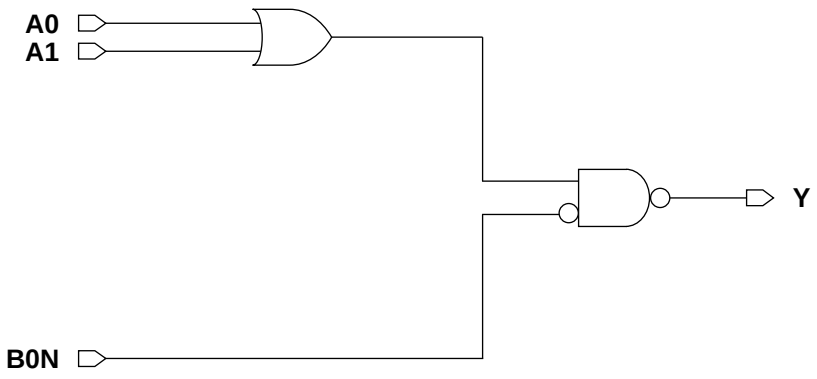
Function Table

A0	A1	B0N	Y
0	0	x	1
x	x	1	1
x	1	0	0
1	x	0	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI21BX0P5MA10TR	2.00	1.60
OAI21BX0P7MA10TR	2.00	1.60
OAI21BX1MA10TR	2.00	1.60
OAI21BX1P4MA10TR	2.00	2.40
OAI21BX2MA10TR	2.00	2.40
OAI21BX3MA10TR	2.00	3.20
OAI21BX4MA10TR	2.00	4.00
OAI21BX6MA10TR	2.00	5.80
OAI21BX8MA10TR	2.00	7.40

Functional Schematic



AC Power

Pin	Power (uW/MHz)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0	0.0003	0.0004	0.0005	0.0009	0.0013	0.0016	0.0021	0.0033	0.0044
A1	0.0004	0.0006	0.0008	0.0014	0.0018	0.0026	0.0036	0.0054	0.0072
B0N	0.0016	0.0018	0.0020	0.0027	0.0035	0.0049	0.0063	0.0093	0.0122

Pin Capacitance

Pin	Capacitance (pF)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0	0.0012	0.0015	0.0019	0.0027	0.0035	0.0052	0.0069	0.0102	0.0135
A1	0.0010	0.0013	0.0017	0.0027	0.0034	0.0050	0.0067	0.0099	0.0133
B0N	0.0009	0.0009	0.0009	0.0009	0.0011	0.0015	0.0018	0.0028	0.0035

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0 → Y ↑	0.0255	0.0236	0.0218	0.0198	0.0187	0.0185	0.0184	0.0181	0.0177
A0 → Y ↓	0.0170	0.0164	0.0158	0.0164	0.0155	0.0153	0.0152	0.0150	0.0149
A1 → Y ↑	0.0268	0.0252	0.0236	0.0243	0.0229	0.0219	0.0219	0.0215	0.0212
A1 → Y ↓	0.0187	0.0184	0.0178	0.0202	0.0190	0.0184	0.0185	0.0182	0.0181
B0N → Y ↑	0.0289	0.0288	0.0300	0.0292	0.0293	0.0285	0.0273	0.0264	0.0257
B0N → Y ↓	0.0353	0.0355	0.0378	0.0381	0.0392	0.0374	0.0366	0.0345	0.0343

Delays at 25°C,1.0V, Typical Process (Cont'd.)

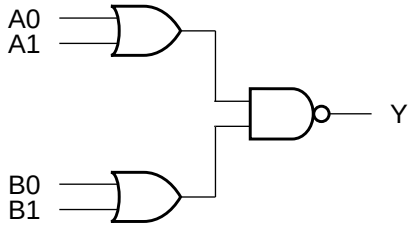
Description	K_{load} (ns/pF)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0 → Y ↑	9.7292	7.0941	5.1062	3.2787	2.3664	1.5656	1.1747	0.7790	0.5830
A0 → Y ↓	5.8112	4.2961	3.0176	2.1325	1.4927	1.0004	0.7386	0.4944	0.3723
A1 → Y ↑	9.7247	7.0916	5.1045	3.2777	2.3657	1.5651	1.1743	0.7788	0.5829
A1 → Y ↓	5.8179	4.2903	3.0237	2.1428	1.5030	1.0084	0.7527	0.5038	0.3804
B0N → Y ↑	7.3611	5.6233	4.0686	3.0156	2.0517	1.3884	1.0263	0.6882	0.5130
B0N → Y ↓	5.8223	4.2915	3.0245	2.1433	1.5034	1.0087	0.7531	0.5037	0.3804

Cell Description

The OAI22 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet (B0 + B1)}$$

Logic Symbol



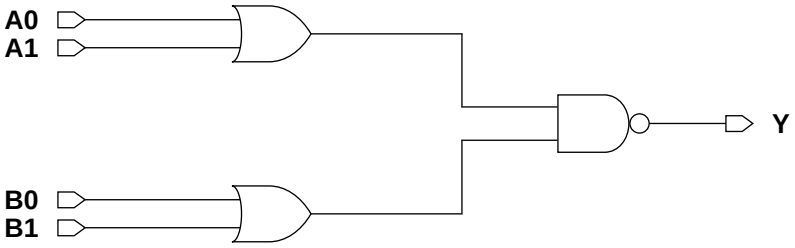
Function Table

A0	A1	B0	B1	Y
0	0	x	x	1
x	x	0	0	1
x	1	x	1	0
x	1	1	x	0
1	x	x	1	0
1	x	1	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI22X0P5MA10TR	2.00	1.40
OAI22X0P7MA10TR	2.00	1.40
OAI22X1MA10TR	2.00	1.40
OAI22X1P4MA10TR	2.00	2.40
OAI22X2MA10TR	2.00	2.40
OAI22X3MA10TR	2.00	3.40
OAI22X4MA10TR	2.00	4.80
OAI22X6MA10TR	2.00	6.80
OAI22X8MA10TR	2.00	9.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A0	0.0002	0.0002	0.0003	0.0005	0.0007	0.0012	0.0018	0.0027	0.0035
A1	0.0005	0.0006	0.0008	0.0012	0.0016	0.0028	0.0038	0.0057	0.0077
B0	0.0002	0.0002	0.0003	0.0005	0.0007	0.0012	0.0019	0.0027	0.0035
B1	0.0004	0.0006	0.0008	0.0011	0.0016	0.0028	0.0037	0.0056	0.0075

Pin Capacitance

Pin	Capacitance (pF)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A0	0.0012	0.0014	0.0018	0.0027	0.0034	0.0052	0.0070	0.0105	0.0140
A1	0.0011	0.0013	0.0017	0.0027	0.0034	0.0051	0.0067	0.0100	0.0133
B0	0.0012	0.0014	0.0018	0.0027	0.0034	0.0052	0.0070	0.0103	0.0139
B1	0.0011	0.0014	0.0017	0.0027	0.0035	0.0051	0.0067	0.0100	0.0135

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A0 → Y ↑	0.0326	0.0291	0.0270	0.0282	0.0260	0.0252	0.0242	0.0239	0.0241
A0 → Y ↓	0.0214	0.0195	0.0183	0.0190	0.0177	0.0188	0.0183	0.0182	0.0181
A1 → Y ↑	0.0339	0.0311	0.0289	0.0302	0.0283	0.0284	0.0279	0.0275	0.0275
A1 → Y ↓	0.0228	0.0215	0.0202	0.0207	0.0195	0.0212	0.0215	0.0214	0.0213
B0 → Y ↑	0.0205	0.0173	0.0163	0.0181	0.0164	0.0163	0.0155	0.0155	0.0155
B0 → Y ↓	0.0156	0.0137	0.0132	0.0143	0.0130	0.0143	0.0143	0.0144	0.0144
B1 → Y ↑	0.0229	0.0205	0.0190	0.0203	0.0190	0.0195	0.0191	0.0190	0.0189
B1 → Y ↓	0.0175	0.0164	0.0154	0.0161	0.0149	0.0170	0.0172	0.0173	0.0172

Delays at 25°C,1.0V, Typical Process (Cont'd.)

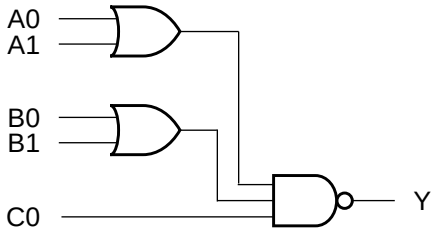
Description	K_{load} (ns/pF)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A0 → Y ↑	9.5980	7.0148	5.0338	3.4321	2.4760	1.5658	1.1686	0.7778	0.5832
A0 → Y ↓	5.7959	4.2836	3.0245	2.1279	1.4945	0.9982	0.7484	0.5038	0.3773
A1 → Y ↑	9.5945	7.0132	5.0325	3.4314	2.4756	1.5655	1.1680	0.7775	0.5830
A1 → Y ↓	5.7439	4.2498	3.0023	2.1125	1.4810	0.9951	0.7526	0.5086	0.3827
B0 → Y ↑	9.3820	6.8669	4.9141	3.4348	2.4764	1.5662	1.1723	0.7783	0.5827
B0 → Y ↓	5.7541	4.2376	2.9849	2.1281	1.4942	1.0024	0.7560	0.5125	0.3856
B1 → Y ↑	9.3788	6.8661	4.9126	3.4339	2.4760	1.5657	1.1717	0.7779	0.5825
B1 → Y ↓	5.7592	4.2576	3.0064	2.1065	1.4852	0.9916	0.7526	0.5085	0.3819

Cell Description

The OAI221 cell provides the logical inverted AND of two OR groups and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet (B0 + B1) \bullet C0}$$

Logic Symbol



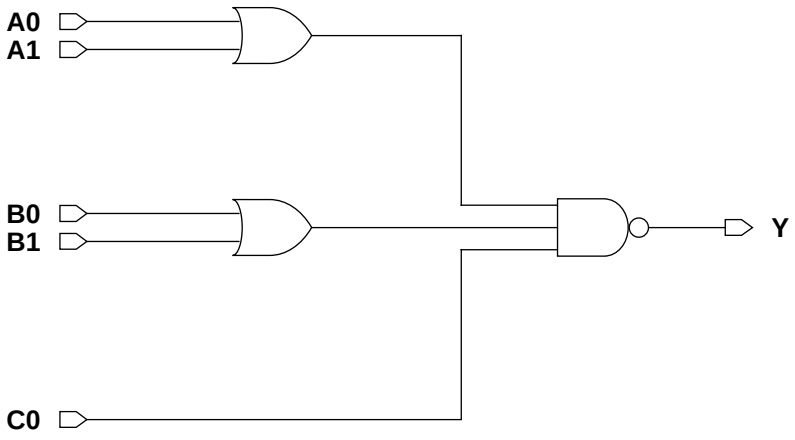
Function Table

A0	A1	B0	B1	C0	Y
0	0	x	x	x	1
x	x	0	0	x	1
x	x	x	x	0	1
x	1	x	1	1	0
x	1	1	x	1	0
1	x	x	1	1	0
1	x	1	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI221X0P5MA10TR	2.00	2.00
OAI221X0P7MA10TR	2.00	2.00
OAI221X1MA10TR	2.00	2.00
OAI221X1P4MA10TR	2.00	3.20
OAI221X2MA10TR	2.00	3.20
OAI221X3MA10TR	2.00	4.60
OAI221X4MA10TR	2.00	5.80

Functional Schematic



AC Power

Pin	Power (uW/MHz)						
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M
A0	0.0002	0.0002	0.0003	0.0005	0.0007	0.0011	0.0015
A1	0.0004	0.0006	0.0008	0.0012	0.0016	0.0023	0.0033
B0	0.0002	0.0003	0.0004	0.0005	0.0007	0.0011	0.0015
B1	0.0004	0.0006	0.0008	0.0012	0.0017	0.0024	0.0033
C0	0.0005	0.0006	0.0008	0.0011	0.0015	0.0022	0.0030

Pin Capacitance

Pin	Capacitance (pF)						
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M
A0	0.0012	0.0015	0.0018	0.0029	0.0036	0.0055	0.0072
A1	0.0011	0.0014	0.0017	0.0029	0.0036	0.0051	0.0070
B0	0.0012	0.0014	0.0018	0.0027	0.0035	0.0054	0.0070
B1	0.0011	0.0014	0.0017	0.0029	0.0036	0.0051	0.0070
C0	0.0010	0.0012	0.0015	0.0023	0.0029	0.0042	0.0057

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)						
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M
A0 → Y ↑	0.0425	0.0395	0.0378	0.0383	0.0358	0.0349	0.0348
A0 → Y ↓	0.0282	0.0258	0.0247	0.0250	0.0232	0.0236	0.0236
A1 → Y ↑	0.0444	0.0417	0.0400	0.0403	0.0379	0.0368	0.0369
A1 → Y ↓	0.0306	0.0283	0.0272	0.0268	0.0250	0.0258	0.0256
B0 → Y ↑	0.0316	0.0283	0.0273	0.0275	0.0257	0.0248	0.0250
B0 → Y ↓	0.0238	0.0213	0.0205	0.0204	0.0190	0.0196	0.0192
B1 → Y ↑	0.0343	0.0309	0.0296	0.0301	0.0283	0.0270	0.0275
B1 → Y ↓	0.0268	0.0242	0.0232	0.0229	0.0213	0.0220	0.0216
C0 → Y ↑	0.0190	0.0178	0.0171	0.0163	0.0153	0.0156	0.0156
C0 → Y ↓	0.0195	0.0177	0.0172	0.0158	0.0146	0.0164	0.0157

Delays at 25°C,1.0V, Typical Process (Cont'd.)

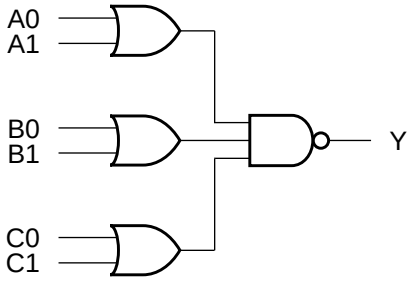
Description	K_{load} (ns/pF)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A0 → Y ↑	9.9093	7.2358	5.2330	3.6272	2.5982	1.7108	1.2819
A0 → Y ↓	6.7974	4.8643	3.4757	2.4531	1.7386	1.1808	0.8832
A1 → Y ↑	9.9081	7.2350	5.2324	3.6268	2.5979	1.7106	1.2818
A1 → Y ↓	6.8408	4.8963	3.4989	2.4110	1.7067	1.1781	0.8709
B0 → Y ↑	9.7982	7.1447	5.1762	3.5413	2.5553	1.6836	1.2611
B0 → Y ↓	6.7955	4.8405	3.4520	2.4544	1.7394	1.1783	0.8831
B1 → Y ↑	9.7972	7.1438	5.1753	3.5410	2.5551	1.6833	1.2609
B1 → Y ↓	6.8411	4.8964	3.4991	2.4289	1.7151	1.1782	0.8771
C0 → Y ↑	8.1276	6.2099	4.4943	2.9968	2.1730	1.4683	1.0874
C0 → Y ↓	6.8423	4.8963	3.4996	2.4388	1.7289	1.1784	0.8779

Cell Description

The OAI222 cell provides the logical inverted AND of three OR groups. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + A1) \bullet (B0 + B1) \bullet (C0 + C1)}$$

Logic Symbol



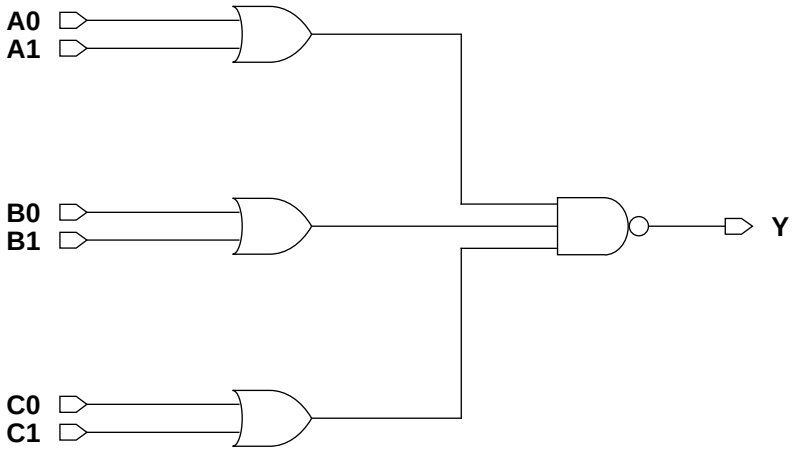
Function Table

A0	A1	B0	B1	C0	C1	Y
0	0	x	x	x	x	1
x	x	0	0	x	x	1
x	x	x	x	0	0	1
x	1	x	1	1	x	0
x	1	x	1	x	1	0
x	1	1	x	1	x	0
x	1	1	x	x	1	0
1	x	x	1	1	x	0
1	x	x	1	x	1	0
1	x	1	x	1	x	0
1	x	1	x	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI222X0P5MA10TR	2.00	2.20
OAI222X0P7MA10TR	2.00	2.20
OAI222X1MA10TR	2.00	2.20
OAI222X1P4MA10TR	2.00	3.80
OAI222X2MA10TR	2.00	3.80
OAI222X3MA10TR	2.00	5.40
OAI222X4MA10TR	2.00	6.80

Functional Schematic



AC Power

Pin	Power (uW/MHz)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A0	0.0002	0.0002	0.0003	0.0005	0.0006	0.0010	0.0013
A1	0.0005	0.0006	0.0008	0.0011	0.0016	0.0024	0.0031
B0	0.0002	0.0002	0.0003	0.0005	0.0007	0.0010	0.0013
B1	0.0004	0.0006	0.0008	0.0011	0.0016	0.0024	0.0032
C0	0.0002	0.0002	0.0003	0.0005	0.0006	0.0010	0.0013
C1	0.0004	0.0006	0.0008	0.0012	0.0016	0.0024	0.0032

Pin Capacitance

Pin	Capacitance (pF)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A0	0.0013	0.0016	0.0019	0.0029	0.0036	0.0055	0.0072
A1	0.0011	0.0014	0.0017	0.0029	0.0036	0.0051	0.0070
B0	0.0012	0.0015	0.0019	0.0027	0.0035	0.0054	0.0070
B1	0.0011	0.0014	0.0017	0.0028	0.0035	0.0051	0.0070
C0	0.0013	0.0015	0.0019	0.0029	0.0037	0.0056	0.0073
C1	0.0012	0.0014	0.0018	0.0029	0.0037	0.0052	0.0071

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A0 → Y ↑	0.0552	0.0519	0.0478	0.0474	0.0442	0.0437	0.0427
A0 → Y ↓	0.0372	0.0340	0.0318	0.0317	0.0294	0.0303	0.0296
A1 → Y ↑	0.0562	0.0534	0.0496	0.0494	0.0464	0.0455	0.0448
A1 → Y ↓	0.0385	0.0357	0.0338	0.0335	0.0312	0.0325	0.0316
B0 → Y ↑	0.0422	0.0390	0.0361	0.0357	0.0332	0.0326	0.0321
B0 → Y ↓	0.0325	0.0293	0.0275	0.0279	0.0260	0.0263	0.0261
B1 → Y ↑	0.0438	0.0408	0.0381	0.0380	0.0356	0.0348	0.0344
B1 → Y ↓	0.0340	0.0310	0.0295	0.0297	0.0277	0.0286	0.0282
C0 → Y ↑	0.0287	0.0257	0.0237	0.0239	0.0223	0.0223	0.0217
C0 → Y ↓	0.0229	0.0204	0.0194	0.0192	0.0178	0.0195	0.0188
C1 → Y ↑	0.0300	0.0274	0.0258	0.0260	0.0246	0.0241	0.0238

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
C1 → Y ↓	0.0246	0.0223	0.0216	0.0213	0.0201	0.0215	0.0210

Delays at 25°C,1.0V, Typical Process (Cont'd.)

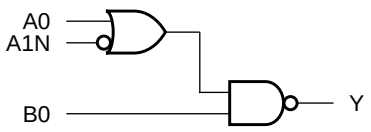
Description	K_{load} (ns/pF)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A0 → Y ↑	9.9662	7.3323	5.2486	3.5849	2.5713	1.7073	1.2743
A0 → Y ↓	6.8046	4.8393	3.4647	2.4544	1.7456	1.1708	0.8798
A1 → Y ↑	9.9642	7.3311	5.2480	3.5845	2.5711	1.7072	1.2741
A1 → Y ↓	6.7647	4.7960	3.4348	2.4347	1.7290	1.1682	0.8755
B0 → Y ↑	9.7796	7.1954	5.1688	3.5351	2.5319	1.6812	1.2560
B0 → Y ↓	6.8077	4.8185	3.4429	2.4544	1.7447	1.1709	0.8809
B1 → Y ↑	9.7772	7.1939	5.1678	3.5347	2.5316	1.6809	1.2558
B1 → Y ↓	6.7625	4.8099	3.4440	2.4208	1.7153	1.1682	0.8721
C0 → Y ↑	10.0103	7.3669	5.2739	3.6247	2.6013	1.7192	1.2811
C0 → Y ↓	6.7418	4.7927	3.4307	2.4452	1.7406	1.1680	0.8790
C1 → Y ↑	10.0050	7.3636	5.2722	3.6235	2.6007	1.7186	1.2807
C1 → Y ↓	6.7650	4.8093	3.4437	2.4400	1.7355	1.1682	0.8754

Cell Description

The OAI2XB1 cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \overline{(A0 + \overline{A1N}) \bullet B0}$$

Logic Symbol



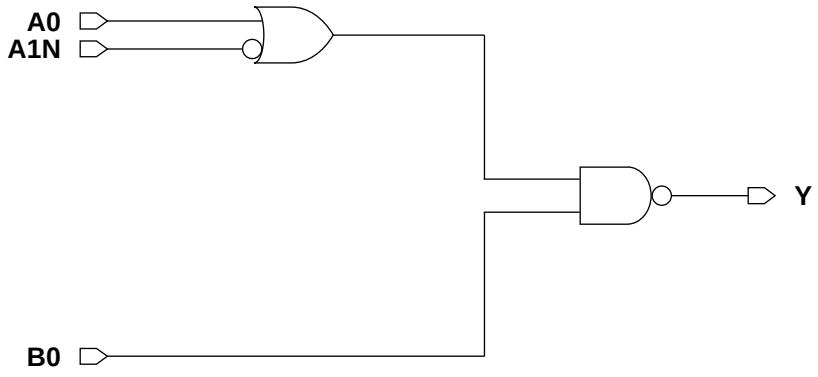
Function Table

A0	A1N	B0	Y
0	1	x	1
x	x	0	1
x	0	1	0
1	x	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
OAI2XB1X0P5MA10TR	2.00	1.60
OAI2XB1X0P7MA10TR	2.00	1.60
OAI2XB1X1MA10TR	2.00	1.60
OAI2XB1X1P4MA10TR	2.00	2.40
OAI2XB1X2MA10TR	2.00	2.40
OAI2XB1X3MA10TR	2.00	3.20
OAI2XB1X4MA10TR	2.00	4.20
OAI2XB1X6MA10TR	2.00	5.80
OAI2XB1X8MA10TR	2.00	7.60

Functional Schematic



AC Power

Pin	Power (uW/MHz)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0	0.0004	0.0005	0.0007	0.0010	0.0014	0.0021	0.0031	0.0046	0.0061
A1N	0.0016	0.0017	0.0018	0.0026	0.0032	0.0044	0.0054	0.0078	0.0106
B0	0.0005	0.0007	0.0008	0.0012	0.0015	0.0023	0.0030	0.0045	0.0060

Pin Capacitance

Pin	Capacitance (pF)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0	0.0012	0.0014	0.0018	0.0027	0.0034	0.0051	0.0068	0.0103	0.0137
A1N	0.0009	0.0009	0.0009	0.0011	0.0013	0.0017	0.0025	0.0033	0.0045
B0	0.0011	0.0013	0.0016	0.0021	0.0026	0.0039	0.0052	0.0077	0.0102

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0 → Y ↑	0.0247	0.0233	0.0215	0.0208	0.0193	0.0188	0.0179	0.0176	0.0177
A0 → Y ↓	0.0153	0.0146	0.0136	0.0135	0.0125	0.0125	0.0125	0.0122	0.0123
A1N → Y ↑	0.0408	0.0412	0.0408	0.0411	0.0393	0.0373	0.0373	0.0364	0.0372
A1N → Y ↓	0.0400	0.0426	0.0444	0.0456	0.0439	0.0413	0.0407	0.0400	0.0407
B0 → Y ↑	0.0145	0.0139	0.0130	0.0123	0.0113	0.0119	0.0115	0.0110	0.0111
B0 → Y ↓	0.0136	0.0128	0.0120	0.0110	0.0102	0.0114	0.0116	0.0114	0.0115

Delays at 25°C,1.0V, Typical Process (Cont'd.)

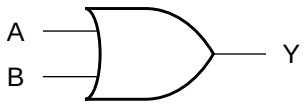
Description	K_{load} (ns/pF)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A0 → Y ↑	9.6392	7.0395	5.0509	3.4100	2.4531	1.6211	1.1582	0.7701	0.5773
A0 → Y ↓	5.8385	4.3129	3.0534	2.1340	1.5199	1.0253	0.7622	0.5100	0.3834
A1N → Y ↑	9.6373	7.0392	5.0504	3.4102	2.4530	1.6210	1.1579	0.7700	0.5772
A1N → Y ↓	5.8329	4.3014	3.0570	2.1111	1.5021	1.0232	0.7691	0.5156	0.3890
B0 → Y ↑	7.5238	5.7803	4.1740	2.8946	2.0845	1.3788	1.0600	0.6964	0.5228
B0 → Y ↓	5.8321	4.2984	3.0534	2.1209	1.5108	1.0219	0.7683	0.5152	0.3886

Cell Description

The OR2 cell provides the logical OR of two inputs (A,B). The output (Y) is represented by the logic equation:

$Y = (A + B)$

Logic Symbol



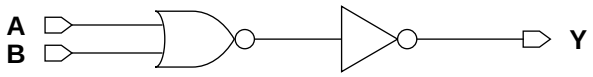
Function Table

A	B	Y
0	0	0
x	1	1
1	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
OR2X0P5MA10TR	2.00	1.20
OR2X0P7MA10TR	2.00	1.20
OR2X1MA10TR	2.00	1.20
OR2X1P4MA10TR	2.00	2.00
OR2X2MA10TR	2.00	2.00
OR2X3MA10TR	2.00	2.60
OR2X4MA10TR	2.00	3.00
OR2X6MA10TR	2.00	4.60
OR2X8MA10TR	2.00	5.60
OR2X11MA10TR	2.00	7.40

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A	0.0002	0.0003	0.0004	0.0005	0.0007	0.0011	0.0015	0.0023
B	0.0005	0.0005	0.0007	0.0011	0.0014	0.0022	0.0028	0.0042

AC Power (Cont'd.)

Pin	Power (uW/MHz)	
	X8P0M	**X11P0M**
A	0.0030	0.0043
B	0.0057	0.0080

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A	0.0012	0.0012	0.0013	0.0021	0.0024	0.0038	0.0044	0.0070
B	0.0012	0.0012	0.0013	0.0021	0.0025	0.0037	0.0043	0.0067

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)	
	X8P0M	**X11P0M**
A	0.0088	0.0121
B	0.0087	0.0118

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A → Y ↑	0.0277	0.0275	0.0256	0.0257	0.0243	0.0247	0.0237	0.0238
A → Y ↓	0.0409	0.0415	0.0381	0.0378	0.0357	0.0361	0.0346	0.0343
B → Y ↑	0.0297	0.0294	0.0277	0.0269	0.0256	0.0266	0.0258	0.0260
B → Y ↓	0.0439	0.0445	0.0410	0.0400	0.0381	0.0385	0.0371	0.0367

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)	
	X8P0M	**X11P0M**
A → Y ↑	0.0234	0.0236
A → Y ↓	0.0334	0.0335
B → Y ↑	0.0255	0.0258
B → Y ↓	0.0359	0.0360

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A → Y ↑	4.5630	3.3536	2.3951	1.6519	1.1913	0.7809	0.5788	0.3841
A → Y ↓	3.0820	2.3242	1.6005	1.0832	0.7668	0.5107	0.3692	0.2448
B → Y ↑	4.5655	3.3549	2.3962	1.6526	1.1918	0.7815	0.5793	0.3844
B → Y ↓	3.0816	2.3239	1.6003	1.0831	0.7667	0.5107	0.3692	0.2448

Delays at 25°C,1.0V, Typical Process (Cont'd.)

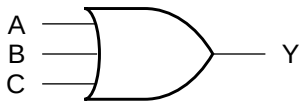
Description	K_{load} (ns/pF)	
	X8P0M	**X11P0M**
A → Y ↑	0.2872	0.2090
A → Y ↓	0.1862	0.1331
B → Y ↑	0.2875	0.2092
B → Y ↓	0.1862	0.1331

Cell Description

The OR3 cell provides the logical OR of three inputs (A,B,C). The output (Y) is represented by the logic equation:

$Y = (A + B + C)$

Logic Symbol



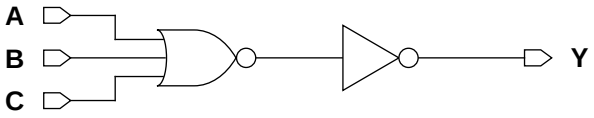
Function Table

A	B	C	Y
0	0	0	0
x	x	1	1
x	1	x	1
1	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
OR3X0P5MA10TR	2.00	1.40
OR3X0P7MA10TR	2.00	2.00
OR3X1MA10TR	2.00	2.00
OR3X1P4MA10TR	2.00	2.40
OR3X2MA10TR	2.00	3.40
OR3X3MA10TR	2.00	4.80
OR3X4MA10TR	2.00	6.60
OR3X6MA10TR	2.00	8.60
OR3X8MA10TR	2.00	11.20

Functional Schematic



AC Power

Pin	Power (uW/MHz)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A	0.0003	0.0004	0.0005	0.0007	0.0011	0.0020	0.0026	0.0038	0.0048
B	0.0003	0.0004	0.0005	0.0007	0.0011	0.0017	0.0022	0.0033	0.0044
C	0.0007	0.0009	0.0012	0.0016	0.0024	0.0036	0.0049	0.0072	0.0097

Pin Capacitance

Pin	Capacitance (pF)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A	0.0015	0.0019	0.0022	0.0029	0.0041	0.0058	0.0080	0.0115	0.0157
B	0.0014	0.0019	0.0022	0.0029	0.0039	0.0056	0.0077	0.0110	0.0150
C	0.0014	0.0019	0.0022	0.0030	0.0039	0.0056	0.0077	0.0111	0.0150

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A → Y ↑	0.0273	0.0253	0.0238	0.0231	0.0237	0.0226	0.0229	0.0225	0.0227
A → Y ↓	0.0455	0.0415	0.0395	0.0395	0.0380	0.0364	0.0365	0.0360	0.0365
B → Y ↑	0.0300	0.0282	0.0268	0.0261	0.0277	0.0269	0.0272	0.0267	0.0268
B → Y ↓	0.0512	0.0470	0.0452	0.0455	0.0459	0.0450	0.0449	0.0441	0.0441
C → Y ↑	0.0313	0.0298	0.0284	0.0276	0.0306	0.0298	0.0302	0.0297	0.0300
C → Y ↓	0.0540	0.0492	0.0474	0.0481	0.0490	0.0485	0.0483	0.0474	0.0473

Delays at 25°C,1.0V, Typical Process (Cont'd.)

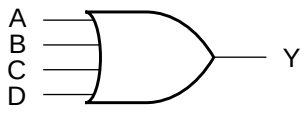
Description	K_{load} (ns/pF)								
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M	X8P0M
A → Y ↑	4.5399	3.3093	2.3678	1.6268	1.1757	0.7834	0.5826	0.3869	0.2900
A → Y ↓	2.8614	2.0838	1.5251	1.0752	0.7286	0.4945	0.3728	0.2494	0.1851
B → Y ↑	4.5463	3.3140	2.3710	1.6287	1.1780	0.7852	0.5839	0.3877	0.2906
B → Y ↓	2.8609	2.0836	1.5250	1.0751	0.7286	0.4945	0.3728	0.2494	0.1851
C → Y ↑	4.5502	3.3172	2.3732	1.6309	1.1814	0.7876	0.5858	0.3890	0.2916
C → Y ↓	2.8605	2.0834	1.5249	1.0751	0.7286	0.4945	0.3728	0.2494	0.1851

Cell Description

The OR4 cell provides the logical OR of four inputs (A,B,C,D). The output (Y) is represented by the logic equation:

$Y = (A + B + C + D)$

Logic Symbol



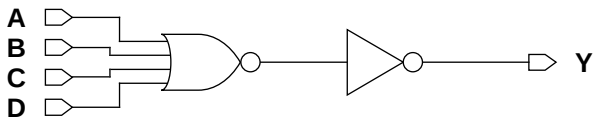
Function Table

A	B	C	D	Y
0	0	0	0	0
x	x	x	1	1
x	x	1	x	1
x	1	x	x	1
1	x	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
OR4X0P5MA10TR	2.00	2.20
OR4X0P7MA10TR	2.00	2.20
OR4X1MA10TR	2.00	2.20
OR4X1P4MA10TR	2.00	3.00
OR4X2MA10TR	2.00	3.40
OR4X3MA10TR	2.00	3.80
OR4X4MA10TR	2.00	5.40
OR4X6MA10TR	2.00	7.20
OR4X8MA10TR	2.00	9.20

Functional Schematic



AC Power

Pin	Power (uW/MHz)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A	0.0002	0.0002	0.0003	0.0004	0.0006	0.0009	0.0012	0.0018	0.0024
B	0.0005	0.0005	0.0006	0.0009	0.0013	0.0018	0.0024	0.0037	0.0049
C	0.0002	0.0002	0.0003	0.0004	0.0006	0.0009	0.0012	0.0018	0.0024
D	0.0005	0.0005	0.0006	0.0009	0.0013	0.0018	0.0025	0.0037	0.0049

Pin Capacitance

Pin	Capacitance (pF)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A	0.0012	0.0012	0.0013	0.0015	0.0023	0.0028	0.0041	0.0059	0.0078
B	0.0010	0.0010	0.0011	0.0013	0.0022	0.0028	0.0038	0.0057	0.0074
C	0.0011	0.0011	0.0012	0.0015	0.0022	0.0028	0.0040	0.0059	0.0078
D	0.0012	0.0012	0.0013	0.0013	0.0022	0.0028	0.0038	0.0057	0.0074

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A → Y ↑	0.0303	0.0304	0.0295	0.0291	0.0268	0.0253	0.0262	0.0256	0.0257
A → Y ↓	0.0432	0.0442	0.0430	0.0411	0.0366	0.0344	0.0351	0.0346	0.0351
B → Y ↑	0.0319	0.0320	0.0312	0.0310	0.0292	0.0278	0.0285	0.0280	0.0282
B → Y ↓	0.0444	0.0454	0.0445	0.0427	0.0389	0.0369	0.0373	0.0370	0.0375
C → Y ↑	0.0315	0.0317	0.0311	0.0334	0.0302	0.0288	0.0298	0.0293	0.0293
C → Y ↓	0.0436	0.0448	0.0442	0.0462	0.0404	0.0386	0.0395	0.0388	0.0391
D → Y ↑	0.0334	0.0334	0.0326	0.0354	0.0328	0.0313	0.0322	0.0317	0.0319
D → Y ↓	0.0470	0.0480	0.0472	0.0478	0.0429	0.0412	0.0417	0.0411	0.0415

Delays at 25°C,1.0V, Typical Process (Cont'd.)

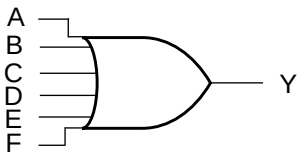
Description	K_{load} (ns/pF)								
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**	**X8P0M**
A → Y ↑	6.0505	4.4820	3.2537	2.2434	1.5949	1.0620	0.7931	0.5289	0.3967
A → Y ↓	5.3105	3.8826	2.7821	1.6980	1.1828	0.8025	0.5945	0.4043	0.3042
B → Y ↑	6.0553	4.4853	3.2559	2.2449	1.5960	1.0627	0.7937	0.5293	0.3970
B → Y ↓	5.3115	3.8827	2.7821	1.6979	1.1828	0.8024	0.5947	0.4042	0.3042
C → Y ↑	5.9963	4.4554	3.2704	2.2437	1.5956	1.0623	0.7936	0.5292	0.3969
C → Y ↓	5.3117	3.8841	2.7840	1.7018	1.1850	0.8039	0.5957	0.4049	0.3047
D → Y ↑	5.9988	4.4572	3.2714	2.2450	1.5966	1.0629	0.7941	0.5295	0.3972
D → Y ↓	5.3113	3.8836	2.7838	1.7018	1.1850	0.8038	0.5957	0.4049	0.3047

Cell Description

The OR6 cell provides the logical OR of six inputs (A,B,C,D,E,F). The output (Y) is represented by the logic equation:

$Y = (A + B + C + D + E + F)$

Logic Symbol



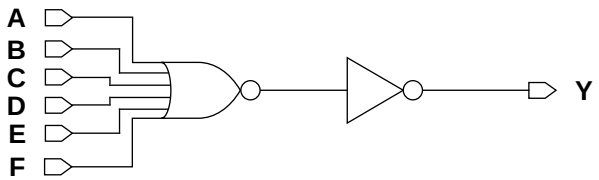
Function Table

A	B	C	D	E	F	Y
0	0	0	0	0	0	0
x	x	x	x	x	1	1
x	x	x	x	1	x	1
x	x	x	1	x	x	1
x	x	1	x	x	x	1
x	1	x	x	x	x	1
1	x	x	x	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
OR6X0P5MA10TR	2.00	2.60
OR6X0P7MA10TR	2.00	2.60
OR6X1MA10TR	2.00	2.60
OR6X1P4MA10TR	2.00	4.20
OR6X2MA10TR	2.00	4.20
OR6X3MA10TR	2.00	6.60
OR6X4MA10TR	2.00	9.20
OR6X6MA10TR	2.00	13.40

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M
A	0.0002	0.0003	0.0004	0.0005	0.0007	0.0012	0.0019	0.0027
B	0.0002	0.0003	0.0004	0.0005	0.0007	0.0012	0.0016	0.0023
C	0.0006	0.0006	0.0008	0.0012	0.0015	0.0025	0.0034	0.0050
D	0.0003	0.0003	0.0004	0.0005	0.0007	0.0012	0.0019	0.0027
E	0.0002	0.0003	0.0004	0.0005	0.0007	0.0012	0.0016	0.0023
F	0.0005	0.0006	0.0008	0.0012	0.0015	0.0025	0.0033	0.0050

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M
A	0.0014	0.0014	0.0016	0.0022	0.0026	0.0040	0.0052	0.0078
B	0.0011	0.0012	0.0014	0.0022	0.0026	0.0038	0.0050	0.0076
C	0.0012	0.0012	0.0014	0.0023	0.0027	0.0038	0.0050	0.0076
D	0.0013	0.0013	0.0015	0.0022	0.0026	0.0040	0.0052	0.0079
E	0.0012	0.0013	0.0014	0.0022	0.0026	0.0038	0.0050	0.0076
F	0.0013	0.0013	0.0015	0.0022	0.0026	0.0038	0.0050	0.0076

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M	X6P0M
A → Y ↑	0.0348	0.0340	0.0317	0.0297	0.0276	0.0278	0.0281	0.0285
A → Y ↓	0.0540	0.0532	0.0492	0.0423	0.0397	0.0389	0.0380	0.0389
B → Y ↑	0.0373	0.0366	0.0346	0.0334	0.0314	0.0317	0.0332	0.0335
B → Y ↓	0.0580	0.0572	0.0538	0.0482	0.0456	0.0464	0.0466	0.0472
C → Y ↑	0.0392	0.0385	0.0366	0.0358	0.0338	0.0352	0.0363	0.0367
C → Y ↓	0.0603	0.0596	0.0562	0.0506	0.0481	0.0494	0.0496	0.0503
D → Y ↑	0.0363	0.0358	0.0338	0.0340	0.0317	0.0308	0.0317	0.0321
D → Y ↓	0.0533	0.0534	0.0503	0.0469	0.0443	0.0417	0.0416	0.0423
E → Y ↑	0.0393	0.0388	0.0369	0.0378	0.0355	0.0348	0.0369	0.0370
E → Y ↓	0.0585	0.0586	0.0557	0.0528	0.0502	0.0492	0.0502	0.0506
F → Y ↑	0.0406	0.0398	0.0377	0.0402	0.0379	0.0384	0.0401	0.0404

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
F → Y ↓	0.0618	0.0618	0.0585	0.0551	0.0526	0.0523	0.0533	0.0537

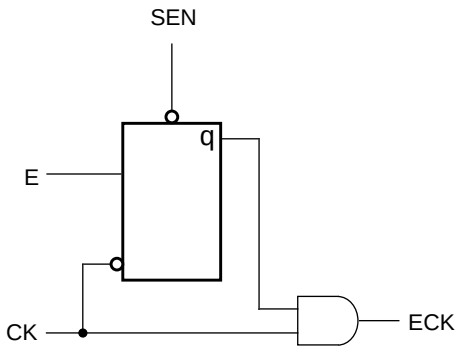
Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**	**X6P0M**
A → Y ↑	6.0602	4.4750	3.2487	2.1841	1.5834	1.0544	0.7916	0.5281
A → Y ↓	5.3424	3.8837	2.7688	1.6915	1.2142	0.7973	0.5971	0.3995
B → Y ↑	6.0667	4.4802	3.2522	2.1866	1.5852	1.0558	0.7929	0.5290
B → Y ↓	5.3424	3.8836	2.7690	1.6912	1.2141	0.7973	0.5971	0.3995
C → Y ↑	6.0734	4.4848	3.2557	2.1894	1.5871	1.0579	0.7944	0.5299
C → Y ↓	5.3424	3.8837	2.7688	1.6911	1.2141	0.7972	0.5971	0.3995
D → Y ↑	5.9410	4.4075	3.1822	2.1851	1.5840	1.0545	0.7918	0.5284
D → Y ↓	5.3345	3.8808	2.7683	1.6934	1.2161	0.7980	0.5977	0.3999
E → Y ↑	5.9464	4.4116	3.1850	2.1871	1.5855	1.0557	0.7929	0.5291
E → Y ↓	5.3341	3.8805	2.7685	1.6933	1.2159	0.7980	0.5978	0.3999
F → Y ↑	5.9505	4.4145	3.1870	2.1893	1.5872	1.0576	0.7942	0.5300
F → Y ↓	5.3336	3.8793	2.7683	1.6933	1.2160	0.7980	0.5977	0.3999

Cell Description

The POSTICG cell is a transparent low integrated latch clock gate. It is therefore compatible for use with positive-edge triggered flops. The high phase of the clock input (CK) is qualified by the latched enable signal (E) and the active-low asynchronous enable (SEN) to create the gated clock (ECK).

Logic Symbol



Function Table

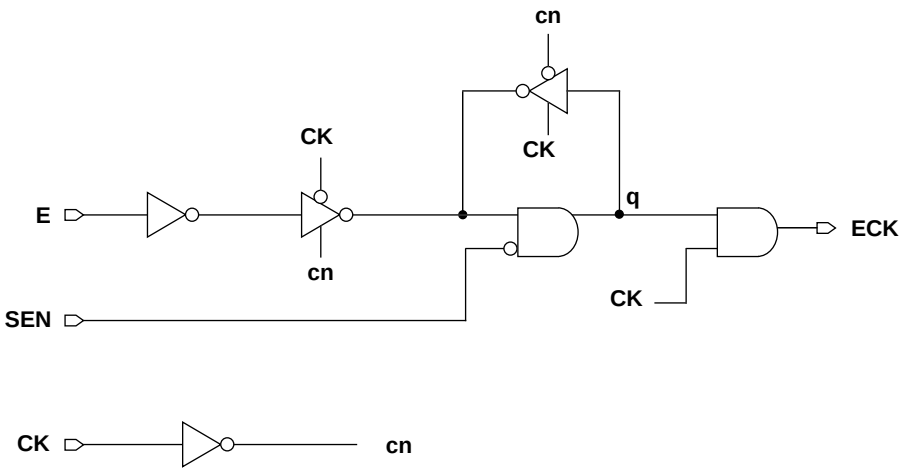
CK	SEN	E	q[n+1]	ECK[n+1]
0	1	1	1	0
0	0	0	1	0
0	0	1	1	0
0	1	0	0	0
1	x	x	q[n]	q[n]

- Note: q is an internal node and is not accessible.

Cell Size

Drive Strength	Height (um)	Width (um)
POSTICGX0P5BA10TR	2.00	3.40
POSTICGX0P6BA10TR	2.00	3.40
POSTICGX0P7BA10TR	2.00	3.40
POSTICGX0P8BA10TR	2.00	3.40
POSTICGX1BA10TR	2.00	3.40
POSTICGX1P2BA10TR	2.00	3.80
POSTICGX1P4BA10TR	2.00	3.80
POSTICGX1P7BA10TR	2.00	3.80
POSTICGX2BA10TR	2.00	3.80
POSTICGX2P5BA10TR	2.00	4.00
POSTICGX3BA10TR	2.00	4.00
POSTICGX3P5BA10TR	2.00	4.60
POSTICGX4BA10TR	2.00	4.60
POSTICGX5BA10TR	2.00	4.80
POSTICGX6BA10TR	2.00	5.20
POSTICGX7P5BA10TR	2.00	6.20
POSTICGX9BA10TR	2.00	6.60
POSTICGX11BA10TR	2.00	7.40
POSTICGX13BA10TR	2.00	7.60
POSTICGX16BA10TR	2.00	8.80

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P5B	**X0P6B**	**X0P7B**	**X0P8B**	**X1P0B**	**X1P2B**	**X1P4B**	**X1P7B**
E	0.0015	0.0015	0.0015	0.0016	0.0016	0.0016	0.0017	0.0017
SEN	0.0007	0.0007	0.0008	0.0008	0.0008	0.0008	0.0009	0.0009
CK	0.0023	0.0023	0.0023	0.0024	0.0024	0.0025	0.0026	0.0027
ECK	0.0041	0.0042	0.0043	0.0044	0.0046	0.0051	0.0053	0.0057

AC Power (Cont'd.)

Pin	Power (uW/MHz)							
	X2P0B	**X2P5B**	**X3P0B**	**X3P5B**	**X4P0B**	**X5P0B**	**X6P0B**	**X7P5B**
E	0.0018	0.0019	0.0019	0.0021	0.0022	0.0024	0.0027	0.0031
SEN	0.0010	0.0011	0.0012	0.0013	0.0014	0.0017	0.0019	0.0024
CK	0.0029	0.0031	0.0033	0.0036	0.0038	0.0044	0.0048	0.0059
ECK	0.0062	0.0072	0.0078	0.0090	0.0095	0.0115	0.0131	0.0163

AC Power (Cont'd.)

Pin	Power (uW/MHz)			
	X9P0B	**X11P0B**	**X13P0B**	**X16P0B**
E	0.0035	0.0040	0.0045	0.0053
SEN	0.0028	0.0033	0.0037	0.0045
CK	0.0067	0.0079	0.0088	0.0107
ECK	0.0188	0.0227	0.0255	0.0306

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5B	**X0P6B**	**X0P7B**	**X0P8B**	**X1P0B**	**X1P2B**	**X1P4B**	**X1P7B**
E	0.0010	0.0010	0.0010	0.0010	0.0010	0.0010	0.0010	0.0010
SEN	0.0010	0.0010	0.0010	0.0010	0.0010	0.0011	0.0011	0.0011
CK	0.0030	0.0030	0.0030	0.0030	0.0030	0.0031	0.0032	0.0033

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)							
	X2P0B	**X2P5B**	**X3P0B**	**X3P5B**	**X4P0B**	**X5P0B**	**X6P0B**	**X7P5B**
E	0.0010	0.0010	0.0010	0.0011	0.0011	0.0011	0.0012	0.0012
SEN	0.0011	0.0012	0.0012	0.0013	0.0013	0.0015	0.0016	0.0022
CK	0.0034	0.0038	0.0039	0.0044	0.0045	0.0051	0.0055	0.0070

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)			
	X9P0B	**X11P0B**	**X13P0B**	**X16P0B**
E	0.0013	0.0014	0.0016	0.0018
SEN	0.0024	0.0026	0.0029	0.0033
CK	0.0076	0.0090	0.0097	0.0118

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5B	**X0P6B**	**X0P7B**	**X0P8B**	**X1P0B**	**X1P2B**	**X1P4B**	**X1P7B**
CK → ECK ↑	0.0392	0.0400	0.0410	0.0411	0.0400	0.0374	0.0367	0.0365
CK → ECK ↓	0.0354	0.0364	0.0373	0.0378	0.0369	0.0354	0.0349	0.0343

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)							
	X2P0B	**X2P5B**	**X3P0B**	**X3P5B**	**X4P0B**	**X5P0B**	**X6P0B**	**X7P5B**
CK → ECK ↑	0.0360	0.0328	0.0319	0.0336	0.0327	0.0322	0.0319	0.0319
CK → ECK ↓	0.0341	0.0330	0.0325	0.0324	0.0323	0.0316	0.0317	0.0303

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)			
	X9P0B	**X11P0B**	**X13P0B**	**X16P0B**
CK → ECK ↑	0.0313	0.0312	0.0300	0.0304
CK → ECK ↓	0.0304	0.0305	0.0301	0.0297

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X0P5B	**X0P6B**	**X0P7B**	**X0P8B**	**X1P0B**	**X1P2B**	**X1P4B**	**X1P7B**
CK → ECK ↑	4.5966	3.9204	3.4971	3.1267	2.5381	1.9020	1.6540	1.3686
CK → ECK ↓	4.0616	3.5664	3.1284	2.8166	2.2999	1.7893	1.5030	1.2063

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X2P0B	**X2P5B**	**X3P0B**	**X3P5B**	**X4P0B**	**X5P0B**	**X6P0B**	**X7P5B**
CK → ECK ↑	1.1874	0.9334	0.7887	0.6659	0.5874	0.4703	0.3886	0.3101
CK → ECK ↓	1.0242	0.8197	0.6837	0.6037	0.5301	0.4177	0.3503	0.2787

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)			
	X9P0B	**X11P0B**	**X13P0B**	**X16P0B**
CK → ECK ↑	0.2585	0.2105	0.1796	0.1455
CK → ECK ↓	0.2326	0.1888	0.1646	0.1351

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)							
		X0P5B	**X0P6B**	**X0P7B**	**X0P8B**	**X1P0B**	**X1P2B**	**X1P4B**	**X1P7B**
E	setup ↑ → CK	0.0586	0.0586	0.0586	0.0586	0.0586	0.0586	0.0586	0.0586
	setup ↓ → CK	0.0469	0.0469	0.0469	0.0469	0.0469	0.0469	0.0469	0.0469
	hold ↑ → CK	-0.0273	-0.0273	-0.0273	-0.0273	-0.0273	-0.0273	-0.0273	-0.0273
	hold ↓ → CK	-0.0312	-0.0312	-0.0312	-0.0312	-0.0312	-0.0312	-0.0312	-0.0312
CK	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830	0.8830	0.8830	0.8830

Timing Constraints at 25°C,1.0V, Typical Process (Cont'd.)

Pin	Requirement	Interval (ns)							
		X2P0B	**X2P5B**	**X3P0B**	**X3P5B**	**X4P0B**	**X5P0B**	**X6P0B**	**X7P5B**
E	setup ↑ → CK	0.0586	0.0586	0.0586	0.0586	0.0586	0.0547	0.0547	0.0508
	setup ↓ → CK	0.0469	0.0469	0.0469	0.0469	0.0469	0.0430	0.0430	0.0469
	hold ↑ → CK	-0.0273	-0.0273	-0.0273	-0.0273	-0.0234	-0.0234	-0.0234	-0.0195
	hold ↓ → CK	-0.0312	-0.0312	-0.0312	-0.0312	-0.0312	-0.0312	-0.0312	-0.0312
CK	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830	0.8830	0.8830	0.8830

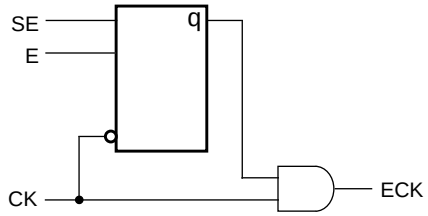
Timing Constraints at 25°C,1.0V, Typical Process (Cont'd.)

Pin	Requirement	Interval (ns)			
		X9P0B	**X11P0B**	**X13P0B**	**X16P0B**
E	setup ↑ → CK	0.0508	0.0469	0.0469	0.0469
	setup ↓ → CK	0.0430	0.0430	0.0430	0.0391
	hold ↑ → CK	-0.0195	-0.0195	-0.0195	-0.0156
	hold ↓ → CK	-0.0312	-0.0312	-0.0312	-0.0273
CK	minpwl	0.8830	0.8830	0.8830	0.8830

Cell Description

The PREICG cell is a transparent low integrated latch clock gate. It is therefore compatible for use with positive-edge triggered flops. The high phase of the clock input (CK) is qualified by the latched enable signal (E) and the active-high scan enable (SE) to create the gated clock (ECK).

Logic Symbol



Function Table

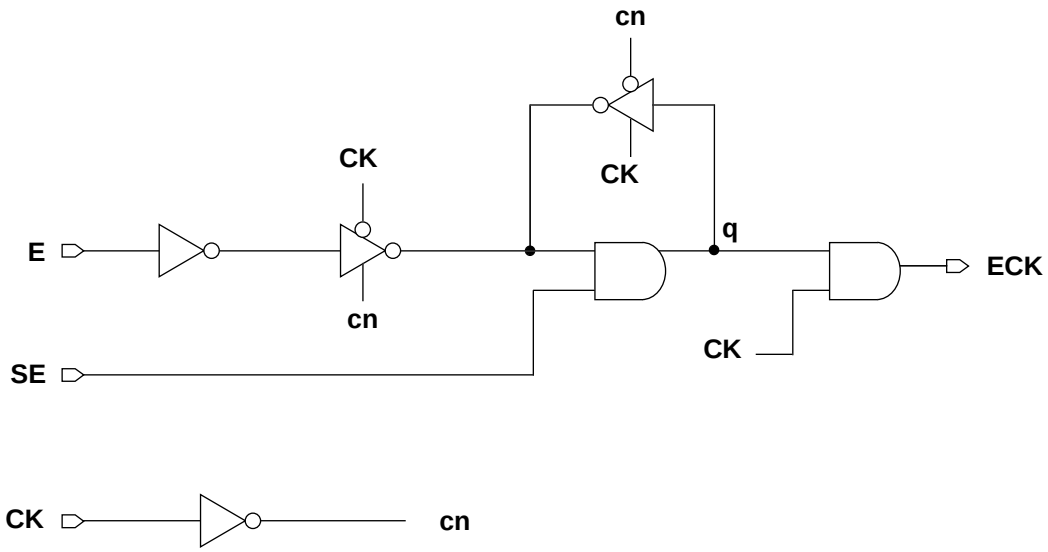
CK	SE	E	q[n+1]	ECK[n+1]
1	x	x	q[n]	q[n]
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0

- Note: q is an internal node and is not accessible.

Cell Size

Drive Strength	Height (um)	Width (um)
PREICGX0P5BA10TR	2.00	3.60
PREICGX0P6BA10TR	2.00	3.60
PREICGX0P7BA10TR	2.00	3.60
PREICGX0P8BA10TR	2.00	3.60
PREICGX1BA10TR	2.00	3.60
PREICGX1P2BA10TR	2.00	3.80
PREICGX1P4BA10TR	2.00	3.80
PREICGX1P7BA10TR	2.00	3.80
PREICGX2BA10TR	2.00	3.80
PREICGX2P5BA10TR	2.00	4.00
PREICGX3BA10TR	2.00	4.00
PREICGX3P5BA10TR	2.00	4.60
PREICGX4BA10TR	2.00	4.60
PREICGX5BA10TR	2.00	4.80
PREICGX6BA10TR	2.00	5.20
PREICGX7P5BA10TR	2.00	6.20
PREICGX9BA10TR	2.00	6.60
PREICGX11BA10TR	2.00	7.40
PREICGX13BA10TR	2.00	7.80
PREICGX16BA10TR	2.00	9.20

Functional Schematic



AC Power

Pin	Power (uW/MHz)							
	X0P5B	**X0P6B**	**X0P7B**	**X0P8B**	**X1P0B**	**X1P2B**	**X1P4B**	**X1P7B**
E	0.0018	0.0018	0.0018	0.0018	0.0019	0.0019	0.0019	0.0020
SE	0.0023	0.0023	0.0023	0.0023	0.0024	0.0024	0.0024	0.0025
CK	0.0022	0.0022	0.0023	0.0023	0.0023	0.0024	0.0025	0.0026
ECK	0.0039	0.0041	0.0042	0.0043	0.0045	0.0051	0.0053	0.0056

AC Power (Cont'd.)

Pin	Power (uW/MHz)							
	X2P0B	**X2P5B**	**X3P0B**	**X3P5B**	**X4P0B**	**X5P0B**	**X6P0B**	**X7P5B**
E	0.0020	0.0021	0.0022	0.0024	0.0024	0.0028	0.0030	0.0035
SE	0.0025	0.0026	0.0027	0.0029	0.0030	0.0034	0.0036	0.0047
CK	0.0027	0.0030	0.0032	0.0036	0.0039	0.0044	0.0048	0.0059
ECK	0.0060	0.0071	0.0077	0.0089	0.0095	0.0113	0.0129	0.0157

AC Power (Cont'd.)

Pin	Power (uW/MHz)			
	X9P0B	**X11P0B**	**X13P0B**	**X16P0B**
E	0.0042	0.0049	0.0053	0.0062
SE	0.0055	0.0062	0.0069	0.0079
CK	0.0067	0.0079	0.0089	0.0107
ECK	0.0182	0.0221	0.0246	0.0297

Pin Capacitance

Pin	Capacitance (pF)							
	X0P5B	**X0P6B**	**X0P7B**	**X0P8B**	**X1P0B**	**X1P2B**	**X1P4B**	**X1P7B**
E	0.0009	0.0009	0.0009	0.0009	0.0009	0.0009	0.0009	0.0009
SE	0.0011	0.0011	0.0011	0.0011	0.0011	0.0011	0.0011	0.0011
CK	0.0027	0.0027	0.0027	0.0027	0.0027	0.0029	0.0029	0.0030

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)							
	X2P0B	**X2P5B**	**X3P0B**	**X3P5B**	**X4P0B**	**X5P0B**	**X6P0B**	**X7P5B**
E	0.0009	0.0009	0.0009	0.0010	0.0010	0.0011	0.0011	0.0012
SE	0.0011	0.0011	0.0012	0.0012	0.0013	0.0013	0.0014	0.0018
CK	0.0031	0.0034	0.0036	0.0043	0.0045	0.0050	0.0054	0.0068

Pin Capacitance (Cont'd.)

Pin	Capacitance (pF)			
	X9P0B	**X11P0B**	**X13P0B**	**X16P0B**
E	0.0014	0.0015	0.0016	0.0018
SE	0.0021	0.0023	0.0025	0.0027
CK	0.0074	0.0088	0.0096	0.0117

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)							
	X0P5B	**X0P6B**	**X0P7B**	**X0P8B**	**X1P0B**	**X1P2B**	**X1P4B**	**X1P7B**
CK → ECK ↑	0.0374	0.0389	0.0398	0.0409	0.0397	0.0387	0.0379	0.0370
CK → ECK ↓	0.0327	0.0341	0.0349	0.0358	0.0349	0.0344	0.0338	0.0334

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)							
	X2P0B	**X2P5B**	**X3P0B**	**X3P5B**	**X4P0B**	**X5P0B**	**X6P0B**	**X7P5B**
CK → ECK ↑	0.0364	0.0361	0.0352	0.0342	0.0337	0.0336	0.0328	0.0321
CK → ECK ↓	0.0333	0.0334	0.0330	0.0326	0.0329	0.0323	0.0319	0.0304

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)			
	X9P0B	**X11P0B**	**X13P0B**	**X16P0B**
CK → ECK ↑	0.0315	0.0316	0.0305	0.0307
CK → ECK ↓	0.0304	0.0305	0.0302	0.0298

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X0P5B	**X0P6B**	**X0P7B**	**X0P8B**	**X1P0B**	**X1P2B**	**X1P4B**	**X1P7B**
CK → ECK ↑	4.5747	3.8821	3.3774	2.9877	2.4823	1.9540	1.6912	1.4034
CK → ECK ↓	3.9749	3.4027	2.9288	2.6109	2.1196	1.6855	1.4488	1.2319

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)							
	X2P0B	**X2P5B**	**X3P0B**	**X3P5B**	**X4P0B**	**X5P0B**	**X6P0B**	**X7P5B**
CK → ECK ↑	1.2185	0.9486	0.8036	0.6708	0.5918	0.4737	0.3904	0.3102
CK → ECK ↓	1.0476	0.8930	0.7306	0.6048	0.5318	0.4199	0.3506	0.2799

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)			
	X9P0B	**X11P0B**	**X13P0B**	**X16P0B**
CK → ECK ↑	0.2585	0.2108	0.1793	0.1452
CK → ECK ↓	0.2326	0.1888	0.1649	0.1350

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)							
		X0P5B	**X0P6B**	**X0P7B**	**X0P8B**	**X1P0B**	**X1P2B**	**X1P4B**	**X1P7B**
E	setup ↑ → CK	0.0586	0.0586	0.0586	0.0586	0.0586	0.0586	0.0586	0.0586
	setup ↓ → CK	0.0664	0.0664	0.0664	0.0664	0.0664	0.0664	0.0664	0.0703
	hold ↑ → CK	-0.0273	-0.0273	-0.0273	-0.0273	-0.0273	-0.0273	-0.0273	-0.0273
	hold ↓ → CK	-0.0508	-0.0508	-0.0508	-0.0508	-0.0508	-0.0508	-0.0508	-0.0508
SE	setup ↑ → CK	0.0625	0.0625	0.0625	0.0625	0.0625	0.0625	0.0625	0.0625
	setup ↓ → CK	0.0703	0.0703	0.0703	0.0703	0.0703	0.0703	0.0703	0.0703
	hold ↑ → CK	-0.0312	-0.0312	-0.0312	-0.0312	-0.0312	-0.0312	-0.0312	-0.0312
	hold ↓ → CK	-0.0508	-0.0508	-0.0547	-0.0508	-0.0547	-0.0547	-0.0547	-0.0547
CK	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830	0.8830	0.8830	0.8830

Timing Constraints at 25°C,1.0V, Typical Process (Cont'd.)

Pin	Requirement	Interval (ns)							
		X2P0B	**X2P5B**	**X3P0B**	**X3P5B**	**X4P0B**	**X5P0B**	**X6P0B**	**X7P5B**
E	setup ↑ → CK	0.0586	0.0586	0.0586	0.0547	0.0547	0.0508	0.0508	0.0469
	setup ↓ → CK	0.0703	0.0703	0.0703	0.0664	0.0664	0.0625	0.0625	0.0586
	hold ↑ → CK	-0.0273	-0.0273	-0.0273	-0.0234	-0.0234	-0.0234	-0.0195	-0.0195
	hold ↓ → CK	-0.0508	-0.0508	-0.0508	-0.0508	-0.0508	-0.0469	-0.0469	-0.0430
SE	setup ↑ → CK	0.0625	0.0586	0.0586	0.0586	0.0586	0.0547	0.0508	0.0508
	setup ↓ → CK	0.0703	0.0703	0.0703	0.0664	0.0664	0.0664	0.0625	0.0625
	hold ↑ → CK	-0.0312	-0.0312	-0.0312	-0.0273	-0.0273	-0.0234	-0.0234	-0.0234
	hold ↓ → CK	-0.0547	-0.0547	-0.0547	-0.0508	-0.0508	-0.0508	-0.0469	-0.0469
CK	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830	0.8830	0.8830	0.8830

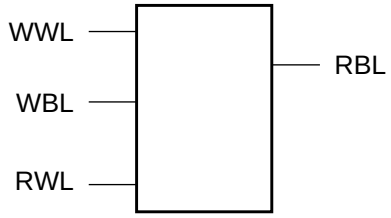
Timing Constraints at 25°C,1.0V, Typical Process (Cont'd.)

Pin	Requirement	Interval (ns)			
		X9P0B	**X11P0B**	**X13P0B**	**X16P0B**
E	setup ↑ → CK	0.0469	0.0469	0.0430	0.0430
	setup ↓ → CK	0.0586	0.0547	0.0547	0.0508
	hold ↑ → CK	-0.0195	-0.0195	-0.0156	-0.0156
	hold ↓ → CK	-0.0430	-0.0430	-0.0391	-0.0391
SE	setup ↑ → CK	0.0508	0.0508	0.0508	0.0469
	setup ↓ → CK	0.0625	0.0586	0.0586	0.0547
	hold ↑ → CK	-0.0234	-0.0234	-0.0195	-0.0195
	hold ↓ → CK	-0.0469	-0.0469	-0.0430	-0.0430
CK	minpwl	0.8830	0.8830	0.8830	0.8830

Cell Description

The RF1R1WS is a one write-port and one read-port register file cell. All word-lines are single rail and active-high. All bit-lines are single rail. The cell is marked not to be used by synthesis flows.

Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
RF1R1WSX1MA10TR	2.00	3.20
RF1R1WSX1P4MA10TR	2.00	4.00
RF1R1WSX2MA10TR	2.00	4.00

Function Table

WBL	WWL	nm[n+1]
0	1	1
1	1	0
x	0	nm[n]

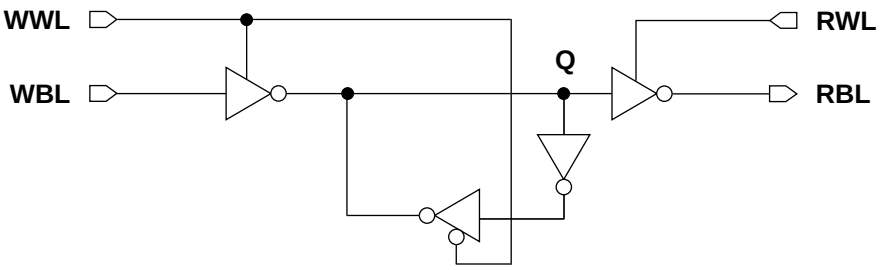
- Functions for Write Operations

Function Table (Cont'd.)

RWL	nm	RBL
1	0	1
1	1	0
0	0	Hi-Z
0	1	Hi-Z

- Functions for Read Operations

Functional Schematic



AC Power

Pin	Power (uW/MHz)		
	X1P0M	X1P4M	X2P0M
WWL	0.0026	0.0028	0.0029
WBL	0.0069	0.0088	0.0102
RWL	0.0018	0.0024	0.0029
RBL	0.0046	0.0066	0.0080

Pin Capacitance

Pin	Capacitance (pF)		
	X1P0M	X1P4M	X2P0M
WWL	0.0022	0.0024	0.0024
WBL	0.0016	0.0017	0.0018
RWL	0.0015	0.0020	0.0024
RBL	0.0013	0.0013	0.0016

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)			K_{load} (ns/pF)		
	X1P0M	X1P4M	X2P0M	X1P0M	X1P4M	X2P0M
WWL → RBL ↑	0.0350	0.0367	0.0368	3.3470	2.3002	1.6700
WWL → RBL ↓	0.0523	0.0543	0.0551	2.3778	1.6398	1.1722
WBL → RBL ↑	0.0411	0.0423	0.0421	3.3470	2.3003	1.6703
WBL → RBL ↓	0.0533	0.0558	0.0569	2.3783	1.6398	1.1722
RWL → RBL ↑	0.0118	0.0100	0.0094	3.3134	2.2826	1.6578
RWL → RBL ↓	0.0060	0.0051	0.0050	2.3435	1.6125	1.1500

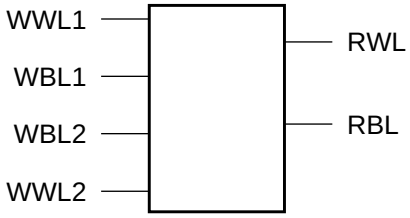
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)		
		X1P0M	X1P4M	X2P0M
WWL	minpwh	0.8830	0.8830	0.8830
WBL	setup ↑ → WWL	0.0352	0.0391	0.0391
	setup ↓ → WWL	0.0391	0.0391	0.0430
	hold ↑ → WWL	-0.0273	-0.0273	-0.0273
	hold ↓ → WWL	-0.0234	-0.0273	-0.0273

Cell Description

The RF1R2WS is a two write-port and one read-port register file cell. All word-lines are single rail and active-high. The user is required to ensure the two write word-lines are never active at the same time. All bit-lines are single rail. The cell is marked not to be used by synthesis flows.

Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
RF1R2WSX1MA10TR	2.00	4.80
RF1R2WSX1P4MA10TR	2.00	5.60
RF1R2WSX2MA10TR	2.00	5.60

Function Table

WBL1	WBL2	WWL1	WWL2	nm[n+1]
1	0	1	1	x
0	1	1	1	x
1	1	1	1	0
0	0	1	1	1
1	x	1	0	0
0	x	1	0	1
x	1	0	1	0
x	0	0	1	1
x	x	0	0	nm[n]

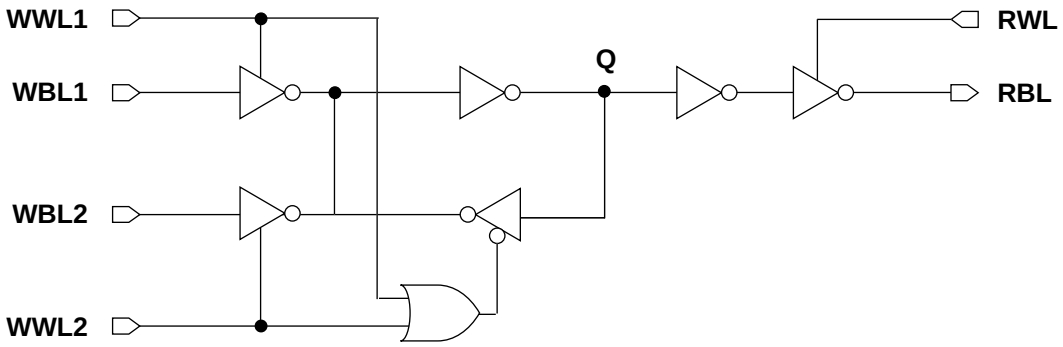
- Functions for Write Operations

Function Table (Cont'd.)

RWL	nm	RBL
1	0	1
1	1	0
0	0	Hi-Z
0	1	Hi-Z

- Functions for Read Operations

Functional Schematic



AC Power

Pin	Power (uW/MHz)		
	X1P0M	X1P4M	X2P0M
WBL1	0.0084	0.0103	0.0117
WBL2	0.0085	0.0104	0.0118
WWL1	0.0049	0.0068	0.0079
WWL2	0.0052	0.0071	0.0082
RWL	0.0021	0.0028	0.0033
RBL	0.0018	0.0018	0.0022

Pin Capacitance

Pin	Capacitance (pF)		
	X1P0M	X1P4M	X2P0M
WBL1	0.0015	0.0015	0.0015
WBL2	0.0015	0.0015	0.0015
WWL1	0.0016	0.0017	0.0017
WWL2	0.0016	0.0017	0.0017
RWL	0.0015	0.0021	0.0025
RBL	0.0013	0.0015	0.0017

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)			K_{load} (ns/pF)		
	X1P0M	X1P4M	X2P0M	X1P0M	X1P4M	X2P0M
WBL1 → RBL ↑	0.0487	0.0513	0.0526	3.3217	2.2812	1.6595
WBL1 → RBL ↓	0.0610	0.0669	0.0701	2.3719	1.6646	1.1998
WBL2 → RBL ↑	0.0489	0.0522	0.0535	3.3231	2.2826	1.6604
WBL2 → RBL ↓	0.0639	0.0687	0.0715	2.3787	1.6675	1.2015
WWL1 → RBL ↑	0.0426	0.0454	0.0466	3.3216	2.2811	1.6594
WWL1 → RBL ↓	0.0592	0.0638	0.0661	2.3720	1.6643	1.1998
WWL2 → RBL ↑	0.0437	0.0467	0.0478	3.3233	2.2825	1.6603
WWL2 → RBL ↓	0.0613	0.0652	0.0674	2.3783	1.6673	1.2014
RWL → RBL ↑	0.0119	0.0097	0.0091	3.2840	2.2606	1.6438
RWL → RBL ↓	0.0061	0.0054	0.0052	2.3206	1.6212	1.1635

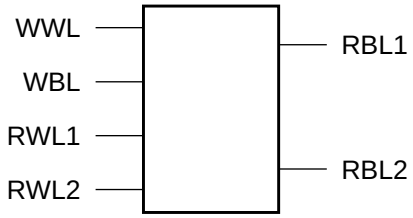
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)		
		X1P0M	**X1P4M**	**X2P0M**
WBL1	setup ↑ → WWL1	0.0469	0.0469	0.0508
	setup ↓ → WWL1	0.0469	0.0547	0.0547
	hold ↑ → WWL1	-0.0312	-0.0352	-0.0352
	hold ↓ → WWL1	-0.0312	-0.0352	-0.0352
WBL2	setup ↑ → WWL2	0.0430	0.0469	0.0508
	setup ↓ → WWL2	0.0469	0.0508	0.0547
	hold ↑ → WWL2	-0.0312	-0.0352	-0.0391
	hold ↓ → WWL2	-0.0312	-0.0352	-0.0391
WWL1	minpwh	0.8830	0.8830	0.8830
WWL2	minpwh	0.8830	0.8830	0.8830

Cell Description

The RF2R1WS is a one write-port and two read-port register file cell. The word-line is single rail and active-high. All bit-lines are single rail. The cell is marked not to be used by synthesis flows.

Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
RF2R1WSX1MA10TR	2.00	4.40
RF2R1WSX1P4MA10TR	2.00	6.00
RF2R1WSX2MA10TR	2.00	6.00

Function Table

WBL	WWL	nm[n+1]
0	1	1
1	1	0
x	0	nm[n]

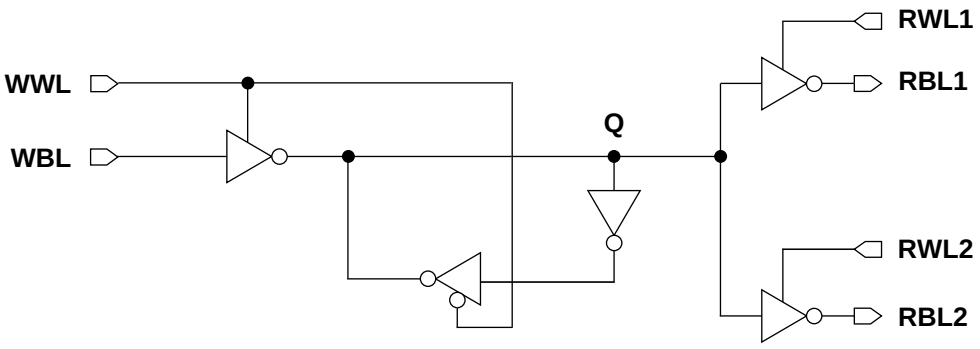
- Functions for Write Operations

Function Table (Cont'd.)

RWL1/rdwl2	nm	RBL1/rdbl2
1	1	0
1	0	1
0	0	Hi-Z
0	1	Hi-Z

- Functions for Read Operations

Functional Schematic



AC Power

Pin	Power (uW/MHz)		
	X1P0M	X1P4M	X2P0M
WBL	0.0103	0.0139	0.0172
WWL	0.0062	0.0103	0.0127
RWL1	0.0020	0.0027	0.0032
RWL2	0.0020	0.0027	0.0033
RBL1	0.0027	0.0034	0.0043

Pin Capacitance

Pin	Capacitance (pF)		
	X1P0M	X1P4M	X2P0M
WBL	0.0018	0.0018	0.0017
WWL	0.0017	0.0017	0.0017
RWL1	0.0017	0.0023	0.0028
RWL2	0.0017	0.0024	0.0029
RBL1	0.0013	0.0013	0.0015
RBL2	0.0013	0.0014	0.0017

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)			K_{load} (ns/pF)		
	X1P0M	X1P4M	X2P0M	X1P0M	X1P4M	X2P0M
WBL → RBL1 ↑	0.0456	0.0537	0.0587	3.3201	2.3022	1.6794
WBL → RBL1 ↓	0.0619	0.0755	0.0828	2.3240	1.6671	1.1995
WWL → RBL1 ↑	0.0403	0.0488	0.0532	3.3198	2.3019	1.6794
WWL → RBL1 ↓	0.0595	0.0725	0.0784	2.3242	1.6671	1.1995
RWL1 → RBL1 ↑	0.0115	0.0089	0.0085	3.2836	2.2786	1.6599
RWL1 → RBL1 ↓	0.0058	0.0051	0.0049	2.2707	1.6053	1.1466
WBL → RBL2 ↑	0.0459	0.0542	0.0587	3.2919	2.2901	1.6677
WBL → RBL2 ↓	0.0623	0.0760	0.0829	2.3484	1.6764	1.2016
WWL → RBL2 ↑	0.0405	0.0493	0.0532	3.2916	2.2899	1.6677
WWL → RBL2 ↓	0.0599	0.0730	0.0784	2.3485	1.6767	1.2016
RWL2 → RBL2 ↑	0.0118	0.0099	0.0093	3.2541	2.2649	1.6473
RWL2 → RBL2 ↓	0.0061	0.0050	0.0050	2.2967	1.6171	1.1495

Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)		
		X1P0M	X1P4M	X2P0M
WBL	setup ↑ → WWL	0.0430	0.0469	0.0547
	setup ↓ → WWL	0.0469	0.0547	0.0625
	hold ↑ → WWL	-0.0273	-0.0352	-0.0391
	hold ↓ → WWL	-0.0273	-0.0352	-0.0391
WWL	minpwh	0.8830	0.8830	0.8830

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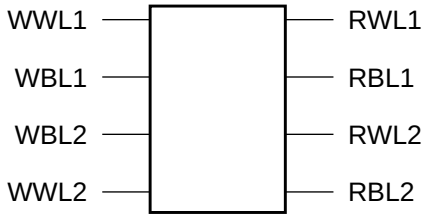
Cell Description

The RF2R2WS is a two write-port and two read-port register file cell. All word-lines are single rail and active-high. The user is required to ensure the two write word-lines are never active at the same time. All bit-lines are single rail. The cell is marked not to be used by synthesis flows.

Logic Symbol



Cell Size

Drive Strength	Height (um)	Width (um)
RF2R2WSX1MA10TR	2.00	6.00
RF2R2WSX1P4MA10TR	2.00	7.60
RF2R2WSX2MA10TR	2.00	7.60

Function Table

WBL1	WBL2	WWL1	WWL2	nm[n+1]
1	0	1	1	x
0	1	1	1	x
1	1	1	1	0
0	0	1	1	1
1	x	1	0	0
0	x	1	0	1
x	1	0	1	0
x	0	0	1	1
x	x	0	0	nm[n]

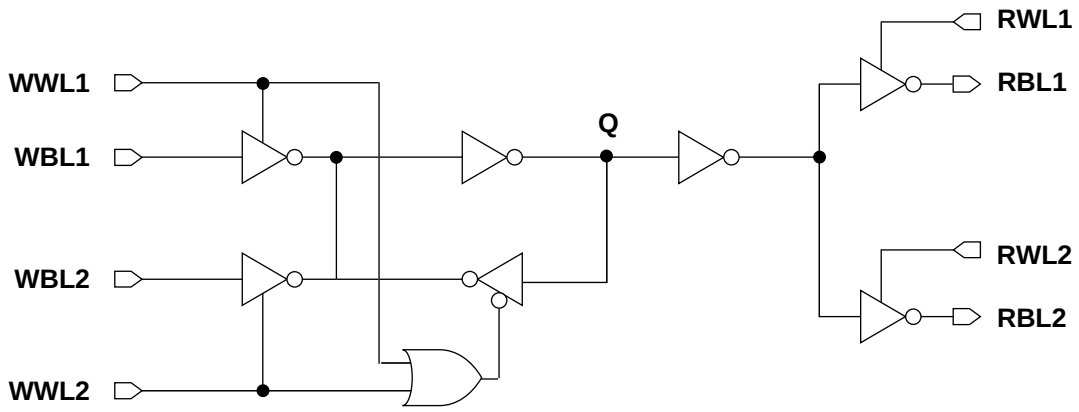
- Functions for Write Operations

Function Table (Cont'd.)

RWL1/rdwl2	nm	RBL1/rdbl2
1	1	0
1	0	1
0	0	Hi-Z
0	1	Hi-Z

- Functions for Read Operations

Functional Schematic



AC Power

Pin	Power (uW/MHz)		
	X1P0M	X1P4M	X2P0M
WBL1	0.0114	0.0156	0.0193
WBL2	0.0116	0.0158	0.0194
WWL1	0.0074	0.0110	0.0137
WWL2	0.0077	0.0113	0.0139
RWL1	0.0023	0.0030	0.0035
RWL2	0.0023	0.0031	0.0037
RBL1	0.0027	0.0034	0.0043

Pin Capacitance

Pin	Capacitance (pF)		
	X1P0M	X1P4M	X2P0M
WBL1	0.0015	0.0015	0.0015
WBL2	0.0015	0.0015	0.0015
WWL1	0.0016	0.0017	0.0017
WWL2	0.0016	0.0017	0.0017
RWL1	0.0014	0.0020	0.0023
RWL2	0.0017	0.0024	0.0029
RBL1	0.0013	0.0013	0.0016
RBL2	0.0013	0.0013	0.0017

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)			K_{load} (ns/pF)		
	X1P0M	X1P4M	X2P0M	X1P0M	X1P4M	X2P0M
WBL1 → RBL1 ↑	0.0567	0.0639	0.0678	3.3103	2.2872	1.6701
WBL1 → RBL1 ↓	0.0752	0.0868	0.0930	2.3827	1.7301	1.2481
WBL2 → RBL1 ↑	0.0577	0.0643	0.0679	3.3128	2.2881	1.6708
WBL2 → RBL1 ↓	0.0780	0.0883	0.0935	2.3892	1.7322	1.2481
WWL1 → RBL1 ↑	0.0514	0.0583	0.0616	3.3103	2.2868	1.6699
WWL1 → RBL1 ↓	0.0725	0.0827	0.0875	2.3829	1.7302	1.2482
WWL2 → RBL1 ↑	0.0529	0.0592	0.0621	3.3125	2.2884	1.6707
WWL2 → RBL1 ↓	0.0747	0.0839	0.0878	2.3889	1.7320	1.2480
RWL1 → RBL1 ↑	0.0116	0.0094	0.0091	3.2651	2.2562	1.6466
RWL1 → RBL1 ↓	0.0058	0.0051	0.0050	2.2956	1.6490	1.1829
WBL1 → RBL2 ↑	0.0571	0.0645	0.0680	3.3022	2.2912	1.6667
WBL1 → RBL2 ↓	0.0753	0.0873	0.0931	2.3853	1.7047	1.2219
WBL2 → RBL2 ↑	0.0582	0.0649	0.0681	3.3046	2.2923	1.6673
WBL2 → RBL2 ↓	0.0782	0.0887	0.0936	2.3919	1.7068	1.2219
WWL1 → RBL2 ↑	0.0518	0.0589	0.0618	3.3021	2.2911	1.6670
WWL1 → RBL2 ↓	0.0726	0.0832	0.0876	2.3853	1.7048	1.2220
WWL2 → RBL2 ↑	0.0533	0.0598	0.0624	3.3044	2.2927	1.6672
WWL2 → RBL2 ↓	0.0748	0.0843	0.0879	2.3915	1.7066	1.2218
RWL2 → RBL2 ↑	0.0118	0.0101	0.0094	3.2563	2.2598	1.6429

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	Intrinsic Delay (ns)			K_{load} (ns/pF)		
	X1P0M	X1P4M	X2P0M	X1P0M	X1P4M	X2P0M
RWL2 → RBL2 ↓	0.0061	0.0051	0.0051	2.2997	1.6235	1.1556

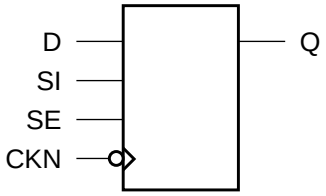
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)		
		X1P0M	X1P4M	X2P0M
WBL1	setup ↑ → WWL1	0.0508	0.0586	0.0625
	setup ↓ → WWL1	0.0586	0.0664	0.0742
	hold ↑ → WWL1	-0.0391	-0.0430	-0.0469
	hold ↓ → WWL1	-0.0391	-0.0469	-0.0508
WBL2	setup ↑ → WWL2	0.0508	0.0586	0.0625
	setup ↓ → WWL2	0.0586	0.0664	0.0703
	hold ↑ → WWL2	-0.0391	-0.0430	-0.0469
	hold ↓ → WWL2	-0.0430	-0.0469	-0.0508
WWL1	minpwh	0.8830	0.8830	0.8830
WWL2	minpwh	0.8830	0.8830	0.8830

Cell Description

The SDFFNQ cell is a negative-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE).

Logic Symbol



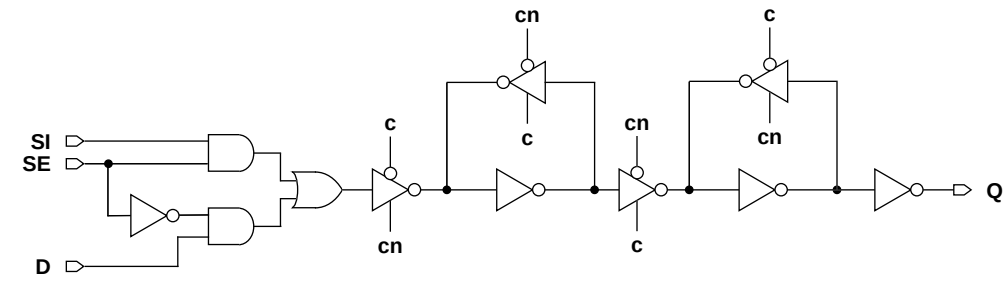
Function Table

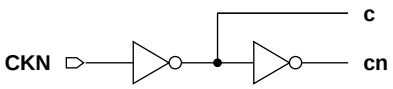
D	SI	SE	CKN	Q[n+1]
1	x	0	⌝_	1
0	x	0	⌝_	0
x	x	x	_⌜	Q[n]
x	1	1	⌝_	1
x	0	1	⌝_	0

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFNQX1MA10TR	2.00	5.20
SDFFNQX2MA10TR	2.00	5.60
SDFFNQX3MA10TR	2.00	6.00

Functional Schematic





AC Power

Pin	Power (uW/MHz)		
	X1P0M	X2P0M	X3P0M
SI	0.0067	0.0079	0.0085
SE	0.0063	0.0073	0.0078
D	0.0058	0.0068	0.0071
CKN	0.0048	0.0054	0.0061
Q	0.0049	0.0066	0.0085

Pin Capacitance

Pin	Capacitance (pF)		
	X1P0M	X2P0M	X3P0M
SI	0.0007	0.0007	0.0007
SE	0.0023	0.0025	0.0025
D	0.0014	0.0016	0.0016
CKN	0.0010	0.0010	0.0011

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)			K_{load} (ns/pF)		
	X1P0M	X2P0M	X3P0M	X1P0M	X2P0M	X3P0M
CKN → Q ↑	0.0908	0.0858	0.0873	2.3366	1.1589	0.7819
CKN → Q ↓	0.0855	0.0837	0.0870	1.4532	0.7200	0.4594

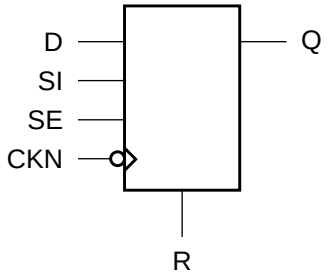
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)		
		X1P0M	X2P0M	X3P0M
SI	setup ↑ → CKN	0.0664	0.0742	0.0781
	setup ↓ → CKN	0.1172	0.1289	0.1367
	hold ↑ → CKN	-0.0352	-0.0430	-0.0469
	hold ↓ → CKN	-0.0742	-0.0742	-0.0820
SE	setup ↑ → CKN	0.1250	0.1367	0.1445
	setup ↓ → CKN	0.0508	0.0430	0.0430
	hold ↑ → CKN	-0.0312	-0.0430	-0.0430
	hold ↓ → CKN	-0.0234	-0.0195	-0.0195
D	setup ↑ → CKN	0.0273	0.0195	0.0195
	setup ↓ → CKN	0.0469	0.0430	0.0430
	hold ↑ → CKN	-0.0039	0.0000	0.0000
	hold ↓ → CKN	-0.0273	-0.0234	-0.0234
CKN	minpwl	0.8830	0.8830	0.8830
	minpwh	0.8830	0.8830	0.8830

Cell Description

The SDFFNRPQ cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-high reset (R).

Logic Symbol



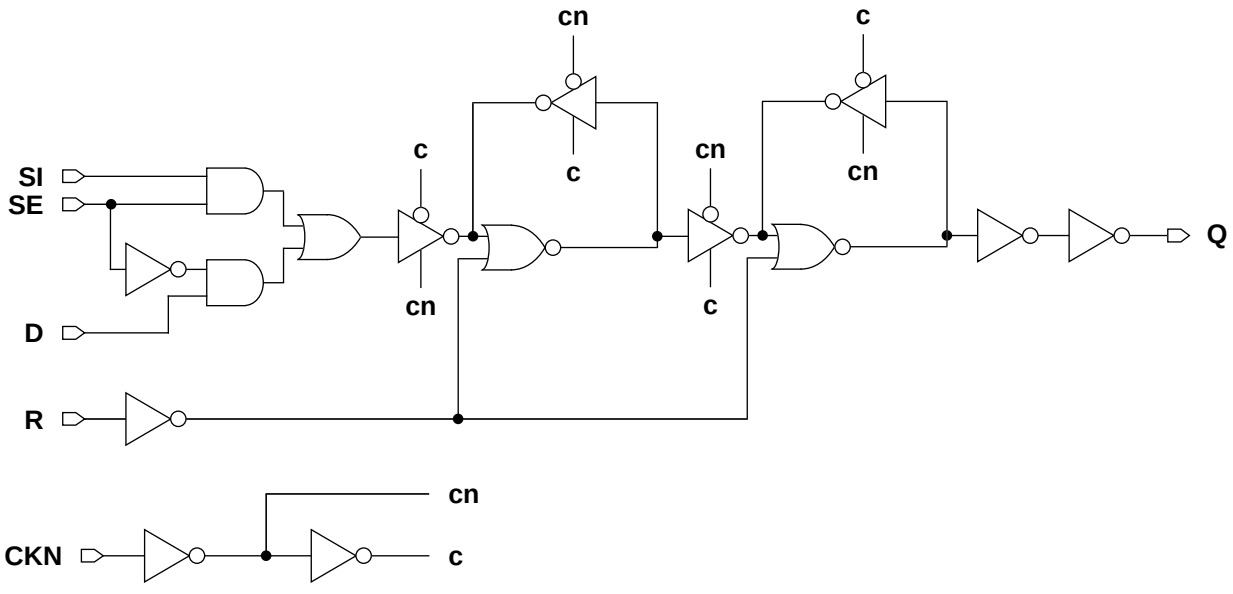
Function Table

R	D	SI	SE	CKN	Q[n+1]
1	x	x	x	↓	0
0	1	x	0	↓	1
0	0	x	0	↓	0
0	x	0	1	↓	0
0	x	1	1	↓	1
0	x	x	x	↑	Q[n]

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFNRPQX1MA10TR	2.00	5.80
SDFFNRPQX2MA10TR	2.00	6.40
SDFFNRPQX3MA10TR	2.00	6.60

Functional Schematic



AC Power

Pin	Power (uW/MHz)		
	X1P0M	X2P0M	X3P0M
SI	0.0067	0.0077	0.0082
SE	0.0071	0.0084	0.0087
D	0.0059	0.0069	0.0073
CKN	0.0050	0.0056	0.0062
R	0.0016	0.0021	0.0024
Q	0.0056	0.0071	0.0090

Pin Capacitance

Pin	Capacitance (pF)		
	X1P0M	X2P0M	X3P0M
SI	0.0007	0.0007	0.0007
SE	0.0023	0.0025	0.0025
D	0.0013	0.0016	0.0016
CKN	0.0010	0.0010	0.0011
R	0.0016	0.0017	0.0017

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)			K_{load} (ns/pF)		
	X1P0M	X2P0M	X3P0M	X1P0M	X2P0M	X3P0M
CKN → Q ↑	0.1037	0.0945	0.0981	2.3118	1.1484	0.7781
CKN → Q ↓	0.0976	0.0938	0.0969	1.4570	0.7093	0.4560
R → Q ↓	0.0566	0.0578	0.0658	1.4547	0.7084	0.4557

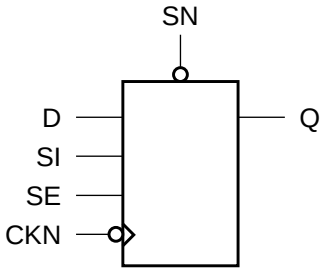
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)		
		X1P0M	**X2P0M**	**X3P0M**
SI	setup ↑ → CKN	0.0703	0.0781	0.0781
	setup ↓ → CKN	0.1211	0.1367	0.1406
	hold ↑ → CKN	-0.0352	-0.0391	-0.0430
	hold ↓ → CKN	-0.0820	-0.0898	-0.0859
SE	setup ↑ → CKN	0.1250	0.1445	0.1484
	setup ↓ → CKN	0.0547	0.0469	0.0469
	hold ↑ → CKN	-0.0312	-0.0391	-0.0391
	hold ↓ → CKN	-0.0234	-0.0195	-0.0195
D	setup ↑ → CKN	0.0352	0.0234	0.0234
	setup ↓ → CKN	0.0469	0.0430	0.0469
	hold ↑ → CKN	-0.0039	0.0039	0.0039
	hold ↓ → CKN	-0.0312	-0.0273	-0.0273
CKN	minpwl	0.8830	0.8830	0.8830
	minpwh	0.8830	0.8830	0.8830
R	minpwh	0.8830	0.8830	0.8830
	recovery	-0.0234	-0.0273	-0.0273
	removal	0.0625	0.0703	0.0703

Cell Description

The SDFFNSQ cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN).

Logic Symbol



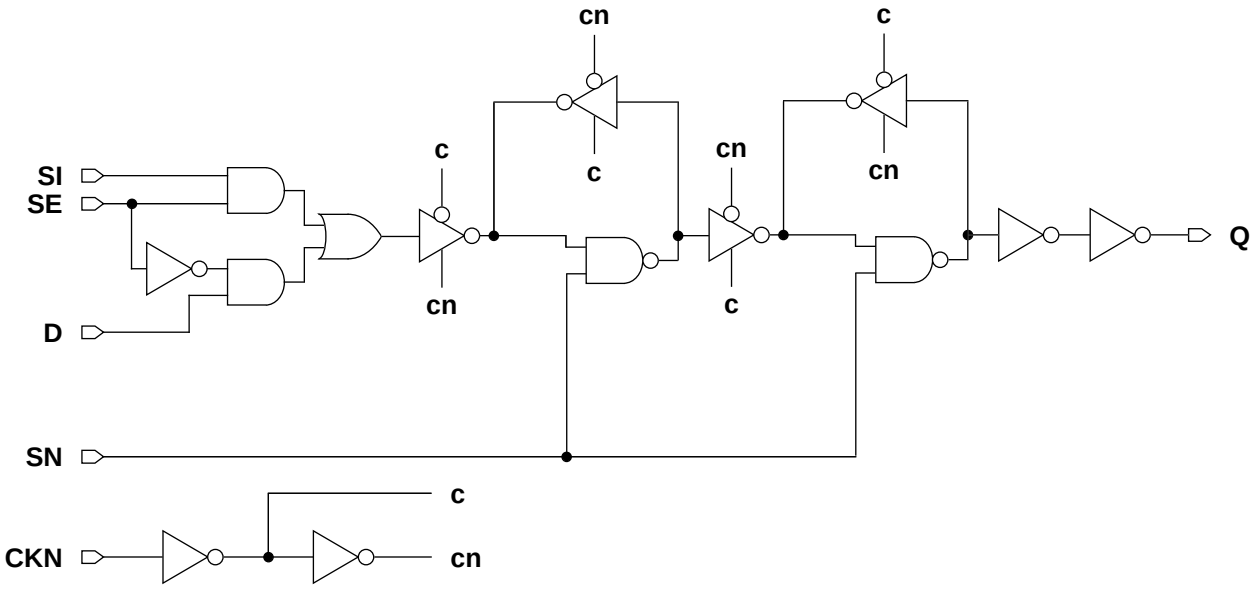
Function Table

SN	D	SI	SE	CKN	Q
1	1	x	0	↓	1
1	0	x	0	↓	0
1	x	x	x	↑	Q[n]
1	x	1	1	↓	1
1	x	0	1	↓	0
0	x	x	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFNSQX1MA10TR	2.00	6.20
SDFFNSQX2MA10TR	2.00	6.40
SDFFNSQX3MA10TR	2.00	7.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)		
	X1P0M	X2P0M	X3P0M
SI	0.0069	0.0080	0.0084
SE	0.0073	0.0083	0.0087
D	0.0062	0.0072	0.0076
CKN	0.0051	0.0057	0.0064
SN	0.0017	0.0021	0.0024
Q	0.0053	0.0070	0.0092

Pin Capacitance

Pin	Capacitance (pF)		
	X1P0M	X2P0M	X3P0M
SI	0.0007	0.0007	0.0007
SE	0.0023	0.0025	0.0025
D	0.0014	0.0017	0.0017
CKN	0.0010	0.0010	0.0011
SN	0.0017	0.0018	0.0018

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)			K_{load} (ns/pF)		
	X1P0M	X2P0M	X3P0M	X1P0M	X2P0M	X3P0M
CKN → Q ↑	0.0951	0.0921	0.0958	2.3355	1.1640	0.7815
CKN → Q ↓	0.0920	0.0901	0.0962	1.4538	0.7258	0.4603
SN → Q ↑	0.0575	0.0608	0.0699	2.3329	1.1639	0.7813

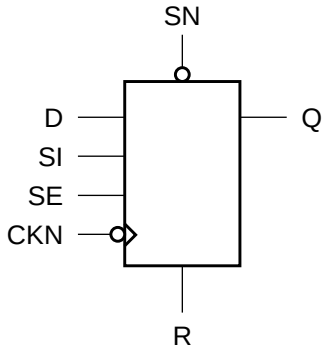
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)		
		X1P0M	**X2P0M**	**X3P0M**
SI	setup ↑ → CKN	0.0742	0.0820	0.0859
	setup ↓ → CKN	0.1133	0.1211	0.1289
	hold ↑ → CKN	-0.0391	-0.0469	-0.0469
	hold ↓ → CKN	-0.0703	-0.0703	-0.0703
SE	setup ↑ → CKN	0.1211	0.1328	0.1367
	setup ↓ → CKN	0.0547	0.0469	0.0508
	hold ↑ → CKN	-0.0352	-0.0469	-0.0469
	hold ↓ → CKN	-0.0273	-0.0195	-0.0234
D	setup ↑ → CKN	0.0352	0.0273	0.0273
	setup ↓ → CKN	0.0430	0.0391	0.0430
	hold ↑ → CKN	-0.0078	0.0000	0.0000
	hold ↓ → CKN	-0.0273	-0.0195	-0.0195
CKN	minpwl	0.8830	0.8830	0.8830
	minpwh	0.8830	0.8830	0.8830
SN	minpwl	0.8830	0.8830	0.8830
	recovery	-0.0234	-0.0234	-0.0195
	removal	0.0469	0.0508	0.0469

Cell Description

The SDFFNSRPQ cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), asynchronous active-high reset (R) and asynchronous active-low set (SN). Set (SN) is dominant over reset (R) if both are asserted.

Logic Symbol



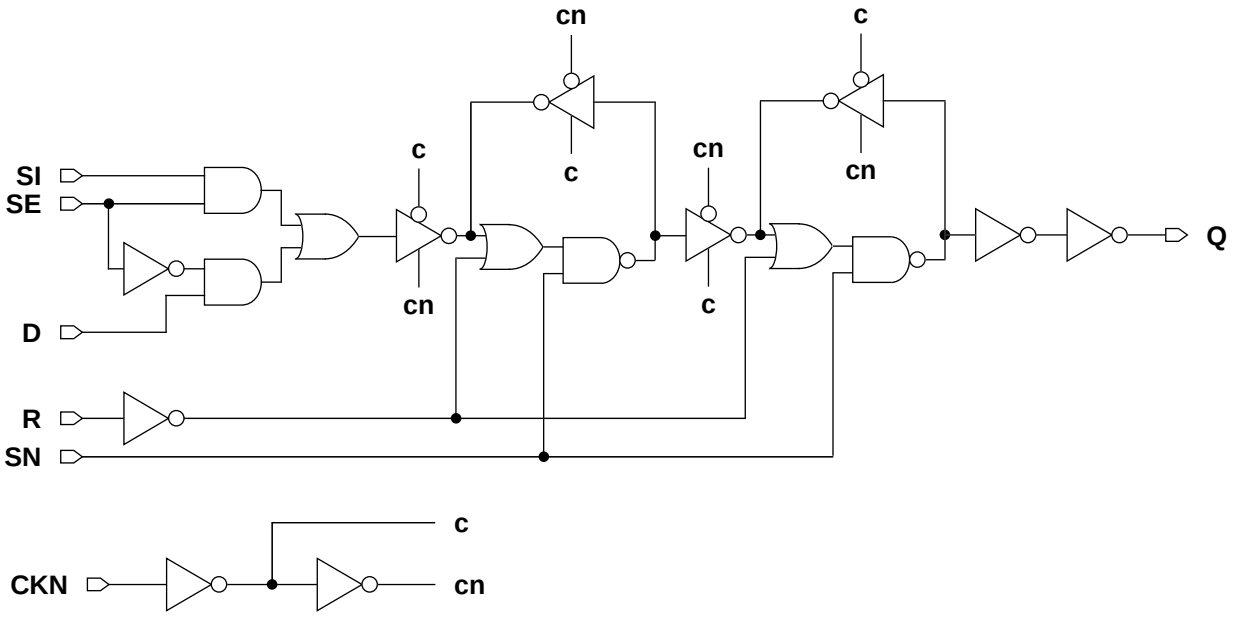
Function Table

SN	R	D	SI	SE	CKN	Q[n+1]
1	0	1	x	0	⎺_	1
1	0	0	x	0	⎺_	0
1	0	x	x	x	_/⎺	1
1	0	x	1	1	⎺_	1
1	0	x	0	1	⎺_	0
1	1	x	x	x	x	0
0	0	x	x	x	x	1
0	1	x	x	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFNSRPQX1MA10TR	2.00	7.00
SDFFNSRPQX2MA10TR	2.00	7.40
SDFFNSRPQX3MA10TR	2.00	7.60

Functional Schematic



AC Power

Pin	Power (uW/MHz)		
	X1P0M	X2P0M	X3P0M
SI	0.0066	0.0078	0.0082
SE	0.0071	0.0082	0.0085
D	0.0060	0.0071	0.0074
CKN	0.0048	0.0054	0.0059
SN	0.0018	0.0022	0.0024
R	0.0020	0.0024	0.0027
Q	0.0052	0.0071	0.0091

Pin Capacitance

Pin	Capacitance (pF)		
	X1P0M	X2P0M	X3P0M
SI	0.0007	0.0007	0.0007
SE	0.0023	0.0025	0.0025
D	0.0013	0.0016	0.0016
CKN	0.0010	0.0010	0.0011
SN	0.0026	0.0029	0.0028
R	0.0019	0.0021	0.0021

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)			K_{load} (ns/pF)		
	X1P0M	X2P0M	X3P0M	X1P0M	X2P0M	X3P0M
CKN → Q ↑	0.1121	0.1077	0.1084	2.3372	1.1523	0.7823
CKN → Q ↓	0.1083	0.1084	0.1072	1.4583	0.7165	0.4618
SN → Q ↑	0.0622	0.0680	0.0723	2.3337	1.1516	0.7821
SN → Q ↓	0.0746	0.0824	0.0885	1.4567	0.7159	0.4616
R → Q ↓	0.0727	0.0811	0.0869	1.4566	0.7159	0.4616

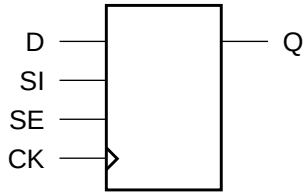
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)		
		X1P0M	**X2P0M**	**X3P0M**
SI	setup ↑ → CKN	0.0781	0.0820	0.0898
	setup ↓ → CKN	0.1289	0.1367	0.1406
	hold ↑ → CKN	-0.0273	-0.0352	-0.0391
	hold ↓ → CKN	-0.0781	-0.0781	-0.0781
SE	setup ↑ → CKN	0.1367	0.1445	0.1484
	setup ↓ → CKN	0.0625	0.0586	0.0586
	hold ↑ → CKN	-0.0234	-0.0352	-0.0391
	hold ↓ → CKN	-0.0195	-0.0195	-0.0195
D	setup ↑ → CKN	0.0430	0.0352	0.0391
	setup ↓ → CKN	0.0547	0.0469	0.0469
	hold ↑ → CKN	0.0000	0.0000	0.0000
	hold ↓ → CKN	-0.0273	-0.0234	-0.0234
CKN	minpwl	0.8830	0.8830	0.8830
	minpwh	0.8830	0.8830	0.8830
SN	minpwl	0.8830	0.8830	0.8830
	recovery	0.0000	-0.0078	-0.0039
	removal	0.0195	0.0273	0.0234
R	minpwh	0.8830	0.8830	0.8830
	recovery	-0.0078	-0.0117	-0.0078
	removal	0.0430	0.0430	0.0430

Cell Description

The SDFFQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE). The cell has a single output (Q).

Logic Symbol



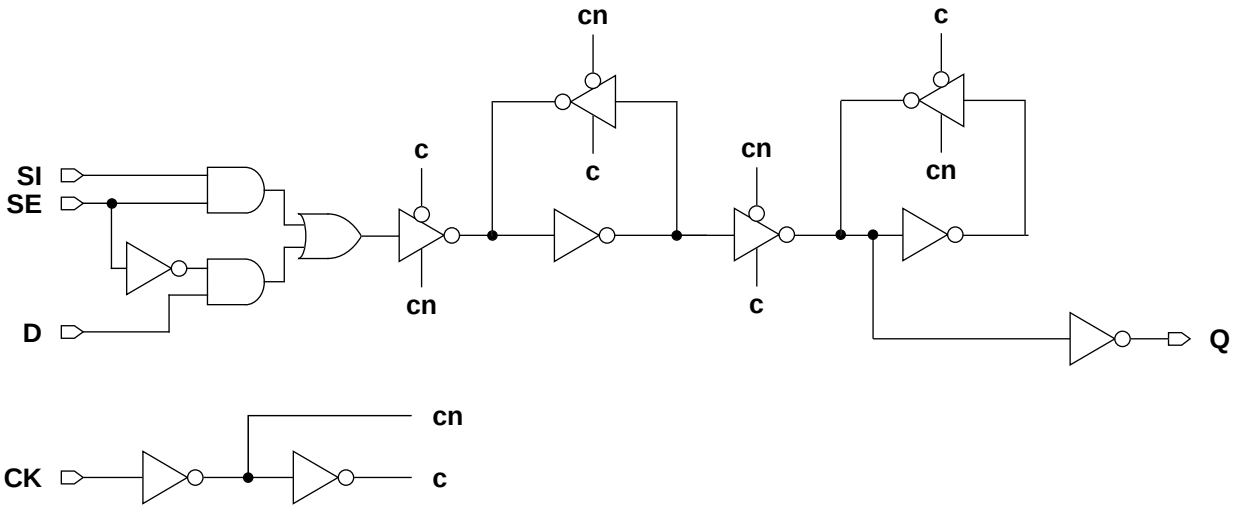
Function Table

D	SI	SE	CK	Q[n+1]
1	x	0	⎍	1
0	x	0	⎍	0
x	x	x	⎎	Q[n]
x	1	1	⎍	1
x	0	1	⎍	0

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFQX0P5MA10TR	2.00	5.00
SDFFQX1MA10TR	2.00	5.40
SDFFQX2MA10TR	2.00	5.60
SDFFQX3MA10TR	2.00	6.00
SDFFQX4MA10TR	2.00	6.60

Functional Schematic



AC Power

Pin	Power (uW/MHz)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
SI	0.0051	0.0065	0.0081	0.0092	0.0096
SE	0.0053	0.0063	0.0076	0.0082	0.0086
D	0.0046	0.0057	0.0070	0.0077	0.0081
CK	0.0036	0.0041	0.0047	0.0053	0.0057
Q	0.0032	0.0043	0.0059	0.0082	0.0108

Pin Capacitance

Pin	Capacitance (pF)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
SI	0.0006	0.0007	0.0007	0.0007	0.0007
SE	0.0020	0.0023	0.0024	0.0024	0.0024
D	0.0012	0.0014	0.0018	0.0018	0.0018
CK	0.0009	0.0009	0.0010	0.0011	0.0011

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
CK → Q ↑	0.0922	0.0795	0.0736	0.0736	0.0745
CK → Q ↓	0.1024	0.0867	0.0804	0.0820	0.0763

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)				
	X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
CK → Q ↑	4.1882	2.3320	1.1598	0.7824	0.5809
CK → Q ↓	2.5367	1.3338	0.6608	0.4570	0.3311

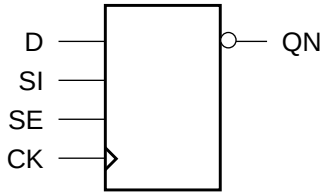
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)				
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
SI	setup ↑ → CK	0.0742	0.0820	0.0977	0.0977	0.1016
	setup ↓ → CK	0.1094	0.1016	0.1211	0.1328	0.1328
	hold ↑ → CK	-0.0469	-0.0547	-0.0625	-0.0664	-0.0664
	hold ↓ → CK	-0.0547	-0.0547	-0.0625	-0.0703	-0.0664
SE	setup ↑ → CK	0.1289	0.1172	0.1445	0.1523	0.1562
	setup ↓ → CK	0.0664	0.0586	0.0547	0.0547	0.0586
	hold ↑ → CK	-0.0469	-0.0508	-0.0625	-0.0625	-0.0625
	hold ↓ → CK	-0.0195	-0.0117	-0.0117	-0.0156	-0.0156
D	setup ↑ → CK	0.0469	0.0352	0.0273	0.0312	0.0312
	setup ↓ → CK	0.0586	0.0391	0.0391	0.0430	0.0430
	hold ↑ → CK	-0.0273	-0.0195	-0.0156	-0.0156	-0.0156
	hold ↓ → CK	-0.0234	-0.0117	-0.0117	-0.0156	-0.0156
CK	minpwh	0.8830	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830

Cell Description

The SDFFQN cell is a positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE). The cell has a single output (QN).

Logic Symbol



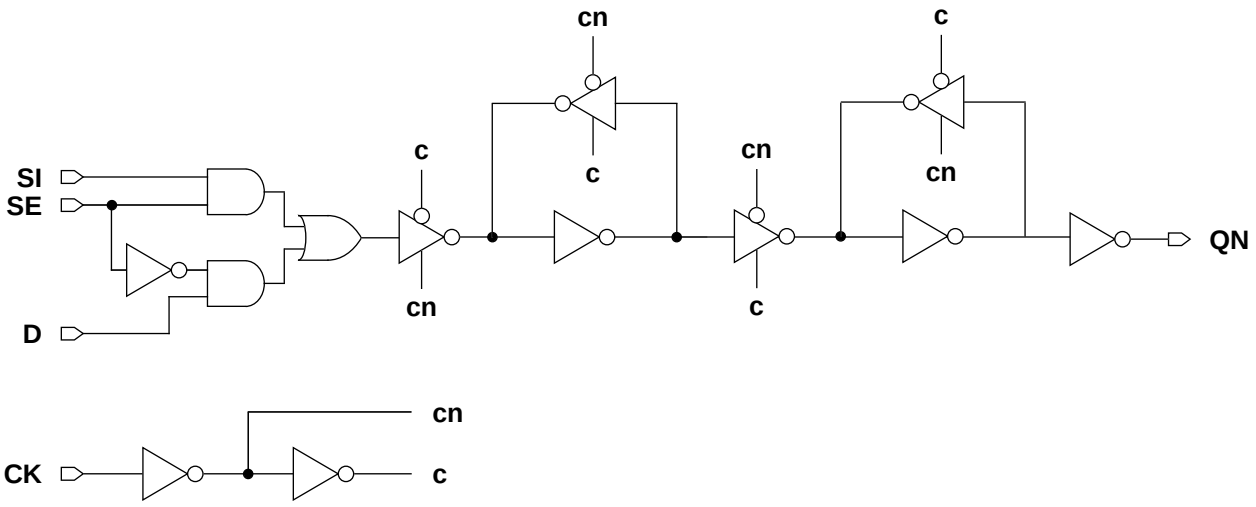
Function Table

D	SI	SE	CK	QN[n+1]
1	x	0	↑	0
0	x	0	↑	1
x	x	x	↓	QN[n]
x	1	1	↑	0
x	0	1	↑	1

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFQNX0P5MA10TR	2.00	5.00
SDFFQNX1MA10TR	2.00	5.40
SDFFQNX2MA10TR	2.00	5.60
SDFFQNX3MA10TR	2.00	6.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)			
	X0P5M	X1P0M	X2P0M	X3P0M
SI	0.0051	0.0068	0.0081	0.0094
SE	0.0052	0.0064	0.0074	0.0080
D	0.0046	0.0059	0.0070	0.0078
CK	0.0035	0.0040	0.0046	0.0055
QN	0.0033	0.0039	0.0059	0.0076

Pin Capacitance

Pin	Capacitance (pF)			
	X0P5M	X1P0M	X2P0M	X3P0M
SI	0.0006	0.0007	0.0007	0.0007
SE	0.0020	0.0023	0.0024	0.0024
D	0.0012	0.0014	0.0018	0.0018
CK	0.0009	0.0009	0.0010	0.0012

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X0P5M	X1P0M	X2P0M	X3P0M	X0P5M	X1P0M	X2P0M	X3P0M
CK → QN ↑	0.0878	0.0746	0.0724	0.0653	4.2610	2.3449	1.1715	0.7900
CK → QN ↓	0.0868	0.0720	0.0756	0.0712	2.9475	1.5475	0.7844	0.5380

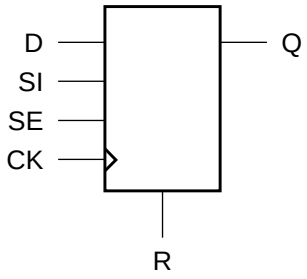
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X0P5M	X1P0M	X2P0M	X3P0M
SI	setup ↑ → CK	0.0781	0.0859	0.1016	0.1094
	setup ↓ → CK	0.1133	0.1094	0.1289	0.1367
	hold ↑ → CK	-0.0469	-0.0547	-0.0625	-0.0625
	hold ↓ → CK	-0.0508	-0.0508	-0.0586	-0.0586
SE	setup ↑ → CK	0.1289	0.1250	0.1484	0.1562
	setup ↓ → CK	0.0703	0.0586	0.0586	0.0586
	hold ↑ → CK	-0.0469	-0.0508	-0.0586	-0.0586
	hold ↓ → CK	-0.0156	-0.0117	-0.0117	-0.0117
D	setup ↑ → CK	0.0469	0.0352	0.0312	0.0352
	setup ↓ → CK	0.0586	0.0430	0.0391	0.0430
	hold ↑ → CK	-0.0273	-0.0195	-0.0156	-0.0156
	hold ↓ → CK	-0.0195	-0.0117	-0.0117	-0.0117
CK	minpwh	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830

Cell Description

The SDFFRPQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-high reset (R). The cell has a single inverted output (Q).

Logic Symbol



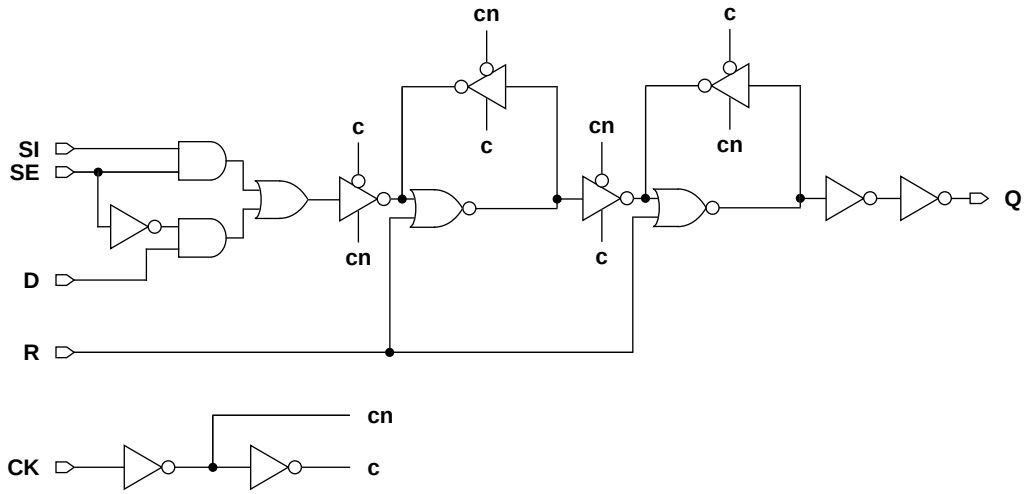
Function Table

R	D	SI	SE	CK	Q
1	x	x	x	⎍	0
0	1	x	0	⎍	1
0	0	x	0	⎍	0
0	x	0	1	⎍	0
0	x	1	1	⎍	1
0	x	x	x	⎎	Q

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFRPQX0P5MA10TR	2.00	5.80
SDFFRPQX1MA10TR	2.00	5.80
SDFFRPQX2MA10TR	2.00	6.40
SDFFRPQX3MA10TR	2.00	6.60
SDFFRPQX4MA10TR	2.00	7.40

Functional Schematic



AC Power

Pin	Power (uW/MHz)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
SI	0.0053	0.0069	0.0082	0.0086	0.0089
SE	0.0057	0.0075	0.0089	0.0094	0.0098
D	0.0047	0.0061	0.0073	0.0076	0.0080
CK	0.0039	0.0044	0.0051	0.0056	0.0059
R	0.0015	0.0017	0.0022	0.0024	0.0027
Q	0.0035	0.0048	0.0065	0.0084	0.0110

Pin Capacitance

Pin	Capacitance (pF)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
SI	0.0007	0.0007	0.0007	0.0007	0.0007
SE	0.0020	0.0022	0.0024	0.0024	0.0024
D	0.0011	0.0014	0.0018	0.0018	0.0018
CK	0.0008	0.0009	0.0010	0.0011	0.0011
R	0.0015	0.0016	0.0018	0.0018	0.0019

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
CK → Q ↑	0.1055	0.0895	0.0799	0.0820	0.0792
CK → Q ↓	0.1145	0.0941	0.0857	0.0894	0.0860
R → Q ↓	0.0597	0.0516	0.0558	0.0632	0.0707

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
CK → Q ↑	4.1638	2.3356	1.1474	0.7776	0.5842
CK → Q ↓	2.6356	1.3329	0.6515	0.4548	0.3347
R → Q ↓	2.6236	1.3312	0.6513	0.4547	0.3348

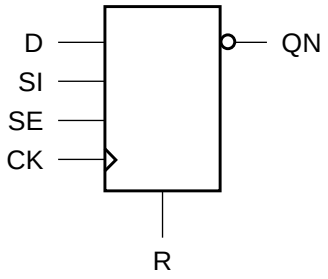
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)				
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
SI	setup ↑ → CK	0.0938	0.0898	0.1016	0.1055	0.1094
	setup ↓ → CK	0.1172	0.1133	0.1328	0.1367	0.1445
	hold ↑ → CK	-0.0508	-0.0586	-0.0664	-0.0664	-0.0625
	hold ↓ → CK	-0.0586	-0.0664	-0.0742	-0.0781	-0.0781
SE	setup ↑ → CK	0.1289	0.1289	0.1523	0.1562	0.1641
	setup ↓ → CK	0.0859	0.0625	0.0625	0.0625	0.0664
	hold ↑ → CK	-0.0469	-0.0547	-0.0625	-0.0625	-0.0586
	hold ↓ → CK	-0.0234	-0.0195	-0.0156	-0.0156	-0.0195
D	setup ↑ → CK	0.0625	0.0430	0.0352	0.0352	0.0391
	setup ↓ → CK	0.0625	0.0508	0.0430	0.0430	0.0469
	hold ↑ → CK	-0.0273	-0.0195	-0.0156	-0.0156	-0.0156
	hold ↓ → CK	-0.0273	-0.0195	-0.0156	-0.0156	-0.0195
CK	minpwh	0.8830	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830
R	minpwh	0.8830	0.8830	0.8830	0.8830	0.8830
	recovery	0.0234	0.0000	0.0039	0.0039	0.0039
	removal	0.0117	0.0391	0.0391	0.0430	0.0352

Cell Description

The SDFFRPQN cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-high reset (R). The cell has a single inverted output (QN).

Logic Symbol



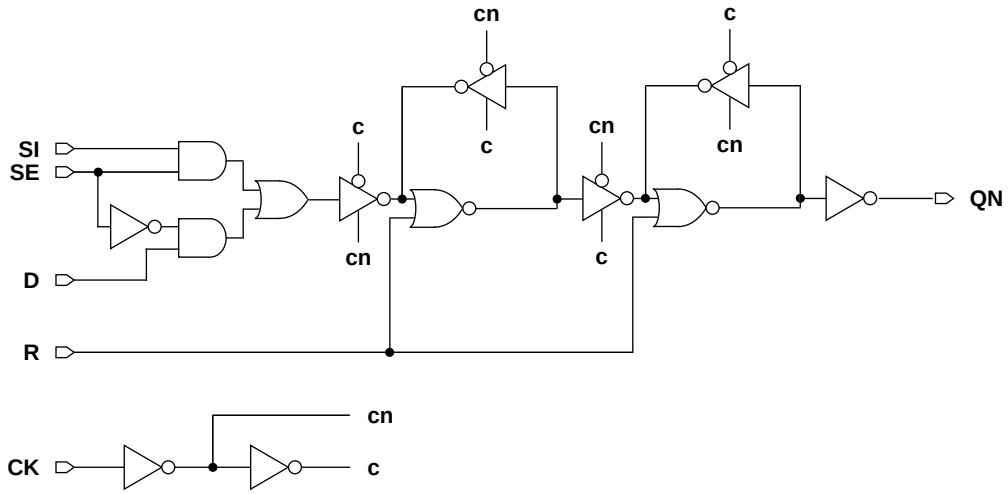
Function Table

R	D	SI	SE	CK	QN
1	x	x	x	⎍	1
0	1	x	0	⎍	0
0	0	x	0	⎍	1
0	x	0	1	⎍	1
0	x	1	1	⎍	0
0	x	x	x	⎍	QN

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFRPQNX0P5MA10TR	2.00	5.80
SDFFRPQNX1MA10TR	2.00	5.80
SDFFRPQNX2MA10TR	2.00	6.40
SDFFRPQNX3MA10TR	2.00	7.00

Functional Schematic



AC Power

Pin	Power (uW/MHz)			
	X0P5M	X1P0M	X2P0M	X3P0M
SI	0.0053	0.0069	0.0082	0.0086
SE	0.0056	0.0075	0.0087	0.0092
D	0.0048	0.0062	0.0073	0.0077
CK	0.0038	0.0043	0.0048	0.0056
R	0.0014	0.0015	0.0020	0.0022
QN	0.0038	0.0046	0.0068	0.0093

Pin Capacitance

Pin	Capacitance (pF)			
	X0P5M	X1P0M	X2P0M	X3P0M
SI	0.0007	0.0007	0.0007	0.0007
SE	0.0020	0.0023	0.0024	0.0025
D	0.0011	0.0015	0.0018	0.0018
CK	0.0009	0.0009	0.0010	0.0012
R	0.0015	0.0016	0.0018	0.0019

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X0P5M	X1P0M	X2P0M	X3P0M	X0P5M	X1P0M	X2P0M	X3P0M
CK → QN ↑	0.0931	0.0809	0.0747	0.0738	4.2525	2.3532	1.1673	0.7923
CK → QN ↓	0.0995	0.0864	0.0836	0.0874	2.9953	1.5847	0.7513	0.5508
R → QN ↑	0.0359	0.0389	0.0501	0.0600	4.1897	2.3428	1.1670	0.7916

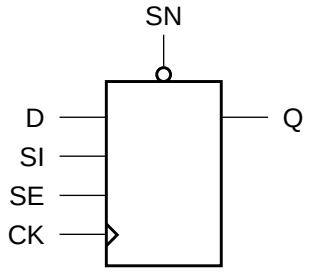
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**
SI	setup ↑ → CK	0.0977	0.0938	0.1055	0.1094
	setup ↓ → CK	0.1172	0.1133	0.1367	0.1445
	hold ↑ → CK	-0.0508	-0.0586	-0.0625	-0.0547
	hold ↓ → CK	-0.0547	-0.0625	-0.0703	-0.0703
SE	setup ↑ → CK	0.1328	0.1328	0.1562	0.1641
	setup ↓ → CK	0.0859	0.0625	0.0625	0.0664
	hold ↑ → CK	-0.0469	-0.0547	-0.0586	-0.0508
	hold ↓ → CK	-0.0234	-0.0156	-0.0117	-0.0156
D	setup ↑ → CK	0.0664	0.0391	0.0352	0.0391
	setup ↓ → CK	0.0664	0.0469	0.0430	0.0469
	hold ↑ → CK	-0.0234	-0.0156	-0.0156	-0.0117
	hold ↓ → CK	-0.0234	-0.0156	-0.0117	-0.0156
CK	minpwh	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830
R	minpwh	0.8830	0.8830	0.8830	0.8830
	recovery	0.0273	0.0039	0.0000	0.0039
	removal	0.0117	0.0352	0.0352	0.0312

Cell Description

The SDFFSQ cell is a high-speed, positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN). The cell has a single output (Q).

Logic Symbol



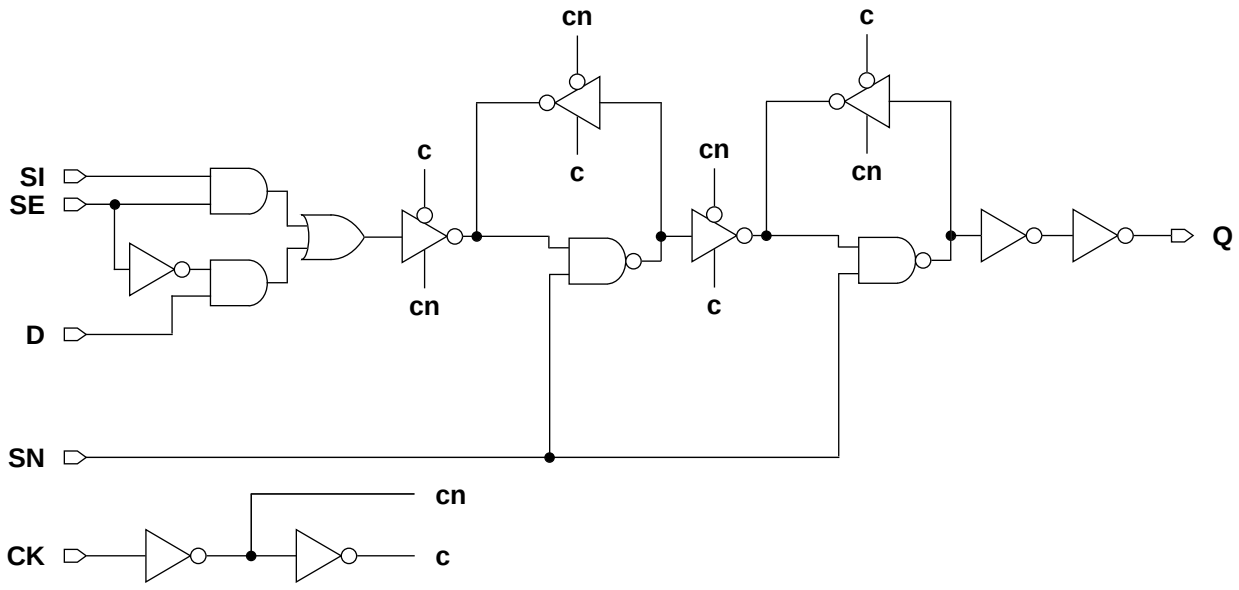
Function Table

SN	D	SI	SE	CK	Q[n+1]
1	1	x	0	↑	1
1	0	x	0	↑	0
1	x	x	x	↓	Q[n]
1	x	1	1	↑	1
1	x	0	1	↑	0
0	x	x	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFSQX0P5MA10TR	2.00	6.20
SDFFSQX1MA10TR	2.00	6.20
SDFFSQX2MA10TR	2.00	6.40
SDFFSQX3MA10TR	2.00	6.80
SDFFSQX4MA10TR	2.00	7.40

Functional Schematic



AC Power

Pin	Power (uW/MHz)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
SI	0.0056	0.0065	0.0084	0.0088	0.0091
SE	0.0054	0.0070	0.0088	0.0093	0.0097
D	0.0050	0.0059	0.0075	0.0078	0.0081
CK	0.0037	0.0042	0.0049	0.0055	0.0058
SN	0.0014	0.0019	0.0024	0.0026	0.0029
Q	0.0035	0.0049	0.0065	0.0083	0.0111

Pin Capacitance

Pin	Capacitance (pF)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
SI	0.0007	0.0007	0.0007	0.0007	0.0007
SE	0.0021	0.0022	0.0024	0.0024	0.0024
D	0.0011	0.0013	0.0018	0.0018	0.0018
CK	0.0009	0.0009	0.0010	0.0011	0.0012
SN	0.0018	0.0022	0.0027	0.0027	0.0026

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
CK → Q ↑	0.0991	0.0860	0.0772	0.0778	0.0771
CK → Q ↓	0.1085	0.0950	0.0874	0.0898	0.0856
SN → Q ↑	0.0680	0.0640	0.0673	0.0713	0.0782

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
CK → Q ↑	4.2368	2.3328	1.1602	0.7816	0.5811
CK → Q ↓	2.5781	1.3345	0.6625	0.4580	0.3327
SN → Q ↑	4.2394	2.3328	1.1602	0.7818	0.5810

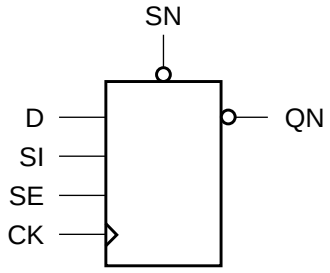
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)				
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**	**X4P0M**
SI	setup ↑ → CK	0.0820	0.0859	0.1055	0.1055	0.1133
	setup ↓ → CK	0.1133	0.0977	0.1211	0.1250	0.1328
	hold ↑ → CK	-0.0508	-0.0586	-0.0703	-0.0703	-0.0703
	hold ↓ → CK	-0.0547	-0.0508	-0.0625	-0.0664	-0.0664
SE	setup ↑ → CK	0.1289	0.1172	0.1445	0.1484	0.1523
	setup ↓ → CK	0.0703	0.0625	0.0586	0.0586	0.0625
	hold ↑ → CK	-0.0469	-0.0547	-0.0664	-0.0703	-0.0664
	hold ↓ → CK	-0.0195	-0.0156	-0.0117	-0.0156	-0.0156
D	setup ↑ → CK	0.0469	0.0391	0.0312	0.0352	0.0391
	setup ↓ → CK	0.0586	0.0469	0.0391	0.0391	0.0430
	hold ↑ → CK	-0.0234	-0.0195	-0.0156	-0.0156	-0.0195
	hold ↓ → CK	-0.0195	-0.0156	-0.0117	-0.0156	-0.0156
CK	minpwh	0.8830	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830
SN	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830
	recovery	-0.0273	-0.0312	-0.0312	-0.0312	-0.0234
	removal	0.0508	0.0586	0.0625	0.0625	0.0508

Cell Description

The SDFFSQN cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN). The cell has a single output (QN).

Logic Symbol



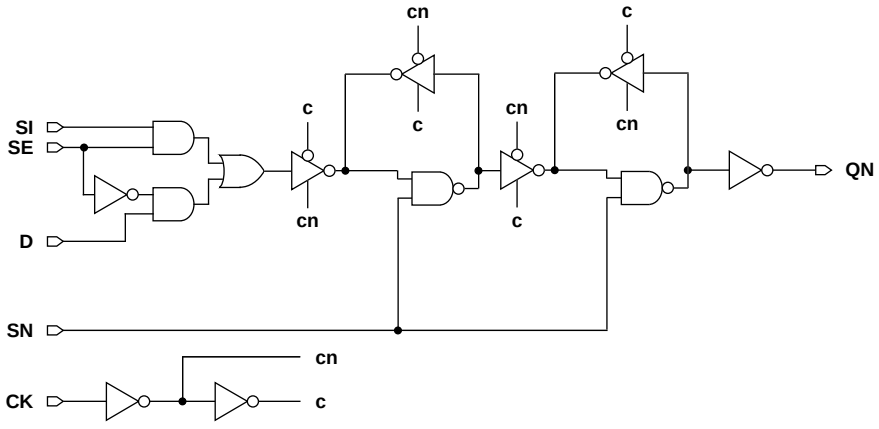
Function Table

SN	D	SI	SE	CK	QN
1	1	x	0	⎍	0
1	0	x	0	⎍	1
1	x	x	x	⎎	QN[n]
1	x	1	1	⎍	0
1	x	0	1	⎍	1
0	x	x	x	x	0

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFSQNX0P5MA10TR	2.00	6.20
SDFFSQNX1MA10TR	2.00	6.20
SDFFSQNX2MA10TR	2.00	6.40
SDFFSQNX3MA10TR	2.00	6.80

Functional Schematic



AC Power

Pin	Power (uW/MHz)			
	X0P5M	X1P0M	X2P0M	X3P0M
SI	0.0057	0.0070	0.0083	0.0087
SE	0.0054	0.0073	0.0086	0.0090
D	0.0051	0.0062	0.0075	0.0078
CK	0.0036	0.0042	0.0048	0.0055
SN	0.0015	0.0019	0.0024	0.0027
QN	0.0036	0.0043	0.0065	0.0090

Pin Capacitance

Pin	Capacitance (pF)			
	X0P5M	X1P0M	X2P0M	X3P0M
SI	0.0007	0.0007	0.0007	0.0007
SE	0.0021	0.0022	0.0024	0.0024
D	0.0011	0.0013	0.0018	0.0018
CK	0.0009	0.0009	0.0010	0.0012
SN	0.0019	0.0025	0.0027	0.0027

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X0P5M	X1P0M	X2P0M	X3P0M	X0P5M	X1P0M	X2P0M	X3P0M
CK → QN ↑	0.0930	0.0807	0.0805	0.0781	4.3121	2.3485	1.1755	0.7955
CK → QN ↓	0.0896	0.0772	0.0805	0.0831	3.0691	1.5367	0.7699	0.5320
SN → QN ↓	0.0536	0.0558	0.0701	0.0844	2.8649	1.4957	0.7563	0.5243

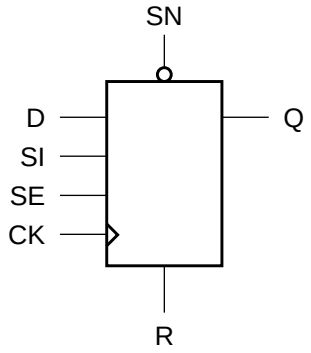
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)			
		X0P5M	**X1P0M**	**X2P0M**	**X3P0M**
SI	setup ↑ → CK	0.0859	0.0938	0.1055	0.1094
	setup ↓ → CK	0.1094	0.1016	0.1211	0.1289
	hold ↑ → CK	-0.0508	-0.0625	-0.0703	-0.0664
	hold ↓ → CK	-0.0469	-0.0469	-0.0547	-0.0586
SE	setup ↑ → CK	0.1250	0.1172	0.1445	0.1523
	setup ↓ → CK	0.0742	0.0664	0.0586	0.0625
	hold ↑ → CK	-0.0469	-0.0586	-0.0664	-0.0664
	hold ↓ → CK	-0.0195	-0.0156	-0.0078	-0.0117
D	setup ↑ → CK	0.0508	0.0430	0.0312	0.0352
	setup ↓ → CK	0.0625	0.0469	0.0391	0.0430
	hold ↑ → CK	-0.0273	-0.0195	-0.0156	-0.0156
	hold ↓ → CK	-0.0234	-0.0156	-0.0078	-0.0117
CK	minpwh	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830
SN	minpwl	0.8830	0.8830	0.8830	0.8830
	recovery	-0.0312	-0.0352	-0.0312	-0.0234
	removal	0.0547	0.0664	0.0625	0.0547

Cell Description

The SDFFSRPQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (R) and set (SN). Set (SN) dominates reset (R).

Logic Symbol



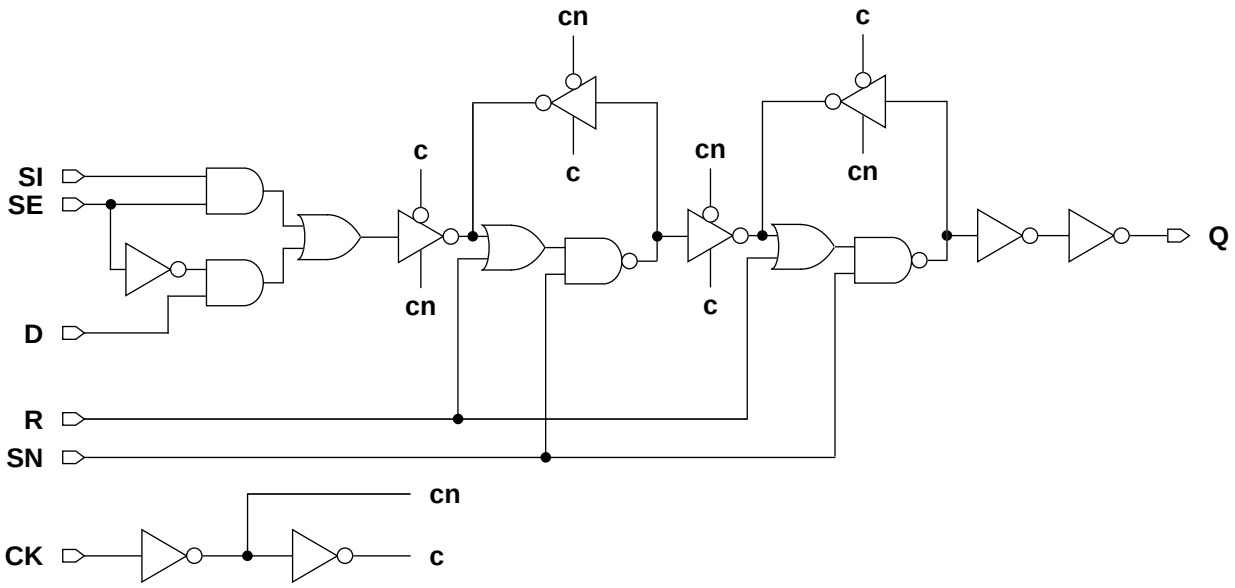
Function Table

SN	R	D	SI	SE	CK	Q
1	0	1	x	0	⎍	1
1	0	0	x	0	⎍	0
1	0	x	x	x	⎎	1
1	0	x	1	1	⎍	1
1	0	x	0	1	⎍	0
1	1	x	x	x	x	0
0	0	x	x	x	x	1
0	1	x	x	x	x	1

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFSRPQX0P5MA10TR	2.00	7.00
SDFFSRPQX1MA10TR	2.00	7.00
SDFFSRPQX2MA10TR	2.00	7.20
SDFFSRPQX3MA10TR	2.00	7.60
SDFFSRPQX4MA10TR	2.00	8.20

Functional Schematic



AC Power

Pin	Power (uW/MHz)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
SI	0.0054	0.0070	0.0082	0.0086	0.0089
SE	0.0060	0.0075	0.0087	0.0091	0.0095
D	0.0049	0.0063	0.0074	0.0078	0.0081
CK	0.0051	0.0056	0.0064	0.0070	0.0073
SN	0.0014	0.0021	0.0024	0.0026	0.0029
R	0.0015	0.0022	0.0026	0.0029	0.0032
Q	0.0041	0.0054	0.0072	0.0090	0.0120

Pin Capacitance

Pin	Capacitance (pF)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
SI	0.0007	0.0007	0.0007	0.0007	0.0007
SE	0.0021	0.0023	0.0024	0.0024	0.0025
D	0.0011	0.0014	0.0018	0.0018	0.0018
CK	0.0009	0.0010	0.0011	0.0011	0.0011
SN	0.0023	0.0028	0.0029	0.0029	0.0029
R	0.0016	0.0020	0.0021	0.0022	0.0023

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
CK → Q ↑	0.1188	0.0970	0.0926	0.0911	0.0894
CK → Q ↓	0.1317	0.1026	0.1011	0.1012	0.0989
SN → Q ↑	0.0699	0.0694	0.0752	0.0767	0.0817
SN → Q ↓	0.0753	0.0666	0.0751	0.0821	0.0913
R → Q ↓	0.0737	0.0648	0.0736	0.0804	0.0895

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)				
	X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
CK → Q ↑	4.2379	2.3323	1.1542	0.7824	0.5853
CK → Q ↓	2.6099	1.3465	0.6737	0.4591	0.3331
SN → Q ↑	4.2355	2.3330	1.1542	0.7825	0.5851
SN → Q ↓	2.5921	1.3445	0.6733	0.4590	0.3332
R → Q ↓	2.5922	1.3445	0.6732	0.4590	0.3331

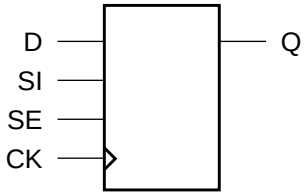
Timing Constraints at 25°C,1.0V, Typical Process

Pin	Requirement	Interval (ns)				
		X0P5M	X1P0M	X2P0M	X3P0M	X4P0M
SI	setup ↑ → CK	0.0977	0.0977	0.1094	0.1133	0.1172
	setup ↓ → CK	0.1250	0.1250	0.1445	0.1445	0.1523
	hold ↑ → CK	-0.0508	-0.0547	-0.0586	-0.0586	-0.0547
	hold ↓ → CK	-0.0664	-0.0625	-0.0703	-0.0742	-0.0703
SE	setup ↑ → CK	0.1367	0.1406	0.1641	0.1641	0.1719
	setup ↓ → CK	0.0859	0.0664	0.0664	0.0703	0.0742
	hold ↑ → CK	-0.0469	-0.0508	-0.0547	-0.0586	-0.0508
	hold ↓ → CK	-0.0273	-0.0156	-0.0117	-0.0156	-0.0156
D	setup ↑ → CK	0.0664	0.0469	0.0391	0.0430	0.0469
	setup ↓ → CK	0.0664	0.0508	0.0469	0.0469	0.0547
	hold ↑ → CK	-0.0273	-0.0195	-0.0117	-0.0156	-0.0117
	hold ↓ → CK	-0.0273	-0.0156	-0.0117	-0.0156	-0.0156
CK	minpwh	0.8830	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830
SN	minpwl	0.8830	0.8830	0.8830	0.8830	0.8830
	recovery	-0.0156	-0.0156	-0.0117	-0.0117	-0.0039
	removal	0.0352	0.0352	0.0352	0.0312	0.0234
R	minpwh	0.8830	0.8830	0.8830	0.8830	0.8830
	recovery	0.0234	0.0117	0.0117	0.0156	0.0195
	removal	0.0156	0.0234	0.0234	0.0195	0.0156

Cell Description

The SDFFYQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI) and active-high scan enable (SE). The cell has a single output (Q) and overdriven feedback loops to increase mean time between failure (MTBF) due to metastability.

Logic Symbol



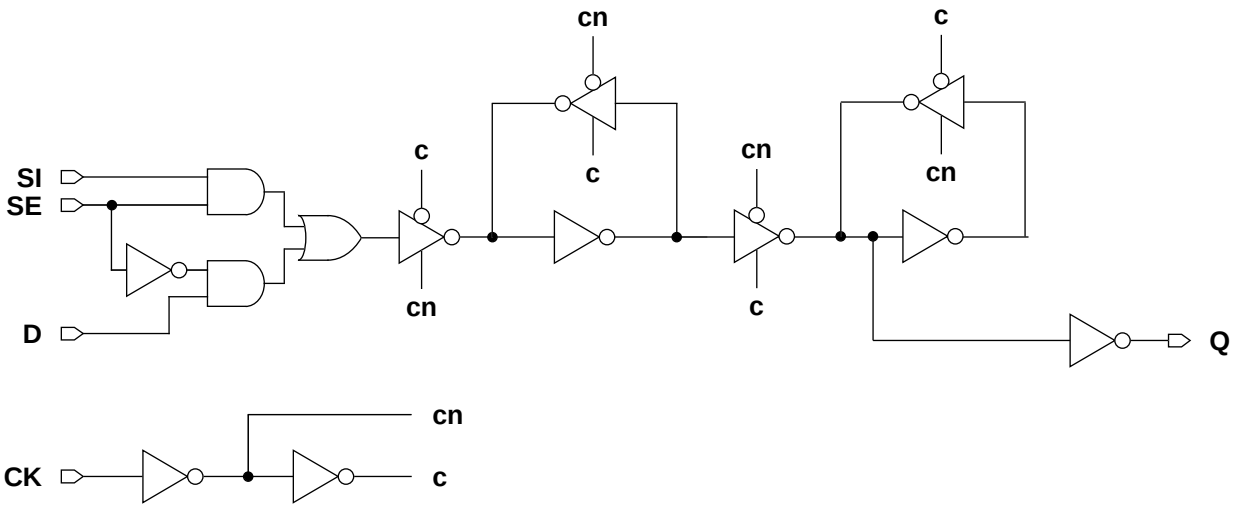
Function Table

D	SI	SE	CK	Q[n+1]
1	x	0	↑	1
0	x	0	↑	0
x	x	x	↓	Q[n]
x	1	1	↑	1
x	0	1	↑	0

Cell Size

Drive Strength	Height (um)	Width (um)
SDFFYQX1MA10TR	2.00	5.20
SDFFYQX2MA10TR	2.00	5.60
SDFFYQX3MA10TR	2.00	6.00
SDFFYQX4MA10TR	2.00	6.40

Functional Schematic



AC Power

Pin	Power (uW/MHz)			
	X1P0M	X2P0M	X3P0M	X4P0M
SI	0.0074	0.0089	0.0091	0.0099
SE	0.0072	0.0083	0.0091	0.0095
D	0.0064	0.0077	0.0078	0.0085
CK	0.0053	0.0066	0.0064	0.0074
Q	0.0049	0.0066	0.0091	0.0120

Pin Capacitance

Pin	Capacitance (pF)			
	X1P0M	X2P0M	X3P0M	X4P0M
SI	0.0007	0.0007	0.0007	0.0007
SE	0.0024	0.0025	0.0025	0.0025
D	0.0015	0.0018	0.0018	0.0018
CK	0.0013	0.0017	0.0012	0.0014

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)				K_{load} (ns/pF)			
	X1P0M	X2P0M	X3P0M	X4P0M	X1P0M	X2P0M	X3P0M	X4P0M
CK → Q ↑	0.0756	0.0665	0.0752	0.0710	2.3407	1.1620	0.7832	0.5845
CK → Q ↓	0.0793	0.0723	0.0850	0.0756	1.4560	0.6637	0.4582	0.3344

Timing Constraints at 25°C,1.0V, Typical Process

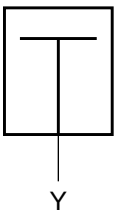
Pin	Requirement	Interval (ns)			
		X1P0M	X2P0M	X3P0M	X4P0M
SI	setup ↑ → CK	0.0898	0.1055	0.1016	0.1055
	setup ↓ → CK	0.1172	0.1367	0.1406	0.1445
	hold ↑ → CK	-0.0625	-0.0703	-0.0703	-0.0703
	hold ↓ → CK	-0.0703	-0.0781	-0.0820	-0.0781
SE	setup ↑ → CK	0.1328	0.1562	0.1602	0.1641
	setup ↓ → CK	0.0625	0.0625	0.0586	0.0625
	hold ↑ → CK	-0.0625	-0.0703	-0.0664	-0.0664
	hold ↓ → CK	-0.0195	-0.0195	-0.0156	-0.0195
D	setup ↑ → CK	0.0391	0.0352	0.0352	0.0391
	setup ↓ → CK	0.0469	0.0469	0.0430	0.0469
	hold ↑ → CK	-0.0234	-0.0195	-0.0195	-0.0195
	hold ↓ → CK	-0.0195	-0.0195	-0.0156	-0.0195
CK	minpwh	0.8830	0.8830	0.8830	0.8830
	minpwl	0.8830	0.8830	0.8830	0.8830

Cell Description

The TIEHI cell drives the output (Y) to a logic high. The output is driven through diffusion and not tied directly to the power rail to provide some ESD protection. The output (Y) is represented by the logic equation:

$Y = 1$

Logic Symbol



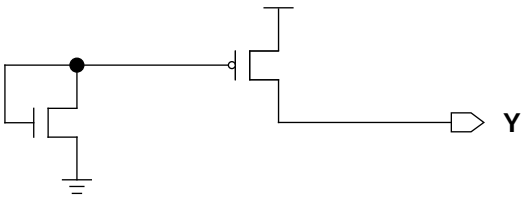
Function Table

Y
1

Cell Size

Drive Strength	Height (um)	Width (um)
TIEHIX1MA10TR	2.00	0.80

Functional Schematic

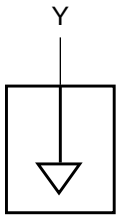


Cell Description

The TIELO cell drives the output (Y) to a logic low. The output is driven through diffusion and not tied directly to the power rail to provide some ESD protection. The output (Y) is represented by the logic equation:

$Y = 0$

Logic Symbol



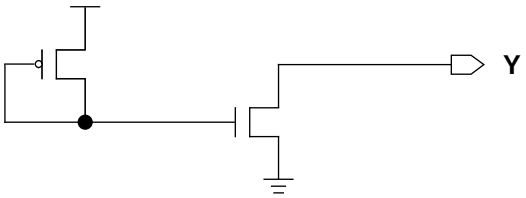
Function Table

Y
0

Cell Size

Drive Strength	Height (um)	Width (um)
TIELOX1MA10TR	2.00	0.80

Functional Schematic

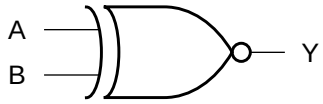


Cell Description

The XNOR2 cell provides a logical EXCLUSIVE NOR of two inputs (A,B). The output (Y) is represented by the logic equation:

$Y = (A \bullet B) + (\overline{A} \bullet \overline{B})$

Logic Symbol



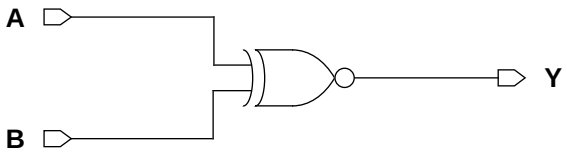
Function Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
XNOR2X0P5MA10TR	2.00	2.00
XNOR2X0P7MA10TR	2.00	2.00
XNOR2X1MA10TR	2.00	2.00
XNOR2X1P4MA10TR	2.00	3.20
XNOR2X2MA10TR	2.00	3.60
XNOR2X3MA10TR	2.00	4.00
XNOR2X4MA10TR	2.00	6.20

Functional Schematic



AC Power

Pin	Power (uW/MHz)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A	0.0033	0.0038	0.0046	0.0067	0.0086	0.0119	0.0165
B	0.0035	0.0043	0.0054	0.0084	0.0110	0.0156	0.0215

Pin Capacitance

Pin	Capacitance (pF)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A	0.0020	0.0021	0.0024	0.0030	0.0041	0.0054	0.0073
B	0.0011	0.0014	0.0017	0.0026	0.0033	0.0049	0.0064

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A → Y ↑	0.0173	0.0164	0.0155	0.0188	0.0171	0.0150	0.0157
A → Y ↓	0.0198	0.0184	0.0176	0.0200	0.0183	0.0165	0.0176
B → Y ↑	0.0342	0.0297	0.0265	0.0359	0.0283	0.0261	0.0271
B → Y ↓	0.0357	0.0321	0.0291	0.0293	0.0285	0.0267	0.0276

Delays at 25°C,1.0V, Typical Process (Cont'd.)

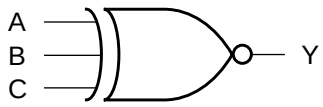
Description	K_{load} (ns/pF)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A → Y ↑	6.7218	5.0666	3.6681	3.2709	1.8264	1.1996	0.9026
A → Y ↓	4.6670	3.4315	2.4373	1.7550	1.2963	0.8375	0.6375
B → Y ↑	6.6934	5.0166	3.6357	3.2974	1.8253	1.2070	0.9047
B → Y ↓	4.7272	3.4705	2.4395	1.8042	1.2840	0.8316	0.6289

Cell Description

The XNOR3 cell provides a logical EXCLUSIVE NOR of three inputs (A,B,C). The output (Y) is represented by the following equation:

$Y = \overline{A \oplus B \oplus C}$

Logic Symbol



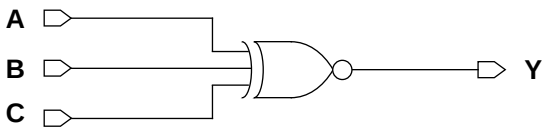
Function Table

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
XNOR3X0P5MA10TR	2.00	3.80
XNOR3X0P7MA10TR	2.00	3.80
XNOR3X1MA10TR	2.00	3.80
XNOR3X1P4MA10TR	2.00	6.00
XNOR3X2MA10TR	2.00	6.80
XNOR3X3MA10TR	2.00	8.00
XNOR3X4MA10TR	2.00	10.20

Functional Schematic



AC Power

Pin	Power (uW/MHz)						
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M
A	0.0044	0.0055	0.0065	0.0083	0.0110	0.0153	0.0192
B	0.0077	0.0091	0.0107	0.0153	0.0201	0.0266	0.0346
C	0.0087	0.0109	0.0128	0.0186	0.0238	0.0328	0.0424

Pin Capacitance

Pin	Capacitance (pF)						
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M
A	0.0015	0.0017	0.0018	0.0023	0.0027	0.0037	0.0045
B	0.0020	0.0024	0.0027	0.0035	0.0046	0.0059	0.0078
C	0.0012	0.0015	0.0017	0.0026	0.0031	0.0047	0.0059

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)						
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M
A → Y ↑	0.0477	0.0443	0.0444	0.0415	0.0433	0.0395	0.0395
A → Y ↓	0.0458	0.0421	0.0426	0.0413	0.0430	0.0406	0.0401
B → Y ↑	0.0780	0.0703	0.0694	0.0725	0.0705	0.0646	0.0639
B → Y ↓	0.0893	0.0803	0.0816	0.0798	0.0793	0.0712	0.0713
C → Y ↑	0.0929	0.0852	0.0823	0.0830	0.0816	0.0743	0.0735
C → Y ↓	0.1034	0.0947	0.0932	0.0898	0.0897	0.0809	0.0810

Delays at 25°C,1.0V, Typical Process (Cont'd.)

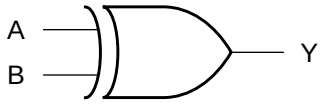
Description	K_{load} (ns/pF)						
	X0P5M	X0P7M	X1P0M	X1P4M	X2P0M	X3P0M	X4P0M
A → Y ↑	4.5688	3.3407	2.4079	1.6438	1.1866	0.7861	0.5960
A → Y ↓	2.9777	2.1359	1.5454	1.0527	0.7699	0.5127	0.3817
B → Y ↑	4.5300	3.3142	2.3881	1.6322	1.1783	0.7818	0.5923
B → Y ↓	3.0487	2.1834	1.5733	1.0766	0.7846	0.5178	0.3859
C → Y ↑	4.5297	3.3142	2.3882	1.6321	1.1782	0.7818	0.5923
C → Y ↓	3.0491	2.1837	1.5735	1.0769	0.7847	0.5185	0.3859

Cell Description

The XOR2 cell provides a logical EXCLUSIVE OR of two inputs (A,B). The output (Y) is represented by the logic equation:

$Y = (A \bullet \overline{B}) + (\overline{A} \bullet B)$

Logic Symbol



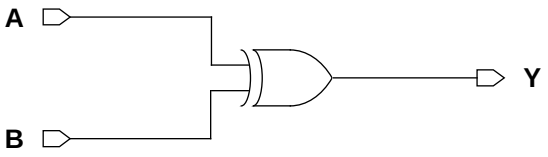
Function Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Cell Size

Drive Strength	Height (um)	Width (um)
XOR2X0P5MA10TR	2.00	2.00
XOR2X0P7MA10TR	2.00	2.00
XOR2X1MA10TR	2.00	2.00
XOR2X1P4MA10TR	2.00	3.20
XOR2X2MA10TR	2.00	3.60
XOR2X3MA10TR	2.00	4.20
XOR2X4MA10TR	2.00	6.20

Functional Schematic



AC Power

Pin	Power (uW/MHz)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A	0.0032	0.0037	0.0046	0.0068	0.0086	0.0121	0.0164
B	0.0039	0.0047	0.0061	0.0093	0.0121	0.0172	0.0239

Pin Capacitance

Pin	Capacitance (pF)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A	0.0019	0.0021	0.0024	0.0035	0.0045	0.0059	0.0079
B	0.0011	0.0014	0.0018	0.0026	0.0033	0.0048	0.0064

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A → Y ↑	0.0181	0.0165	0.0152	0.0199	0.0172	0.0153	0.0160
A → Y ↓	0.0188	0.0178	0.0170	0.0190	0.0168	0.0159	0.0165
B → Y ↑	0.0335	0.0288	0.0261	0.0349	0.0272	0.0248	0.0260
B → Y ↓	0.0362	0.0326	0.0301	0.0301	0.0292	0.0271	0.0285

Delays at 25°C,1.0V, Typical Process (Cont'd.)

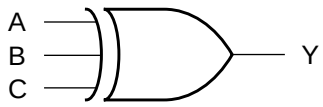
Description	K_{load} (ns/pF)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A → Y ↑	6.7127	4.9960	3.5946	3.2937	1.8267	1.1957	0.9066
A → Y ↓	4.6549	3.4221	2.4053	1.8055	1.2810	0.8262	0.6270
B → Y ↑	6.7045	5.0246	3.6180	3.2921	1.8251	1.1950	0.9060
B → Y ↓	4.7329	3.4729	2.4368	1.8292	1.2840	0.8321	0.6272

Cell Description

The XOR3 cell provides a logical EXCLUSIVE OR of three inputs (A,B,C). The output (Y) is represented by the following equation:

$Y = A \oplus B \oplus C$

Logic Symbol



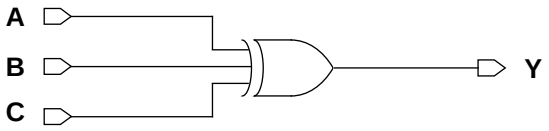
Function Table

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Cell Size

Drive Strength	Height (um)	Width (um)
XOR3X0P5MA10TR	2.00	3.80
XOR3X0P7MA10TR	2.00	3.80
XOR3X1MA10TR	2.00	3.80
XOR3X1P4MA10TR	2.00	6.00
XOR3X2MA10TR	2.00	7.00
XOR3X3MA10TR	2.00	8.00
XOR3X4MA10TR	2.00	10.40

Functional Schematic



AC Power

Pin	Power (uW/MHz)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A	0.0044	0.0054	0.0065	0.0081	0.0110	0.0150	0.0191
B	0.0082	0.0095	0.0113	0.0160	0.0209	0.0278	0.0362
C	0.0092	0.0113	0.0134	0.0193	0.0246	0.0339	0.0440

Pin Capacitance

Pin	Capacitance (pF)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A	0.0023	0.0027	0.0031	0.0036	0.0047	0.0063	0.0078
B	0.0021	0.0023	0.0027	0.0035	0.0047	0.0059	0.0078
C	0.0012	0.0016	0.0017	0.0026	0.0031	0.0046	0.0059

Delays at 25°C,1.0V, Typical Process

Description	Intrinsic Delay (ns)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A → Y ↑	0.0428	0.0407	0.0398	0.0367	0.0397	0.0366	0.0364
A → Y ↓	0.0510	0.0481	0.0494	0.0449	0.0488	0.0443	0.0446
B → Y ↑	0.0784	0.0710	0.0697	0.0723	0.0697	0.0651	0.0646
B → Y ↓	0.0898	0.0807	0.0818	0.0797	0.0791	0.0713	0.0713
C → Y ↑	0.0932	0.0851	0.0826	0.0827	0.0805	0.0750	0.0743
C → Y ↓	0.1037	0.0945	0.0934	0.0895	0.0893	0.0810	0.0810

Delays at 25°C,1.0V, Typical Process (Cont'd.)

Description	K_{load} (ns/pF)						
	X0P5M	**X0P7M**	**X1P0M**	**X1P4M**	**X2P0M**	**X3P0M**	**X4P0M**
A → Y ↑	4.5296	3.3222	2.3824	1.6316	1.1756	0.7818	0.5803
A → Y ↓	3.0210	2.1684	1.5624	1.0705	0.7697	0.5091	0.3791
B → Y ↑	4.5304	3.3224	2.3813	1.6318	1.1762	0.7818	0.5805
B → Y ↓	3.0483	2.1845	1.5725	1.0785	0.7740	0.5113	0.3808
C → Y ↑	4.5296	3.3220	2.3814	1.6318	1.1760	0.7818	0.5804
C → Y ↓	3.0488	2.1848	1.5727	1.0798	0.7740	0.5117	0.3809