# High Density 65nm/90nm ArtiGrid™ (OTC) Features Memory Compiler Application Note

**Confidential**

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**Proprietary Notice**



**Confidentiality Status**

# Revision History

| Part Number | Release Date | Comments |
|---|---|---|
| app_metro_otc_2005q3v1 | July 2005 | Initial Release |
| app-metro-otc-2006q1v1 | January 2006 | Add confidentiality material and Format upgrade |
| app-metro-otc-2006q3v1 | July 2006 | Updated metal information. |
| app-metro-otc-2007q2v1ARM PAN 0032A | June 2007 | Update copyright and preface |
| ARM PAN 0032A | August 2009 | Replaced Metro product name with high density, added revision history page and updated copyright information. |
| ARM PAN 0032A | September 2009 | Update Date Rev |

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# Typographic Conventions

The following typographic conventions are used to assist you in distinguishing special notations, values, and elements described in this manual.

| Visual Cue | Meaning |
|---|---|
| (Bullet) • | Bulleted list of important items. |
| `Courier Type` | Commands typed on the keyboard, either examples or instructions. |
| Dash (- )<br>`Courier Type` | Text set in Courier type and preceded by a dash represents a command name (for example, -`libname`). |
| *<italic type>*<br>*italic type* | Variable names you select, such as file and directory names are enclosed within angle brackets ( < > ). Italic type is used to show variable values, file, and directory names. |
| (Ellipsis) … | Indicates commands or options that may be added. |
| *Italic Type with Initial Capital Letters* | Document, chapter, section and reference manual names. |

# 1. Overview

In addition to the rings-based power routing, ARMmemory compilers now allow ringless power routing through the ArtiGrid™ over-the-cell (OTC) power routing option. When the ArtiGrid option is selected through the GUI or command line, vertical Metal4 straps of power (VDD) and ground (GND) are visible to the chip-level routing tools.

## 1.1 ArtiGrid for Single and Dual-Port SRAM, and ROM Compilers

Both types of high density SRAM (RA1 and RA2) and high density ROM compilers use the same ArtiGrid methodology. The basic ArtiGrid characteristics for all 65nm and 90nm SRAM and ROM compilers are listed in Table 1.

**Table 1. ArtiGrid Characteristics for high density SRAM and ROM Compilers (65nm and 90nm)**

| Parameter | Value |
|---|---|
| Minimum width of ArtiGrid VDD and GND Metal4 straps | Top metal via4 plus Metal4 overlap |
| Minimum connection/stripe to maintain power density | 1 |

Nanoroute, Astro, or similar routing tools can be used to connect the vertical Metal4 straps to/from Metal5 and Metal 6. ArtiGrid for SRAM and ROM compilers only have the vertical Metal4 straps over the instance.

You must route chip-level ground (VSS) and VDD horizontally in M5 or higher and drop vias down to M4 to connect to every power/ground strap.

## 1.2 ArtiGrid for 65nm and 90nm Single-Port Register Files

ArtiGrid in the 65nm and 90nm single port register file differs from the SRAM and ROM compilers as the power and ground straps are in Metal3. ArtiGrid has the vertical M3 straps over the instance periphery only.

Nanoroute, Astro, or similar routing tools are used to verify that the vertical M3 straps can be connected to/from M4 and M5.

You must route chip-level ground (VSS) and VDD horizontally in M4 and drop vias down to M3 to connect to every power/ground strap.

**Table 2. ArtiGrid Characteristics for Single Port Register File Generator (90nm)**

| Parameter | Value |
|---|---|
| Minimum width for VDD and GND Metal4 straps. | via3 plus Metal3 overlap |
| Minimum connection/stripe to maintain power density | 1 |

## 1.3 ArtiGrid for 65nm and 90nm Two-Port Register Files

ArtiGrid in the 65nm and 90nm two-port register file is different from the SRAM and ROM compilers in that the power and ground straps are in Metal3. ArtiGrid has the vertical M3 straps over the instance periphery only.

ArtiGrid in the two-port register file also differs from the single port register file in that the power and ground straps are over the I/O sections on opposite sides of the instance, and not just one side. Both sets of the power and ground straps need to be connected to the chip level power grid.

Nanoroute, Astro, or similar routing tools are used to verify that the vertical M3 straps can be connected to/from M4 and M5.

You must route chip-level ground (VSS) and VDD horizontally in M4 and drop vias down to M3 to connect to every power/ground strap.

**Table 3. ArtiGrid Characteristics for Two-Port Register File Generator (90nm)**

| Parameter | Value |
|---|---|
| Minimum width for VDD and GND Metal4 straps. | via3 plus Metal3 overlap |
| Minimum connection/stripe to maintain power density | 2 (Top and Bottom) |

# Appendix A- Revisions

This appendix describes the technical changes between released issues of this book.

**Table A-1. Issue A**

| Change | Location |
|---|---|
| Replaced Metro product name with High Density | Entire book |