

ECE385

DIGITAL SYSTEMS LABORATORY

Instantiation Megafunctions (IP modules)

Megafunctions are what Intel calls their reconfigurable Intellectual Property (IP) modules. These modules are pre-designed FPGA components (such as interfaces, memory controllers, computation accelerators, etc.) which can be licensed from Intel or third parties and instantiated into an FPGA design. Typically, these can be configured graphically through a GUI, or through code via SystemVerilog parameters. For the SLC-3 lab, you will configure an on-chip memory Megafunction for use as your main memory. **Note if you do not do this, you will be missing the ram module.**

To start, open your existing SLC-3 project that you have created. You can then expand the IP Catalog panel (by default located on the right side). Select RAM: 1-PORT and name your “IP Variant” as *ram*.

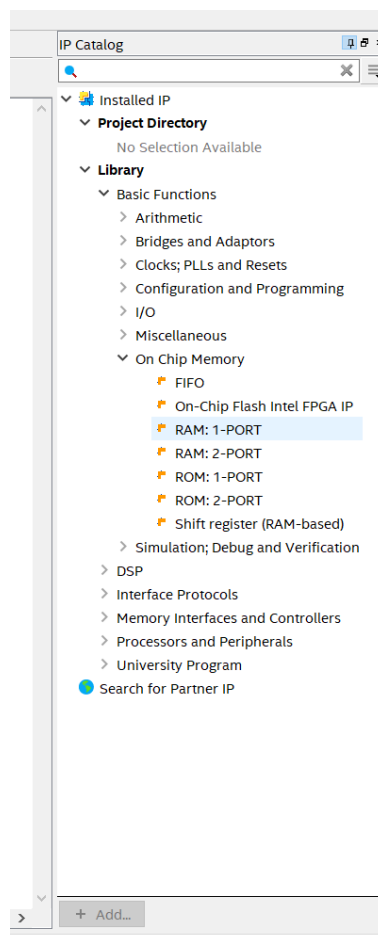


Figure 1 IP Catalog

IMF.2

You will then be presented with the following GUI tool. Populate the following according to the screenshots and click Finish. **Note the size of the RAM is 1k x 16, which is smaller than the CPU's address space.**

The figure displays four sequential screenshots of the MegaWizard Plug-In Manager GUI for the RAM: 1-PORT component, showing the configuration steps from page 1 to page 4.

Page 1 of 6: The "RAM: 1-PORT" wizard is shown. The "Parameter Settings" tab is active. The "Widths/Blk Type/Cks" section shows "data[15..0]", "wren", "address[9..0]", "rden", and "clock". The "Block type: M9K" is selected. The "Currently selected device family: MAX 10" is shown. The "Match project/default" checkbox is checked. The "How wide should the 'q' output bus be?" is set to 16 bits. The "How many 16-bit words of memory?" is set to 1024 words. The "What should the memory block type be?" section has "M9K" selected. The "Set the maximum block depth to" is set to Auto words. The "What clocking method would you like to use?" section has "Single clock" selected.

Page 2 of 6: The "RAM: 1-PORT" wizard is shown. The "Read During Write Option" tab is active. The "Which ports should be registered?" section has "data" and "wren" input ports, "address" input port, and "q" output port checked. The "Create one clock enable signal for each clock signal." checkbox is unchecked. The "Create byte enable for port A" checkbox is unchecked. The "What is the width of a byte for byte enables?" is set to 8 bits. The "Create an 'aclr' asynchronous clear for the registered ports" checkbox is unchecked. The "Create a 'rden' read enable signal" checkbox is checked.

Page 3 of 6: The "RAM: 1-PORT" wizard is shown. The "Read During Write Option" tab is active. The "Single Port Read-During-Write Option" section has "What should the q output be when reading from a memory location being written to?" set to "Don't Care". The "Get x's for write masked bytes instead of old data when byte enable is used" checkbox is unchecked.

Page 4 of 6: The "RAM: 1-PORT" wizard is shown. The "Read During Write Option" tab is active. The "Do you want to specify the initial content of the memory?" section has "No, leave it blank" selected. The "Initialize memory content data to X0C..X on power-up in simulation" checkbox is unchecked. The "Yes, use this file for the memory content data" option is selected. The "File name:" field is empty. The "The initial content file should conform to which port's dimensions?" dropdown is set to "PORT_A". The "Allow In-System Memory Content Editor to capture and update content independently of the system clock" checkbox is unchecked. The "The 'Instance ID' of this RAM is:" field is set to "NONE".

Although it is possible to populate the memory contents from the Megafunction GUI, we provide a module called `instantiateram.sv` which initializes the on-chip memory from the FPGA logic on reset. This is so the memory contents can be restored during a reset, rather than requiring a full FPGA reprogramming to restore.