ECE385
DIGITAL SYSTEMS LABORATORY
Instantiation Megafunctions (IP modules)

Megafunctions are what Intel calls their reconfigurable Intellectual Property (IP) modules. These modules are pre-designed FPGA components (such as interfaces, memory controllers, computation accelerators, etc.) which can be licensed from Intel or third parties and instantiated into an FPGA design. Typically, these can be configured graphically through a GUI, or through code via SystemVerilog parameters. For the SLC-3 lab, you will configure an on-chip memory Megafunction for use as your main memory. **Note if you do not do this, you will be missing the ram module.**

To start, open your existing SLC-3 project that you have created. You can then expand the IP Catalog panel (by default located on the right side). Select RAM: 1-PORT and name your "IP Variant" as ***ram***.

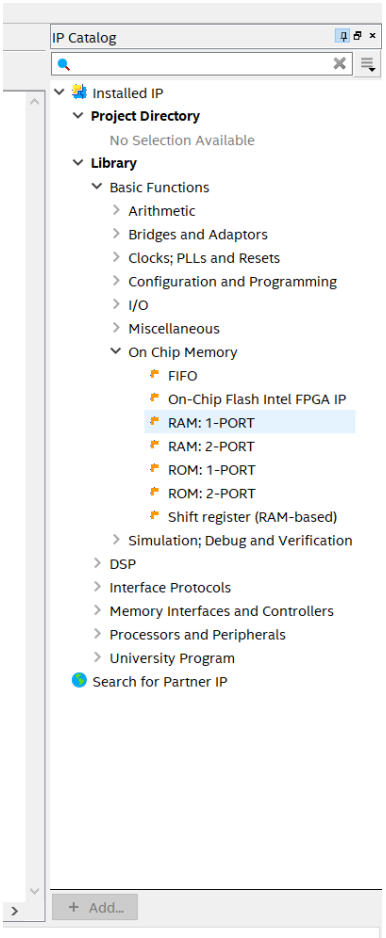
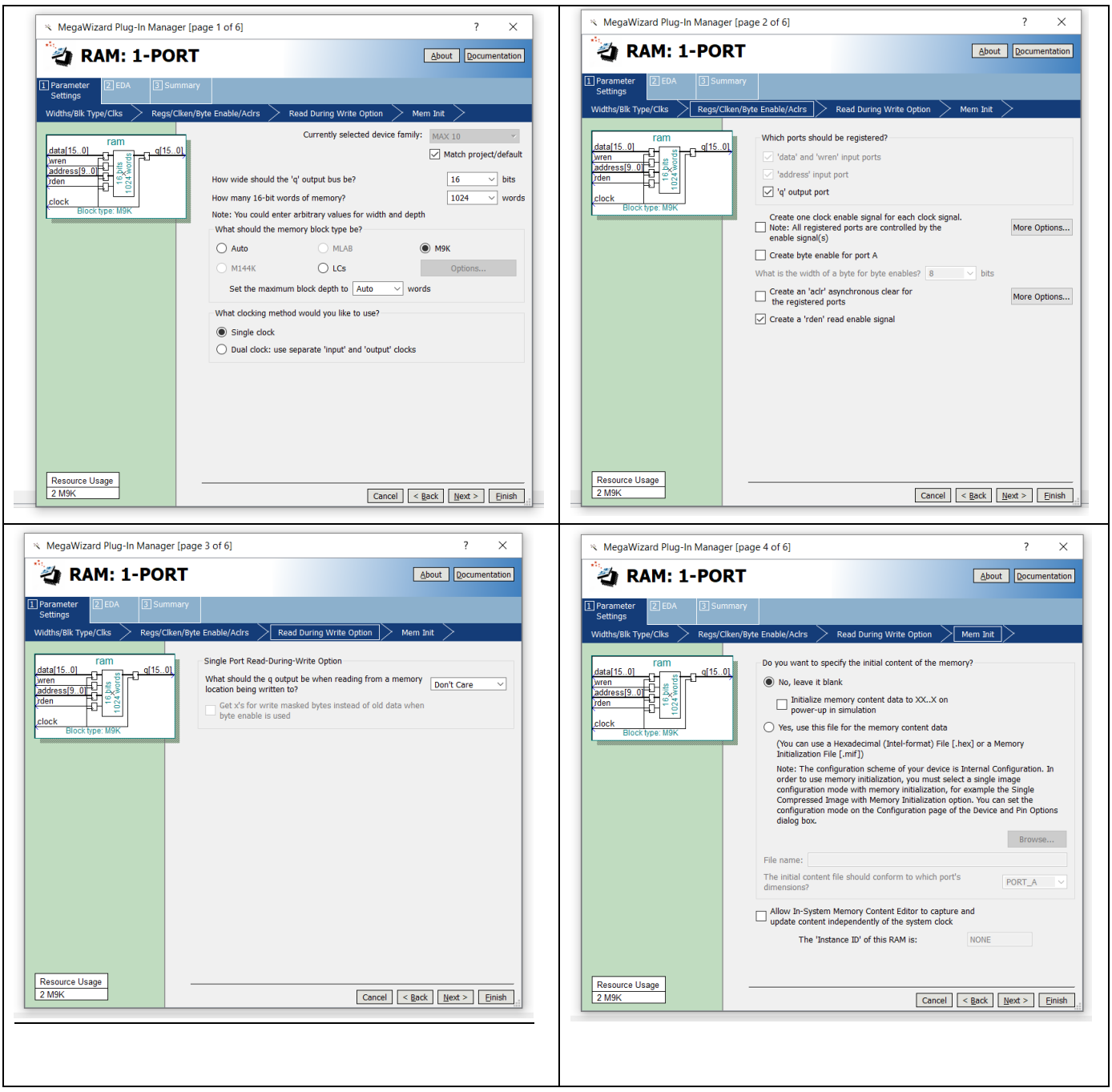


Figure 1 IP Catalog

You will then be presented with the following GUI tool. Populate the following according to the screenshots and click Finish. **Note the size of the RAM is 1k x 16, which is smaller than the CPU's address space.**



Although it is possible to populate the memory contents from the Megafunction GUI, we provide a module called instantiateram.sv which initializes the on-chip memory from the FPGA logic on reset. This is so the memory contents can be restored during a reset, rather than requiring a full FPGA reprogramming to restore.