ECE 385

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Experiment #5 EC

MIPS Calculations

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NL / Friday 9:15 AM - 9:30 AM
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Overview

SignalTap, a Logic Analyzer IP Core that is integrated into the FPGA fabric of a given design, was used to probe signals during each test program: XOR, Multiplier, and Sort. The signals that were probed were the Program Counter (PC), and HEX0, HEX1, HEX2, and HEX3. The PC register was chosen as the trigger signal. SignalTap was configured to trigger on specific PC values for each of the three required tests. Once the waveforms were captured, they were analyzed to determine the SLC-3 MIPS (millions of instructions per second). The number of instructions were counted for each test. Moreover, the number of cycles was determined by the number of samples taken during each test. This metric was utilized because each sample is taken on the positive edge of the system clock, which corresponds to one clock cycle.

XOR Test Results

The trigger for this test was PC = 0x1A, which corresponds to the moment after the second input value is entered. The captured logic analyzer waveform is shown below in Figure 1. The number of cycles was able to be measured from the sample bar above Figure 1. The number of instructions was counted from the full SignalTap waveform.

$$\textbf{\textit{Calculations:}}\ 9\ Instructions,\ 67\ Cycles$$

$$\frac{9\ Instructions}{67\ Cycles} \times 50,000,000\ \frac{Cycles}{Second} \approx 6,716,418\ \frac{Instructions}{Second} \approx 6.716\ MIPS$$

START: 0 END: 67

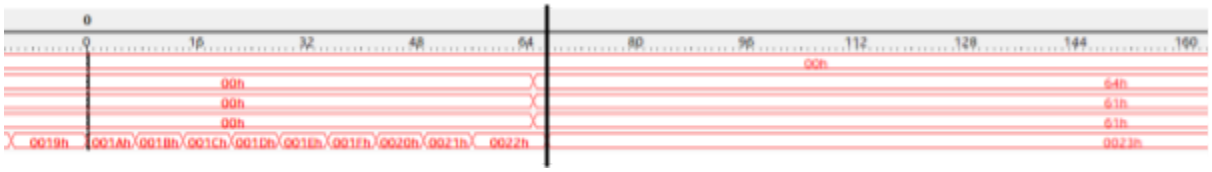

Figure 1: XOR Test SignalTap Waveform

Multiplier Test Results

The trigger for this test was PC = 0x3A, which starts capturing right after the second input value is entered. The captured logic analyzer waveform is shown below in Figure 2 and Figure 3. The number of cycles was able to be measured from the sample bar above Figure 3. The number of instructions was counted from the full SignalTap waveform.

$$\textbf{\textit{Calculations:}}\ \ 79\ Instructions,\ 580\ Cycles$$

$$\frac{79\ Instructions}{580\ Cycles} \times 50,000,000\ \frac{Cycles}{Second} \approx 6,810,344\ \frac{Instructions}{Second} \approx 6.810\ MIPS$$

START: 0

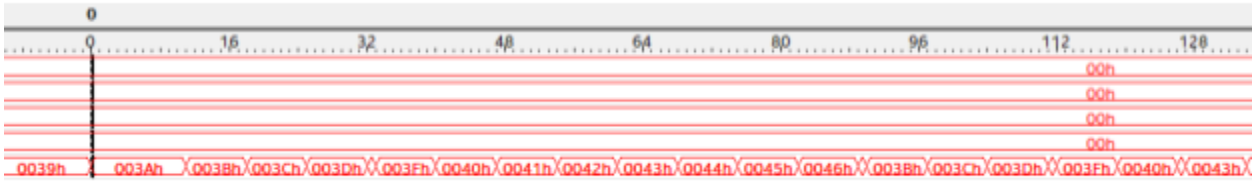

Figure 3: Multiplier Test SignalTap Waveform - Head

END: 580

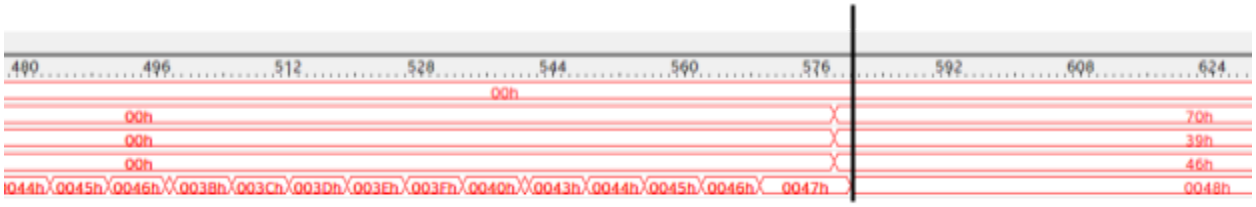

Figure 3: Multiplier Test SignalTap Waveform - Tail

Sort Test Results

The trigger for this test was PC = 0x77, which is the first instruction when executing the bubble sort algorithm. The captured logic analyzer waveform is shown below in Figure 4 and Figure 5. The number of cycles was able to be measured from the sample bar above Figure 5. The number of instructions was computed using a Python program illustrated in Figure 6 and Figure 7.

$$\textbf{\textit{Calculations:}}\ \ 1,638\ Instructions,\ 12,150\ Cycles$$

$$\frac{1{,}638\ Instructions}{12{,}150\ Cycles} \times 50,000,000\ \frac{Cycles}{Second} \approx 6,740,741\ \frac{Instructions}{Second} \approx 6.741\ MIPS$$

START: 0

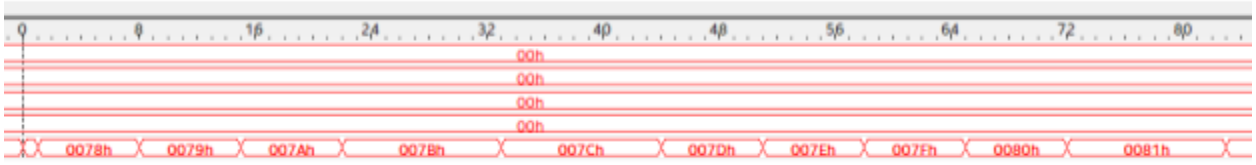

Figure 4: Sort Test SignalTap Waveform - Head

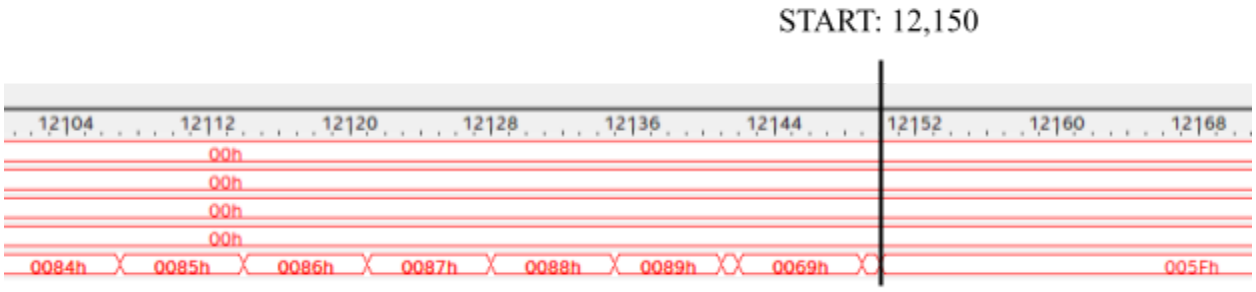

Figure 5: Sort Test SignalTap Waveform - Tail

```
# Counts Number of Unique Instructions

instructions = open("Sort_Test.txt", 'r')

previous = "prev"
num_instructions = 0
for inst in instructions:
    if (previous != inst[-7:]):
        num_instructions += 1
        previous = inst[-7:]

print ("There were {} instructions executed!" .format(num_instructions))

instructions.close()
```

```
There were 1638 instructions executed!
```

Figure 6: Instruction Counting Python Script

```
1  0 0077h
2  1 0078h
3  2 0078h
4  3 0078h
5  4 0078h
6  5 0078h
7  6 0078h
8  7 0078h
9  8 0079h
10 9 0079h
11 10 0079h
12 11 0079h
13 12 0079h
14 13 0079h
15 14 0079h
16 15 007Ah
17 16 007Ah
```

Continues Until…
14335 005Fh

Figure 7: "Sort_Test.txt" SignalTap Sampled Instructions File

Conclusion

After computing the results from each test, the average SLC-3 MIPS is:

$$\textbf{\textit{Calculations:}}\ \frac{6.716\ MIPS + 6.810\ MIPS + 6.741\ MIPS}{3} = \frac{20.267\ MIPS}{3} \approx 6.756\ MIPS$$

This is comparable to the Intel 8048 from 1980!