| Data Path Control Signals | | | |
|---------------------------|--------|----------------------------------|---------------------------------|
| Signal Name | # bits | Signal Values | |
| LD_MAR | 1 | NO, LOAD | |
| LD_MDR | 1 | NO, LOAD | |
| LD_IR | 1 | NO, LOAD | |
| LD_BEN | 1 | NO, LOAD | |
| LD_CC | 1 | NO, LOAD | |
| LD_REG | 1 | NO, LOAD | |
| LD_PC | 1 | NO, LOAD | |
| LD_LED | 1 | NO, LOAD (for PAUSE instruction) | |
| GatePC | 1 | NO, YES | |
| GateMDR | 1 | NO, YES | |
| GateALU | 1 | NO, YES | |
| GateMARMUX | 1 | NO, YES | |
| ALUK | 2 | ADD, AND, NOT, PASSA | |
| PCMUX | 2 | PC + 1 | ;select pc+1 |
| | | BUS | ;select value from bus |
| | | ADDER | ;select output of address adder |
| DRMUX | 1 | IR[11:9] | ;destination IR[11:9] |
| | | 3'b111 | ;destination R7 |
| SR1MUX | 1 | IR[11:9] | ;source IR[11:9] |
| | | IR[8:6] | ;source IR[8:6] |
| SR2MUX | 1 | SR2 OUT | ;value from SR2 |
| | | imm5 | ;immediate value |
| ADDR1MUX | 1 | PC, BaseR | |
| ADDR2MUX | 2 | ZERO | ;select the value zero |
| | | offset6 | ;select SEXT[IR[5:0]] |
| | | PCoffset9 | ;select SEXT[IR[8:0]] |
| | | PCoffset11 | ;select SEXT[IR[10:0]] |
| Mem_OE | 1 | NO, YES (active low) | |
| Mem_WE | 1 | NO, YES (active low) | |