Paul Martin

Austin, TX
-Email me on Indeed: http://www.indeed.com/r/Paul-Martin/1bff1f067e580d98

Work Experience

Aleksander Dec

Supervisor - New York, NY
April 2008 to November 2008

Analog Devices Inc.: Direct contract hire for their SPD group. Worked on analog circuits, I/O buffers, diodes, resistors, I/O pad ring circuits, trademark and ID logos, as well as circuits for test chip (DFT). Used Stella LVS verification and Cadence
DRC verification tools.

Supervisor

Peter Szabo - Austin, TX
March 2006 to February 2008

Silicon Aid Solutions Inc.: Contracting for Texas Instruments in the Ferrari
Group.
Worked on I/O circuits, core digital circuits, signal arrays, routing congestion,
IR drop fixes, metal density issues, antenna issues, and ESD issues. Used shielding to fix noise and cross talk problems. A c021.m process and K2 verification tools were used.

Supervisor

Susan Laird - Austin, TX
February 2005 to February 2006

Universal CADworks Inc.: Contracting for Motorola/Freescale Semiconductor in the Network Computing Systems Group on the Apollo 8 project. Worked on I/O buffers, memory, signal arrays, routing congestion, IR drop fixes, and analog circuits.
Fixed EM, metal density, antenna, and ESD issues. Used shielding to fix noise and cross talk. Validated circuits against design rules using Assura LVS reliability verification checks. Provided feasibility studies and engineer change recommendations.

Intel Corporation

Dave Barrera - Austin, TX
March 2003 to September 2004

Direct hire employee for seven years. Worked in the Folsom
Design Center in the Desktop Products Group. Worked on Pentium, Pentium Pro,
Pentium II, Pentium III, and Pentium IV microprocessors. Worked on I/O, L2 caches, static and dynamic memory, signal arrays, twisted pairs, thermal diodes, routing congestion, IR drop and analog circuits. Used shielding to fix noise and cross talk. Fixed EM, metal density, antenna, and ESD issues. Validated circuits against design rules using Hercules LVS verification checks. Provided feasibility studies and engineer change recommendations.

Supervisor/Manager
Mahnaz Padash - Folsom, CA
September 1995 to January 2003

Oxford International
Contract for Epoch Microelectronics. Help tape out of analog
RF chip for Toshiba. Using Cadence XL and Calibre. Built and verified to design rules and schematic high and low band limiting amplifiers, digital to analog converters
(DAC) and attenuators. Built poly resistors, inductors, poly capacitors, and MIM capacitors and balanced circuits. Working seven days a week for four weeks.

Education

Associate of Science in Electrical and Electronic Engineering
American River College - Sacramento, CA
1991 to 1995

Skills

- Experience in analog/digital mixed signal layout design
- Experience in tight matching, low capacitance, low power analog blocks, resistors, capacitors, high voltage devices, pad I/O, ESD structures etc.
- CMOS block and chip level layout
- Custom and standard cell-based floor planning and hierarchical layout assembly
- Understanding of IR drop, RC delay, electro-migration, self-heating and cross capacitance
- Design for Manufacturing (DFM) and Design for Testing (DFT)
- Mentor Graphics and Cadence layout tools
- Excellent communication skills and able to work with multi-function teams.
- Knowledge of Calibre
- DRC
- LVS