MICHAEL HAENDEL

Electrical Engineer V
Austin, TX
-Email me on Indeed: http://www.indeed.com/r/MICHAEL-HAENDEL/c8ab53bebf346287

BSEE, MSEE specializing in Digital Signal Processing, FPGA, and Computer Architecture. Overall 20 years experience as an Electrical
Engineer, with 8 years experience with FPGA/CPLD/VHDL/Verilog, 4 years experience with Embedded Firmware, 3 years Digital Design, Analog
Design, 1 year PCB/Schematic Capture, 3 years C/C++/UNIX/Linux, 2 years Digital Signal Processing/ Communications Design.

Authorized to work in the US for any employer

Work Experience

Electrical Engineer V

Macaulay Brown, Inc - San Antonio, TX
January 2009 to January 2010

Duties Include: Ida Pro / OillyDbg cryptographic analysis/synthesis, Xilinx FPGA bit-stream analysis, and hardware analysis, 40 hours Wind
River RTOS training. Worked with Python programming language

Contractor / Signal Integrity Engineer

TAC World Wide Consulting / Dell Computer, Inc - Austin, TX
June 2008 to October 2008

Duties Include: Hardware signal integrity analysis of DDR2, I2C, proprietary busses and circuits, schematic design, testing of server printed wire
boards.

Project Engineer III

Symtx Test, Inc - Austin, TX
September 2007 to January 2008

Duties include: FPGA Design, Digital Signal Processing and Digital Hardware Design Embedded and hardware design and analysis,
documentation, and VHDL Programming targeting Altera Stratix II, implementing Weather Doppler Radar digital signal processing algorithms,
FPDP Array Storage Hard Drive Arrays, RF/IF Signal Processing, Matlab/Simulink Algorithm Development. Mentor Graphics DxDesigner design and modification of Radar interface unit

Contractor / FPGA Designer

Triple Crown Consulting / Rockwell Collins, Inc - Cedar Rapids, IA
March 2007 to June 2007

Duties include: Embedded and hardware design and analysis, documentation, and VHDL Programming targeting Altera Cyclone III, Xilinx

VirtexE, Xilinx Virtex 4 FPGAs, implementing airbourne and ground based communication systems. EDA Tools:Telelogic DOORS 8.1/DO-256,
MG HDL Designer, Aretna Spyglass, Synopsis Simplicity, and Modelsim7.1, Matlab algorithm development.

Consultant / FPGA Designer

Volt Consulting / Rockwell Collins, Inc - Cedar Rapids, IA
November 2006 to December 2006

Duties include: Hardware Design Analysis, Documentation, and VHDL Programming targeting two Altera MAX 7000 CPLDs.

Contractor / FPGA Designer

Oxford International Consulting / Luna Innovations, Inc - Blacksburg, VA
October 2006 to November 2006

Duties include: VHDL programming targeting Altera Stratix II FPGA to be implemented in an ultrasonic imaging medical electronic device.

Research Assistant

University of Central Florida - Orlando, FL
May 2005 to December 2005

Duties include: VHDL programming targeting a Xilinx Virtex II Pro FPGA, embedded in an Avnet Virtex II Pro Development Board. Two
contracts were supported, a NASA project investigating evolvable hardware targeted for space borne applications, and an Air Force project
investigating fragmentation, mutation and repair of FPGA hardware configurations the tools utilized for the task were: Matlab simulation,
ModelSim XE 6.3.03i, and Xilinx Navigator 6.3.03i, and Xilinx SDK Embedded Development Kit 6.3.i, Microblaze. This work was performed
concurrently during the year of 2005, while pursuing and completing a master's degree in electrical engineering, specializing in digital signal
processing. Additionally satisfied requirements MSCpE/Digital Architecture Track.

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Contractor / FPGA Designer

System Pros / Oxford International Consulting / Sypris Electronics, Inc - Tampa, FL
September 2004 to December 2004

Duties include: VHDL programming targeting a Xilinx Spartan III FPGA for use in COMSEC Type 1 Trunk Encoder Encryption / Decryption / Cryptographic Unit, in compliance with Line Encryption Units standards being developed for the NSA, Army, and Navy. My assignment was
exclusively to the KIV-19M program. Work experience with ARM 7 processor implementing cryptographic algorithms. The tools utilized for the task were: ModelSim XE, PE, SE, and Xilinx Navigator 6.3.

Contractor / FPGA Designer

ATI Consulting / Northrop-Grumman, Inc - Baltimore, MD
September 2003 to August 2004

Duties include: FPGA, VHDL and analog and digital hardware design for airborne radar / electronic countermeasure systems. Additional duties
include documentation, presentations, testing, and project scheduling for the Northrop Grumman EA6B III and the Northrop Grumman F18G.
Worked with high speed digital design of a large Xilinx CPLD operating at 100MHz, and additional multiple clock domains of 25MHz, 50Mhz.

Electrical Engineer II

Harris Corporation Corp - Palm Bay, FL
April 2000 to August 2002

Duties Include: Digital design, VHDL programming and test benching, hardware flight integrity analysis / simulation, analysis of analog circuits,
as well as increased basic understanding of signal processing, RF circuits, and antenna design. Additionally, experience was gained with embedded programming for the Motorola 68HC16, configuring a Data IO programmer, and utilizing basic pieces of test equipment. Acquired
experience test benching VHDL for clearance project, Fibre-Channel Arbitrated Loop network for Advanced Joint Strike Fighter / Apache
Helicopter. Additional experience includes: hardware flight integrity analysis for the Comanche Helicopter, VHDL test benching for a memory
controller and VHDL programming, analysis, and design for a section of a video digital pipeline algorithms. Presented results of simulation / analysis of a high speed design, as a preliminary design review for a VHDL project. Programmed Xilinx Virtex/VirtexE FPGAs.

Member Technical Staff 1

Lucent Technologies, Inc - Naperville, IL
December 1997 to November 1999

Duties include: C/UNIX programming for class 5E Lucent telecommunication switches, diagnostics, telecommunication related skills. Utilized a variety of proprietary tool sets used for software revision management. My responsibility included: POTS, ISDN, and proprietary optical
diagnostics, switch configuration and testing, and new software development. Gained experience with basic telecom maintenance, and attended
Lucent Lecture Series, Lucent Technical Roadmap Series, Department and Group meetings, and received 40 hours of Lucent technical
education per year. Additional education includes forty hours of Visual C++/OOP utilizing MFC / COM.

Consultant / Telecom Designer

O'Brien Consulting / AT&T, Inc - Chicago, IL
May 1997 to October 1997

Duties include: New fiber-optic layout of Chicago Metro and Chicago Suburban loops. Worked with engineering, and used AutoCAD 14,
concurrently while attending University of Illinois at Chicago.

Additional 10 years of work history available upon request.

Education

MSEE in Electrical Engineering
University of Central Florida
May 2006

BSEE in Electrical Engineering
Southern Illinois University
May 1990

Skills

- ANALOG (3 years)
- FPGA (3 years)
- VHDL (4 years)
- XILINX (5 years)
- RF (2 years)
- C/C++
- MATLAB
- Software Development
- Java
- Software Testing
- Python
- JavaScript
- Scripting

Additional Information

SKILLS
VHDL FPGA Verilog EDA Firmware Cryptography Digital
Analog PCB DSP Matlab C/C++ Linux Virtual OS
Assembler Telecom Controls PLC Filters TCL 6811
x86 Xilinx Altera Reconfiguration Testbench Signal Integrity UL
PSpice EDK Chipscope ISE Quartus DDR2 I2C
HDL Designer Symplicity ModelSim 800Mhz RF MathCAD POTS
ISDN RS232 RS485 Mil Std 1553 Virtex X Spartan X Cyclone X
Wind River RTOS FORTRAN BASIC SpecctraQuest NCVHDL VisualElite
PADS DxDesigner RADAR SCADA Schematic SpyGlass Control
ADC/DAC/PLL VHDL Cores Airborne Fibre Channel Doppler Documentation AutoCad
DO 254 Simulink System Generator StateCAD Parallel Proc Medical Consumer