An RC Oscillator With Comparator Offset Cancellation and Current Consumption Reduction Technique

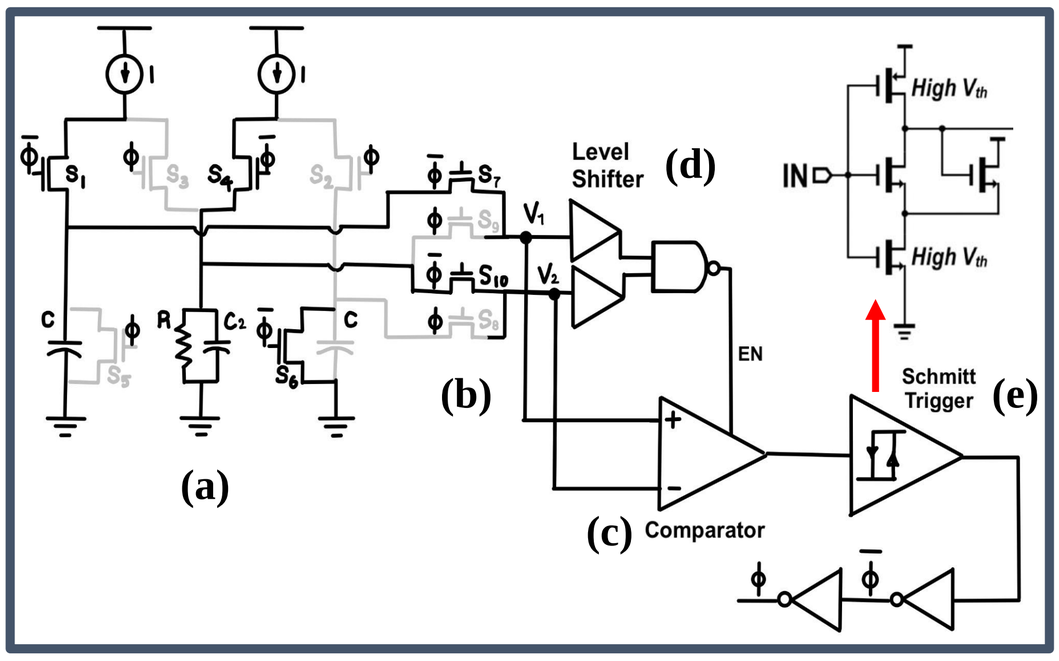
Yu-Min Han, Yu-Tzu Liu, Tun-Hsien Chien

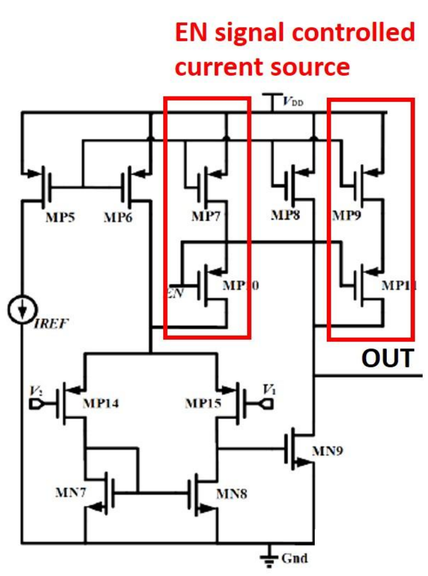
Research Project under Electronics Research IC Lab
Advisor: Prof. Tsung-Hsien Lin

I. Abstract

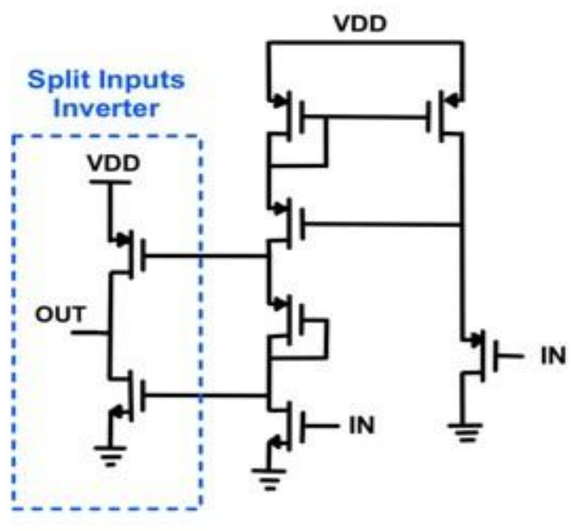
This project presents a low-power RC oscillator featuring offset cancellation[1] and enhanced energy efficiency. A level shifter is introduced as a logic-control switch for the comparator, significantly reducing current consumption during idle periods[2]. The oscillator operates at $1\,V$ with an oscillation frequency of $18.37\,kHz$ and a power consumption of just $72.02\,nW$. Simulated using a $180\,nm$ TSMC CMOS process, the design demonstrates a temperature accuracy of $\pm 0.52\%$ over $-50\,℃$ to $120\,℃$. Across a supply voltage range of 0.95 to $1.05\,V$, the frequency exhibits a line sensitivity of 0.66%/V. The oscillator achieves a fast startup, with frequency settling within 4 cycles.

II. Proposed Architecture





(c)



(d)

(a) RC core circuit charges and discharges capacitors C to create an oscillation. The total period is: $t_{period} = 2RC + t_{delay}$.

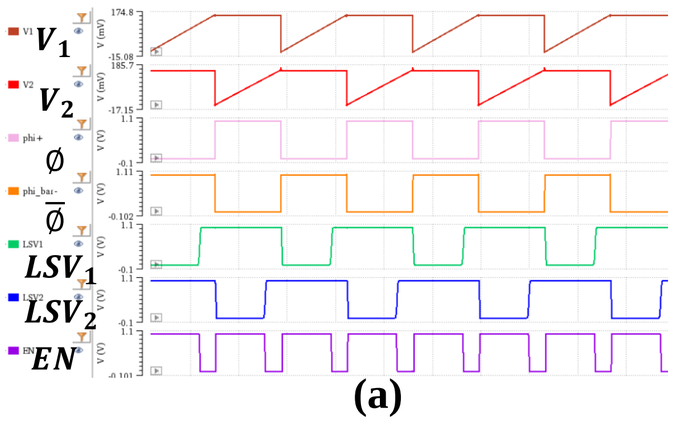
(b) 4-point probe reducing sensitivity to mismatch-induced voltage errors and frequency variation.

(c) Using minimal transistors and an EN signal allowed us to achieve ultra-low delays while cutting idle power.

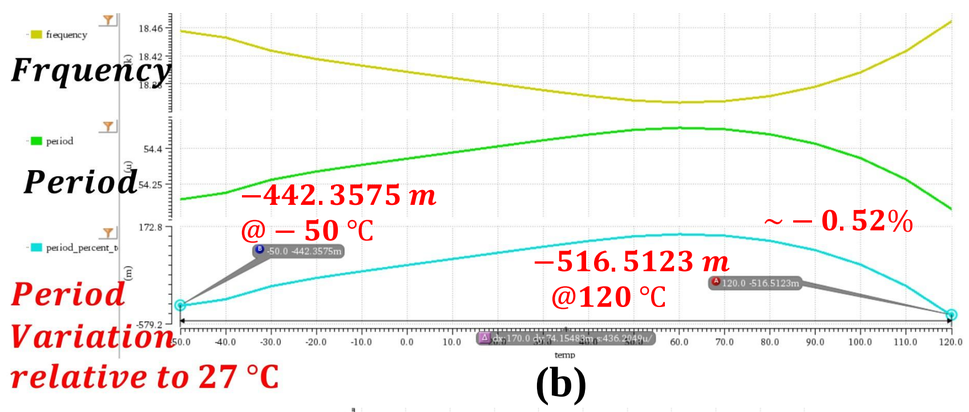
(d) Generates an enable signal only when the comparator is required. LS input tracks the RC charging voltage. Output goes high near $I \cdot R$ and resets low when input drops to 0.

(e) A 4T Schmitt trigger prevents potential glitching by separating its output switching thresholds.

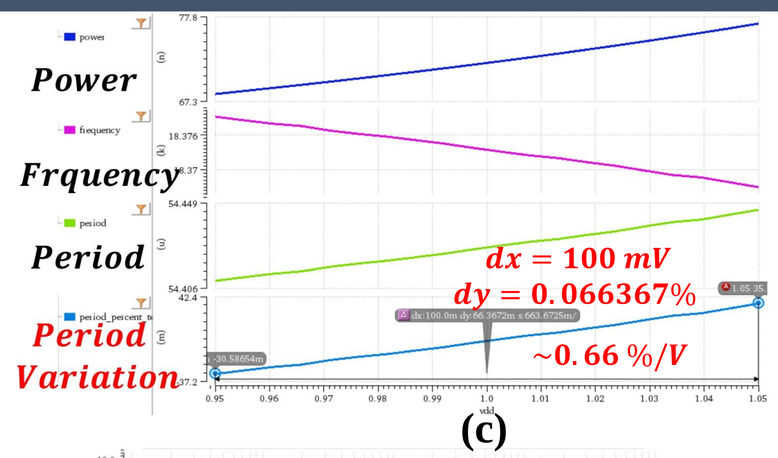
III. Simulation Result



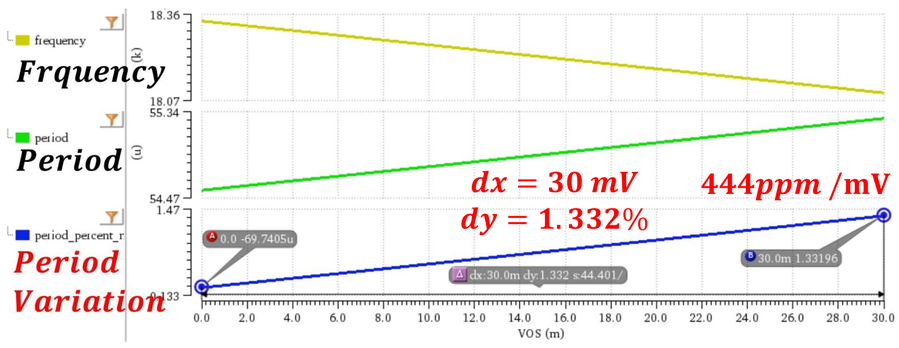
(a)



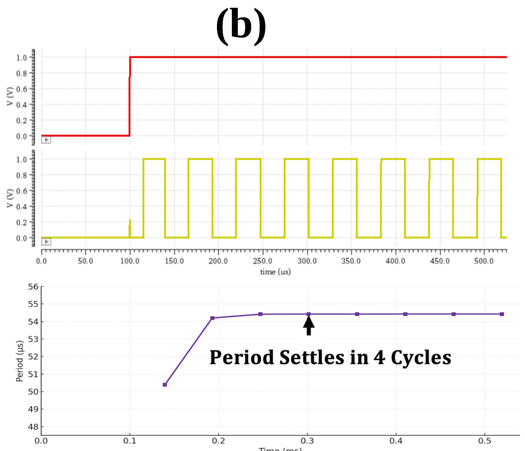
(b)



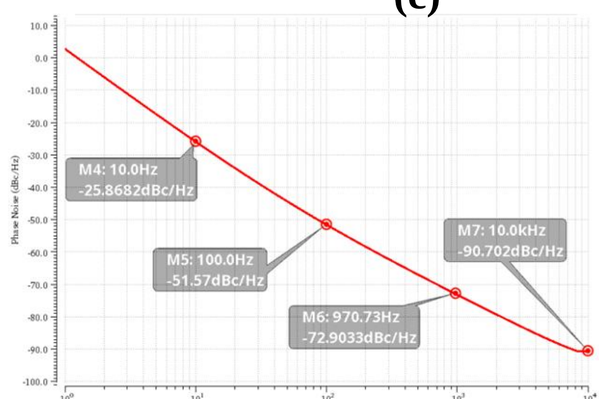
(c)



(d)



(e)



(f)

(a) Nominal performance waveform, (b) Temperature variation result, (c) Supply voltage variation result,
(d) Period variation vs Vos under $\alpha, \beta = 2.5\%$, (e) Setup behavior, (f) Phase noise versus frequency offset

IV. Comparison Table

Spec	Reference Paper [1]	Proposed Circuit
Technology	$65\,nm$	$180\,nm$
Frequency	$18.5\,kHz$	$18.5\,kHz$
Power	$130\,nW$	$72.02\,nW$
Temp. Accuracy (%)	$\pm 0.18 \sim \pm 0.55$ $(-40\,°C \sim 90°C)$	± 0.52 $(-50\,°C \sim 120°C)$
Voltage Accuracy $(0.95\,V \sim 1.05\,V)$	$< 5\,\%/V$	$0.66\,\%/V$
Start up cycles	4	4

V. Reference

[1] A. Paidimarri, B. H. Calhoun, and A. P. Chandrakasan, **"An RC Oscillator With Comparator Offset Cancellation,"** *IEEE Journal of Solid-State Circuits*, vol. 51, no. 8, pp. 1866–1876, 2016. DOI:10.1109/JSSC.2016.2569484.

[2] H. Zhang and Y. Wang, **"A 5.27nw/khz Low Power Relaxation Oscillator with Current Consumption Reduction Technique,"** in *2024 IEEE 7th Advanced Information Technology, Electronic and Automation Control Conference (IAEAC)*, vol. 7, 2024, pp. 1336–1339.

[3] S. Kabirpour and M. Jalali, **"A Power-Delay and Area Efficient Voltage Level Shifter Based on a Reflected-Output Wilson Current Mirror Level Shifter,"** *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 2, pp. 250–254, Feb. 2020. DOI: 10.1109/TCSII.2019.2927431.

[4] J. P. Kulkarni, K. Kim, and K. Roy, **"A 160 mv Robust Schmitt Trigger Based Subthreshold SRAM,"** *IEEE Journal of Solid-State Circuits*, vol. 42, no. 10, pp. 2303–2313, Oct. 2007. DOI: 10.1109/JSSC.2007.897148.