113-2 Final Presentation:
An RC Oscillator With Comparator Offset Cancellation

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May 29, 2025

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Outline (1/2)

- Abstract
- Proposed architecture
  - RC Core
  - Switch Matrix
  - Comparator
  - Level Shifter
  - Schmitt Trigger

Outline (2/2)

- Simulation result
  - Nominal performance
  - Temperature Variation
  - Supply Voltage Variation
  - Device Mismatch
    - Comparator
    - Current
    - Capacitor
  - Noise Analysis
  - Setup time
  - Comparison Table
- Conclusion
- References

Abstract

Abstract

This project presents a **low-power RC oscillator** featuring **offset cancellation**[1] and enhanced energy efficiency. A **level shifter** is introduced as a logic-control switch for the comparator, significantly reducing current consumption during idle periods[2]. The oscillator operates at **1 V** with an oscillation frequency of **18.37 kHz** and a power consumption of just **72.02 nW**. Simulated using a **180 nm TSMC CMOS process**, the design demonstrates a temperature accuracy of $\pm$ **0.52%** over $-$**50** $^{\circ}\mathrm{C}$ **to 120** $^{\circ}\mathrm{C}$. Across a supply voltage range of **0.95 to 1.05 V**, the frequency exhibits a linear sensitivity of **0.66%/V**. Additionally, the oscillator achieves a **fast startup**, with frequency settling within **4 cycles**.

Proposed architecture

Architecture Overview

- **RC Core**
- **Switch Matrix**
- **Comparator**
- **Level Shifter**
- **Schmitt Trigger**

I. Proposed architecture

- During $\phi = 0$, V_2 sets a reference ($I \cdot R$); V_1 ramps and triggers the comparator when exceeding $I \cdot R$, switching to $\phi = 1$ (symmetric operation).
- A Schmitt trigger suppresses output glitches during phase shifts.
- To save power, the RC core generates an enable signal (EN) that activates the comparator only during comparisons.

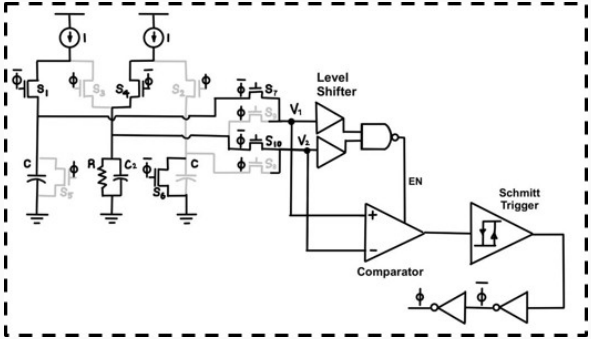

Fig. 1. Architecture of the RC oscillator

I-A. *RC Core*

- $R = 7.5\ \mathrm{M\Omega}$, $C = 3.6\ \mathrm{pF}$
  $\rightarrow$ RC time constant $= 27\ \mu\mathrm{s}$
- Charging current $I = 20\ \mathrm{nA}$
  $\rightarrow$ Voltage swing $\approx 156.7\ \mathrm{mV}$
- Capacitor C_2 helps suppress glitches on V_1 / V_2 during phase transitions and stabilizes V_2.
- The total period is: $t_{\mathrm{period}} = 2RC + t_{\mathrm{delay}}$, where t_{delay} comes from the comparator and Schmitt trigger. t_{delay} is minimized by using a high-speed comparator in our design.
- Oscillation frequency $\approx$ **18.3736** kHz (at $27\,^{\circ}\mathrm{C}$)

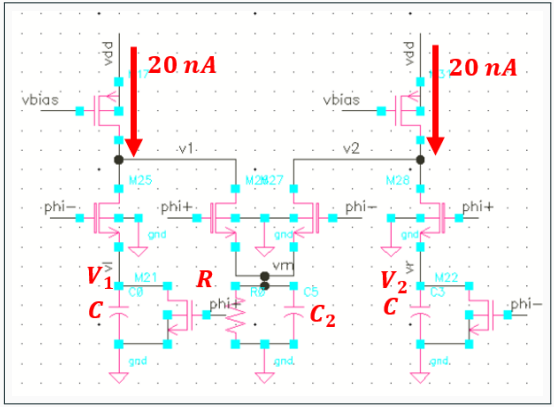

Fig. 2. Schematic of the RC core

I-B. *Switch Matrix*

- Using a **4-point probe** (Fig. 4) removes resistance constraints on $S_1 \sim S_4$, reducing sensitivity to mismatch-induced voltage errors and frequency variation.
- $S_7 \sim S_{10}$ multiplex voltages to the comparator and carry no current, simplifying design.
- Using smaller switches helps minimize glitches during phase transitions, improving signal integrity.

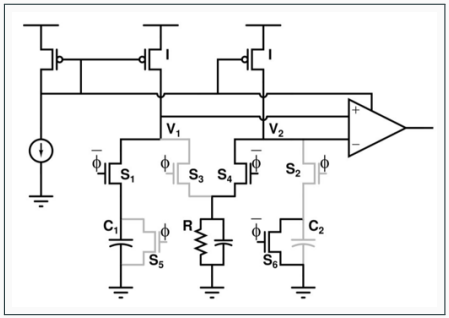

Fig. 3. Original RC architecture

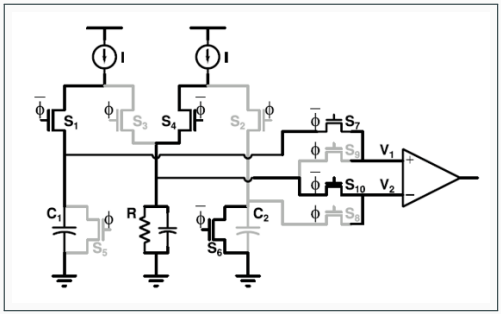

Fig. 4. 4-point probe RC architecture

I-C. *Comparator*

- We used minimal-sized transistors for ultra-low delay ~ 400 ns.
- We added an **EN signal** to shut down idle current sources, cutting power without sacrificing speed.

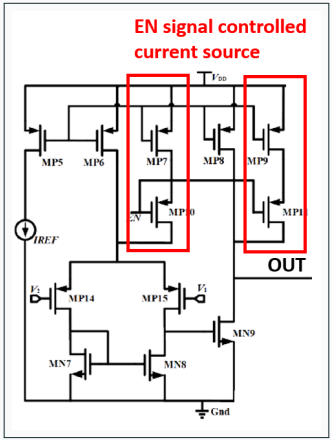

Fig. 5. Comparator schematic with EN-controlled current source

I-D. *Level Shifter*

- Converts low-level *RC* signals to high-level logic with low power and fast response.
- M_{p1} splits the input to reduce short-circuit current at the output buffer.
- M_{p2} pulls node Q high when input is low, preventing current leakage into the RC core and preserving frequency stability.
- In this design, LS input tracks the *RC* charging voltage. Output goes high near $I \cdot R$ and resets low when input drops to 0. (Fig. 7)[3]

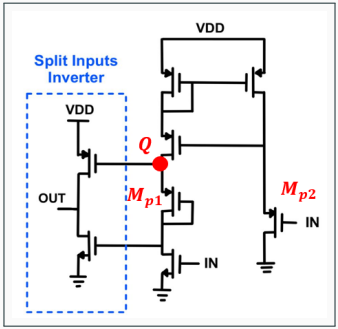

Fig. 6. Proposed level shifter architecture

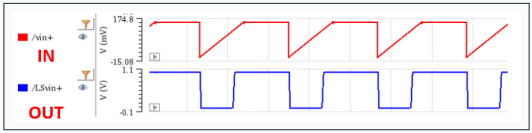

Fig. 7. Timing diagram of level shifter

I-E. *Schmitt Trigger*

- Our goal is simply to **separate the output switching thresholds** rather than to space them evenly; accordingly, only four transistors are required[4].

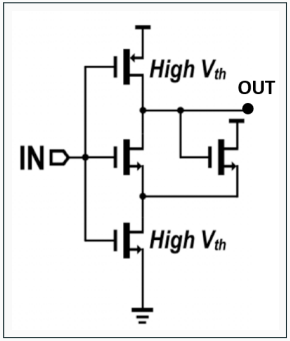

Fig. 8. 4T Schmitt trigger

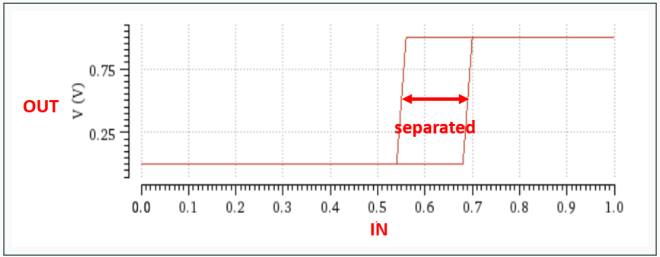

Fig. 9. Simulation result of 4T ST

Simulation result

II. *Simulation Results*

- All simulations were conducted using the **T18 CMOS process**.
- For nominal threshold voltage devices, the `nmos2v` and `pmos2v` models were used. For high-threshold voltage transistors, the `nmos3v` and `pmos3v` models were applied.
- All simulations were performed under the **TT (typical-typical)** process corner.

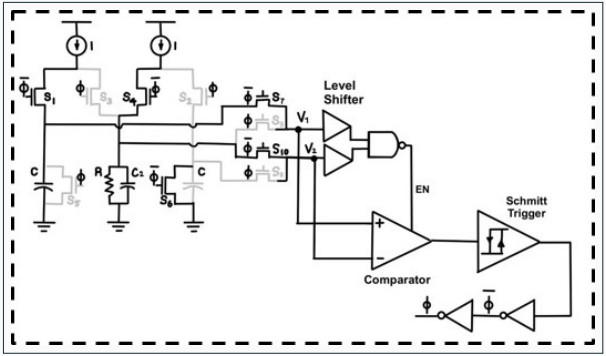

Fig. 1. Architecture of the RC oscillator

II. *Simulation Results* — Outline

- **Nominal Performance**
- Temperature Variation
- Supply Voltage Variation
- Device Mismatch
  - Comparator
  - Capacitor
  - Current Source
- Noise Analysis
- Setup Time
- Comparison Table

II-A. *Nominal Performance*

Parameter	Value
Frequency	18.37 kHz
Period	54.43 μs
Power	72.02 nW

Table 1. Nominal performance of the oscillator

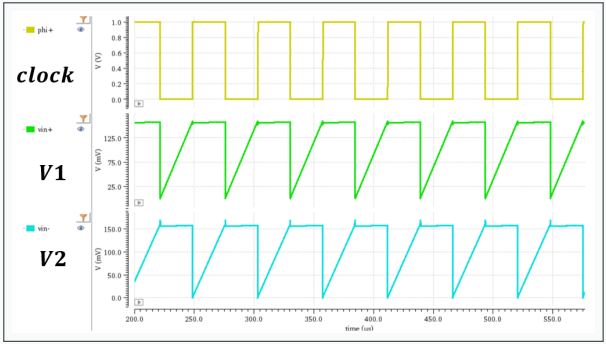

Fig. 10. Clock, V_1, and V_2 waveforms

II. *Simulation Results* — Outline

- Nominal Performance
- **Temperature Variation**
- **Supply Voltage Variation**
- Device Mismatch
  - Capacitor
  - Comparator
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- Comparison table

II-B. *Temperature & Supply Voltage Variation*

Parameter	Value
Temp. Acc. ($-50\,^{\circ}\mathrm{C}$ to $120\,^{\circ}\mathrm{C}$)	± 0.52 %
Vol. Acc. ($0.95\ V \sim 1.05\ V$)	0.66 %/V

Table 2. Accuracy summary under temperature and voltage variation

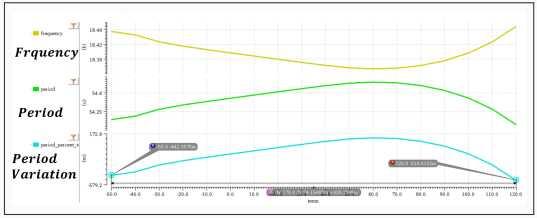

Fig. 11. Temperature variation result

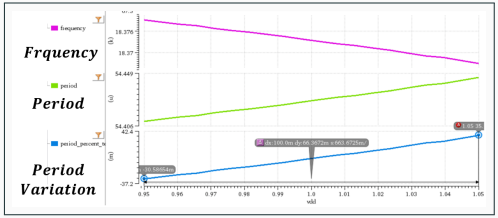

Fig. 12. Supply voltage variation result

II. *Simulation Results* — Outline

- Nominal Performance
- Temperature Variation
- Supply Voltage Variation
- **Device Mismatch**
  - Comparator
  - Capacitor
  - Current Source
- Noise Analysis
- Setup Time
- Comparison Table

II-C. *Recall: Offset Cancellation Mechanism*

Reviewing:

- The oscillator period is determined by two charging phases.
- With offset voltage V_{os}, its impact is largely canceled as it appears with opposite sign in each half cycle.
- Only under mismatch (e.g., current or capacitance), V_{os} will partially remain.

Key equation :

$$t_{\mathrm{period}} \approx 2RC\left[1 + 2\alpha\beta + \frac{V_{\mathrm{os}}}{IR}(\alpha + \beta)\right] + 2t_{\mathrm{delay}}$$

where α, β represent mismatch in C and I

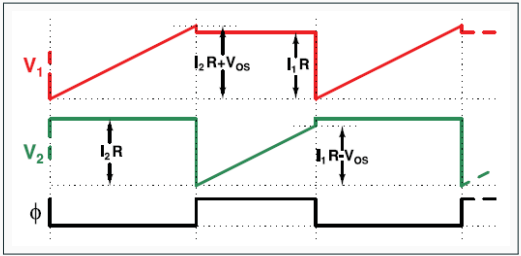

Fig. 13. Waveform showing offset cancellation behavior

II-C1. *Offset-only Effect*

- In this setup, only comparator offset V_{os} is swept, while current and capacitor are matched ($\alpha = \beta = 0$).
- According to the equation:

$$t_{\mathrm{period}} \approx 2RC + V_{\mathrm{os}} \left(\frac{C_1}{I_1} - \frac{C_2}{I_2} \right) + 2t_{\mathrm{delay}}$$

when $\frac{C_1}{I_1} = \frac{C_2}{I_2}$, the impact of V_{os} cancels out.

- Simulation confirms the variation is extremely small:

$$\text{Line Sensitivity} \approx 4.33\ \mathrm{ppm/mV}$$

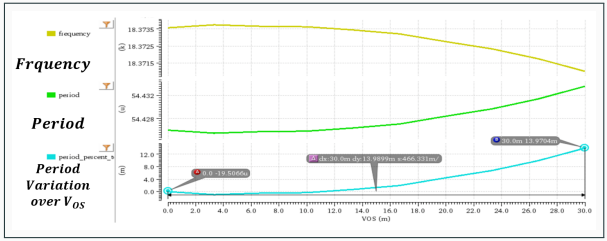

Fig. 14. Period variation versus V_{os} (no mismatch)

II-C2. *Mismatch: Comparator Offset under Mismatch*

- Now we introduce mismatch in current and capacitor: $\alpha = \beta = 2.5\%$.
- According to the formula:

$$t_{\text{period}} \approx 2RC\left[1 + 2\alpha\beta + \frac{V_{\text{os}}}{IR}(\alpha + \beta)\right] + 2t_{\text{delay}}$$

- V_{os} term no longer cancels. It now causes a linear period variation.
- Simulation result shows
  Line Sensitivity $\approx$ **444** ppm/mV

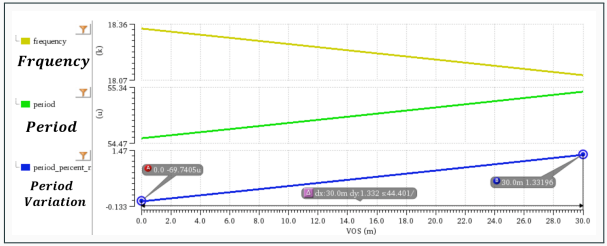

Fig. 15. Period variation vs V_{os} under $\alpha = \beta = 2.5\%$

II-C3. *Offset Cancellation Observation*

Observation:

- From previous simulations, total period variation is small.
- But when comparing both half cycles at $V_{\mathrm{os}} = 0$ and $10\ \mathrm{mV}$, the change in each half period is significant and opposite.
- This shows the effect of **offset cancellation** —offset shifts one half up, the other down.
- As a result, the overall period remains relatively stable.

Current mismatch: 2.5% **Capacitor mismatch: 2.5%**	$V_{\mathrm{os}} = 0$	$V_{\mathrm{os}} = 10\ \mathrm{mV}$
Half period 1 (μs)	27.7635	29.5333 (+6.374%)
Half period 2 (μs)	26.6527	24.9726 (-6.304%)
Total period (μs)	54.4162	54.5059 (+0.165%)

Table 3. Period observation

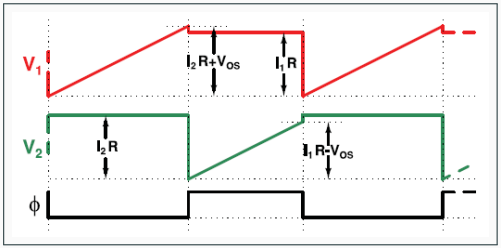

Fig. 16. Cancellation of V_{os} across two charging phases

II-C4. *Bonus: Individual α, β Effects (No V_{os})*

- In this additional simulation, we removed offset ($V_{os} = 0$) and swept:
  - α only (capacitor mismatch)
  - β only (current mismatch)

$$t_{\text{period},\alpha} \approx 2RC + 2t_{\text{delay}} \quad (1)$$

$$t_{\text{period},\beta} \approx 2RC\left[1 + 2\beta^2\right] + 2t_{\text{delay}} \quad (2)$$

- This demonstrates the robustness of the oscillator even under mismatch.

Mismatch Type	Impact (ppm/%)
Current Mismatch	627.7
Capacitor Mismatch	35.6

Table 4. Period variation slope from individual mismatch

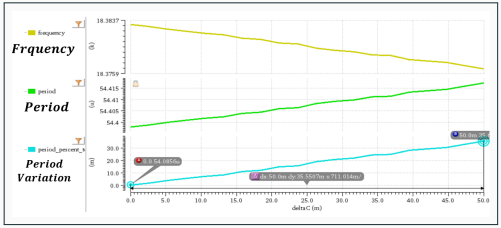

Fig. 17. Sweep of α (capacitor mismatch)

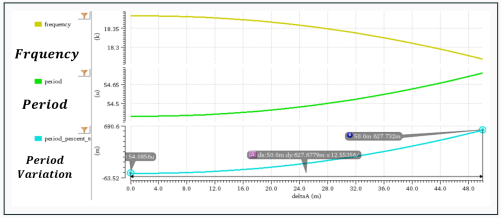

Fig. 18. Sweep of β (current source mismatch)

II. *Simulation Results* — Outline

- Nominal Performance
- Temperature Variation
- Supply Voltage Variation
- Device Mismatch
  - Comparator
  - Capacitor
  - Current Source
- **Noise Analysis**
- Setup Time
- Comparison Table

II-D1. *Phase Noise Analysis*

Overview:

- Phase noise represents the short-term frequency stability of the oscillator.
- It is defined as the noise power at a given frequency offset from the carrier, expressed in dBc/Hz.
- In our design, the phase noise follows a typical slope:

$$-25.87\,\mathrm{dBc/Hz@10\,Hz}, \quad -90.7\,\mathrm{dBc/Hz@10\,kHz}$$

- The result indicates acceptable phase noise for low-frequency clock generation.

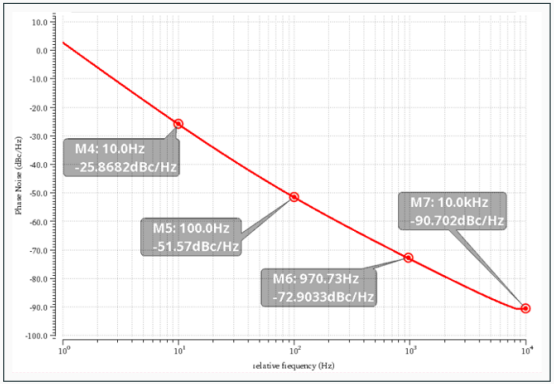

Fig. 19. Phase noise versus frequency offset

II-D2. *Allan Deviation Analysis*

Overview:

- Allan deviation $\sigma_y(\tau)$ characterizes long-term stability and noise type.
- For $\tau < 1$ s, our data shows a slope of approximately $-1/2$.
- This indicates that our oscillator is dominated by white phase noise in this range.
- Due to simulation limits, we only measured up to $\tau \approx 1$ s.
- Further explanation is provided in Appendix B.

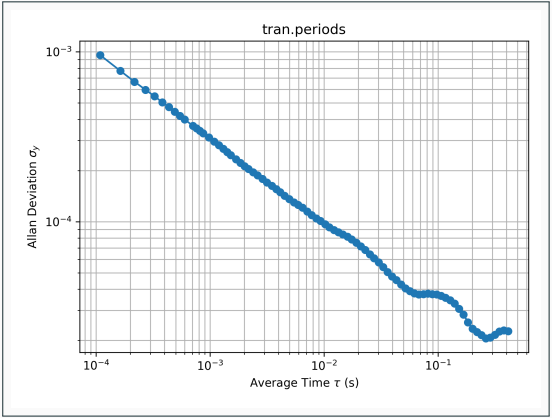

Fig. 20. Allan deviation of the oscillator vs averaging time τ

II. *Simulation Results* — Outline

- Nominal Performance
- Temperature Variation
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- Device Mismatch
  - Comparator
  - Capacitor
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- Comparison Table

II-E. *Setup Time Analysis*

Overview:

- Setup time indicates the number of cycles required for the oscillator to stabilize after power-up.
- As shown, the oscillator begins generating a stable waveform immediately after V_{DD} is applied.
- The output period converges within 4 clock cycles.

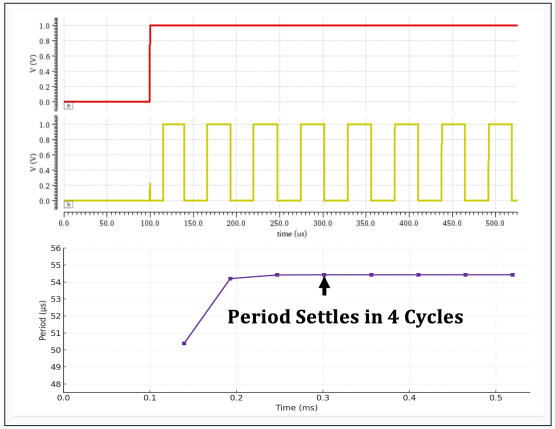

Fig. 21. Setup behavior showing convergence within 4 cycles

II. *Simulation Results* — Outline

- Nominal Performance
- Temperature Variation
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- Device Mismatch
  - Comparator
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- **Comparison Table**

II.F *Comparison Table*

Spec	Paper	Proposed Circuit
Technology	65 nm	180 nm
Frequency	18.5 kHz	18.37 kHz
Power	130 nW	72.02 nW
Temp. Accuracy (%)	$\pm 0.18 \sim \pm 0.55$ $(-40\,°C \sim 90°C)$	± 0.52 $(-50\,°C \sim 120°C)$
Voltage Accuracy $(0.95\,V \sim 1.05\,V)$	$< 5\,\%/V$	$0.66\,\%/V$
Start up cycles	4	4

Conclusion

III. *Conclusion*

This project presents the design of a low-power relaxation oscillator implemented in a **180 nm CMOS process**. An **offset cancellation scheme** is adopted to enhance accuracy, and **power consumption is minimized** by integrating a logic-controlled switch into the voltage comparator. This allows high current only during evaluation and significantly reduces idle power.

The oscillator achieves a **startup time of only 4 cycles** and demonstrates robust performance across varying conditions:

- Operates with a power consumption of **72.02 nW**.
- Maintains temperature stability within $\pm$**0.52%** over a wide range of $-50^{\circ}\mathrm{C}$ **to** $120^{\circ}\mathrm{C}$.
- Exhibits a line supply sensitivity of **0.66%/V** across **0.95 V to 1.05 V**.

These results demonstrate the oscillator's **suitability for energy-efficient and temperature-resilient timing applications**.

Appendix

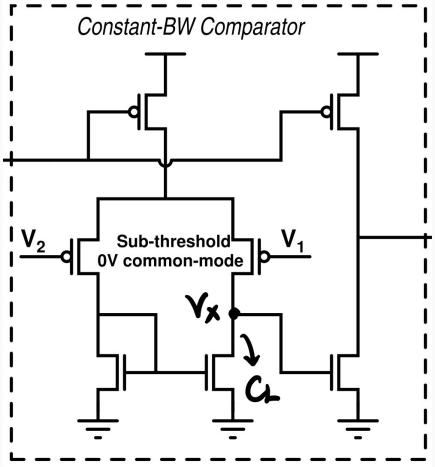
Appendix A. Delay $\propto \sqrt{C}$

The comparator delay t_{delay} is shown to be proportional to $\sqrt{C}$ based on the small-signal response of the first stage of the comparator.
When the input ramp ΔV_{in} increases linearly with time.
An integration-based model leads to:

$$C_L \frac{dV_x}{dt} \propto g_m \cdot \Delta V_{\text{in}} \propto g_m \cdot t$$

$$\Rightarrow \quad \Delta V_x \propto \int \frac{g_m}{C_L} \cdot t\, dt \propto \frac{g_m}{C_L} \cdot t^2$$

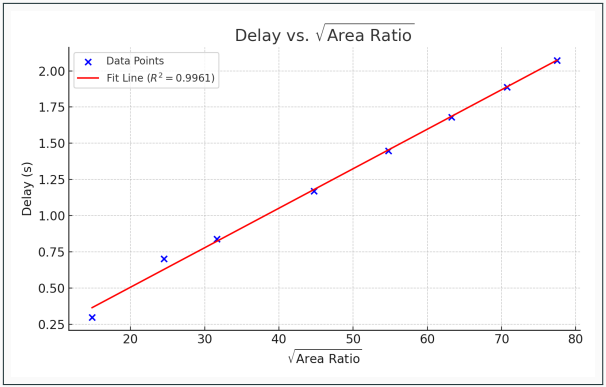
$$\Rightarrow \quad t \propto \sqrt{\frac{C_L}{g_m}} \propto \sqrt{C_L}$$



Appendix A. Delay $\propto \sqrt{C} \propto \sqrt{\textit{Area Ratio}}$

$\sqrt{\text{Area Ratio}}$	Delay (s)
14.83	0.2989
24.49	0.7039
31.62	0.8401
44.72	1.1713
54.77	1.4469
63.25	1.6805
70.71	1.8866
77.46	2.0732

Table 1: Delay vs. $\sqrt{\text{Area Ratio}}$ Data



Appendix B. Trade-Off in Allan Deviation Measurement

Concept: Allan deviation is sensitive to quantization error in period measurement.

Suppose that the oscillator period is $T = 50$ μ s and the measurement resolution is δt.

The normalized error caused by the 1-tick quantization is:

$$\epsilon = \frac{\delta t}{T} \times 10^6 \text{ ppm}$$

For the Allan deviation using the period difference:

$$\sigma_y(\tau) \approx \frac{\epsilon}{\sqrt{12}}$$

Hence, **the step size** is proportional to error floor; **finer step** improves the resolution but requires more data.

There's a practical trade-off between accuracy and time required.

Appendix B. Trade-Off in Allan Deviation Measurement

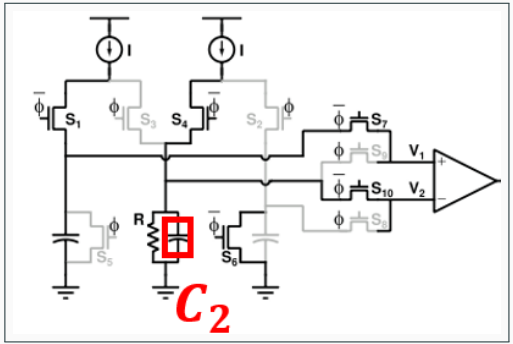
δt	$\delta t / T$ (%)	ϵ (ppm)	$\sigma_y(\tau)$ (ppm)
5 μs	10	100 000	28 900
0.5 μs	1	10 000	2 890
0.05 μs	0.1	1 000	289
0.01 μs	0.02	200	58
1 ns	0.002	20	5.8

Table 2: Step size vs. Allan deviation ($T = 50\,\mu$s)

Appendix C. Setup-Time vs. Glitch Trade-off

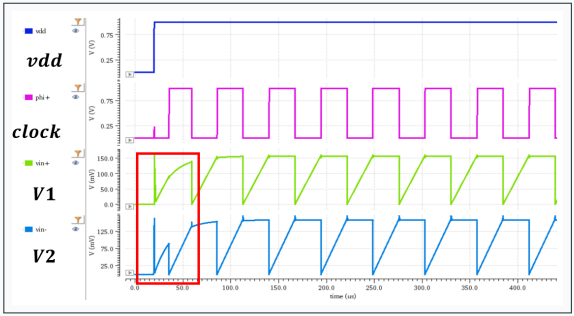
Idea: The auxiliary capacitor C_2 (highlighted on the right) forms an RC low-pass filter that *suppresses charge glitches* on V_1/V_2 when phases switch.

- **With** C_2 $\Rightarrow$ No output glitches —but the extra load delays the comparator, so the period settles after **4 cycles** (longer setup—time).
- **Without** C_2 $\Rightarrow$ Fast start-up (almost 0-cycle setup) —but noticeable glitches on the first transition.

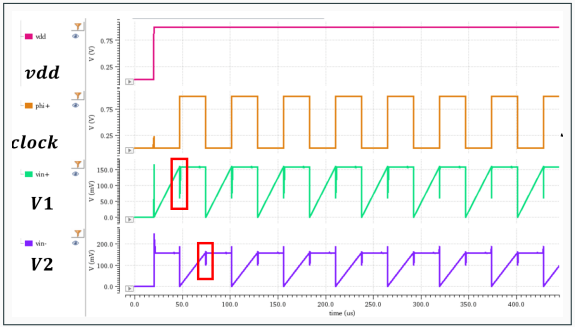


(a) Location of C_2

Startup Waveforms Comparison



(a) With C_2: clean waveform but **4-cycle** setup



(b) Without C_2: small glitch, **instant** setup

References i

[1] A. Paidimarri, B. H. Calhoun, and A. P. Chandrakasan, **"An RC Oscillator With Comparator Offset Cancellation,"** *IEEE Journal of Solid-State Circuits*, vol. 51, no. 8, pp. 1866–1876, 2016. DOI: 10.1109/JSSC.2016.2569484.

[2] H. Zhang and Y. Wang, **"A 5.27nw/khz Low Power Relaxation Oscillator with Current Consumption Reduction Technique,"** in *2024 IEEE 7th Advanced Information Technology, Electronic and Automation Control Conference (IAEAC)*, vol. 7, 2024, pp. 1336–1339.

References ii

[3] S. Kabirpour and M. Jalali, **"A Power-Delay and Area Efficient Voltage Level Shifter Based on a Reflected-Output Wilson Current Mirror Level Shifter,"** *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 2, pp. 250–254, Feb. 2020. DOI: 10.1109/TCSII.2019.2927431.

[4] J. P. Kulkarni, K. Kim, and K. Roy, **"A 160 mv Robust Schmitt Trigger Based Subthreshold SRAM,"** *IEEE Journal of Solid-State Circuits*, vol. 42, no. 10, pp. 2303–2313, Oct. 2007. DOI: 10.1109/JSSC.2007.897148.

Thank You

Thanks for Listening!