An RC Oscillator With Comparator Offset Cancellation and Current Consumption Reduction Technique

Yu-Min Han, Yu-Tzu Liu, Tun-Hsien Chien

Research Project under Electronics Research IC Lab
Advisor: Prof. Tsung-Hsien Lin

Contents

I Abstract

This report presents the design and simulation of a **low-power RC relaxation oscillator** that incorporates **comparator offset cancellation** and **energy-efficient operation techniques**. To minimize idle power consumption, a **level shifter** is introduced to act as a **logic-controlled switch**, enabling the comparator only during the necessary comparison phase. This reduces **static current draw** without sacrificing speed or accuracy.

The oscillator is designed using a **180 nm TSMC CMOS process**, operating at a supply voltage of **1 V**. Simulation results show a **nominal oscillation frequency of 18.37 kHz** with a **power consumption of only 72.02 nW**. Furthermore, the oscillator achieves a **startup time of merely 4 cycles**, demonstrating excellent responsiveness.

The design exhibits a **temperature accuracy of ±0.52%** across the range from −50°C to 120°C, and a **supply voltage sensitivity of 0.66%/V** from 0.95 V to 1.05 V. The **offset cancellation mechanism** effectively suppresses comparator offset impact under matched conditions, and maintains **low sensitivity even under moderate mismatch**. These features make the oscillator suitable for **energy-constrained applications** requiring **precise and stable timing sources**.

II Proposed Architecture

This section presents the architecture of the proposed RC oscillator, which emphasizes low power consumption and high robustness. The oscillator operates in two non-overlapping phases. During $\phi = 0$, the voltage V_2 sets a reference at $I \cdot R$, while V_1 ramps up. When V_1 exceeds V_2, a comparator triggers and switches to $\phi = 1$, reversing the roles. This symmetric operation ensures balanced charging/discharging and supports offset cancellation.

To minimize power consumption, the RC core generates an enable signal (EN) that activates the comparator only during comparisons. A Schmitt trigger is included to prevent output glitches during phase transitions.

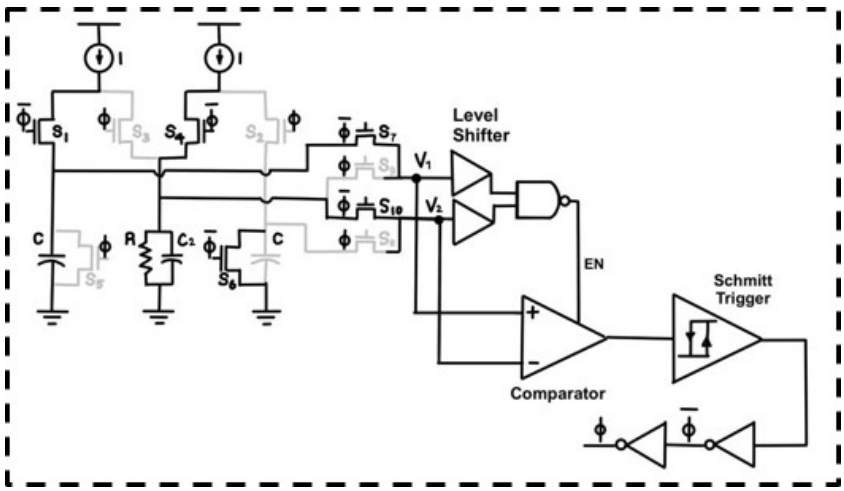


Figure 1: Architecture of the RC oscillator

II.i RC Core

The RC core is implemented using a resistor $R = 7.5$ MΩ and a capacitor $C = 3.6$ pF, resulting in an RC time constant of 27 μs. With a constant current source $I = 20$ nA, the voltage swing reaches approximately 156.7 mV. An auxiliary capacitor C_2 is introduced to suppress voltage glitches during switching events and stabilize the reference voltage V_2.

The oscillator period is given by:

$$t_{\text{period}} = 2RC + t_{\text{delay}}$$

where t_{delay} represents delay introduced by the comparator and Schmitt trigger. This delay is minimized using a high-speed comparator, leading to a simulated oscillation frequency of 18.3736 kHz at 27°C.

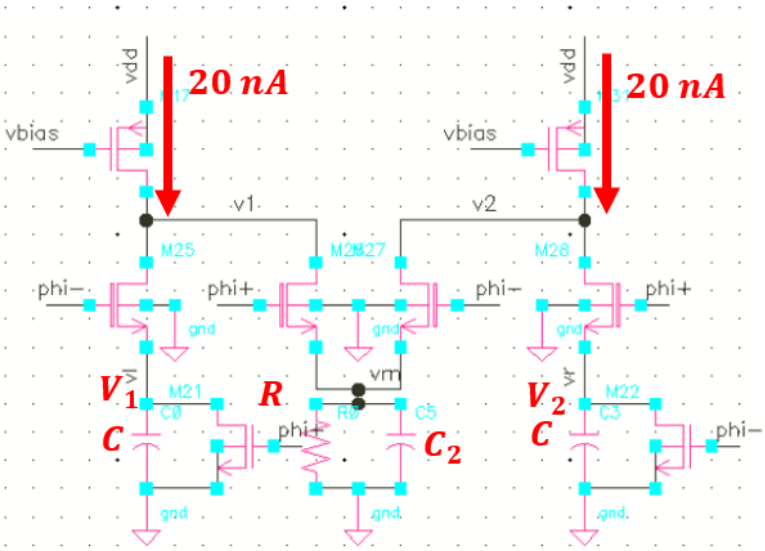
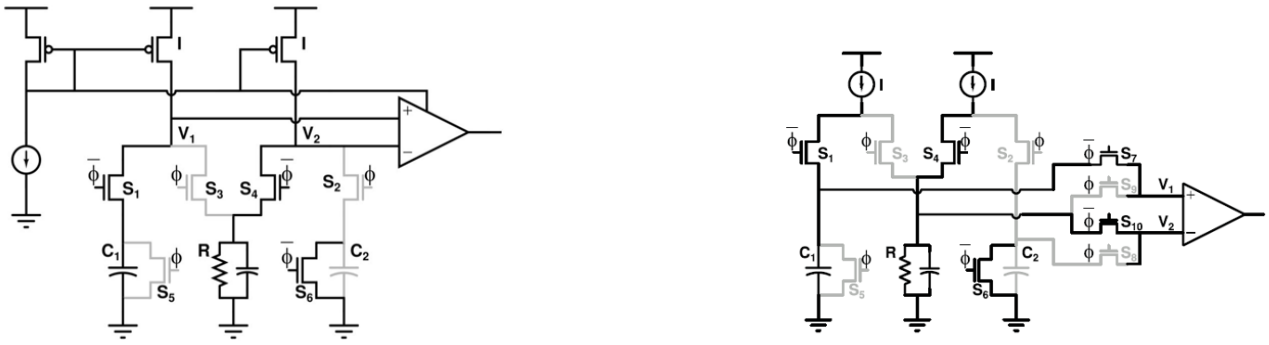


Figure 2: Schematic of the RC core

II.ii Switch Matrix

To improve accuracy and reduce mismatch sensitivity, a 4-point probe configuration is adopted. This setup eliminates resistance constraints on switches S_1 through S_4, thus minimizing the impact of on-resistance variation.

Multiplexing switches S_7 to S_{10} route the signals to the comparator without drawing current, simplifying the routing and improving signal integrity. Moreover, using smaller-sized transistors for the switches helps to suppress glitches during transitions.



(a) Original RC architecture (b) 4-point probe RC architecture

Figure 3: Comparison between original and 4-point probe RC architecture

II.iii Comparator

The comparator is designed for ultra-low delay (∼400 ns) using minimal-sized transistors. An EN signal disables the current source when not in use, reducing static power without sacrificing performance. The comparator' s architecture ensures fast decision making while avoiding unnecessary power consumption during idle phases.

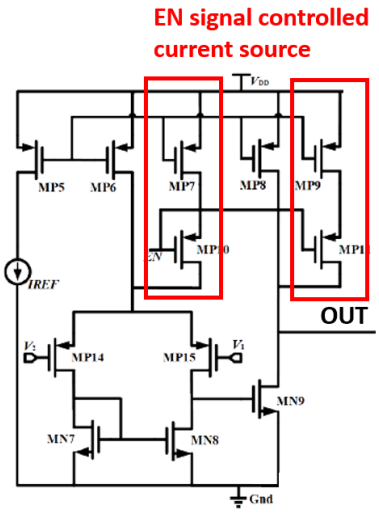


Figure 4: Comparator schematic with EN-controlled current source

II.iv Level Shifter

A low-power level shifter converts analog voltages from the RC domain to digital control signals. The level shifter uses a PMOS-based structure:

- Mp1 splits the input path to limit short-circuit current at the buffer.
- Mp2 pulls the intermediate node high when input is low, preventing leakage current.

The level shifter input tracks the charging voltage of the RC core. Its output rises when the input nears $I \cdot R$ and resets to low as the input falls to zero, enabling comparator activity only when necessary.

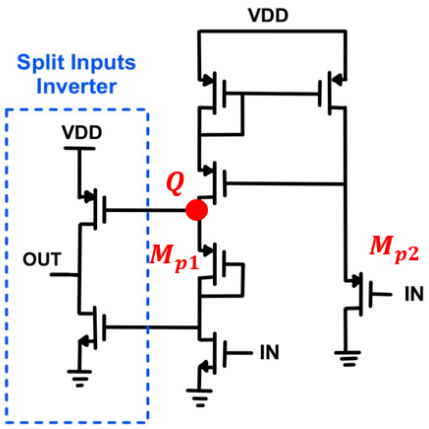


Figure 5: Proposed level shifter architecture

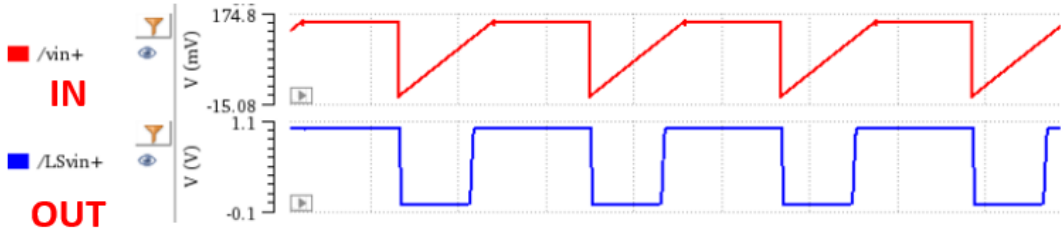


Figure 6: Timing diagram of level shifter

II.v Schmitt Trigger

A 4-transistor (4T) Schmitt trigger is used to separate switching thresholds, ensuring clean transitions and preventing glitches. Unlike conventional designs that space thresholds evenly, this implementation focuses on separating the high-to-low and low-to-high trip points effectively with minimal transistor count, contributing to area and power efficiency.

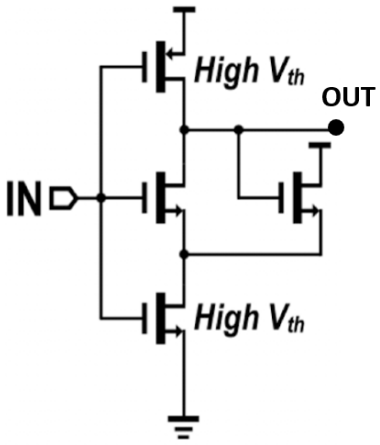


Figure 7: 4T Schmitt trigger schematic

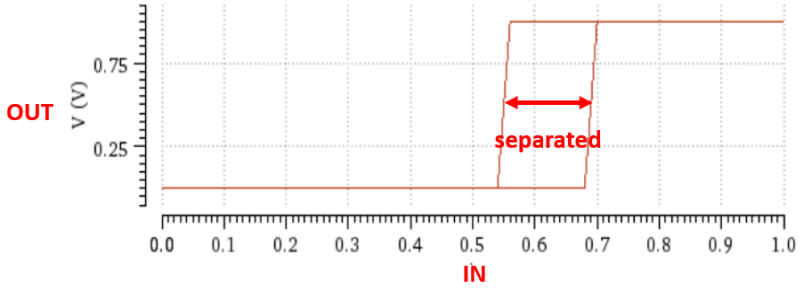


Figure 8: Simulation result showing separated switching thresholds

III Simulation Results

This section presents post-layout simulation results of the proposed oscillator using the TSMC 180 nm CMOS process. We analyze nominal performance, sensitivity to voltage and temperature variations, offset cancellation, mismatch behavior, noise characteristics, and setup time.

III.i Nominal Performance

The oscillator achieves a nominal frequency of 18.37 kHz and power consumption of only 72.02 nW at 1 V. The output waveform and comparator inputs validate correct phase operation and voltage swing.

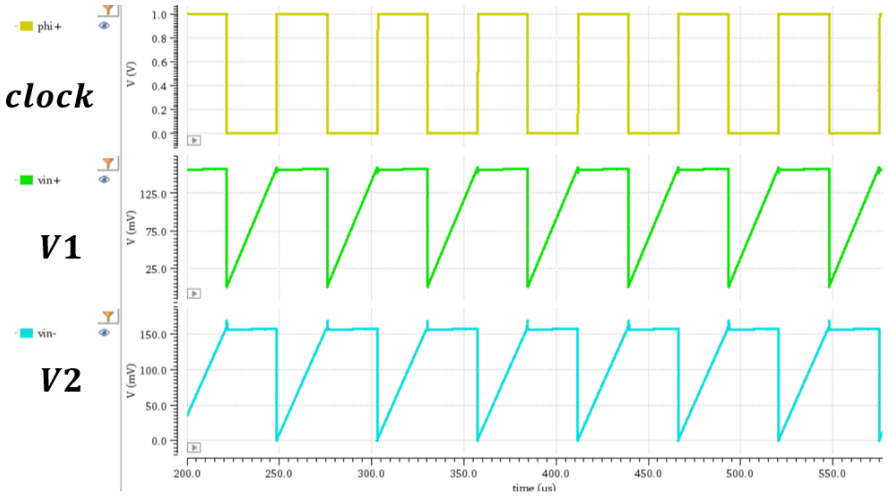


Figure 9: Clock, V1, and V2 waveforms in nominal condition

III.ii Temperature and Supply Voltage Variation

The oscillator maintains stable operation over a wide temperature range and supply voltage range. The frequency sensitivity is approximately 0.66%/V from 0.95 V to 1.05 V, and the temperature-induced period variation is within ±0.52%.

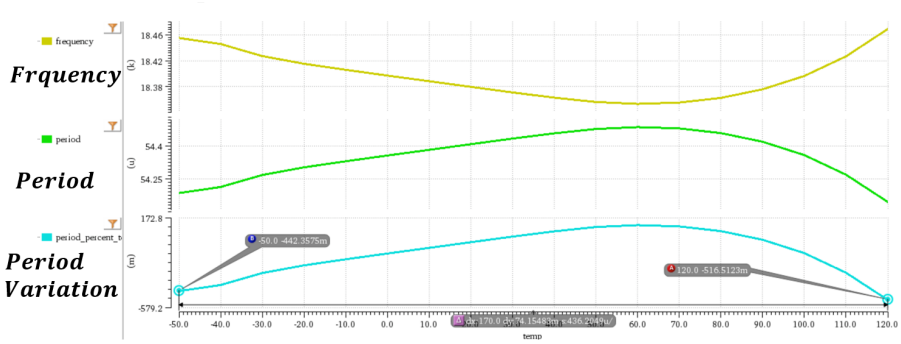


Figure 10: Frequency and period variation over temperature (−50°C to 120°C)

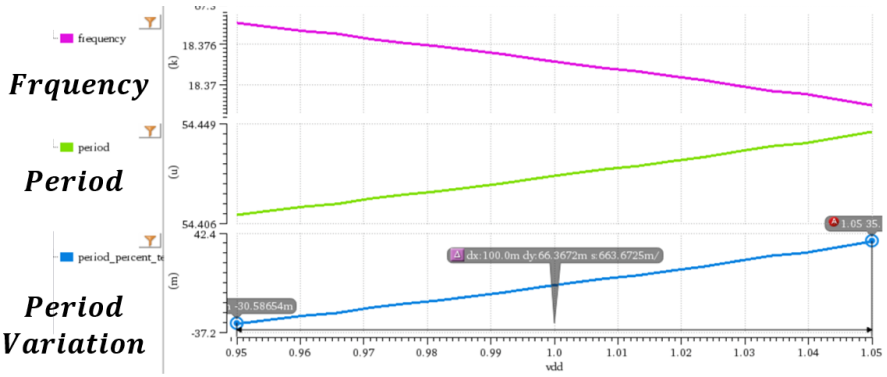


Figure 11: Frequency and period variation over supply voltage (0.95 V to 1.05 V)

III.iii Offset Cancellation Mechanism

The oscillator operates in two symmetric charging phases, each involving a current source and an RC charging path. In the presence of a comparator input offset voltage V_{os}, the impact of this offset is largely cancelled over the full cycle due to its opposite contribution in the two half-phases.

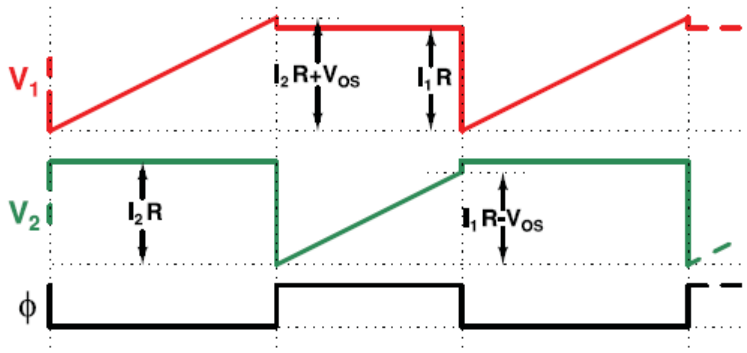


Figure 12: Waveform illustrating V_{os} cancellation in two charging phases

The ideal period without mismatch is:

$$t_{\text{period}} = \frac{RC_1I_2}{I_1} + \frac{RC_2I_1}{I_2} + V_{\text{os}}\left(\frac{C_1}{I_1} - \frac{C_2}{I_2}\right) + 2t_{\text{delay}}.$$

Assuming mismatch in current and capacitance is characterized by small variations α and β, we define:

$$C_1 = C(1+\alpha), \quad C_2 = C(1-\alpha), \quad I_1 = I(1-\beta), \quad I_2 = I(1+\beta).$$

Substituting into the period expression and simplifying gives:

$$t_{\text{period}} \approx 2RC\left[1 + 2\alpha\beta + \frac{V_{\text{os}}}{IR}(\alpha+\beta)\right] + 2t_{\text{delay}}.$$

From this result, we observe that: - When $\alpha = \beta = 0$, the term involving V_{os} cancels out entirely. - When mismatch exists, the offset-induced error becomes linearly proportional to $(\alpha + \beta)$.

This confirms that our design naturally cancels out offset in ideal symmetric conditions and maintains low sensitivity even in the presence of moderate mismatch.

III.iii.a Offset-Only Simulation

Vos is swept without introducing mismatch ($\alpha = \beta = 0$). The period remains stable, confirming cancellation. (4.33 ppm/mV)

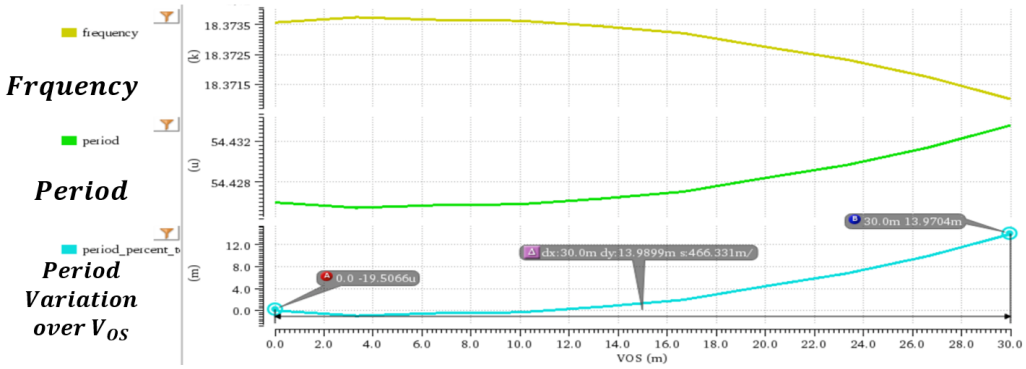


Figure 13: Period variation over Vos with matched current and capacitor

III.iii.b Offset Under Mismatch

With $\alpha = \beta = 2.5\%$, the offset no longer cancels and causes clear linear variation in period.($444\ ppm/mV$)

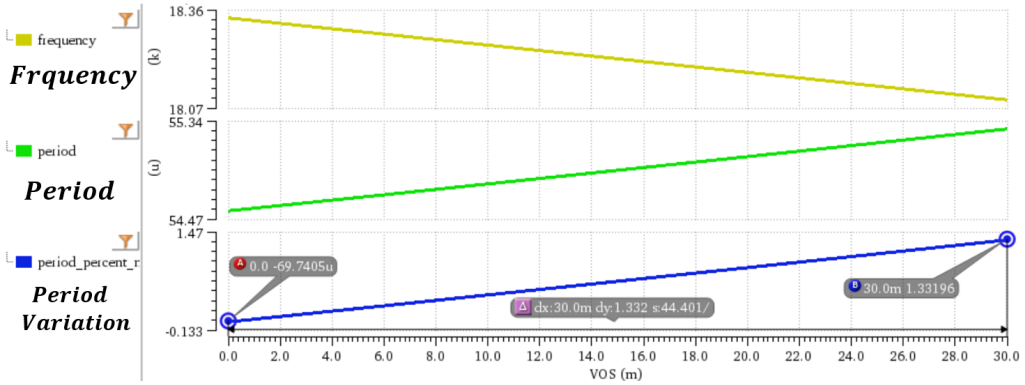


Figure 14: Period variation over Vos under mismatch ($\alpha = \beta = 2.5\%$)

Offset Cancellation Observation

To further illustrate the offset cancellation mechanism, we analyze the individual half periods under a mismatch condition with $\alpha = \beta = 2.5\%$. Two cases are compared: $V_{\text{os}} = 0$ and $V_{\text{os}} = 10$ mV.

Simulation results show that while each half period changes significantly—one increases, the other decreases—the overall period remains nearly unchanged. This behavior confirms that the offset V_{os} contributes additively in one phase and subtractively in the other, effectively cancelling out over a full cycle.

Table 1: Period observation under 2.5% mismatch and V_{os} variation

	$V_{os} = 0$	$V_{os} = 10$ **mV**	**Change**
Half period 1 (μs)	27.7635	29.5333	+6.374%
Half period 2 (μs)	26.6527	24.9726	−6.304%
Total period (μs)	54.4162	54.5059	+0.165%

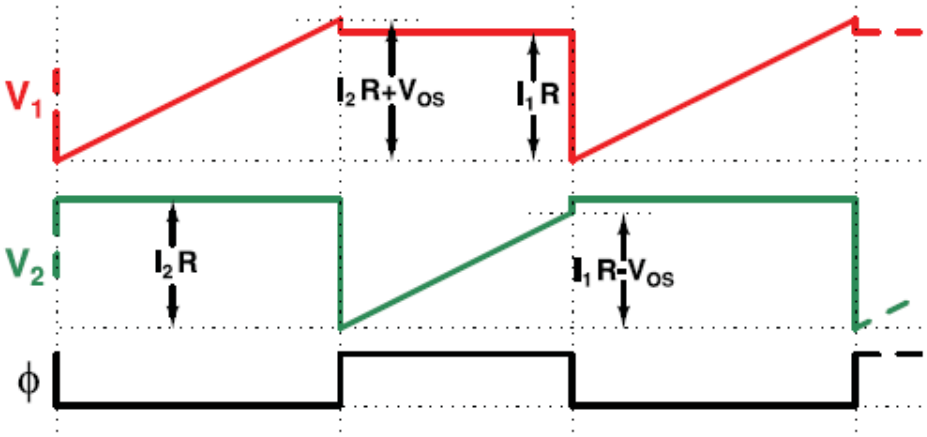
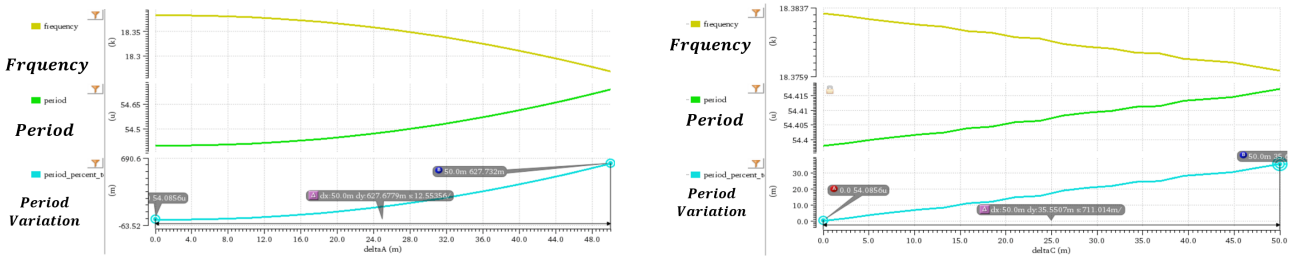


Figure 15: Cancellation of V_{os} across two charging phases

These results visually and numerically validate that the proposed architecture cancels out the comparator input offset over one full oscillation cycle, even in the presence of moderate mismatch.

III.iii.c Individual Mismatch Effects

We sweep β (current mismatch only) and α (capacitance mismatch only) independently to quantify their individual contributions.



(a) Current mismatch only(627.7 ppm/mV) (b) Capacitor mismatch only(35.6 ppm/mV)

Figure 16: Period variation with individual mismatch sources

III.iv Noise Performance

III.iv.a Phase Noise

Phase noise is measured across multiple offset frequencies. The design achieves -25.9 dBc/Hz at 10 Hz and -90.7 dBc/Hz at 10 kHz.

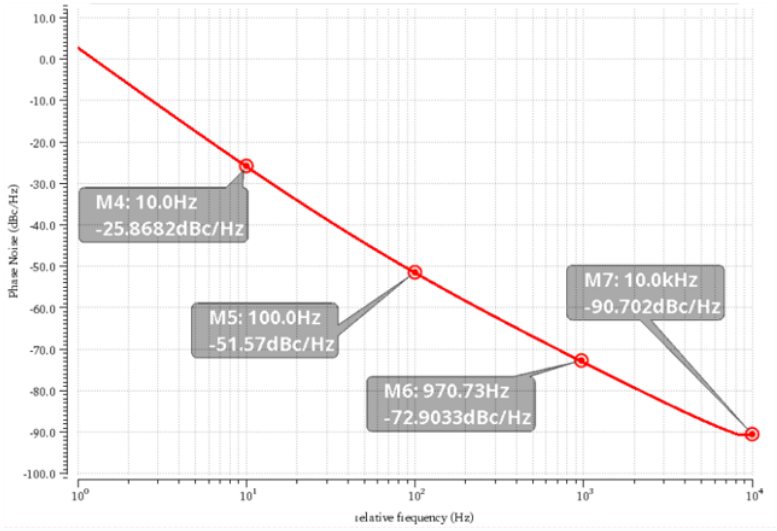


Figure 17: Phase noise plot across frequency offset

III.iv.b Allan Deviation

Allan deviation characterizes long-term timing stability. Our results show a slope close to $-1/2$ for $\tau < 1$ s, indicating white phase noise.

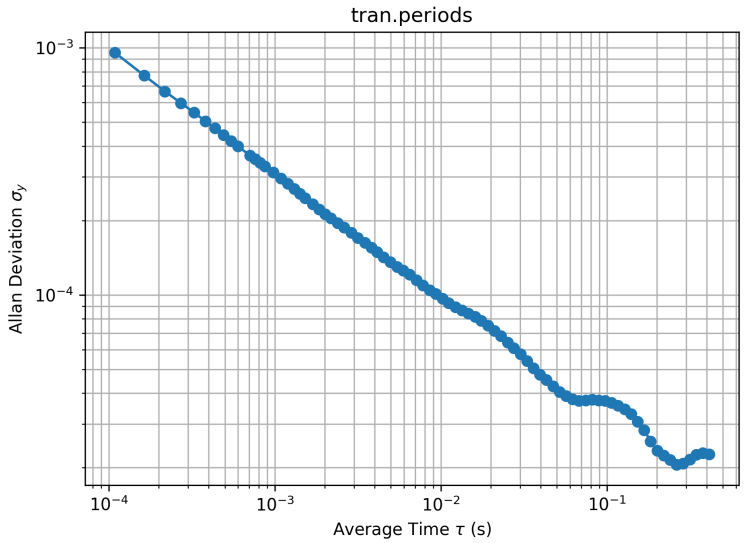


Figure 18: Allan deviation versus averaging time

III.v Setup Time

Simulation confirms that the oscillator reaches frequency stability within 4 cycles after power-up.

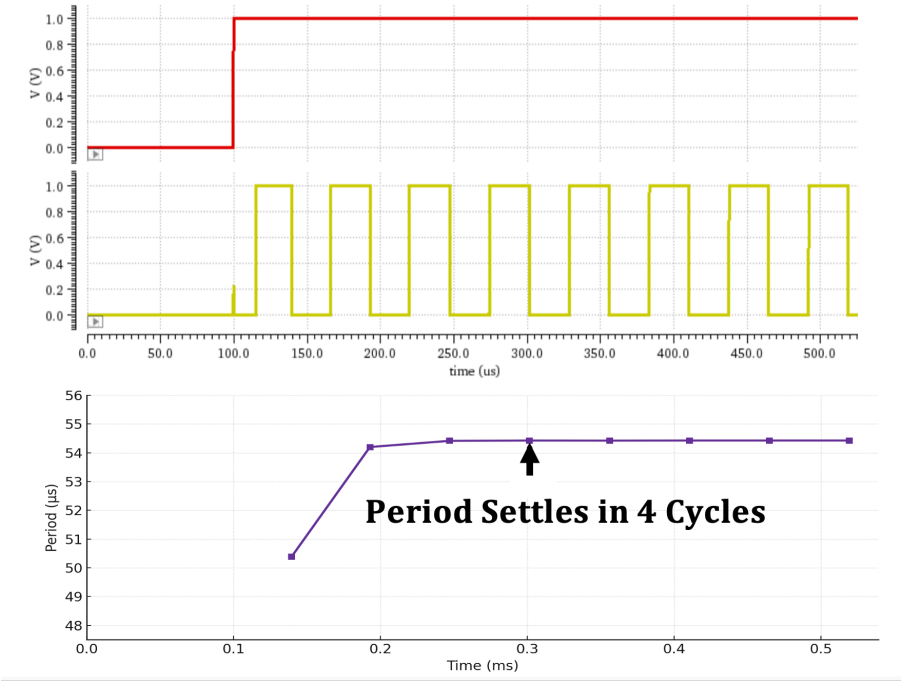


Figure 19: Oscillator output settles within 4 clock cycles

III.vi Comparison with Prior Work

We compare our design against a previously published low-power RC oscillator. The proposed design offers lower power, better voltage stability, and a wider operating temperature range.

Spec	Paper	Proposed Circuit
Technology	65 nm	180 nm
Frequency	18.5 kHz	18.37 kHz
Power	130 nW	72.02 nW
Temp. Accuracy (%)	$\pm 0.18 \sim \pm 0.55$ $(-40\,°C \sim 90°C)$	± 0.52 $(-50\,°C \sim 120°C)$
Voltage Accuracy $(0.95\,V \sim 1.05\,V)$	$< 5\ \%/V$	$0.66\ \%/V$
Start up cycles	4	4

Figure 20: Comparison between our oscillator and prior work

IV Conclusion

In this project, we proposed and verified a **low-power RC relaxation oscillator** featuring **comparator offset cancellation** and **energy-efficient techniques**. The architecture incorporates a **logic-controlled comparator enable signal** and a **Schmitt trigger** to suppress phase transition glitches, while a **compact level shifter** efficiently translates analog voltages to digital control signals.

Implemented using a **180 nm TSMC CMOS process**, the proposed oscillator achieves an **oscillation frequency of 18.37 kHz** and **ultra-low power consumption of only 72.02 nW** at 1 V. Post-layout simulation results demonstrate excellent robustness across process-voltage-temperature (PVT) variations, including:

- **Temperature accuracy**: within $\pm 0.52\%$ from $-50°C$ to $120°C$.
- **Voltage sensitivity**: $0.66\%/V$ across the range 0.95 V to 1.05 V.
- **Startup time**: only **4 oscillation cycles**.

Offset cancellation is validated both analytically and through simulation, showing **strong immunity under matched conditions** and **moderate sensitivity under mismatch**. **Noise performance** is also acceptable for low-frequency clock generation, with **phase noise of -90.7 dBc/Hz at 10 kHz** and **white-dominated Allan deviation behavior**.

Compared to prior works, our oscillator achieves **better energy efficiency**, **broader temperature range**, and **competitive accuracy**, making it a strong candidate for **ultra-low-power timing applications** in sensor nodes and always-on IoT systems.

References

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