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Instructor's Resource Manual
to accompany

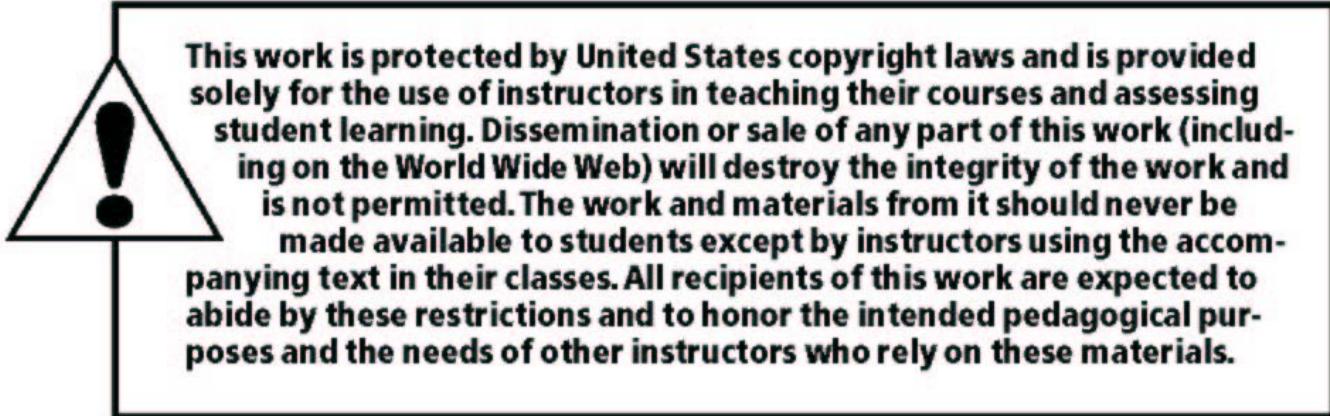
Electronic Devices

Eighth Edition

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Chapter 1

Introduction to Semiconductors

Section 1-1 Atomic Structure

1. An atom with an atomic number of 6 has **6 electrons** and **6 protons**.
 2. The third shell of an atom can have $2n^2 = 2(3)^2 = \mathbf{18}$ electrons.

Section 1-2 Insulators, Conductors, and Semiconductors

Section 1-3 Current in Semiconductors

6. When heat is added to silicon, more free electrons and holes are produced.
 7. Current is produced in silicon at the **conduction** band and the **valence** band.

Section 1-4 N-Type and P-Type Semiconductors

8. Doping is the carefully controlled addition of trivalent or pentavalent atoms to pure (intrinsic) semiconductor material for the purpose of increasing the number of majority carriers (free electrons or holes).
 9. Antimony is a pentavalent (donor) material used for doping to increase free electrons. Boron is a trivalent (acceptor) material used for doping to increase the holes.

Section 1-5 The Diode

- 10.** The electric field across the *pn* junction of a diode is created by donor atoms in the *n* region losing free electrons to acceptor atoms in the *p* region. This creates positive ions in the *n* region near the junction and negative ions in the *p* region near the junction. A field is then established between the ions.
 - 11.** The barrier potential of a diode represents an energy gradient that must be overcome by conduction electrons and produces a voltage drop, not a source of energy.

Chapter 1

Section 1-6 Biasing a Diode

12. To forward-bias a diode, the positive terminal of a voltage source must be connected to the **p** region.
13. A series resistor is needed to **limit the current** through a forward-biased diode to a value that will not damage the diode because the diode itself has very little resistance.

Section 1-7 Voltage-Current Characteristic of a Diode

14. To generate the forward bias portion of the characteristic curve, connect a voltage source across the diode for forward bias and place an ammeter in series with the diode and a voltmeter across the diode. Slowly increase the voltage from zero and plot the forward voltage versus the current.
15. A temperature increase would cause the barrier potential of a silicon diode to decrease from 0.7 V to 0.6 V.

Section 1-8 Diode Models

16. (a) The diode is reverse-biased.
(c) The diode is forward-biased.
(b) The diode is forward-biased.
(d) The diode is forward-biased.
17. (a) $V_R = 5 \text{ V} - 8 \text{ V} = -3 \text{ V}$
(b) $V_F = 0.7 \text{ V}$
(c) $V_F = 0.7 \text{ V}$
(d) $V_F = 0.7 \text{ V}$
18. (a) $V_R = 5 \text{ V} - 8 \text{ V} = -3 \text{ V}$
(b) $V_F = 0 \text{ V}$
(c) $V_F = 0 \text{ V}$
(d) $V_F = 0 \text{ V}$
19. Ignoring r'_R :
(a) $V_R \approx 5 \text{ V} - 8 \text{ V} = -3 \text{ V}$
(b) $I_F = \frac{100 \text{ V} - 0.7 \text{ V}}{560 \Omega + 10 \Omega} = 174 \text{ mA}$
$$V_F = I_F r'_d + V_B = (174 \text{ mA})(10 \Omega) + 0.7 \text{ V} = 2.44 \text{ V}$$

(c) $I_{tot} = \frac{30 \text{ V}}{R_{tot}} = \frac{30 \text{ V}}{4.85 \text{ k}\Omega} = 6.19 \text{ mA}$
$$I_F = \frac{6.19 \text{ mA}}{2} = 3.1 \text{ mA}$$

$$V_F = I_F r'_d + 0.7 \text{ V} = (3.1 \text{ mA})(10 \Omega) + 0.7 \text{ V} = 0.731 \text{ V}$$

- (d) Approximately all of the current from the 20 V source is through the diode. No current from the 10 V source is through the diode.

$$I_F = \frac{20 \text{ V} - 0.7 \text{ V}}{10 \text{ k}\Omega + 10 \Omega} = 1.92 \text{ mA}$$

$$V_F = (1.92 \text{ mA})(10 \Omega) + 0.7 \text{ V} = \mathbf{0.719 \text{ V}}$$

Section 1-9 Testing a Diode

20. (a) Since $V_D = 25 \text{ V} = 0.5V_S$, the diode is **open**.
(b) The diode is forward-biased but since $V_D = 15 \text{ V} = V_S$, the diode is **open**.
(c) The diode is reverse-biased but since $V_R = 2.5 \text{ V} = 0.5V_S$, the diode is **shorted**.
(d) The diode is reverse-biased and $V_R = 0 \text{ V}$. The diode is **operating properly**.
21. $V_A = V_{S1} = +25 \text{ V}$
 $V_B = V_{S1} - 0.7 \text{ V} = 25 \text{ V} - 0.7 \text{ V} = +24.3 \text{ V}$
 $V_C = V_{S2} + 0.7 \text{ V} = 8 \text{ V} + 0.7 \text{ V} = +8.7 \text{ V}$
 $V_D = V_{S2} = +8.0 \text{ V}$

Multisim Troubleshooting Problems

The solutions showing instrument connections for problems 22 through 30 are available from the Instructor Resource Center. The faults in the circuit files may be accessed using the password *book* (all lowercase).

To access supplementary materials online, instructors need to request an instructor access code. Go to www.prenhall.com, click the **Instructor Resource Center** link, and then click **Register Today** for an instructor access code. Within 48 hours after registering, you will receive a confirming e-mail that includes an instructor access code. Once you have received your code, go to the site and log on for full instructions on downloading the materials you wish to use.

22. Diode shorted
23. Diode open
24. Diode open
25. Diode shorted
26. No fault
27. Diode shorted
28. Diode leaky
29. Diode open
30. Diode shorted

Chapter 2

Diode Applications

Section 2-1 Half-Wave Rectifiers

1. See Figure 2-1.

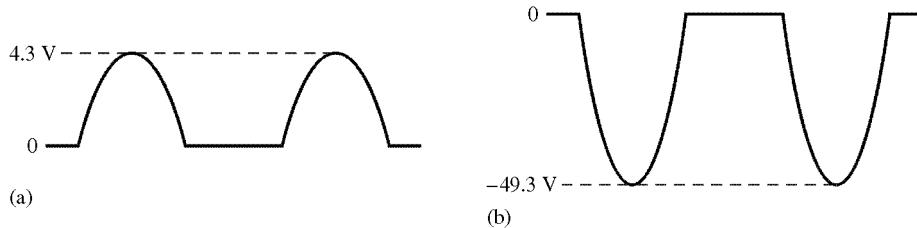


Figure 2-1

2. (a) PIV = $V_p = 5 \text{ V}$ (b) PIV = $V_p = 50 \text{ V}$

$$3. \quad V_{AVG} = \frac{V_p}{\pi} = \frac{200 \text{ V}}{\pi} = 63.7 \text{ V}$$

$$4. \quad (a) \quad I_F = \frac{V_{(p)in} - 0.7 \text{ V}}{R} = \frac{5 \text{ V} - 0.7 \text{ V}}{47 \Omega} = \frac{4.3 \text{ V}}{47 \Omega} = 91.5 \text{ mA}$$

$$(b) \quad I_F = \frac{V_{(p)in} - 0.7 \text{ V}}{R} = \frac{50 \text{ V} - 0.7 \text{ V}}{3.3 \text{ k}\Omega} = \frac{49.3 \text{ V}}{3.3 \text{ k}\Omega} = 14.9 \text{ mA}$$

$$5. \quad V_{sec} = nV_{pri} = (0.2)120 \text{ V} = 24 \text{ V rms}$$

$$6. \quad V_{sec} = nV_{pri} = (0.5)120 \text{ V} = 60 \text{ V rms}$$

$$V_{p(sec)} = 1.414(60 \text{ V}) = 84.8 \text{ V}$$

$$V_{avg(sec)} = \frac{V_{p(sec)}}{\pi} = \frac{84.8 \text{ V}}{\pi} = 27.0 \text{ V}$$

$$P_{L(p)} = \frac{(V_{p(sec)} - 0.7 \text{ V})^2}{R_t} = \frac{(84.1 \text{ V})^2}{220 \Omega} = \mathbf{32.1 \text{ W}}$$

$$P_{L(\text{avg})} = \frac{(V_{\text{avg(sec)}})^2}{R_L} = \frac{(27.0 \text{ V})^2}{220 \Omega} = \mathbf{3.31 \text{ W}}$$

Section 2-2 Full-Wave Rectifiers

7. (a) $V_{AVG} = \frac{V_p}{\pi} = \frac{5 \text{ V}}{\pi} = 1.59 \text{ V}$
- (b) $V_{AVG} = \frac{2V_p}{\pi} = \frac{2(100 \text{ V})}{\pi} = 63.7 \text{ V}$
- (c) $V_{AVG} = \frac{2V_p}{\pi} + 10 \text{ V} = \frac{2(10 \text{ V})}{\pi} + 10 \text{ V} = 16.4 \text{ V}$
- (d) $V_{AVG} = \frac{2V_p}{\pi} - 15 \text{ V} = \frac{2(40 \text{ V})}{\pi} - 15 \text{ V} = 10.5 \text{ V}$

8. (a) Center-tapped full-wave rectifier
 (b) $V_{p(sec)} = (0.25)(1.414)120 \text{ V} = 42.4 \text{ V}$
 (c) $\frac{V_{p(sec)}}{2} = \frac{42.4 \text{ V}}{2} = 21.2 \text{ V}$
 (d) See Figure 2-2. $V_{RL} = 21.2 \text{ V} - 0.7 \text{ V} = 20.5 \text{ V}$

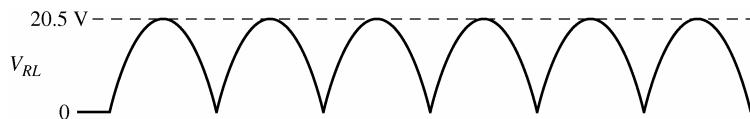


Figure 2-2

- (e) $I_F = \frac{\frac{V_{p(sec)}}{2} - 0.7 \text{ V}}{R_L} = \frac{20.5 \text{ V}}{1.0 \text{ k}\Omega} = 20.5 \text{ mA}$
- (f) PIV = $21.2 \text{ V} + 20.5 \text{ V} = 41.7 \text{ V}$
9. $V_{AVG} = \frac{120 \text{ V}}{2} = 60 \text{ V}$ for each half
- $$V_{AVG} = \frac{V_p}{\pi}$$
- $$V_p = \pi V_{AVG} = \pi(60 \text{ V}) = 186 \text{ V}$$
10. See Figure 2-3.

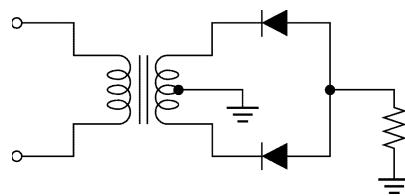


Figure 2-3

Chapter 2

11. $PIV = V_p = \frac{\pi V_{AVG(out)}}{2} = \frac{\pi(50 \text{ V})}{2} = 78.5 \text{ V}$

12. $PIV = V_{p(out)} = 1.414(20 \text{ V}) = 28.3 \text{ V}$

13. See Figure 2-4.

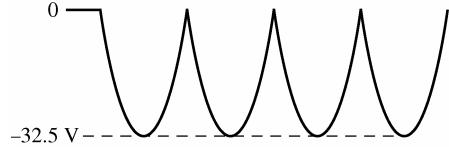


Figure 2-4

Section 2-3 Power Supply Filters and Regulators

14. $V_{r(pp)} = 0.5 \text{ V}$

$$r = \frac{V_{r(pp)}}{V_{DC}} = \frac{0.5 \text{ V}}{75 \text{ V}} = 0.00667$$

15. $V_{r(pp)} = \frac{V_{p(in)}}{fR_L C} = \frac{30 \text{ V}}{(120 \text{ Hz})(600 \Omega)(50 \mu\text{F})} = 8.33 \text{ V pp}$

$$V_{DC} = \left(1 - \frac{1}{2fR_L C}\right) V_{p(in)} = \left(1 - \frac{1}{(240 \text{ Hz})(600 \Omega)(50 \mu\text{F})}\right) 30 \text{ V} = 25.8 \text{ V}$$

16. $\% r = \left(\frac{V_{r(pp)}}{V_{DC}}\right) 100 = \left(\frac{8.33 \text{ V}}{25.8 \text{ V}}\right) 100 = 32.3\%$

17. $V_{r(pp)} = (0.01)(18 \text{ V}) = 180 \text{ mV}$

$$V_{r(pp)} = \left(\frac{1}{fR_L C}\right) V_{p(in)}$$

$$C = \left(\frac{1}{fR_L V_r}\right) V_{p(in)} = \left(\frac{1}{(120 \text{ Hz})(1.5 \text{ k}\Omega)(180 \text{ mV})}\right) 18 \text{ V} = 556 \mu\text{F}$$

18. $V_{r(pp)} = \frac{V_{p(in)}}{fR_L C} = \frac{80 \text{ V}}{(120 \text{ Hz})(10 \text{ k}\Omega)(10 \mu\text{F})} = 6.67 \text{ V}$

$$V_{DC} = \left(1 - \frac{1}{2fR_L C}\right) V_{p(in)} = \left(1 - \frac{1}{(240 \text{ Hz})(10 \text{ k}\Omega)(10 \mu\text{F})}\right) 80 \text{ V} = 76.7 \text{ V}$$

$$r = \frac{V_{r(pp)}}{V_{DC}} = \frac{6.67 \text{ V}}{76.7 \text{ V}} = 0.087$$

19. $V_{p(sec)} = (1.414)(36 \text{ V}) = 50.9 \text{ V}$

$$V_{r(rect)} = V_{p(sec)} - 1.4 \text{ V} = 50.9 \text{ V} - 1.4 \text{ V} = 49.5 \text{ V}$$

$$\text{Neglecting } R_{\text{surge}}, \quad V_{r(pp)} = \left(\frac{1}{fR_L C} \right) V_{p(rect)} = \left(\frac{1}{(120 \text{ Hz})(3.3 \text{ k}\Omega)(100 \mu\text{F})} \right) 49.5 \text{ V} = 1.25 \text{ V}$$

$$V_{DC} = \left(1 - \frac{1}{2fR_L C} \right) V_{p(rect)} = V_{p(rect)} - \frac{V_{r(pp)}}{2} = 49.5 \text{ V} - 0.625 \text{ V} = 48.9 \text{ V}$$

20. $V_{p(sec)} = 1.414(36 \text{ V}) = 50.9 \text{ V}$

See Figure 2-5.

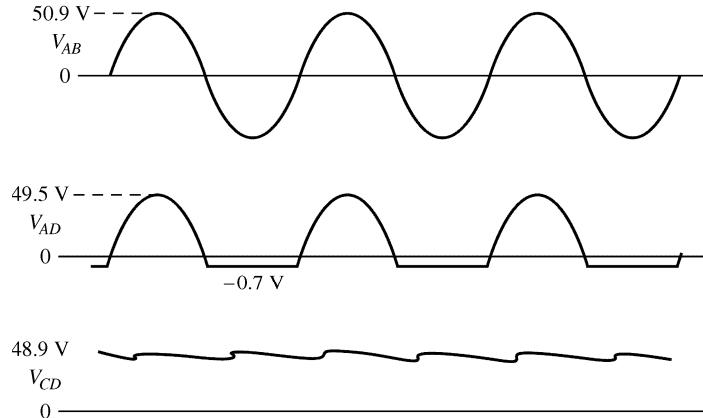


Figure 2-5

21. Load regulation = $\left(\frac{V_{NL} - V_{FL}}{V_{FL}} \right) 100\% = \left(\frac{15.5 \text{ V} - 14.9 \text{ V}}{14.9 \text{ V}} \right) 100\% = 4\%$

22. $V_{FL} = V_{NL} - (0.005)V_{NL} = 12 \text{ V} - (0.005)12 \text{ V} = 11.94 \text{ V}$

Section 2-4 Diode Limiting and Clamping Circuits

23. See Figure 2-6.

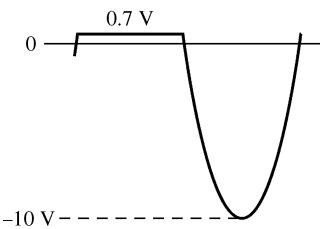


Figure 2-6

Chapter 2

24. Apply Kirchhoff's law at the peak of the positive half cycle:

(b) $25 \text{ V} = V_{R1} + V_{R2} + 0.7 \text{ V}$

$$2V_R = 24.3 \text{ V}$$

$$V_R = \frac{24.3 \text{ V}}{2} = 12.15 \text{ V}$$

$$V_{out} = V_R + 0.7 \text{ V} = 12.15 \text{ V} + 0.7 \text{ V} = 12.85 \text{ V}$$

See Figure 2-7(a).

(c) $V_R = \frac{11.3 \text{ V}}{2} = 5.65 \text{ V}$

$$V_{out} = V_R + 0.7 \text{ V} = 5.65 \text{ V} + 0.7 \text{ V} = 6.35 \text{ V}$$

See Figure 2-7(b).

(d) $V_R = \frac{4.3 \text{ V}}{2} = 2.15 \text{ V}$

$$V_{out} = V_R + 0.7 \text{ V} = 2.15 \text{ V} + 0.7 \text{ V} = 2.85 \text{ V}$$

See Figure 2-7(c).

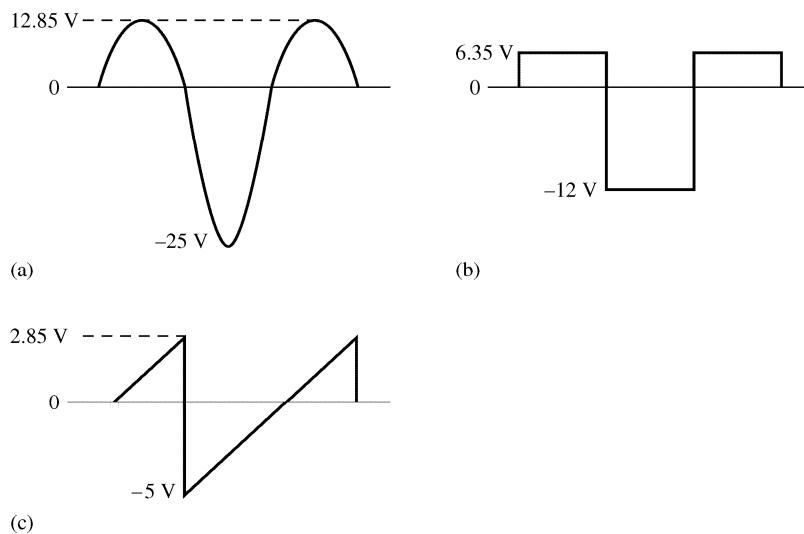


Figure 2-7

25. See Figure 2-8.

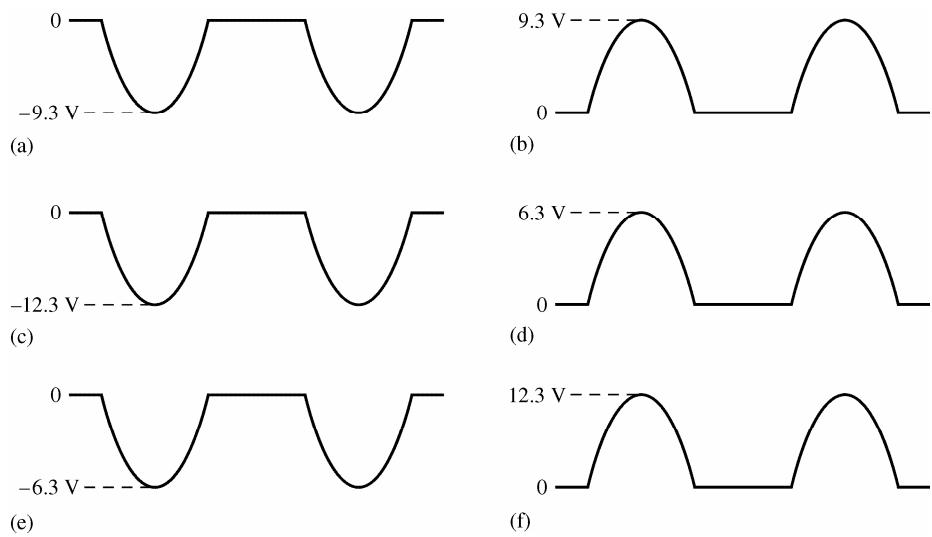


Figure 2-8

26. See Figure 2-9.

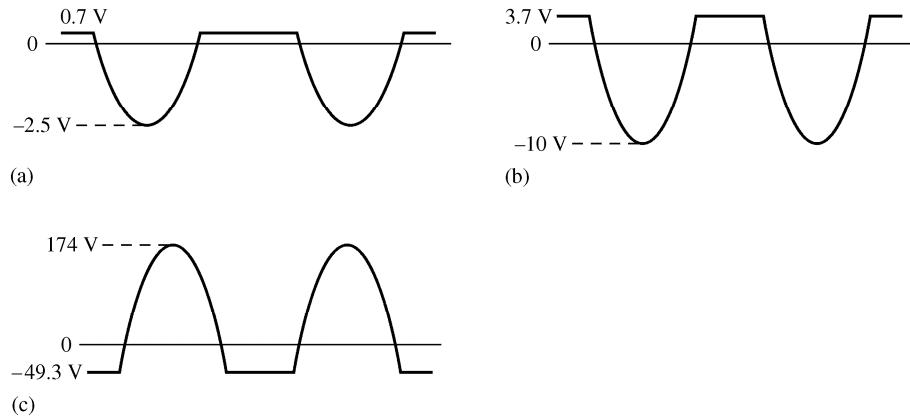


Figure 2-9

27. See Figure 2-10.

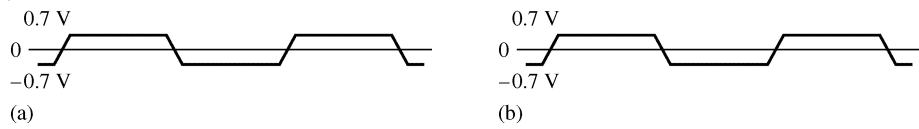


Figure 2-10

28. (a) $I_p = \frac{30\text{ V} - 0.7\text{ V}}{2.2\text{ k}\Omega} = 13.3\text{ mA}$

(b) Same as (a).

Chapter 2

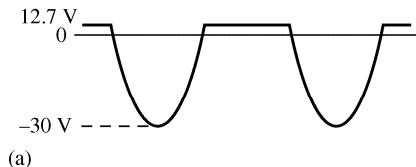
29. (a) $I_p = \frac{30\text{ V} - (12\text{ V} + 0.7\text{ V})}{2.2\text{ k}\Omega} = 7.86\text{ mA}$

(b) $I_p = \frac{30\text{ V} - (12\text{ V} - 0.7\text{ V})}{2.2\text{ k}\Omega} = 8.5\text{ mA}$

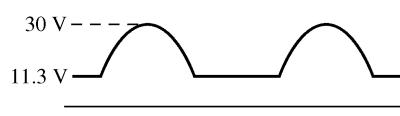
(c) $I_p = \frac{30\text{ V} - (-11.3\text{ V})}{2.2\text{ k}\Omega} = 18.8\text{ mA}$

(d) $I_p = \frac{30\text{ V} - (-12.7\text{ V})}{2.2\text{ k}\Omega} = 19.4\text{ mA}$

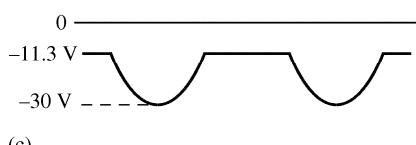
30. See Figure 2-11.



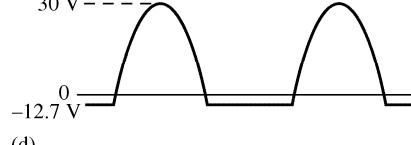
(a)



(b)



(c)



(d)

Figure 2-11

31. (a) A sine wave with a positive peak at 0.7 V, a negative peak at -7.3 V, and a dc value of -3.3 V.
 (b) A sine wave with a positive peak at 29.3 V, a negative peak at -0.7 V, and a dc value of +14.3 V.
 (c) A square wave varying from +0.7 V to -15.3 V with a dc value of -7.3 V.
 (d) A square wave varying from +1.3 V to -0.7 V with a dc value of +0.3 V.
32. (a) A sine wave varying from -0.7 V to +7.3 V with a dc value of +3.3 V.
 (b) A sine wave varying from -29.3 V to +7.3 V with a dc value of +14.3 V.
 (c) A square wave varying from -0.7 V to +15.3 V with a dc value of +7.3 V.
 (d) A square wave varying from -1.3 V to +0.7 V with a dc value of -0.3 V.

Section 2-5 Voltage Multipliers

33. $V_{\text{OUT}} = 2V_{p(\text{in})} = 2(1.414)(20\text{ V}) = 56.6\text{ V}$

See Figure 2-12.

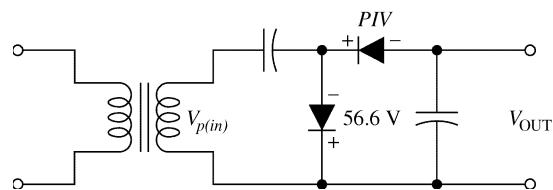


Figure 2-12

- 34.** $V_{\text{OUT}(trip)} = 3V_{p(\text{in})} = 3(1.414)(20 \text{ V}) = 84.8 \text{ V}$
 $V_{\text{OUT}(quad)} = 4V_{p(\text{in})} = 4(1.414)(20 \text{ V}) = 113 \text{ V}$
 See Figure 2-13.

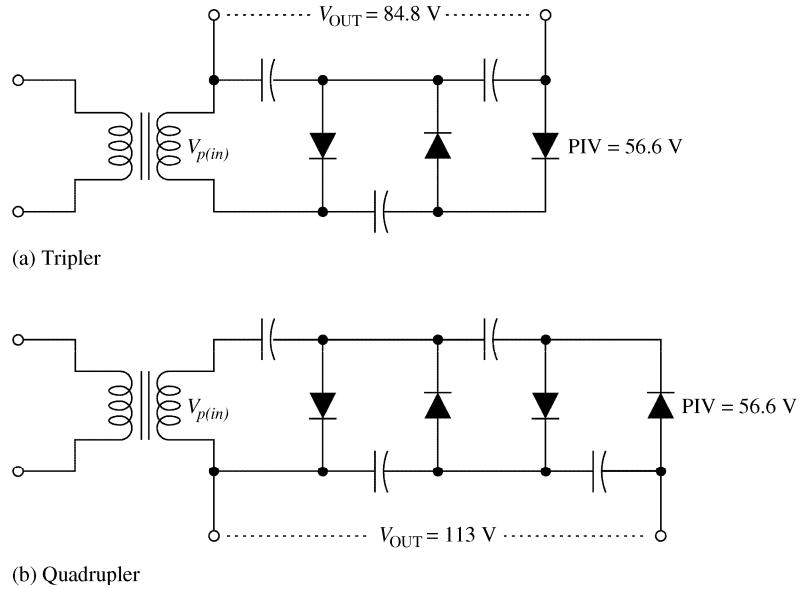


Figure 2-13

Section 2-6 The Diode Datasheet

- 35.** The PIV is specified as the peak repetitive reverse voltage = **100 V**.
- 36.** The PIV is specified as the peak repetitive reverse voltage = **1000 V**.
- 37.** $I_{F(\text{AVG})} = 1.0 \text{ A}$
 $R_{L(\text{min})} = \frac{50 \text{ V}}{1.0 \text{ A}} = 50 \Omega$

Section 2-7 Troubleshooting

- 38.** If a bridge rectifier diode opens, the output becomes a half-wave voltage resulting in an increased ripple at 60 Hz.

39.
$$V_{avg} = \frac{2V_p}{\pi} = \frac{2(115 \text{ V})(1.414)}{\pi} \cong 104 \text{ V}$$

The output of the bridge is correct. However, the 0 V output from the filter indicates that the **surge resistor is open** or that the **capacitor is shorted**.

- 40.** (a) Correct
 (b) Incorrect. Open diode.
 (c) Correct
 (d) Incorrect. Open diode.

Chapter 2

41. $V_{sec} = \frac{120 \text{ V}}{5} = 24 \text{ V rms}$

$$V_{p(sec)} = 1.414(24 \text{ V}) = 33.9 \text{ V}$$

The peak voltage for each half of the secondary is

$$\frac{V_{p(sec)}}{2} = \frac{33.9 \text{ V}}{2} = 17 \text{ V}$$

The peak inverse voltage for each diode is $PIV = 2(17 \text{ V}) + 0.7 \text{ V} = 34.7 \text{ V}$

The peak current through each diode is

$$I_p = \frac{\frac{V_{p(sec)}}{2} - 0.7 \text{ V}}{R_L} = \frac{17.0 \text{ V} - 0.7 \text{ V}}{330 \Omega} = 49.4 \text{ mA}$$

The diode ratings exceed the actual PIV and peak current.

The circuit should not fail.

Application Activity Problems

42. (a) Not plugged into ac outlet or no ac available at outlet. Check plug and/or breaker.

(b) Open transformer winding or open fuse. Check transformer and/or fuse.

(c) Incorrect transformer installed. Replace.

(d) Leaky filter capacitor. Replace.

(e) Rectifier faulty. Replace.

(f) Rectifier faulty. Replace.

43. The rectifier must be connected backwards.

44. -16 V with 60 Hz ripple

Advanced Problems

45. $V_r = \left(\frac{1}{fR_L C} \right) V_{p(in)}$

$$C = \left(\frac{1}{fR_L V_r} \right) V_{p(in)} = \left(\frac{1}{(120 \text{ Hz})(3.3 \text{ k}\Omega)(0.5 \text{ V})} \right) 35 \text{ V} = 177 \mu\text{F}$$

46. $V_{DC} = \left(1 - \frac{1}{2fR_L C} \right) V_{p(in)}$

$$\frac{V_{DC}}{V_{p(in)}} = \left(1 - \frac{1}{2fR_L C} \right)$$

$$\frac{1}{2fR_L C} = 1 - \frac{V_{DC}}{V_{p(in)}}$$

$$\frac{1}{2fR_L \left(1 - \frac{V_{DC}}{V_{p(in)}} \right)} = C$$

$$C = \frac{1}{(240 \text{ Hz})(1.0 \text{ k}\Omega)(1 - 0.933)} = \frac{1}{(240 \text{ Hz})(1.0 \text{ k}\Omega)(0.067)} = 62.2 \mu\text{F}$$

Then

$$V_r = \left(\frac{1}{fR_L C} \right) V_{p(in)} = \left(\frac{1}{(120 \text{ Hz})(1.0 \text{ k}\Omega)(62.2 \mu\text{F})} \right) 15 \text{ V} = 2 \text{ V}$$

- 47.** The capacitor input voltage is

$$V_{p(in)} = (1.414)(24 \text{ V}) - 1.4 \text{ V} = 32.5 \text{ V}$$

$$R_{surge} = \frac{V_{p(in)}}{I_{surge}} = \frac{32.5 \text{ V}}{50 \text{ A}} = 651 \text{ m}\Omega$$

The nearest standard value is 680 mΩ.

- 48.** See Figure 2-14.

The voltage at point A with respect to ground is

$$V_A = 1.414(9 \text{ V}) = 12.7 \text{ V}$$

Therefore,

$$V_B = 12.7 \text{ V} - 0.7 \text{ V} = 12 \text{ V}$$

$$V_r = 0.05V_B = 0.05(12 \text{ V}) = 0.6 \text{ V peak to peak}$$

$$C = \left(\frac{1}{fR_L V_r} \right) V_B = \left(\frac{1}{(120 \text{ Hz})(680 \Omega)(0.6 \text{ V})} \right) 12 \text{ V} = 245 \mu\text{F}$$

The nearest standard value is 270 μF.

Let $R_{surge} = 1.0 \Omega$.

$$I_{surge(max)} = \frac{12 \text{ V}}{1.0 \Omega} = 12 \text{ A}$$

$$I_{F(AV)} = \frac{12 \text{ V}}{680 \Omega} = 17.6 \text{ mA}$$

$$PIV = 2V_{p(out)} + 0.7 \text{ V} = 24.7 \text{ V}$$

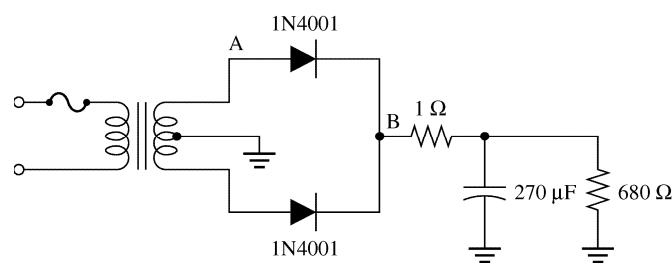


Figure 2-14

Chapter 2

49. See Figure 2-15.

$$I_{L(\max)} = 100 \text{ mA}$$

$$R_L = \frac{9 \text{ V}}{100 \text{ mA}} = 90 \Omega$$

$$V_r = 1.414(0.25 \text{ V}) = 0.354 \text{ V}$$

$$V_r = 2(0.35 \text{ V}) = 0.71 \text{ V peak to peak}$$

$$V_r = \left(\frac{1}{(120 \text{ Hz})(90 \Omega)C} \right) 9 \text{ V}$$

$$C = \frac{9 \text{ V}}{(120 \text{ Hz})(90 \Omega)(0.71 \text{ V})} = 1174 \mu\text{F}$$

Use $C = 1200 \mu\text{F}$.

Each half of the supply uses identical components. 1N4001 diodes are feasible since the average current is $(0.318)(100 \text{ mA}) = 31.8 \text{ mA}$.

$R_{\text{surge}} = 1.0 \Omega$ will limit the surge current to an acceptable value.

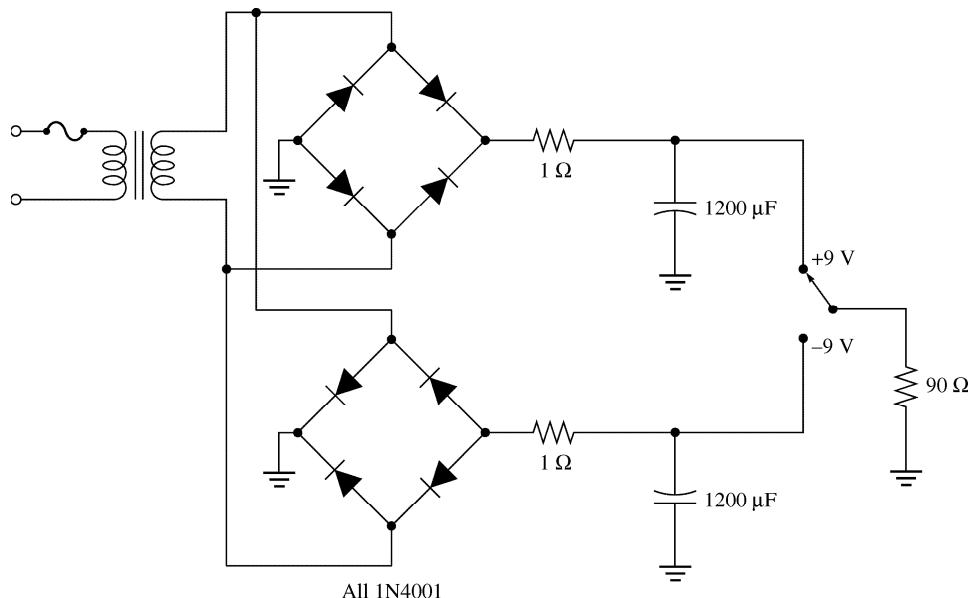


Figure 2-15

50. See Figure 2-16.

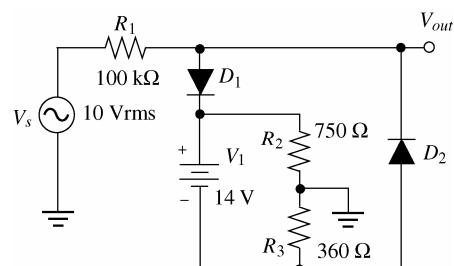


Figure 2-16

$$V_{C1} = (1.414)(120 \text{ V}) - 0.7 \text{ V} = 170 \text{ V}$$

$$V_{C2} = 2(1.414)(120 \text{ V}) - 2(0.7 \text{ V}) = 338 \text{ V}$$

Multisim Troubleshooting Problems

The solutions showing instrument connections for Problems 52 through 60 are available from the Instructor Resource Center. See Chapter 1 for instructions. The faults in the circuit files may be accessed using the password *book* (all lowercase).

- 52.** Diode shorted
- 53.** Diode leaky
- 54.** Diode open
- 55.** Bottom diode open
- 56.** Reduced transformer turns ratio
- 57.** Open filter capacitor
- 58.** Diode leaky
- 59.** D_1 open
- 60.** Load resistor open

Chapter 3

Special-Purpose Diodes

Section 3-1 The Zener Diode

1. See Figure 3-1.

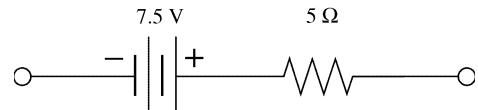


Figure 3-1

2. $I_{ZK} \approx 3 \text{ mA}$
 $V_Z \approx -9 \text{ V}$

3. $Z_Z = \frac{\Delta V_Z}{\Delta I_Z} = \frac{5.65 \text{ V} - 5.6 \text{ V}}{30 \text{ mA} - 20 \text{ mA}} = \frac{0.05 \text{ V}}{10 \text{ mA}} = 5 \Omega$

4. $\Delta I_Z = 50 \text{ mA} - 25 \text{ mA} = 25 \text{ mA}$
 $\Delta V_Z = \Delta I_Z Z_Z = (+25 \text{ mA})(15 \Omega) = +0.375 \text{ V}$
 $V_Z = V_Z + \Delta V_Z = 4.7 \text{ V} + 0.375 \text{ V} = 5.08 \text{ V}$

5. $\Delta T = 70^\circ\text{C} - 25^\circ\text{C} = 45^\circ\text{C}$
 $V_Z = 6.8 \text{ V} + \frac{(6.8 \text{ V})(0.0004/\text{ }^\circ\text{C})}{45^\circ\text{C}} = 6.8 \text{ V} + 0.12 \text{ V} = 6.92 \text{ V}$

Section 3-2 Zener Diode Applications

6. $V_{IN(\min)} = V_Z + I_{ZK}R = 14 \text{ V} + (1.5 \text{ mA})(560 \Omega) = 14.8 \text{ V}$

7. $\Delta V_Z = (I_Z - I_{ZK})Z_Z = (28.5 \text{ mA})(20 \Omega) = 0.57 \text{ V}$
 $V_{OUT} = V_Z - \Delta V_Z = 14 \text{ V} - 0.57 \text{ V} = 13.43 \text{ V}$
 $V_{IN(\min)} = I_{ZK}R + V_{OUT} = (1.5 \text{ mA})(560 \Omega) + 13.43 \text{ V} = 14.3 \text{ V}$

8. $\Delta V_Z = I_Z Z_Z = (40 \text{ mA} - 30 \text{ mA})(30 \Omega) = 0.3 \text{ V}$
 $V_Z = 12 \text{ V} + \Delta V_Z = 12 \text{ V} + 0.3 \text{ V} = 12.3 \text{ V}$
 $R = \frac{V_{IN} - V_Z}{40 \text{ mA}} = \frac{18 \text{ V} - 12.3 \text{ V}}{40 \text{ mA}} = 143 \Omega$

9. $V_Z \cong 12 \text{ V} + 0.3 \text{ V} = 12.3 \text{ V}$
See Figure 3-2.

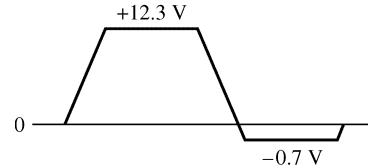


Figure 3-2

10. $V_{Z(\min)} = V_Z - \Delta I_Z Z_Z = 5.1 \text{ V} - (49 \text{ mA} - 1 \text{ mA})(7 \Omega)$
 $= 5.1 \text{ V} - (48 \text{ mA})(7 \Omega) = 5.1 \text{ V} - 0.336 \text{ V} = 4.76 \text{ V}$
 $V_R = 8 \text{ V} - 4.76 \text{ V} = 3.24 \text{ V}$
 $I_T = \frac{V_R}{R} = \frac{3.24 \text{ V}}{22 \Omega} = 147 \text{ mA}$
 $I_{L(\max)} = 147 \text{ mA} - 1 \text{ mA} = \mathbf{146 \text{ mA}}$
 $V_{Z(\max)} = 5.1 \text{ V} + (70 \text{ mA} - 49 \text{ mA})(7 \Omega) = 5.1 \text{ V} + 147 \text{ mV} = 5.25 \text{ V}$
 $V_R = 8 \text{ V} - 5.25 \text{ V} = 2.75 \text{ V}$
 $I_T = \frac{2.75 \text{ V}}{22 \Omega} = 125 \text{ mA}$
 $I_{L(\min)} = 125 \text{ mA} - 70 \text{ mA} = \mathbf{55 \text{ mA}}$

11. % Load regulation = $\frac{V_{Z(\max)} - V_{Z(\min)}}{V_{Z(\min)}} \times 100\% = \frac{5.25 \text{ V} - 4.76 \text{ V}}{4.76 \text{ V}} \times 100\% = \mathbf{10.3\%}$

12. With no load and $V_{IN} = 6 \text{ V}$:

$$I_Z \cong \frac{V_{IN} - V_Z}{R + Z_Z} = \frac{6 \text{ V} - 5.1 \text{ V}}{29 \Omega} = 31 \text{ mA}$$

$$V_{OUT} = V_Z - \Delta I_Z Z_Z = 5.1 \text{ V} - (49 \text{ mA} - 31 \text{ mA})(7 \Omega) = 5.1 \text{ V} - 0.126 \text{ V} = 4.97 \text{ V}$$

With no load and $V_{IN} = 12 \text{ V}$:

$$I_Z \cong \frac{V_{IN} - V_Z}{R + Z_Z} = \frac{12 \text{ V} - 5.1 \text{ V}}{29 \Omega} = 238 \text{ mA}$$

$$V_{OUT} = V_Z + \Delta I_Z Z_Z = 5.1 \text{ V} + (238 \text{ mA} - 49 \text{ mA})(7 \Omega) = 5.1 \text{ V} + 1.32 \text{ V} = 6.42 \text{ V}$$

$$\% \text{ Line regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \times 100\% = \frac{6.42 \text{ V} - 4.97 \text{ V}}{12 \text{ V} - 6 \text{ V}} \times 100\% = \mathbf{24.2\%}$$

13. % Load regulation = $\frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\% = \frac{8.23 \text{ V} - 7.98 \text{ V}}{7.98 \text{ V}} \times 100\% = \mathbf{3.13\%}$

14. % Line regulation = $\frac{\Delta V_{OUT}}{\Delta V_{IN}} \times 100\% = \frac{0.2 \text{ V}}{10 \text{ V} - 5 \text{ V}} \times 100\% = \mathbf{4\%}$

15. % Load regulation = $\frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\% = \frac{3.6 \text{ V} - 3.4 \text{ V}}{3.4 \text{ V}} \times 100\% = \mathbf{5.88\%}$

Chapter 3

Section 3-3 The Varactor Diode

16. At 5 V, $C = 20 \text{ pF}$
At 20 V, $C = 10 \text{ pF}$
 $\Delta C = 20 \text{ pF} - 10 \text{ pF} = 10 \text{ pF}$ (decrease)

17. From the graph, $V_R = 3 \text{ V} @ 25 \text{ pF}$

18. $f_r = \frac{1}{2\pi\sqrt{LC_T}}$

$$C_T = \frac{1}{4\pi^2 L f_r^2} = \frac{1}{4\pi^2 (2 \text{ mH}) (1 \text{ MHz})^2} = 12.7 \text{ pF}$$

Since they are in series, each varactor must have a capacitance of $2C_T = 25.4 \text{ pF}$

19. Each varactor has a capacitance of 25.4 pF. Therefore, from the graph, V_R must be slightly less than 3 V.

Section 3-4 Optical Diodes

20. $I_F = \frac{24 \text{ V}}{680 \Omega} = 35.3 \text{ mA}$

From the graph, the radiant power is approximately **80 mW**.

21. See Figure 3-3.

$$R = \frac{5 \text{ V} - 2.1 \text{ V}}{30 \text{ mA}} = 97 \Omega$$

The nearest standard 1% value is 97.6Ω or the nearest standard 5% value is 91Ω .

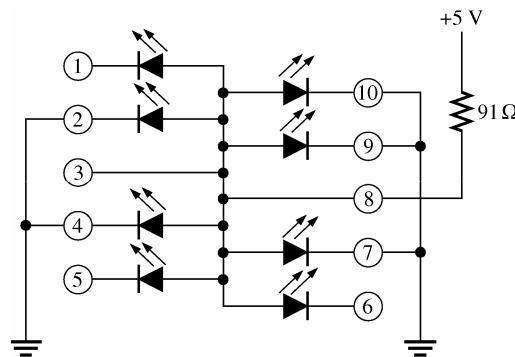


Figure 3-3

22. $V_F \cong 2.2 \text{ V}$ for $I_F = 20 \text{ mA}$

$$\text{Maximum LEDs/branch} = \frac{9 \text{ V}}{2.2 \text{ V}} \cong 4$$

Select 3 LEDs/branch:

$$\text{Number of branches} = \frac{48}{3} = 16$$

$$R_{\text{LIMIT}} = \frac{9 \text{ V} - 3(2.2 \text{ V})}{20 \text{ mA}} = 120 \Omega$$

Use sixteen 120Ω resistors.

23. $V_F \cong 2.5 \text{ V}$ for $I_F = 30 \text{ mA}$

$$\text{Maximum LEDs/branch} = \frac{24 \text{ V}}{2.5 \text{ V}} \cong 9.6$$

Select 5 LEDs/branch:

$$\text{Number of branches} = \frac{100}{5} = 20$$

$$R_{\text{LIMIT}} = \frac{24 \text{ V} - 5(2.5 \text{ V})}{30 \text{ mA}} = 383 \Omega$$

See Figure 3-4.

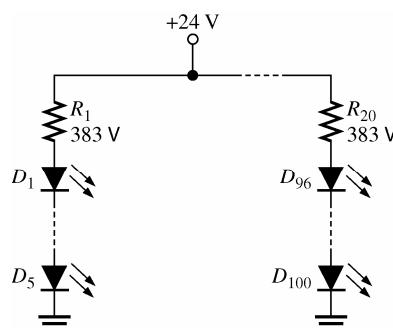


Figure 3-4

24. $I_R = \frac{10 \text{ V}}{200 \text{ k}\Omega} = 50 \mu\text{A}$

Chapter 3

25. (a) $R = \frac{V_S}{I} = \frac{3 \text{ V}}{100 \mu\text{A}} = 30 \text{ k}\Omega$

(b) $R = \frac{V_S}{I} = \frac{3 \text{ V}}{350 \mu\text{A}} = 8.57 \text{ k}\Omega$

(c) $R = \frac{V_S}{I} = \frac{3 \text{ V}}{510 \mu\text{A}} = 5.88 \text{ k}\Omega$

26. The microammeter reading will increase.

Section 3-5 Other Types of Diodes

27. $R = \frac{\Delta V}{\Delta I} = \frac{125 \text{ mV} - 200 \text{ mV}}{0.25 \text{ mA} - 0.15 \text{ mA}} = \frac{-75 \text{ mV}}{0.10 \text{ mA}} = -750 \Omega$

28. Tunnel diodes are used in oscillators.

29. The reflective ends cause the light to bounce back and forth, thus increasing the intensity of the light. The partially reflective end allows a portion of the reflected light to be emitted.

Section 3-6 Troubleshooting

30. (a) All voltages are correct.
(b) V_3 should be 12 V. Zener is open.
(c) V_1 should be 120 V. Fuse is open.
(d) Capacitor C_1 is open.
(e) R is open or D_5 is shorted.

31. (a) With D_5 open, $V_{\text{OUT}} \approx 30 \text{ V}$.
(b) With R open, $V_{\text{OUT}} = 0 \text{ V}$.
(c) With C leaky, V_{OUT} has excessive **120 Hz ripple limited to 12 V**.
(d) With C open, V_{OUT} is **full wave rectified voltage limited to 12 V**.
(e) With D_3 open, V_{OUT} has **60 Hz ripple limited to 12 V**.
(f) With D_2 open, V_{OUT} has **60 Hz ripple limited to 12 V**.
(g) With T open, $V_{\text{OUT}} = 0 \text{ V}$.
(h) With F open, $V_{\text{OUT}} = 0 \text{ V}$.

Application Activity Problems

32. (a) Faulty regulator

33. Incorrect transformer secondary voltage

34. LED open, limiting resistor open, faulty regulator, faulty bridge rectifier

35. $I_L = \frac{12 \text{ V}}{1 \text{ k}\Omega} = 12 \text{ mA}; V_{\text{reg}} = 16 \text{ V} - 12 \text{ V} = 4 \text{ V}$

$$P_{\text{reg}} = (4 \text{ V})(12 \text{ mA}) = 48 \text{ mW}$$

Datasheet Problems

- 36.** From the datasheet of textbook Figure 3-7:
- @ 25°C: $P_{D(\max)} = \mathbf{1.0 \text{ W}}$ for a 1N4738A
 - For a 1N4751A:

$$@ 70^\circ\text{C}; P_{D(\max)} = 1.0 \text{ W} - (6.67 \text{ mW}/^\circ\text{C})(20^\circ\text{C}) = 1.0 \text{ W} - 133 \text{ mW} = \mathbf{867 \text{ mW}}$$

$$@ 100^\circ\text{C}; P_{D(\max)} = 1.0 \text{ W} - (6.67 \text{ mW}/^\circ\text{C})(50^\circ\text{C}) = 1.0 \text{ W} - 333 \text{ mW} = \mathbf{667 \text{ mW}}$$
 - $I_{ZK} = \mathbf{0.5 \text{ mA}}$ for a 1N4738A
 - @ 25°C: $I_{ZM} = 1 \text{ W}/27 \text{ V} = \mathbf{37.0 \text{ mA}}$ for a 1N4750A
 - $\Delta Z_Z = 700 \Omega - 7.0 \Omega = \mathbf{693 \Omega}$ for a 1N4740A
- 37.** From the datasheet of textbook Figure 3-24:
- $I_{F(\max)} = \mathbf{200 \text{ mA}}$
 - $C_{\max} = 11 \text{ pF}$
 - $C_{20} = \frac{C_2}{CR} = \frac{100 \text{ pF}}{6.5} = 15.4 \text{ pF}$; range is 100 pF – 15.4 pF for an 836A.
- 38.** From the datasheet of textbook 3-34:
- 9 V cannot be applied in reverse across a TSMF1000 because $V_{R(\max)} = 5 \text{ V}$.
 - When 5.1 V is used to forward-bias the TSMF1000 for $I_F = 20 \text{ mA}$, $V_F \approx 1.3 \text{ V}$
 - $R = \frac{5.1 \text{ V} - 1.3 \text{ V}}{20 \text{ mA}} = \frac{3.8 \text{ V}}{20 \text{ mA}} = \mathbf{190 \Omega}$
 - At 25°C maximum power dissipation is 190 mW.
If $V_F = 1.5 \text{ V}$ and $I_F = 50 \text{ mA}$, $P_D = 75 \text{ mW}$. The power rating is **not exceeded**.
 - For $I_F = 40 \text{ mA}$, radiant intensity is approximately **0.9 mW/sr**.
 - For $I_F = 100 \text{ mA}$ and $\theta = 20^\circ$, radiant intensity is 40% of maximum or $(0.4)(25 \text{ mW/sr}) = \mathbf{10 \text{ mW/sr}}$
- 39.** From the datasheet of textbook Figure 3-47:
- With no incident light and a 10 kΩ series resistor, the typical voltage across the resistor is approximately $V_R = (1 \text{ nA})(1 \text{ k}\Omega) = \mathbf{1 \mu\text{V}}$.
 - Reverse current is greatest at about **940 nm**.
 - Sensitivity is maximum for $\lambda \approx \mathbf{830 \text{ nm}}$.

Chapter 3

Advanced Problems

40. See Figure 3-5.

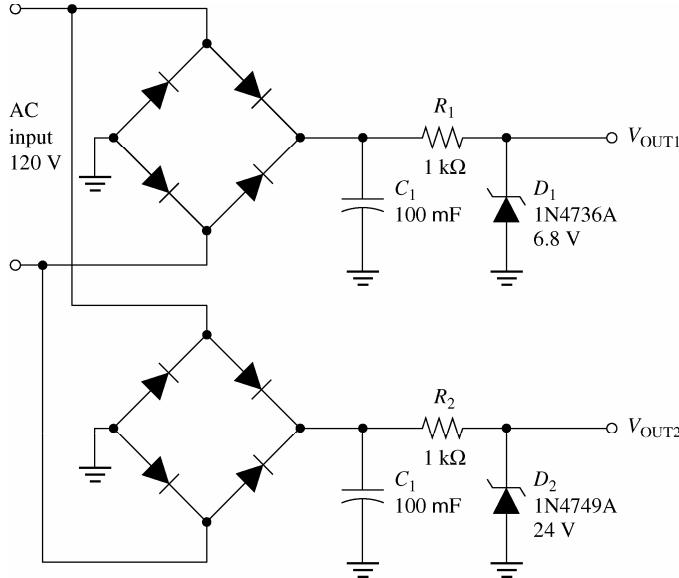


Figure 3-5

41. $V_{\text{OUT(1)}} \approx 6.8 \text{ V}$, $V_{\text{OUT(2)}} \approx 24 \text{ V}$

42. For a $10 \text{ k}\Omega$ load on each output:

$$I_{\text{OUT(1)}} = \frac{V_{\text{OUT1}}}{R_1} \approx \frac{6.8 \text{ V}}{10 \text{ k}\Omega} = 0.68 \text{ mA}$$

$$I_{\text{OUT(2)}} = \frac{V_{\text{OUT2}}}{R_2} \approx \frac{24 \text{ V}}{10 \text{ k}\Omega} = 2.4 \text{ mA}$$

$$V_{R1} \approx 120 \text{ V} - 6.8 \text{ V} = 113.2 \text{ V}$$

$$I_{Z1} = \frac{113.2 \text{ V}}{1 \text{ k}\Omega} - 0.68 \text{ mA} = 112.5 \text{ mA}$$

$$V_{R2} \approx 120 \text{ V} - 24 \text{ V} = 96 \text{ V}$$

$$I_{Z2} = \frac{96 \text{ V}}{1 \text{ k}\Omega} - 2.4 \text{ mA} = 93.6 \text{ mA}$$

$$I_T = 0.68 \text{ mA} + 2.4 \text{ mA} + 112.5 \text{ mA} + 93.6 \text{ mA} = 209.2 \text{ mA}$$

The fuse rating should be 250 mA or **1/4 A**.

43. See Figure 3-6.

Use a 1N4738A zener.

$$I_T = 35 \text{ mA} + 31 \text{ mA} = 66 \text{ mA}$$

$$R = \frac{24 \text{ V} - 8.2 \text{ V}}{66 \text{ mA}} = 239 \Omega$$

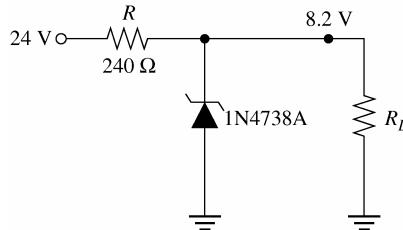


Figure 3-6

44. $C_{\max} = \frac{1}{4\pi^2 L f_{\min}^2} = \frac{1}{4\pi^2 (2 \text{ mH})(350 \text{ kHz})^2} = 103.4 \text{ pF}$

$$C_{\min} = \frac{1}{4\pi^2 L f_{\max}^2} = \frac{1}{4\pi^2 (2 \text{ mH})(850 \text{ kHz})^2} = 17.5 \text{ pF}$$

To achieve this capacitance range, use an 826A varactor and change V_2 to 30 V.

45. See Figure 3-7. From datasheet, $V_F = 2.1 \text{ V}$ for red LED.

$$R = \frac{V_D}{I} = \frac{12 \text{ V} - 2.1 \text{ V}}{20 \text{ mA}} = 495 \Omega$$

Use standard value of 510Ω .

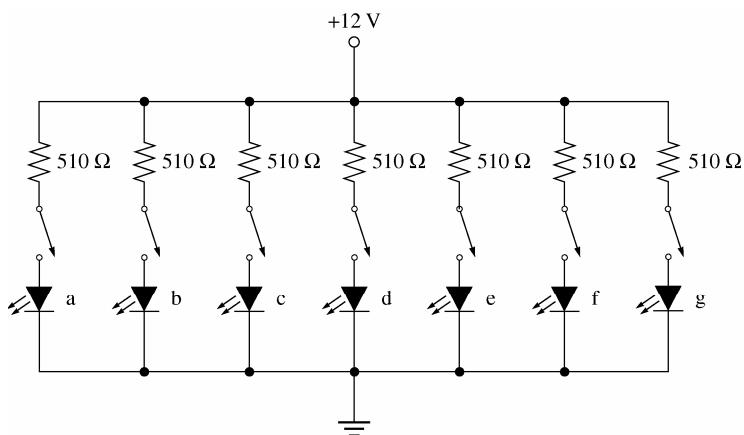


Figure 3-7

46. See Figure 3-8.

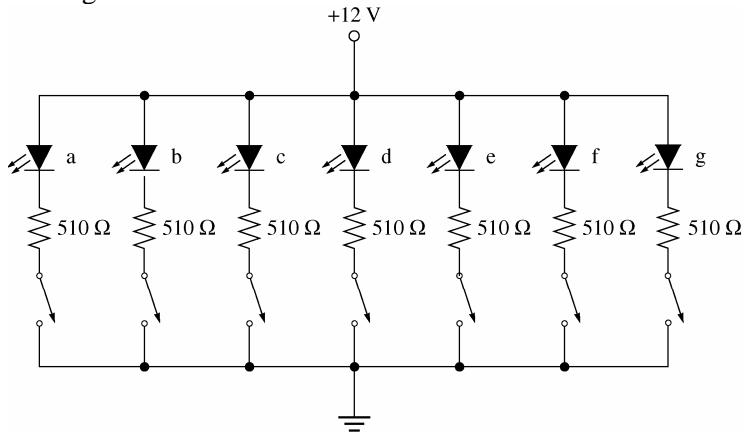


Figure 3-8

Chapter 3

Multisim Troubleshooting Problems

The solutions showing instrument connections for Problems 47 through 50 are available from the Instructor Resource Center. See Chapter 1 for instructions. The faults in the circuit files may be accessed using the password *book* (all lowercase).

- 47.** Zener diode open
- 48.** Capacitor open
- 49.** Zener diode shorted
- 50.** Resistor open

Chapter 4

Bipolar Junction Transistors

Section 4-1 BJT Structure

1. Majority carriers in the base region of an *npn* transistor are **holes**.
2. Because of the narrow base region, the minority carriers invading the base region find a limited number of partners for recombination and, therefore, move across the junction into the collector region rather than out of the base lead.

Section 4-2 Basic BJT Operation

3. The base is narrow and lightly doped so that a small recombination (base) current is generated compared to the collector current.
4. $I_B = 0.02I_E = 0.02(30 \text{ mA}) = 0.6 \text{ mA}$
 $I_C = I_E - I_B = 30 \text{ mA} - 0.6 \text{ mA} = \mathbf{29.4 \text{ mA}}$
5. The base must be negative with respect to the collector and positive with respect to the emitter.
6. $I_C = I_E - I_B = 5.34 \text{ mA} - 475 \mu\text{A} = \mathbf{4.87 \text{ mA}}$

Section 4-3 BJT Characteristics and Parameters

7. $\alpha_{DC} = \frac{I_C}{I_E} = \frac{8.23 \text{ mA}}{8.69 \text{ mA}} = \mathbf{0.947}$
8. $\beta_{DC} = \frac{I_C}{I_B} = \frac{25 \text{ mA}}{200 \mu\text{A}} = \mathbf{125}$
9. $I_B = I_E - I_C = 20.5 \text{ mA} - 20.3 \text{ mA} = 0.2 \text{ mA} = 200 \mu\text{A}$
 $\beta_{DC} = \frac{I_C}{I_B} = \frac{20.3 \text{ mA}}{200 \mu\text{A}} = \mathbf{101.5}$
10. $I_E = I_C + I_B = 5.35 \text{ mA} + 50 \mu\text{A} = 5.40 \text{ mA}$
 $\alpha_{DC} = \frac{I_C}{I_E} = \frac{5.35 \text{ mA}}{5.40 \text{ mA}} = \mathbf{0.99}$
11. $I_C = \alpha_{DC}I_E = 0.96(9.35 \text{ mA}) = \mathbf{8.98 \text{ mA}}$

Chapter 4

12. $I_C = \frac{V_{R_C}}{R_C} = \frac{5 \text{ V}}{1.0 \text{ k}\Omega} = 5 \text{ mA}$

$$\beta_{DC} = \frac{I_C}{I_B} = \frac{5 \text{ mA}}{50 \mu\text{A}} = 100$$

13. $\alpha_{DC} = \frac{\beta_{DC}}{\beta_{DC} + 1} = \frac{100}{101} = 0.99$

14. $I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{3 \text{ V} - 0.7 \text{ V}}{100 \text{ k}\Omega} = 23 \mu\text{A}$

$$I_C = \beta_{DC} I_B = 200(23 \mu\text{A}) = 4.6 \text{ mA}$$

$$I_E = I_C + I_B = 4.6 \text{ mA} + 23 \mu\text{A} = 4.62 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 10 \text{ V} - (4.6 \text{ mA})(1.0 \text{ k}\Omega) = 5.4 \text{ V}$$

15. I_C does not change.

For $V_{CC} = 10 \text{ V}$:

$$V_{CE} = V_{CC} - I_C R_C = 10 \text{ V} - (4.6 \text{ mA})(1.0 \text{ k}\Omega) = 5.4 \text{ V}$$

For $V_{CC} = 15 \text{ V}$:

$$V_{CE} = 15 \text{ V} - (4.6 \text{ mA})(1.0 \text{ k}\Omega) = 10.7 \text{ V}$$

$$\Delta V_{CE} = 10.7 \text{ V} - 5.4 \text{ V} = 5.3 \text{ V} \text{ increase}$$

16. $I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{4 \text{ V} - 0.7 \text{ V}}{4.7 \text{ k}\Omega} = \frac{3.3 \text{ V}}{4.7 \text{ k}\Omega} = 702 \mu\text{A}$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{24 \text{ V} - 8 \text{ V}}{470 \Omega} = 34 \text{ mA}$$

$$I_E = I_C + I_B = 34 \text{ mA} + 702 \mu\text{A} = 34.7 \text{ mA}$$

$$\beta_{DC} = \frac{I_C}{I_B} = \frac{34 \text{ mA}}{702 \mu\text{A}} = 48.4$$

17. (a) $V_{BE} = 0.7 \text{ V}$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{4.3 \text{ V}}{3.9 \text{ k}\Omega} = 1.1 \text{ mA}$$

$$I_C = \beta_{DC} I_B = 50(1.1 \text{ mA}) = 55 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 15 \text{ V} - (55 \text{ mA})(180 \Omega) = 5.10 \text{ V}$$

$$V_{CB} = V_{CE} - V_{BE} = 5.10 \text{ V} - 0.7 \text{ V} = 4.40 \text{ V}$$

(b) $V_{BE} = -0.7 \text{ V}$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{-3 \text{ V} - (-0.7 \text{ V})}{27 \text{ k}\Omega} = \frac{-2.3 \text{ V}}{27 \text{ k}\Omega} = -85.2 \mu\text{A}$$

$$I_C = \beta_{DC} I_B = 125(-85.2 \mu\text{A}) = -10.7 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = -8 \text{ V} - (-10.7 \text{ mA})(390 \Omega) = -3.83 \text{ V}$$

$$V_{CB} = V_{CE} - V_{BE} = -3.83 \text{ V} - (-0.7 \text{ V}) = -3.13 \text{ V}$$

18. (a) $I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{15\text{ V}}{180\Omega} = 83.3\text{ mA}$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5\text{ V} - 0.7\text{ V}}{3.9\text{ k}\Omega} = 1.1\text{ mA}$$

$$I_C = \beta_{DC} I_B = 50(1.1\text{ mA}) = 55\text{ mA}$$

$$I_C < I_{C(sat)}$$

Therefore, the transistor is **not saturated**.

(b) $I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{8\text{ V}}{390\Omega} = 20.5\text{ mA}$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{3\text{ V} - 0.7\text{ V}}{27\text{ k}\Omega} = 85.2\text{ }\mu\text{A}$$

$$I_C = \beta_{DC} I_B = 125(85.2\text{ }\mu\text{A}) = 10.7\text{ mA}$$

$$I_C < I_{C(sat)}$$

Therefore, the transistor is **not saturated**.

19. $V_B = 2\text{ V}$

$$V_E = V_B - V_{BE} = 2\text{ V} - 0.7\text{ V} = 1.3\text{ V}$$

$$I_E = \frac{V_E}{R_E} = \frac{1.3\text{ V}}{1.0\text{ k}\Omega} = 1.3\text{ mA}$$

$$I_C = \alpha_{DC} I_E = (0.98)(1.3\text{ mA}) = 1.27\text{ mA}$$

$$\beta_{DC} = \frac{\alpha_{DC}}{1 - \alpha_{DC}} = \frac{0.98}{1 - 0.98} = 49$$

$$I_B = I_E - I_C = 1.3\text{ mA} - 1.27\text{ mA} = 30\text{ }\mu\text{A}$$

20. (a) $V_B = V_{BB} = 10\text{ V}$

$$V_C = V_{CC} = 20\text{ V}$$

$$V_E = V_B - V_{BE} = 10\text{ V} - 0.7\text{ V} = 9.3\text{ V}$$

$$V_{CE} = V_C - V_E = 20\text{ V} - 9.3\text{ V} = 10.7\text{ V}$$

$$V_{BE} = 0.7\text{ V}$$

$$V_{CB} = V_C - V_B = 20\text{ V} - 10\text{ V} = 10\text{ V}$$

(b) $V_B = V_{BB} = -4\text{ V}$

$$V_C = V_{CC} = -12\text{ V}$$

$$V_E = V_B - V_{BE} = -4\text{ V} - (-0.7\text{ V}) = -3.3\text{ V}$$

$$V_{CE} = V_C - V_E = -12\text{ V} - (-3.3\text{ V}) = -8.7\text{ V}$$

$$V_{BE} = -0.7\text{ V}$$

$$V_{CB} = V_C - V_B = -12\text{ V} - (-4\text{ V}) = -8\text{ V}$$

Chapter 4

21. For $\beta_{DC} = 100$:

$$I_E = \frac{V_B - V_{BE}}{R_E} = \frac{10 \text{ V} - 0.7 \text{ V}}{10 \text{ k}\Omega} = 930 \mu\text{A}$$

$$\alpha_{DC} = \frac{\beta_{DC}}{1 + \beta_{DC}} = \frac{100}{101} = 0.990$$

$$I_C = \alpha_{DC} I_E = (0.990)(930 \mu\text{A}) = 921 \mu\text{A}$$

For $\beta_{DC} = 150$:

$$I_E = 930 \mu\text{A}$$

$$\alpha_{DC} = \frac{\beta_{DC}}{1 + \beta_{DC}} = \frac{150}{151} = 0.993$$

$$I_C = \alpha_{DC} I_E = (0.993)(930 \mu\text{A}) = 924 \mu\text{A}$$

$$\Delta I_C = 924 \mu\text{A} - 921 \mu\text{A} = 3 \mu\text{A}$$

22. $P_{D(max)} = V_{CE} I_C$

$$V_{CE(max)} = \frac{P_{D(max)}}{I_C} = \frac{1.2 \text{ W}}{50 \text{ mA}} = 24 \text{ V}$$

23. $P_{D(max)} = 0.5 \text{ W} - (75^\circ\text{C})(1 \text{ mW}/^\circ\text{C}) = 0.5 \text{ W} - 75 \text{ mW} = 425 \text{ mW}$

Section 4-4 The BJT as an Amplifier

24. $V_{out} = A_v V_{in} = 50(100 \text{ mV}) = 5 \text{ V}$

25. $A_v = \frac{V_{out}}{V_{in}} = \frac{10 \text{ V}}{300 \text{ mV}} = 33.3$

26. $A_v = \frac{R_C}{r'_e} = \frac{560 \Omega}{10 \Omega} = 56$

$$V_c = V_{out} = A_v V_{in} = 56(50 \text{ mV}) = 2.8 \text{ V}$$

27. $I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{2.5 \text{ V} - 0.7 \text{ V}}{100 \text{ k}\Omega} = 18 \mu\text{A}$

$$I_C = \beta_{DC} I_B = 250(18 \mu\text{A}) = 4.5 \text{ mA}$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{9 \text{ V} - 4 \text{ V}}{4.5 \text{ mA}} = 1.1 \text{ k}\Omega$$

28. (a) DC current gain = $\beta_{DC} = 50$

- (b) DC current gain = $\beta_{DC} = 125$

Section 4-5 The BJT as a Switch

29. $I_{C(\text{sat})} = \frac{V_{CC}}{R_C} = \frac{5 \text{ V}}{10 \text{ k}\Omega} = 500 \mu\text{A}$

$$I_{B(\text{min})} = \frac{I_{C(\text{sat})}}{\beta_{DC}} = \frac{500 \mu\text{A}}{150} = 3.33 \mu\text{A}$$

$$I_{B(\text{min})} = \frac{V_{IN(\text{min})} - 0.7 \text{ V}}{R_B}$$

$$R_B I_{B(\text{min})} = V_{IN(\text{min})} - 0.7 \text{ V}$$

$$V_{IN(\text{min})} = R_B I_{B(\text{min})} + 0.7 \text{ V} = (3.33 \mu\text{A})(1.0 \text{ M}\Omega) + 0.7 \text{ V} = 4.03 \text{ V}$$

30. $I_{C(\text{sat})} = \frac{15 \text{ V}}{1.2 \text{ k}\Omega} = 12.5 \text{ mA}$

$$I_{B(\text{min})} = \frac{I_{C(\text{sat})}}{\beta_{DC}} = \frac{12.5 \text{ mA}}{50} = 250 \mu\text{A}$$

$$R_B(\text{min}) = \frac{V_{IN} - 0.7 \text{ V}}{I_{B(\text{min})}} = \frac{4.3 \text{ V}}{250 \mu\text{A}} = 17.2 \text{ k}\Omega$$

$$V_{IN(\text{cutoff})} = 0 \text{ V}$$

Section 4-6 The Phototransistor

31. $I_C = \beta_{DC} I_\lambda = (200)(100 \mu\text{A}) = 20 \text{ mA}$

32. $I_\lambda = (50 \text{ lm/m}^2)(1 \mu\text{A/lm/m}^2) = 50 \mu\text{A}$
 $I_E = \beta_{DC} I_\lambda = (100)(50 \mu\text{A}) = 5 \text{ mA}$

33. $I_{out} = (0.30)(100 \text{ mA}) = 30 \text{ mA}$

34. $\frac{I_{OUT}}{I_{IN}} = 0.6$

$$I_{IN} = \frac{I_{OUT}}{0.6} = \frac{10 \text{ mA}}{0.6} = 16.7 \text{ mA}$$

Section 4-7 Transistor Categories and Packaging

35. See Figure 4-1.

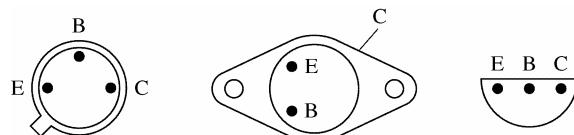


Figure 4-1

36. (a) Small-signal
 (b) Power
 (c) Power
 (d) Small-signal
 (e) RF

Chapter 4

Section 4-8 Troubleshooting

37. With the positive probe on the emitter and the negative probe on the base, the ohmmeter indicates an **open**, since this reverse-biases the base-emitter junction. With the positive probe on the base and the negative probe on the emitter, the ohmmeter indicates a **very low resistance**, since this forward-biases the base-collector junction.
38. (a) Transistor's collector junction or terminal is open.
(b) Collector resistor is open.
(c) Operating properly.
(d) Transistor's base junction or terminal open (no base or collector current).

39. (a) $I_B = \frac{5\text{ V} - 0.7\text{ V}}{68\text{ k}\Omega} = 63.2\text{ }\mu\text{A}$

$$I_C = \frac{9\text{ V} - 3.2\text{ V}}{3.3\text{ k}\Omega} = 1.76\text{ mA}$$

$$\beta_{DC} = \frac{I_C}{I_B} = \frac{1.76\text{ mA}}{63.2\text{ }\mu\text{A}} = 27.8$$

(b) $I_B = \frac{4.5\text{ V} - 0.7\text{ V}}{27\text{ k}\Omega} = 141\text{ }\mu\text{A}$

$$I_C = \frac{24\text{ V} - 16.8\text{ V}}{470\text{ }\Omega} = 15.3\text{ mA}$$

$$\beta_{DC} = \frac{I_C}{I_B} = \frac{15.3\text{ mA}}{141\text{ }\mu\text{A}} = 109$$

Application Activity Problems

40. Q_1 OFF, Q_2 ON
 $I_{R2} = 0, P_{R2} = 0\text{ mW}$
 $I_{R1} = 0, P_{R2} = 0\text{ mW}$
 $I_{R3} = I_{R4} = \frac{12\text{ V} - 0.7\text{ V}}{1.2\text{ k}\Omega + 36\text{ k}\Omega} = 304\text{ }\mu\text{A}$
 $P_{R3} = (304\text{ }\mu\text{A})^2(1.2\text{ k}\Omega) = 110\text{ }\mu\text{W}$
 $P_{R4} = (304\text{ }\mu\text{A})^2(36\text{ k}\Omega) = 3.3\text{ mW}$
 $I_{R5} = \frac{12\text{ V} - 0.176\text{ V}}{620\text{ }\Omega} = 19\text{ mA}$
 $P_{R5} = (19\text{ mA})^2(620\text{ }\Omega) = 224\text{ mW}$

Q_1 ON, Q_2 OFF

$$I_{R2} = \frac{12 \text{ V} - 0.7 \text{ V}}{75 \text{ k}\Omega} = 151 \text{ }\mu\text{A}$$

$$P_{R2} = (151 \text{ }\mu\text{A})^2(75 \text{ k}\Omega) = 1.7 \text{ mW}$$

$$P_{R1} = \frac{(0.7 \text{ V})^2}{1.0 \text{ M}\Omega} = 0.49 \text{ }\mu\text{W}$$

$$I_{R4} \cong \frac{12 \text{ V} - 0.1 \text{ V}}{1.2 \text{ k}\Omega} = 9.9 \text{ mA}$$

$$P_{R4} = (9.9 \text{ mA})^2(1.2 \text{ k}\Omega) = 118 \text{ mW}$$

$$I_{R3} \cong 0, P_{R3} = 0 \text{ mW}$$

$$I_{R5} = 0, P_{R5} = 0 \text{ mW}$$

41. $I_{C(\max)} = 200 \text{ mA}$

$$R_{L(\min)} = \frac{V_{CC}}{I_{C(\max)}} = \frac{12 \text{ V}}{200 \text{ mA}} = 60 \Omega$$

42. See Figure 4-2.

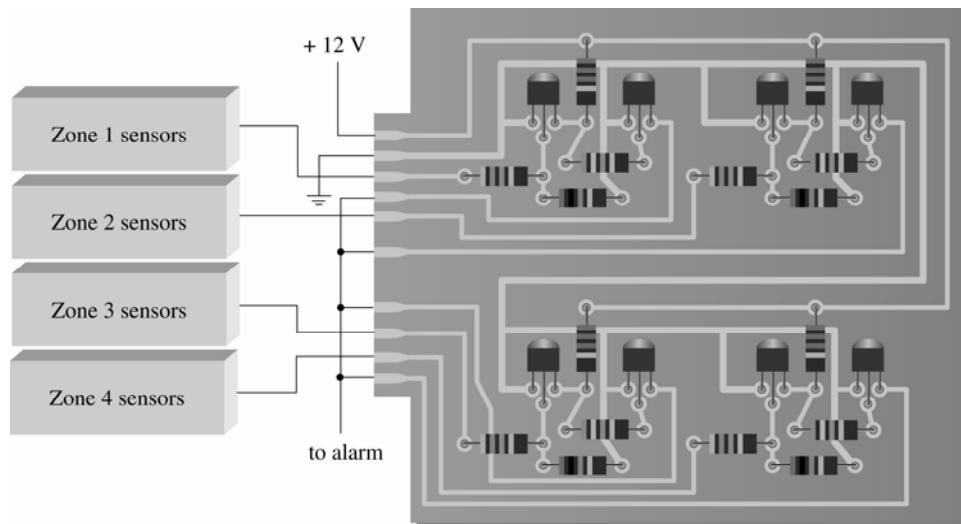


Figure 4-2

Datasheet Problems

43. From the datasheet of textbook Figure 4-20:

(a) For a 2N3904, $V_{CEO(\max)} = 40 \text{ V}$

(b) For a 2N3904, $I_{C(\max)} = 200 \text{ mA}$

(c) For a 2N3904 @ 25°C , $P_{D(\max)} = 625 \text{ mW}$

$$(d) \text{ For a 2N3904 @ } T_C = 50^\circ\text{C}, P_{D(\max)} = 625 \text{ mW} - 5 \text{ mW/}^\circ\text{C}(25^\circ\text{C}) \\ = 625 \text{ mW} - 125 \text{ mW} = 500 \text{ mW}$$

(e) For a 2N3904 with $I_C = 1 \text{ mA}$, $h_{FE(\min)} = 70$

Chapter 4

44. For an MMBT3904 with $T_A = 65^\circ\text{C}$:

$$\begin{aligned}P_{D(\max)} &= 350 \text{ mW} - (65^\circ\text{C} - 25^\circ\text{C})(2.8 \text{ mW}/^\circ\text{C}) \\&= 350 \text{ mW} - 40^\circ\text{C}(2.8 \text{ mW}/^\circ\text{C}) = 350 \text{ mW} - 112 \text{ mW} = \mathbf{238 \text{ mW}}\end{aligned}$$

45. For a PZT3904 with $T_C = 45^\circ\text{C}$:

$$\begin{aligned}P_{D(\max)} &= 1 \text{ W} - (45^\circ\text{C} - 25^\circ\text{C})(8 \text{ mW}/^\circ\text{C}) \\&= 1 \text{ W} - 20^\circ\text{C}(8 \text{ mW}/^\circ\text{C}) = 1 \text{ W} - 160 \text{ mW} = \mathbf{840 \text{ mW}}\end{aligned}$$

46. For the circuits of textbook Figure 4-66:

(a) $I_B = \frac{3 \text{ V} - 0.7 \text{ V}}{330 \Omega} = \frac{2.3 \text{ V}}{330 \Omega} = 6.97 \text{ mA}$

Let $h_{FE} = 30$

$$I_C = 30(6.97 \text{ mA}) = 209 \text{ mA}$$

$$I_{C(\text{sat})} = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} = \frac{30 \text{ V} - 0.2 \text{ V}}{270 \Omega} = 110 \text{ mA}$$

The transistor is saturated since I_C cannot exceed 110 mA.

$$P_D = (0.2 \text{ V})(110 \text{ mA}) = 22 \text{ mW}$$

$$\text{At } 50^\circ\text{C}, P_{D(\max)} = 350 \text{ mW} - (50^\circ\text{C} - 25^\circ\text{C})(2.8 \text{ mW}/^\circ\text{C}) = 280 \text{ mW}$$

No parameter is exceeded.

(b) $V_{CEO} = 45 \text{ V}$ which **exceeds** $V_{CEO(\max)}$.

47. For the circuits of textbook Figure 4-67:

(a) $I_B = \frac{5 \text{ V} - 0.7 \text{ V}}{10 \text{ k}\Omega} = \frac{4.3 \text{ V}}{10 \text{ k}\Omega} = 4.30 \mu\text{A}$

$$h_{FE(\max)} = 300$$

$$I_C = 300(4.30 \mu\text{A}) = 129 \text{ mA}$$

$$I_{C(\text{sat})} = \frac{9 \text{ V}}{1.0 \text{ k}\Omega} = 9 \text{ mA}$$

The transistor is saturated.

(b) $I_B = \frac{3 \text{ V} - 0.7 \text{ V}}{100 \text{ k}\Omega} = \frac{2.3 \text{ V}}{100 \text{ k}\Omega} = 23 \mu\text{A}$

$$h_{FE(\max)} = 300$$

$$I_C = 300(23 \mu\text{A}) = 6.90 \text{ mA}$$

$$I_{C(\text{sat})} = \frac{12 \text{ V}}{560 \Omega} = 21.4 \text{ mA}$$

The transistor is not saturated.

48. $I_{B(\min)} = \frac{I_C}{h_{FE(\max)}} = \frac{10 \text{ mA}}{150} = \mathbf{66.7 \mu\text{A}}$

$$I_{B(\max)} = \frac{I_C}{h_{FE(\min)}} = \frac{10 \text{ mA}}{50} = \mathbf{200 \mu\text{A}}$$

- 49.** For the circuits of textbook Figure 4-69:

$$(a) I_B = \frac{8\text{ V} - 0.7\text{ V}}{68\text{ k}\Omega} = \frac{7.3\text{ V}}{68\text{ k}\Omega} = 107\text{ }\mu\text{A}$$

$$h_{FE} = 150$$

$$I_C = 150(107\text{ }\mu\text{A}) = 16.1\text{ mA}$$

$$V_C = 15\text{ V} - (16.1\text{ mA})(680\text{ }\Omega) = 15\text{ V} - 10.95\text{ V} = 4.05\text{ V}$$

$$V_{CE} = 4.05\text{ V} - 0.7\text{ V} = 3.35\text{ V}$$

$$P_D = (3.35\text{ V})(16.1\text{ mA}) = 53.9\text{ mW}$$

$$\text{At } 40^\circ\text{C}, P_{D(\max)} = 360\text{ mW} - (40^\circ\text{C} - 25^\circ\text{C})(2.06\text{ mW}/^\circ\text{C}) = 329\text{ mW}$$

No parameters are exceeded.

$$(b) I_B = \frac{5\text{ V} - 0.7\text{ V}}{4.7\text{ k}\Omega} = \frac{4.3\text{ V}}{4.7\text{ k}\Omega} = 915\text{ }\mu\text{A}$$

$$h_{FE} = 300$$

$$I_C = 300(915\text{ }\mu\text{A}) = 274\text{ mA}$$

$$I_{C(\text{sat})} \cong \frac{35\text{ V} - 0.3\text{ V}}{470\text{ }\Omega} = 73.8\text{ mA}$$

The transistor is in hard saturation. Assuming $V_{CE(\text{sat})} = 0.3\text{ V}$,

$$P_D = (0.3\text{ V})(73.8\text{ mA}) = 22.1\text{ mW}$$

No parameters are exceeded.

Advanced Problems

$$50. \quad \beta_{DC} = \frac{\alpha_{DC}}{1 - \alpha_{DC}}$$

$$\beta_{DC} - \beta_{DC}\alpha_{DC} = \alpha_{DC}$$

$$\beta_{DC} = \alpha_{DC}(1 + \beta_{DC})$$

$$\alpha_{DC} = \frac{\beta_{DC}}{(1 + \beta_{DC})}$$

$$51. \quad I_C = 150(500\text{ }\mu\text{A}) = 75\text{ mA}$$

$$V_{CE} = 15\text{ V} - (180\text{ }\Omega)(75\text{ mA}) = 1.5\text{ V}$$

Since $V_{CE(\text{sat})} = 0.3\text{ V}$ @ $I_C = 50\text{ mA}$, the transistor comes out of saturation.

52. From the datasheet, $\beta_{DC(\min)} = 15$ (for $I_C = 100\text{ mA}$)

$$I_{B(\max)} = \frac{150\text{ mA}}{15} = 10\text{ mA}$$

$$R_{B(\min)} = \frac{3\text{ V} - 0.7\text{ V}}{10\text{ mA}} = \frac{2.3\text{ V}}{10\text{ mA}} = 230\text{ }\Omega$$

Use the standard value of $240\text{ }\Omega$ for R_B .

To avoid saturation, the load resistance cannot exceed about

$$\frac{9\text{ V} - 1\text{ V}}{150\text{ mA}} = 53.3\text{ }\Omega$$

See Figure 4-3.

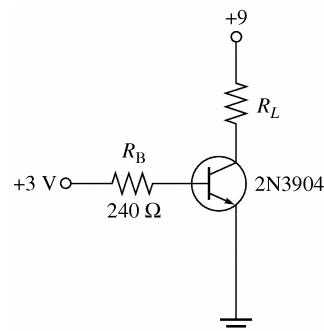


Figure 4-3

Chapter 4

- 53.** Since $I_B = 10 \text{ mA}$ for $I_C = 150 \text{ mA}$,

$$R_{B(\min)} = \frac{9 \text{ V} - 0.7 \text{ V}}{10 \text{ mA}} = \frac{8.3 \text{ V}}{10 \text{ mA}} = 830 \Omega$$

Use 910Ω . The load cannot exceed 53.3Ω .

See Figure 4-4.

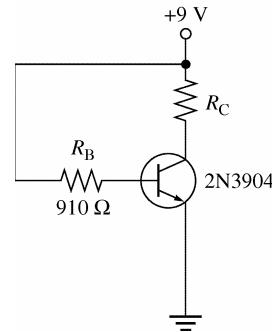


Figure 4-4

- 54.** $R_{C(\min)} = A_v r'_e = 50(8 \Omega) = 400 \Omega$ (Use 430Ω)

$$I_C = \frac{12 \text{ V} - 5 \text{ V}}{430 \Omega} = 16.3 \text{ mA}$$

Assuming $h_{FE} = 100$,

$$I_B = \frac{16.3 \text{ mA}}{100} = 163 \mu\text{A}$$

$$R_{B(\max)} = \frac{4 \text{ V} - 0.7 \text{ V}}{163 \mu\text{A}} = 20.3 \text{ k}\Omega \text{ (Use } 18 \text{ k}\Omega)$$

See Figure 4-5.

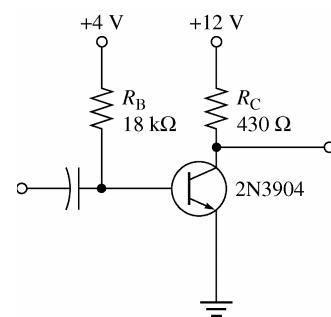


Figure 4-5

Multisim Troubleshooting Problems

The solutions showing instrument connections for Problems 55 through 62 are available from the Instructor Resource Center. See Chapter 1 for instructions. The faults in the circuit files may be accessed using the password *book* (all lowercase).

55. R_B shorted

56. R_C open

57. Collector-emitter shorted

58. Collector-emitter open

59. R_E leaky

60. Collector-emitter shorted

61. R_B open

62. R_C open

Chapter 5

Transistor Bias Circuits

Section 5-1 The DC Operating Point

1. The transistor is biased too close to **saturation**.

$$I_C = \beta_{DC} I_B = 75(150 \mu\text{A}) = 11.3 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 18 \text{ V} - (11.3 \text{ mA})(1.0 \text{ k}\Omega) = 18 \text{ V} - 11.3 \text{ V} = 6.75 \text{ V}$$

Q-point: $V_{CEQ} = 6.75 \text{ V}$, $I_{CQ} = 11.3 \text{ mA}$

$$3. I_{C(sat)} \cong \frac{V_{CC}}{R_C} = \frac{18 \text{ V}}{1.0 \text{ k}\Omega} = 18 \text{ mA}$$

$$4. V_{CE(cutoff)} = 18 \text{ V}$$

5. Horizontal intercept (cutoff):

$$V_{CE} = V_{CC} = 20 \text{ V}$$

Vertical intercept (saturation):

$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{20 \text{ V}}{10 \text{ k}\Omega} = 2 \text{ mA}$$

$$6. I_B = \frac{V_{BB} - 0.7 \text{ V}}{R_B}$$

$$V_{BB} = I_B R_B + 0.7 \text{ V} = (20 \mu\text{A})(1.0 \text{ M}\Omega) + 0.7 \text{ V} = 20.7 \text{ V}$$

$$I_C = \beta_{DC} I_B = 50(20 \mu\text{A}) = 1 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 20 \text{ V} - (1 \text{ mA})(10 \text{ k}\Omega) = 10 \text{ V}$$

7. See Figure 5-1.

$$V_{CE} = V_{CC} - I_C R_C$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{10 \text{ V} - 4 \text{ V}}{5 \text{ mA}} = 1.2 \text{ k}\Omega$$

$$I_B = \frac{I_C}{\beta_{DC}} = \frac{5 \text{ mA}}{100} = 0.05 \text{ mA}$$

$$R_B = \frac{10 \text{ V} - 0.7 \text{ V}}{0.05 \text{ mA}} = 186 \text{ k}\Omega$$

$$P_{D(min)} = V_{CE} I_C = (4 \text{ V})(5 \text{ mA}) = 20 \text{ mW}$$

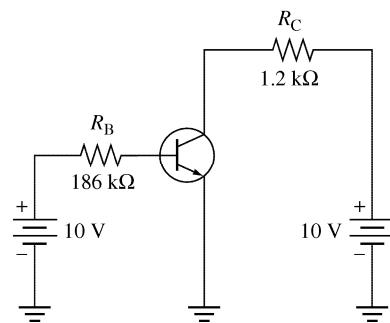


Figure 5-1

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8. $I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{1.5 \text{ V} - 0.7 \text{ V}}{10 \text{ k}\Omega} = 80 \mu\text{A}$

$$I_{C(\text{sat})} = \frac{V_{CC}}{R_C} = \frac{8 \text{ V}}{390 \Omega} = 20.5 \text{ mA}$$

$$I_C = \beta_{DC} I_B = 75(80 \mu\text{A}) = 6 \text{ mA}$$

The transistor is biased in the linear region because
 $0 < I_C < I_{C(\text{sat})}$.

9. (a) $I_{C(\text{sat})} = 50 \text{ mA}$

(b) $V_{CE(\text{cutoff})} = 10 \text{ V}$

(c) $I_B = 250 \mu\text{A}$

$$I_C = 25 \text{ mA}$$

$$V_{CE} = 5 \text{ V}$$

10. (a) $I_C \approx 42 \text{ mA}$

(b) Interpolating between $I_B = 400 \mu\text{A}$ and $I_B = 500 \mu\text{A}$

$$I_B \approx 450 \mu\text{A}$$

(c) $V_{CE} \approx 1.5 \text{ V}$

See Figure 5-2.

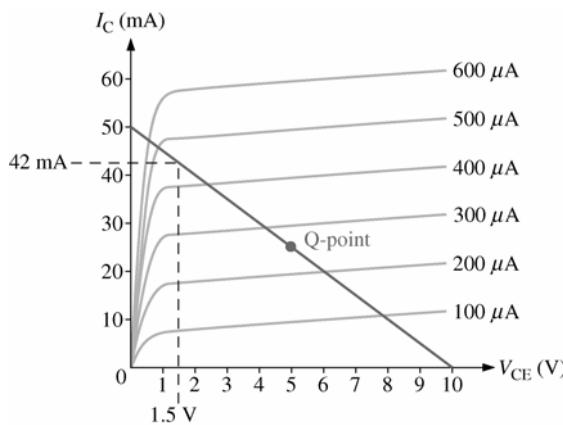


Figure 5-2

Section 5-2 Voltage-Divider Bias

11. $\beta_{DC(\text{min})} R_E = 10 R_2$

$$\beta_{DC(\text{min})} = \frac{10 R_2}{R_E} = \frac{47 \text{ k}\Omega}{680 \Omega} = 69.1$$

12. $I_{C(\text{sat})} = \frac{V_{CC}}{R_C + R_E} = \frac{15 \text{ V}}{2.18 \text{ k}\Omega} = 6.88 \text{ mA}$

$$V_{E(\text{sat})} = I_{C(\text{sat})} R_E = (6.88 \text{ mA})(680 \Omega) = 4.68 \text{ V}$$

$$V_B = V_{E(\text{sat})} + 0.7 \text{ V} = 4.68 \text{ V} + 0.7 \text{ V} = 5.38 \text{ V}$$

$$\left(\frac{R_2 \parallel \beta_{DC} R_E}{R_L + R_2 \parallel \beta_{DC} R_E} \right) 15 \text{ V} = 5.38 \text{ V}$$

$$\begin{aligned}
 (R_2 \parallel \beta_{DC} R_E) (15 \text{ V}) &= (5.38 \text{ V}) (R_1 + R_2 \parallel \beta_{DC} R_E) \\
 (R_2 \parallel \beta_{DC} R_E) (15 \text{ V}) - (R_2 \parallel \beta_{DC} R_E) (5.38 \text{ V}) &= R_1 (5.38 \text{ V}) \\
 (R_2 \parallel \beta_{DC} R_E) (15 \text{ V} - 5.38 \text{ V}) &= (22 \text{ k}\Omega) (5.38 \text{ V}) \\
 R_2 \parallel \beta_{DC} R_E &= \frac{(22 \text{ k}\Omega)(5.38 \text{ V})}{15 \text{ V} - 5.38 \text{ V}} = 12.3 \text{ k}\Omega \\
 \frac{1}{R_2} + \frac{1}{\beta_{DC} R_E} &= \frac{1}{12.3 \text{ k}\Omega} \\
 \frac{1}{R_2} + \frac{1}{102 \text{ k}\Omega} &= \frac{1}{12.3 \text{ k}\Omega} \\
 \frac{1}{R_2} &= 71.5 \mu\text{S} \\
 R_2 &= \mathbf{14 \text{ k}\Omega}
 \end{aligned}$$

13.

$$\begin{aligned}
 V_B &= \left(\frac{R_2}{R_1 + R_2} \right) V_{CC} = \left(\frac{2 \text{ k}\Omega}{24 \text{ k}\Omega} \right) 15 \text{ V} = 1.25 \text{ V} \\
 V_E &= 1.25 \text{ V} - 0.7 \text{ V} = 0.55 \text{ V} \\
 I_E &= \frac{V_E}{R_E} = \frac{0.55 \text{ V}}{680 \Omega} = 809 \mu\text{A} \\
 I_C &\cong \mathbf{809 \mu\text{A}} \\
 V_{CE} &= V_{CC} - I_C R_C - V_E = 15 \text{ V} - (809 \mu\text{A})(1.5 \text{ k}\Omega + 680 \Omega) = \mathbf{13.2 \text{ V}}
 \end{aligned}$$

14.

$$\begin{aligned}
 V_B &= \left(\frac{R_2 \parallel \beta_{DC} R_E}{R_1 + R_2 \parallel \beta_{DC} R_E} \right) V_{CC} = \left(\frac{15 \text{ k}\Omega \parallel (110)(1.0 \text{ k}\Omega)}{47 \text{ k}\Omega + 15 \text{ k}\Omega \parallel (110)(1.0 \text{ k}\Omega)} \right) 9 \text{ V} = \mathbf{1.97 \text{ V}} \\
 V_E &= V_B - 0.7 \text{ V} = 1.97 \text{ V} - 0.7 \text{ V} = \mathbf{1.27 \text{ V}} \\
 I_C &\cong I_E = \frac{V_E}{R_E} = \frac{1.27 \text{ V}}{1.0 \text{ k}\Omega} = 1.27 \text{ mA} \\
 V_C &= V_{CC} - I_C R_C = 9 \text{ V} - (1.27 \text{ mA})(2.2 \text{ k}\Omega) = \mathbf{6.21 \text{ V}}
 \end{aligned}$$

15. See Figure 5-3.

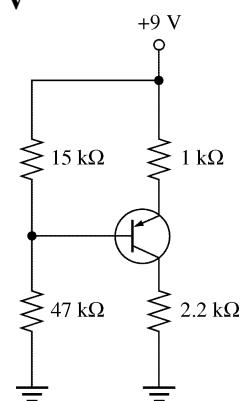


Figure 5-3

16.

- $R_{IN(base)} = \beta_{DC} R_E = 150(560 \Omega) = 84 \text{ k}\Omega$

$$V_B = \left(\frac{5.6 \text{ k}\Omega \parallel 84 \text{ k}\Omega}{33 \text{ k}\Omega + 5.6 \text{ k}\Omega \parallel 84 \text{ k}\Omega} \right) (-12 \text{ V}) = \left(\frac{5.25 \text{ k}\Omega}{38.25 \text{ k}\Omega} \right) (-12 \text{ V}) = \mathbf{-1.65 \text{ V}}$$
- $R_{IN(base)} = 50(560 \Omega) = 28 \text{ k}\Omega$

$$V_B = \left(\frac{5.6 \text{ k}\Omega \parallel 28 \text{ k}\Omega}{33 \text{ k}\Omega + 56 \text{ k}\Omega \parallel 28 \text{ k}\Omega} \right) (-12 \text{ V}) = \left(\frac{4.67 \text{ k}\Omega}{37.7 \text{ k}\Omega} \right) (-12 \text{ V}) = \mathbf{-1.49 \text{ V}}$$

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17. (a) $V_{EQ} = V_B + 0.7 \text{ V} = -1.49 \text{ V} + 0.7 \text{ V} = -0.79 \text{ V}$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{-0.79 \text{ V}}{560 \Omega} = -1.41 \text{ mA}$$

$$V_{CQ} = V_{CC} - I_C R_C = -12 \text{ V} - (-1.41 \text{ mA})(1.8 \text{ k}\Omega) = -9.46 \text{ V}$$

$$V_{CEQ} = V_{CQ} - V_{EQ} = -9.46 \text{ V} - (-0.79 \text{ V}) = -8.67 \text{ V}$$

(b) $P_{D(\min)} = I_{CQ} V_{CEQ} = (-1.41 \text{ mA})(-8.67 \text{ V}) = 12.2 \text{ mW}$

18. $V_B = -1.65 \text{ V}$

$$I_1 = \frac{V_{CC} - V_B}{R_1} = \frac{|-12 \text{ V} - (-1.65 \text{ V})|}{33 \text{ k}\Omega} = 314 \mu\text{A}$$

$$I_2 = \frac{V_B}{R_2} = \frac{|-1.65 \text{ V}|}{5.6 \text{ k}\Omega} = 295 \mu\text{A}$$

$$I_B = I_1 - I_2 = 19 \mu\text{A}$$

Section 5-3 Other Bias Methods

19. Using Equation 5-7:

$$I_E = \frac{-V_{EE} - V_{BE}}{R_E + R_B / \beta_{DC}} = \frac{-(-5 \text{ V}) - 0.7 \text{ V}}{2.2 \text{ k}\Omega + 10 \text{ k}\Omega / 100} = \frac{4.3 \text{ V}}{2.2 \text{ k}\Omega + 0.1 \text{ k}\Omega} = 1.86 \text{ mA}$$

$$I_C \cong I_E = 1.86 \text{ mA}$$

$$I_B = \frac{I_C}{\beta} \cong \frac{1.86 \text{ mA}}{100} = 18.6 \mu\text{A}$$

$$V_B = -I_B R_B = (18.6 \mu\text{A})(10 \text{ k}\Omega) = -0.186 \text{ V}$$

$$V_E = V_B - 0.7 \text{ V} = -0.186 - 0.7 \text{ V} = -0.886 \text{ V}$$

$$V_C = V_{CC} - I_C R_C = 5 \text{ V} - (1.86 \text{ mA})(1.0 \text{ k}\Omega) = 3.14 \text{ V}$$

20. Assume $V_{CE} \cong 0 \text{ V}$ at saturation.

$$V_E = -0.886 \text{ V}$$

$$\text{so } V_{C(\text{sat})} = -0.886$$

$$I_{C(\text{sat})} = \frac{V_{CC} - V_{C(\text{sat})}}{R_C} = \frac{5 \text{ V} - (-0.886 \text{ V})}{1.0 \text{ k}\Omega} = 5.89 \text{ mA}$$

$$R_{E(\min)} = \frac{V_{RE}}{I_{C(\text{sat})}} = \frac{4.11 \text{ V}}{5.89 \text{ mA}} = 698 \Omega$$

21. At 100°C:

$$V_{BE} = 0.7 \text{ V} - (2.5 \text{ mV}/\text{°C})(75 \text{ °C}) = 0.513 \text{ V}$$

$$I_E = \frac{-V_{EE} - V_{BE}}{R_E + R_B / \beta_{DC}} = \frac{-(-5 \text{ V}) - 0.513 \text{ V}}{2.2 \text{ k}\Omega + 10 \text{ k}\Omega / 100} = \frac{4.49 \text{ V}}{2.3 \text{ k}\Omega} = 1.95 \text{ mA}$$

At 25°C:

$$I_E = 1.86 \text{ mA} \text{ (from problem 19)}$$

$$\Delta I_E = 1.95 \text{ mA} - 1.86 \text{ mA} = 0.09 \text{ mA}$$

- 22.** A change in β_{DC} does not affect the circuit when $R_E \gg R_B/\beta_{DC}$.

Since

$$I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B / \beta_{DC}}$$

In the equation, if R_B/β_{DC} is much smaller than R_E , the effect of β_{DC} is negligible.

- 23.** Assume $\beta_{DC} = 100$.

$$I_C \approx I_E = \frac{V_{EE} - V_E}{R_E + R_B / \beta} = \frac{10 \text{ V} - 0.7 \text{ V}}{470 \Omega + 10 \text{ k}\Omega / 100} = 16.3 \text{ mA}$$

$$V_{CE} = V_{EE} - V_{CC} - I_C(R_C + R_E) = 20 \text{ V} - 13.1 \text{ V} = -6.95 \text{ V}$$

- 24.** $V_B = 0.7 \text{ V}$

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + R_B / \beta_{DC}} = \frac{3 \text{ V} - 0.7 \text{ V}}{1.8 \text{ k}\Omega + 33 \text{ k}\Omega / 90} = 1.06 \text{ mA}$$

$$V_C = V_{CC} - I_C R_C = 3 \text{ V} - (1.06 \text{ mA})(1.8 \text{ k}\Omega) = 1.09 \text{ V}$$

- 25.** $I_C = 1.06 \text{ mA}$ from Problem 24.

$$I_C = 1.06 \text{ mA} - (0.25)(1.06 \text{ mA}) = 0.795 \text{ mA}$$

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + R_B / \beta_{DC}}$$

$$R_C = \frac{V_{CC} - V_{BE} - I_C R_B / \beta_{DC}}{I_C} = \frac{3 \text{ V} - 0.7 \text{ V} - (0.795 \text{ mA})(33 \text{ k}\Omega) / 90}{0.795 \text{ mA}} = 2.53 \text{ k}\Omega$$

- 26.** $I_C = 0.795 \text{ mA}$ from Problem 25.

$$V_{CE} = V_{CC} - I_C R_C = 3 \text{ V} - (0.795 \text{ mA})(2.53 \text{ k}\Omega) = 0.989 \text{ V}$$

$$P_{D(\min)} = V_{CE} I_C = (0.989 \text{ V})(0.795 \text{ mA}) = 786 \mu\text{W}$$

- 27.** See Figure 5-4.

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + R_B / \beta_{DC}} = \frac{12 \text{ V} - 0.7 \text{ V}}{1.2 \text{ k}\Omega + 47 \text{ k}\Omega / 200} = 7.87 \text{ mA}$$

$$V_C = V_{CC} - I_C R_C = 12 \text{ V} - (7.87 \text{ mA})(1.2 \text{ k}\Omega) = 2.56 \text{ V}$$

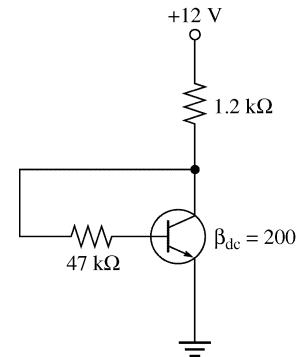


Figure 5-4

- 28.** $V_{BB} = V_{CC}; V_E = 0 \text{ V}$

$$I_B = \frac{V_{CC} - 0.7 \text{ V}}{R_B} = \frac{12 \text{ V} - 0.7 \text{ V}}{22 \text{ k}\Omega} = \frac{11.3 \text{ V}}{22 \text{ k}\Omega} = 514 \mu\text{A}$$

$$I_C = \beta_{DC} I_B = 90(514 \mu\text{A}) = 46.3 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 12 \text{ V} - (46.3 \text{ mA})(100 \Omega) = 7.37 \text{ V}$$

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29. $I_{CQ} = 180(514 \mu\text{A}) = \mathbf{92.5 \text{ mA}}$
 $V_{CEQ} = 12 \text{ V} - (92.5 \text{ mA})(100 \Omega) = \mathbf{2.75 \text{ V}}$
30. I_C changes in the circuit with a common V_{CC} and V_{BB} supply because a change in V_{CC} causes I_B to change which, in turn, changes I_C .
31. $I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{9 \text{ V} - 0.7 \text{ V}}{15 \text{ k}\Omega} = 553 \mu\text{A}$
 $I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{9 \text{ V}}{100 \Omega} = 90 \text{ mA}$
For $\beta_{DC} = 50$:
 $I_C = \beta_{DC}I_B = 50(553 \mu\text{A}) = \mathbf{27.7 \text{ mA}}$
 $V_{CE} = V_{CC} - I_C R_C = 9 \text{ V} - (27.7 \text{ mA})(100 \Omega) = \mathbf{6.23 \text{ V}}$
For $\beta_{DC} = 125$:
 $I_C = \beta_{DC}I_B = 125(553 \mu\text{A}) = \mathbf{69.2 \text{ mA}}$
 $V_{CE} = V_{CC} - I_C R_C = 9 \text{ V} - (69.2 \text{ mA})(100 \Omega) = \mathbf{2.08 \text{ V}}$
Since $I_C < I_{C(sat)}$ for the range of β_{DC} , the circuit remains **biased in the linear region**.

32. $I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{9 \text{ V}}{100 \Omega} = 90 \text{ mA}$
At 0°C:
 $\beta_{DC} = 110 - 110(0.5) = 55$
 $I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{9 \text{ V} - 0.7 \text{ V}}{15 \text{ k}\Omega} = 553 \mu\text{A}$
 $I_C = \beta_{DC}I_B = 55(553 \mu\text{A}) = 30.4 \text{ mA}$
 $V_{CE} = V_{CC} - I_C R_C = 9 \text{ V} - (30.4 \text{ mA})(100 \Omega) = 5.96 \text{ V}$
At 70°C:
 $\beta_{DC} = 110 + 110(0.75) = 193$
 $I_B = 553 \mu\text{A}$
 $I_C = \beta_{DC}I_B = 193(553 \mu\text{A}) = 107 \text{ mA}$
 $I_C > I_{C(sat)}$, therefore the transistor is in saturation at 70°C.
 $\Delta I_C = I_{C(sat)} - I_{C(0^\circ)} = 90 \text{ mA} - 30.4 \text{ mA} = \mathbf{59.6 \text{ mA}}$
 $\Delta V_{CE} \equiv V_{CE(0^\circ)} - V_{CE(sat)} = 5.96 \text{ V} - 0 \text{ V} = \mathbf{5.96 \text{ V}}$

Section 5-4 Troubleshooting

33. The transistor is off; therefore, $V_1 = \mathbf{0 \text{ V}}$, $V_2 = \mathbf{0 \text{ V}}$, $V_3 = \mathbf{8 \text{ V}}$.
34. $V_1 = \mathbf{0.7 \text{ V}}$, $V_2 = \mathbf{0 \text{ V}}$
 $I_B = \frac{8 \text{ V} - 0.7 \text{ V}}{33 \text{ k}\Omega} - \frac{0.7 \text{ V}}{10 \text{ k}\Omega} = 221 \mu\text{A} - 70 \mu\text{A} = 151 \mu\text{A}$
 $I_C = 200(151 \mu\text{A}) = 30.2 \text{ mA}$
 $I_{C(sat)} = \frac{8 \text{ V}}{2.2 \text{ k}\Omega} = 3.64 \text{ mA}$, so $V_C \equiv V_E = \mathbf{0 \text{ V}}$

If the problem is corrected,

$$V_1 = \left(\frac{10 \text{ k}\Omega}{10 \text{ k}\Omega + 33 \text{ k}\Omega} \right) 8 \text{ V} = \mathbf{1.86 \text{ V}}$$

$$V_2 = V_E = 1.86 \text{ V} - 0.7 \text{ V} = \mathbf{1.16 \text{ V}}$$

$$I_E = \frac{1.16 \text{ V}}{1.0 \text{ k}\Omega} = 1.16 \text{ mA}$$

$$V_3 = V_C = 8 \text{ V} - (1.16 \text{ mA})(2.2 \text{ k}\Omega) = \mathbf{5.45 \text{ V}}$$

- 35.** (a) Open collector
 (b) No problems
 (c) Transistor shorted from collector-to-emitter
 (d) Open emitter

- 36.** For $\beta_{DC} = 35$:

$$V_B = \left(\frac{4.5 \text{ k}\Omega}{14.5 \text{ k}\Omega} \right)(-10 \text{ V}) = -3.1 \text{ V}$$

For $\beta_{DC} = 100$:

$$V_B = \left(\frac{5.17 \text{ k}\Omega}{15.17 \text{ k}\Omega} \right)(-10 \text{ V}) = -3.4 \text{ V}$$

The measured base voltage at point 4 is within the correct range.

$$V_E = -3.1 \text{ V} + 0.7 \text{ V} = -2.4 \text{ V}$$

$$I_C \cong I_E = \frac{-2.4 \text{ V}}{680 \Omega} = -3.53 \text{ mA}$$

$$V_C = -10 \text{ V} - (-3.53 \text{ mA})(1.0 \text{ k}\Omega) = -6.47 \text{ V}$$

Allowing for some variation in V_{BE} and for resistor tolerances, the measured collector and emitter voltages are correct.

- 37.** (a) The 680Ω resistor is open:

Meter 1: 10 V

Meter 2: floating

$$\text{Meter 3: } V_B = \left(\frac{5.6 \text{ k}\Omega}{15.6 \text{ k}\Omega} \right)(-10 \text{ V}) = \mathbf{-3.59 \text{ V}}$$

Meter 4: 10 V

- (b) The $5.6 \text{ k}\Omega$ resistor is open.

$$I_B = \frac{9.3 \text{ V}}{10 \text{ k}\Omega + 35(680 \Omega)} = 275 \mu\text{A}$$

$$I_C = 35(275 \mu\text{A}) = 9.6 \text{ mA}$$

$$I_{C(\text{sat})} = \frac{10 \text{ V}}{1680 \Omega} = 5.95 \text{ mA}$$

The transistor is saturated.

Meter 1: 10 V

Meter 2: (5.95 mA)(680 Ω) = 4.05 V

Meter 3: 4.05 V + 0.7 V = 4.75 V

Meter 4: 10 V - (5.95 mA)(1.0 kΩ) = 4.05 V

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- (c) The $10\text{ k}\Omega$ resistor is open. The transistor is off.

*Meter 1: **10 V***

*Meter 2: **0 V***

*Meter 3: **0 V***

*Meter 4: **10 V***

- (d) The $1.0\text{ k}\Omega$ resistor is open. Collector current is zero.

*Meter 1: **10 V***

Meter 2: $1.27\text{ V} - 0.7\text{ V} = \mathbf{0.57\text{ V}}$

$$\text{Meter 3: } \left(\frac{5.6\text{ k}\Omega \parallel 680\text{ }\Omega}{10\text{ k}\Omega + 5.6\text{ k}\Omega \parallel 680\text{ }\Omega} \right) (10\text{ V}) + 0.7\text{ V} = 0.57\text{ V} + 0.7\text{ V} = \mathbf{1.27\text{ V}}$$

Meter 4: floating

- (e) A short from emitter to ground.

*Meter 1: **10 V***

*Meter 2: **0 V***

*Meter 3: **0.7 V***

$$I_B \approx \frac{(10\text{ V} - 0.7\text{ V})}{10\text{ k}\Omega} = \frac{9.3\text{ V}}{10\text{ k}\Omega} = 0.93\text{ mA}$$

$$I_{C(\min)} = 35(0.93\text{ mA}) = 32.6\text{ mA}$$

$$I_{C(\text{sat})} = \frac{10\text{ V}}{1.0\text{ k}\Omega} = 10\text{ mA}$$

The transistor is saturated.

Meter 4: $\approx \mathbf{0\text{ V}}$

- (f) An open base-emitter junction. The transistor is off.

*Meter 1: **10 V***

*Meter 2: **0 V***

$$\text{Meter 3: } \left(\frac{5.6\text{ k}\Omega}{15.6\text{ k}\Omega} \right) (10\text{ V}) = \mathbf{3.59\text{ V}}$$

*Meter 4: **10 V***

Application Activity Problems

- 38.** With R_1 open:

$$V_B = \mathbf{0} \text{ V}, V_E = \mathbf{0} \text{ V}, V_C = V_{CC} = \mathbf{9.1} \text{ V}$$

- 39.** Faults that will cause the transistor of textbook Figure 5-30(a) to go into cutoff:

R_1 open, R_2 shorted, base lead or BE junction open.

- 40.** At 45°C : $R_{\text{Therm}} = 2.7 \text{ k}\Omega$

$$V_B = \left(\frac{R_{\text{Therm}}}{R_1 + R_{\text{Therm}}} \right) 9 \text{ V} = \left(\frac{2.7 \text{ k}\Omega}{7.4 \text{ k}\Omega} \right) 9 \text{ V} = 3.28 \text{ V}$$

$$V_E = V_B - 0.7 \text{ V} = 2.58 \text{ V}$$

$$I_E = I_C = \frac{V_E}{R_3} = \frac{2.58 \text{ V}}{470 \Omega} = 5.49 \text{ mA}$$

$$V_C = V_{\text{OUT}} = 9 \text{ V} - (5.49 \text{ mA})(1 \text{ k}\Omega) = \mathbf{3.51} \text{ V}$$

At 48°C : $R_{\text{Therm}} = 1.78 \text{ k}\Omega$

$$V_B = \left(\frac{1.78 \text{ k}\Omega}{6.48 \text{ k}\Omega} \right) 9 \text{ V} = 2.47 \text{ V}$$

$$V_E = 2.47 \text{ V} - 0.7 \text{ V} = 1.77 \text{ V}$$

$$I_E = I_C = \frac{1.77 \text{ V}}{470 \Omega} = 3.77 \text{ mA}$$

$$V_C = V_{\text{OUT}} = 9 \text{ V} - (3.77 \text{ mA})(1 \text{ k}\Omega) = \mathbf{5.23} \text{ V}$$

At 53°C : $R_{\text{Therm}} = 1.28 \text{ k}\Omega$

$$V_B = \left(\frac{1.28 \text{ k}\Omega}{5.98 \text{ k}\Omega} \right) 9 \text{ V} = 1.93 \text{ V}$$

$$V_E = 1.93 \text{ V} - 0.7 \text{ V} = 1.23 \text{ V}$$

$$I_E = I_C = \frac{1.23 \text{ V}}{470 \Omega} = 2.62 \text{ mA}$$

$$V_C = V_{\text{OUT}} = 9 \text{ V} - (2.62 \text{ mA})(1 \text{ k}\Omega) = \mathbf{6.38} \text{ V}$$

- 41.** The following measurements would indicate an open CB junction:

$$V_C = V_{CC} = \mathbf{+9.1} \text{ V}$$

V_B normal

$V_E \approx \mathbf{0} \text{ V}$

Datasheet Problems

- 42.** For $T = 45^\circ\text{C}$ and $R_2 = 2.7 \text{ k}\Omega$

$$R_{\text{IN(base)}} = 2.7 \text{ k}\Omega \parallel (30)(470 \Omega) = 2.7 \text{ k}\Omega \parallel 14.1 \text{ k}\Omega = 2.27 \text{ k}\Omega \text{ min}$$

$$R_{\text{IN(base)}} = 2.7 \text{ k}\Omega \parallel (300)(470 \Omega) = 2.7 \text{ k}\Omega \parallel 141 \text{ k}\Omega = 2.65 \text{ k}\Omega \text{ max}$$

$$V_{B(\text{min})} = \left(\frac{2.27 \text{ k}\Omega}{2.27 \text{ k}\Omega + 5.6 \text{ k}\Omega} \right) 9.1 \text{ V} = \left(\frac{2.27 \text{ k}\Omega}{7.87} \right) 9.1 \text{ V} = \mathbf{2.62} \text{ V}$$

$$V_{E(\text{min})} = 2.62 \text{ V} - 0.7 \text{ V} = \mathbf{1.92} \text{ V}$$

Chapter 5

$$\text{So, } I_C \approx I_E = \frac{1.92 \text{ V}}{470 \Omega} = 4.09 \text{ mA}$$

$$V_{C(\max)} = 9.1 \text{ V} - (4.09 \text{ mA})(1.0 \text{ k}\Omega) = \mathbf{5.01 \text{ V}}$$

$$V_{B(\max)} = \left(\frac{2.65 \text{ k}\Omega}{2.65 \text{ k}\Omega + 5.6 \text{ k}\Omega} \right) 9.1 \text{ V} = \left(\frac{2.65 \text{ k}\Omega}{8.25 \text{ k}\Omega} \right) 9.1 \text{ V} = \mathbf{2.92 \text{ V}}$$

$$V_{E(\max)} = 2.92 \text{ V} - 0.7 \text{ V} = \mathbf{2.22 \text{ V}}$$

$$\text{So, } I_C \approx I_E = \frac{2.22 \text{ V}}{470 \Omega} = 4.73 \text{ mA}$$

$$V_{C(\min)} = 9.1 \text{ V} - (4.73 \text{ mA})(1.0 \text{ k}\Omega) = \mathbf{4.37 \text{ V}}$$

For $T = 55^\circ\text{C}$ and $R_2 = 1.24 \text{ k}\Omega$:

$$R_{IN(base)} = 1.24 \text{ k}\Omega \parallel (30)(470 \Omega) = 1.24 \text{ k}\Omega \parallel 14.1 \text{ k}\Omega = 1.14 \text{ k}\Omega \text{ min}$$

$$R_{IN(base)} = 1.24 \text{ k}\Omega \parallel (300)(470 \Omega) = 1.24 \text{ k}\Omega \parallel 141 \text{ k}\Omega = 1.23 \text{ k}\Omega \text{ max}$$

$$V_{B(\min)} = \left(\frac{1.14 \text{ k}\Omega}{1.14 \text{ k}\Omega + 5.6 \text{ k}\Omega} \right) 9.1 \text{ V} = \left(\frac{1.14 \text{ k}\Omega}{6.74 \text{ k}\Omega} \right) 9.1 \text{ V} = \mathbf{1.54 \text{ V}}$$

$$V_{E(\min)} = 1.54 \text{ V} - 0.7 \text{ V} = \mathbf{0.839 \text{ V}}$$

$$\text{So, } I_C \approx I_E = \frac{0.839 \text{ V}}{470 \Omega} = 1.78 \text{ mA}$$

$$V_{C(\max)} = 9.1 \text{ V} - (1.78 \text{ mA})(1.0 \text{ k}\Omega) = \mathbf{7.32 \text{ V}}$$

$$V_{B(\max)} = \left(\frac{1.23 \text{ k}\Omega}{1.23 \text{ k}\Omega + 5.6 \text{ k}\Omega} \right) 9.1 \text{ V} = \left(\frac{1.23 \text{ k}\Omega}{6.83 \text{ k}\Omega} \right) 9.1 \text{ V} = \mathbf{1.64 \text{ V}}$$

$$V_{E(\max)} = 1.64 \text{ V} - 0.7 \text{ V} = \mathbf{0.938 \text{ V}}$$

$$\text{So, } I_C \approx I_E = \frac{0.938 \text{ V}}{470 \Omega} = 2.0 \text{ mA}$$

$$V_{C(\min)} = 9.1 \text{ V} - (2.0 \text{ mA})(1.0 \text{ k}\Omega) = \mathbf{7.10 \text{ V}}$$

43. At $T = 45^\circ\text{C}$ for minimum β_{DC} :

$$P_{D(\max)} = (5.01 \text{ V} - 1.92 \text{ V})(4.09 \text{ mA}) = (3.09 \text{ V})(4.09 \text{ mA}) = 12.6 \text{ mW}$$

At $T = 55^\circ\text{C}$ for minimum β_{DC} :

$$P_{D(\max)} = (7.32 \text{ V} - 0.839 \text{ V})(1.78 \text{ mA}) = (6.48 \text{ V})(1.78 \text{ mA}) = 11.5 \text{ mW}$$

For maximum beta values, the results are comparable and nowhere near the maximum.

$$P_{D(\max)} = 625 \text{ mW} - (5.0 \text{ m}/^\circ\text{C})(30^\circ\text{C}) = 475 \text{ mW}$$

No ratings are exceeded.

44. For the datasheet of Figure 5-50 in the textbook:

- For a 2N2222A, $I_{C(\max)} = \mathbf{1 \text{ A}}$ continuous
- For a 2N2118A, $V_{EB(\max)} = \mathbf{6.0 \text{ V}}$

45. For a 2N2222A @ $T = 100^\circ\text{C}$:

$$P_{D(\max)} = 0.8 \text{ W} - (4.57 \text{ mW}/^\circ\text{C})(100^\circ\text{C} - 25^\circ\text{C}) = 0.8 \text{ W} - 343 \text{ mW} = \mathbf{457 \text{ mW}}$$

46. If I_C changes from 1 mA to 500 mA in a 2N2219A, the percentage change in β_{DC} is

$$\Delta\beta_{DC} = \left(\frac{30 - 50}{50} \right) 100\% = \mathbf{-40\%}$$

Advanced Problems

- 47.** See Figure 5-5.

$$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}} = \frac{15 \text{ V} - 5 \text{ V}}{5 \text{ mA}} = 2 \text{ k}\Omega$$

Assume $\beta_{DC} = 100$.

$$I_{BQ} = \frac{I_{CQ}}{\beta_{DC}} = \frac{5 \text{ mA}}{100} = 50 \mu\text{A}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_{BQ}} = \frac{15 \text{ V} - 0.7 \text{ V}}{50 \mu\text{A}} = 286 \text{ k}\Omega$$

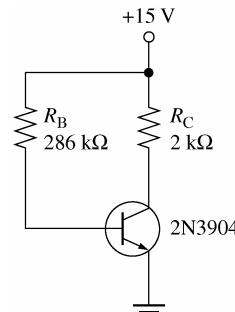


Figure 5-5

- 48.** See Figure 5-6.

Assume $\beta_{DC} = 200$.

$$I_{BQ} = \frac{I_{CQ}}{\beta_{DC}} = \frac{10 \text{ mA}}{200} = 50 \mu\text{A}$$

Let $R_B = 1.0 \text{ k}\Omega$

$$R_E = \frac{12 \text{ V} - (50 \mu\text{A})(1.0 \text{ k}\Omega) - 0.7 \text{ V}}{10 \text{ mA}} = \frac{11.3 \text{ V}}{10 \text{ mA}} = 1.13 \text{ k}\Omega$$

$$R_C = \frac{12 \text{ V} - (-12 \text{ V} + 11.3 \text{ V} + 4 \text{ V})}{10 \text{ mA}} = \frac{8.7 \text{ V}}{10 \text{ mA}} = 870 \Omega$$

870 Ω and 1.13 kΩ are not standard values. $R_C = 820 \Omega$ and $R_E = 1.2 \text{ k}\Omega$ give $I_{CQ} \approx 9.38 \text{ mA}$, $V_{CEQ} \approx 5.05 \text{ V}$.

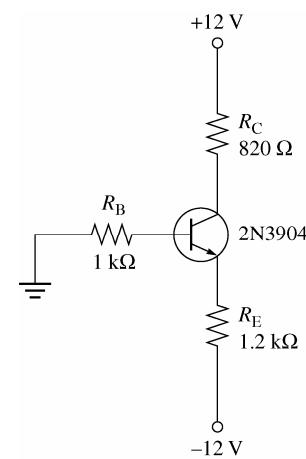


Figure 5-6

- 49.** See Figure 5-7.

$\beta_{DC(min)} \approx 70$. Let $R_E = 1.0 \text{ k}\Omega$.

$$V_E = I_E R_E = 1.5 \text{ mA}(1.0 \text{ k}\Omega) = 1.5 \text{ V}$$

$$V_B = 1.5 \text{ V} + 0.7 \text{ V} = 2.2 \text{ V}$$

$$R_C = \frac{V_{CC} - V_{CEQ} - V_E}{I_{CQ}} = \frac{9 \text{ V} - 1.5 \text{ V} - 3 \text{ V}}{1.5 \text{ mA}} = 3 \text{ k}\Omega$$

$$R_1 + R_2 = \frac{V_{CC}}{I_{CC(max)} - I_{CQ}} = \frac{9 \text{ V}}{5 \text{ mA} - 1.5 \text{ mA}} = 2.57 \text{ k}\Omega \text{ min}$$

Asssume $\beta_{DC} R_E \gg R_2$. The ratio of bias resistors equals the ratio of the voltages as follows.

$$\frac{R_1}{R_2} = \frac{6.8 \text{ V}}{2.2 \text{ V}} = 3.09$$

$$R_1 = 3.09 R_2$$

$$R_1 + R_2 = R_2 + 3.09 R_2 = 2.57 \text{ k}\Omega$$

$$4.09 R_2 = 2.57 \text{ k}\Omega$$

$$R_2 = \frac{2.57 \text{ k}\Omega}{4.09} = 628 \Omega$$

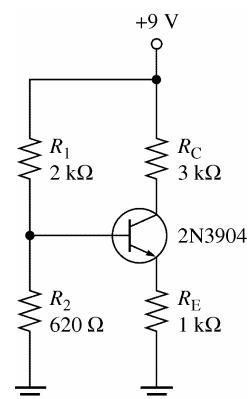


Figure 5-7

Chapter 5

So, $R_2 \approx 620 \Omega$ and $R_1 = 1.92 \text{ k}\Omega \approx 2 \text{ k}\Omega$.

From this,

$$R_{IN(base)} = 70(1.0 \text{ k}\Omega) = 70 \text{ k}\Omega \gg R_2$$

$$\text{so, } V_B = \left(\frac{620 \Omega}{2.62 \text{ k}\Omega} \right) 9 \text{ V} = 2.13 \text{ V}$$

$$V_E = 2.13 \text{ V} - 0.7 \text{ V} = 1.43 \text{ V}$$

$$I_{CQ} \approx I_E = \frac{1.43 \text{ V}}{1.0 \text{ k}\Omega} = 1.43 \text{ mA}$$

$$V_{CEQ} = 9 \text{ V} - (1.43 \text{ mA})(1.0 \text{ k}\Omega + 3 \text{ k}\Omega) = 3.28 \text{ V}$$

50. See Figure 5-8.

$\beta_{DC} \approx 75$.

$$I_{BQ} = \frac{10 \text{ mA}}{75} = 133 \mu\text{A}$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_{CQ}} = \frac{5 \text{ V} - 1.5 \text{ V}}{10 \text{ mA}} = 350 \Omega \text{ (use } 360 \Omega)$$

$$R_B = \frac{V_{CE} - 0.7 \text{ V}}{I_{BQ}} = \frac{1.55 \text{ V} - 0.7 \text{ V}}{133 \mu\text{A}} = 6 \text{ k}\Omega \text{ (use } 6.2 \text{ k}\Omega)$$

$$I_{CQ} = \frac{5 \text{ V} - 0.7 \text{ V}}{360 \Omega + 6.2 \text{ k}\Omega / 75} = 9.71 \text{ mA}$$

$$V_{CEQ} = V_C = 5 \text{ V} - (9.71 \text{ mA})(360 \Omega) = 1.50 \text{ V}$$

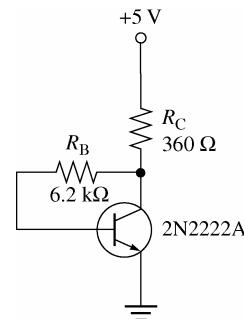


Figure 5-8

51. The 2N3904 in textbook Figure 5-48 **can be replaced** with a 2N2222A and maintain the same voltage range from 45°C to 55°C because the voltage-divider circuit is essentially β independent and the β_{DC} parameters of the two transistors are comparable.
52. For the 2N2222A using the datasheet in textbook Figure 5-51 at $I_C = 150 \text{ mA}$ and $V_{CE} = 1.0 \text{ V}$:
- At $T = -55^\circ\text{C}$, $h_{FE(\min)} = (0.45)(50) = 22.5$
- At $T = 25^\circ\text{C}$, $h_{FE(\min)} = (0.63)(50) = 31.5$
- At $T = 175^\circ\text{C}$, $h_{FE(\min)} = (0.53)(50) = 26.6$
53. If the valve interface circuit loading of the temperature conversion circuit changes from 100 kΩ to 10 kΩ, the Q-point will have a reduced V_{CEQ} because the current through R_C will consist of the same I_C and a larger I_L . I_{CQ} is unaffected in the sense that the transistor collector current is the same, although the collector resistance current is larger. The transistor saturates sooner so that lower temperatures do not register as well, if at all.
54. It is not feasible to operate the circuit from a 5.1 V dc supply and maintain the same range of output voltages because the output voltage at 60°C must be 6.478 V.

Multisim Troubleshooting Problems

The solutions showing instrument connections for Problems 55 through 60 are available from the Instructor's Resource Center. See Chapter 1 for instructions. The faults in the circuit files may be accessed using the password *book* (all lowercase).

- 55.** R_C open
- 56.** R_B open
- 57.** R_2 open
- 58.** Collector-emitter shorted
- 59.** R_C shorted
- 60.** Base-emitter open

Chapter 6

BJT Amplifiers

Section 6-1 Amplifier Operation

1. Slightly greater than **1 mA** minimum
2. From the graph of Figure 6-4, the highest value of dc collector current is about **6 mA**.

Section 6-2 Transistor AC Models

3. $r'_e = \frac{25 \text{ mV}}{I_E} = \frac{25 \text{ mV}}{3 \text{ mA}} = \mathbf{8.33 \Omega}$

4. $\beta_{ac} = h_{fe} = \mathbf{200}$

5. $I_C = \beta_{DC} I_B = 130(10 \mu\text{A}) = 1.3 \text{ mA}$

$$I_E = \frac{I_C}{\alpha_{DC}} = \frac{1.3 \text{ mA}}{0.99} = 1.31 \text{ mA}$$

$$r'_e = \frac{25 \text{ mV}}{I_E} = \frac{25 \text{ mV}}{1.31 \text{ mA}} = \mathbf{19 \Omega}$$

6. $\beta_{DC} = \frac{I_C}{I_B} = \frac{2 \text{ mA}}{15 \mu\text{A}} = \mathbf{133}$

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B} = \frac{0.35 \text{ mA}}{3 \mu\text{A}} = \mathbf{117}$$

Section 6-3 The Common-Emitter Amplifier

7. See Figure 6-1.

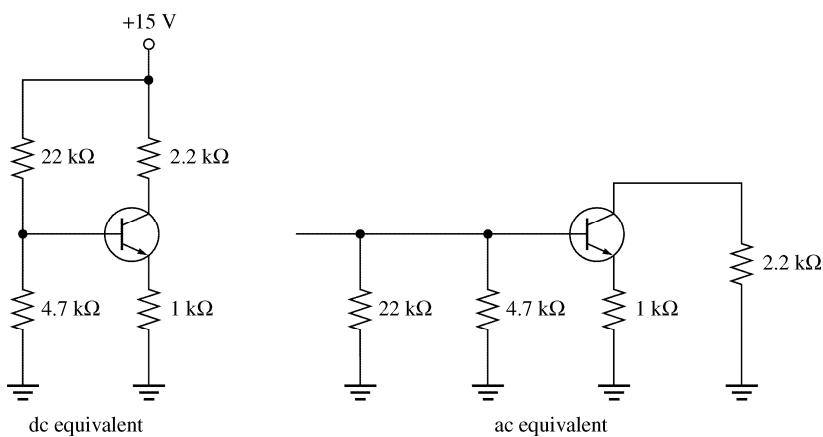


Figure 6-1

8. (a) $V_B = \left(\frac{R_2}{R_1 + R_2} \right) V_{CC} = \left(\frac{4.7 \text{ k}\Omega}{26.7 \text{ k}\Omega} \right) 15 \text{ V} = \mathbf{2.64 \text{ V}}$

(b) $V_E = V_B - 0.7 \text{ V} = 2.64 - 0.7 \text{ V} = \mathbf{1.94 \text{ V}}$

(c) $I_E = \frac{V_E}{R_E} = \frac{1.94 \text{ V}}{1.0 \text{ k}\Omega} = \mathbf{1.94 \text{ mA}}$

(d) $I_C \cong I_E = \mathbf{1.94 \text{ mA}}$

(e) $V_C = V_{CC} - I_C R_C = 15 \text{ V} - (1.94 \text{ mA})(2.2 \text{ k}\Omega) = \mathbf{11.6 \text{ V}}$

9. $I_{CC} = I_{BIAS} + I_C$

$$I_{BIAS} = \frac{V_B}{R_2} = \frac{2.64 \text{ V}}{4.7 \text{ k}\Omega} = 562 \mu\text{A}$$

$I_{CC} = 562 \mu\text{A} + 1.94 \text{ mA} = 2.50 \text{ mA}$

$P = I_{CC} V_{CC} = (2.5 \text{ mA})(15 \text{ V}) = \mathbf{37.5 \text{ mW}}$

10. (a) $V_B = \left(\frac{4.7 \text{ k}\Omega}{4.7 \text{ k}\Omega + 22 \text{ k}\Omega} \right) 15 \text{ V} = 2.64 \text{ V}$

$V_E = 2.64 \text{ V} - 0.7 \text{ V} = 1.94 \text{ V}$

$I_E = \frac{1.94 \text{ V}}{1.0 \text{ k}\Omega} = 1.94 \text{ mA}$

$r'_e \cong \frac{25 \text{ mV}}{I_E} = \frac{25 \text{ mV}}{1.94 \text{ mA}} = 12.9 \Omega$

$R_{in(base)} = \beta_{ac} (r'_e + R_E) = 100(1012.9 \Omega) \cong \mathbf{101 \text{ k}\Omega}$

(b) $R_{in} = R_{in(base)} \parallel R_1 \parallel R_2 = 101 \text{ k}\Omega \parallel 22 \text{ k}\Omega \parallel 4.7 \text{ k}\Omega = \mathbf{3.73 \text{ k}\Omega}$

(c) $A_v = \frac{R_C}{R_E + r'_e} = \frac{2.2 \text{ k}\Omega}{12.02 \Omega} = \mathbf{2.17}$

11. (a) $R_{in(base)} = \beta_{ac} r'_e = 100(12.9 \Omega) = \mathbf{1.29 \text{ k}\Omega}$

(b) $R_{in} = 1.29 \text{ k}\Omega \parallel 22 \text{ k}\Omega \parallel 4.7 \text{ k}\Omega = \mathbf{968 \Omega}$

(c) $A_v = \frac{R_C}{r'_e} = \frac{2.2 \text{ k}\Omega}{12.9 \Omega} = \mathbf{171}$

12. (a) $R_{in(base)} = \beta_{ac} r'_e = 100(12.9 \Omega) = \mathbf{1.29 \text{ k}\Omega}$

(b) $R_{in} = 1.29 \text{ k}\Omega \parallel 22 \text{ k}\Omega \parallel 4.7 \text{ k}\Omega = \mathbf{968 \Omega}$

(c) $A_v = \frac{R_c}{r'_e} = \frac{R_C \parallel R_L}{r'_e} = \frac{2.2 \text{ k}\Omega \parallel 10 \text{ k}\Omega}{12.9 \Omega} = \mathbf{140}$

Chapter 6

13. (a) $V_B = \left(\frac{R_2 \parallel \beta_{DC} R_E}{R_1 + R_2 \parallel \beta_{DC} R_E} \right) V_{CC} = \left(\frac{12 \text{ k}\Omega \parallel 75(1.0 \text{ k}\Omega)}{47 \text{ k}\Omega + 12 \text{ k}\Omega \parallel 75(1.0 \text{ k}\Omega)} \right) 18 \text{ V} = \mathbf{3.25 \text{ V}}$

(b) $V_E = V_B - 0.7 \text{ V} = \mathbf{2.55 \text{ V}}$

(c) $I_E = \frac{V_E}{R_E} = \frac{2.55 \text{ V}}{1.0 \text{ k}\Omega} = \mathbf{2.55 \text{ mA}}$

(d) $I_C \approx I_E = \mathbf{2.55 \text{ mA}}$

(e) $V_C = V_{CC} - I_C R_C = 18 \text{ V} - (2.55 \text{ mA})(3.3 \text{ k}\Omega) = \mathbf{9.59 \text{ V}}$

(f) $V_{CE} = V_C - V_E = 9.59 \text{ V} - 2.55 \text{ V} = \mathbf{7.04 \text{ V}}$

14. From Problem 13, $I_E = 2.55 \text{ mA}$

(a) $R_{in(base)} = \beta_{ac} r'_e \approx \beta_{ac} \left(\frac{25 \text{ mV}}{I_E} \right) = 70 \left(\frac{25 \text{ mV}}{2.55 \text{ mA}} \right) = \mathbf{686 \Omega}$

(b) $R_{in} = R_1 \parallel R_2 \parallel R_{in(base)} = 47 \text{ k}\Omega \parallel 12 \text{ k}\Omega \parallel 686 \Omega = \mathbf{640 \Omega}$

(c) $A_v = \frac{R_C \parallel R_L}{r'_e} = \frac{3.3 \text{ k}\Omega \parallel 10 \text{ k}\Omega}{9.8 \Omega} = \mathbf{253}$

(d) $A_i = \beta_{ac} = \mathbf{70}$

(e) $A_p = A_v A_i = (253)(70) = \mathbf{17,710}$

15. $V_b = \left(\frac{R_{in}}{R_{in} + R_s} \right) V_{in} = \left(\frac{640 \Omega}{640 \Omega + 600 \Omega} \right) 12 \mu\text{V}$

Attenuation of the input network is

$$\left(\frac{R_{in}}{R_{in} + R_s} \right) = \left(\frac{640 \Omega}{640 \Omega + 600 \Omega} \right) = 0.516$$

$A'_v = 0.516 A_v = 0.516(253) = \mathbf{131}$

$\theta = \mathbf{180^\circ}$

16. $V_B = \left(\frac{R_2 \parallel \beta_{DC} R_E}{R_1 + R_2 \parallel \beta_{DC} R_E} \right) V_{CC} = \left(\frac{3.3 \text{ k}\Omega \parallel 150(100 \Omega)}{12 \text{ k}\Omega + 3.3 \text{ k}\Omega \parallel 150(100 \Omega)} \right) 8 \text{ V} = 1.47 \text{ V}$

$I_E = \frac{V_B - 0.7 \text{ V}}{R_E} = \frac{1.47 \text{ V} - 0.7 \text{ V}}{100 \Omega} = 7.7 \text{ mA}$

$r'_e = \frac{25 \text{ mV}}{I_E} = \frac{25 \text{ mV}}{7.7 \text{ mA}} = 3.25 \Omega$

$A_{v(min)} = \frac{R_C}{R_E + r'_e} = \frac{330 \Omega}{100 \Omega + 3.25 \Omega} = \mathbf{3.2}$

$A_{v(max)} = \frac{R_C}{r'_e} = \frac{330 \Omega}{3.25 \Omega} = \mathbf{102}$

- 17.** Maximum gain is at $R_e = 0 \Omega$.

$$R_{IN(base)} = \beta_{DC} R_E = 150(100 \Omega) = 15 \text{ k}\Omega$$

$$V_B = \left(\frac{R_2 \parallel R_{IN(base)}}{R_1 + R_2 \parallel R_{IN(base)}} \right) V_{CC} = \left(\frac{3.3 \text{ k}\Omega \parallel 15 \text{ k}\Omega}{12 \text{ k}\Omega + 3.3 \text{ k}\Omega \parallel 15 \text{ k}\Omega} \right) 8 \text{ V} = 1.47 \text{ V}$$

$$I_E = \frac{V_B - V_{BE}}{R_E} = \frac{1.47 \text{ V} - 0.7 \text{ V}}{100 \Omega} = 7.7 \text{ mA}$$

$$r'_e \equiv \frac{25 \text{ mV}}{7.7 \text{ mA}} = 3.25 \Omega$$

$$A_{v(max)} = \frac{R_C \parallel R_L}{r'_e} = \frac{330 \Omega \parallel 600 \Omega}{3.25 \Omega} = \mathbf{65.5}$$

Minimum gain is at $R_e = 100 \Omega$.

$$A_{v(min)} = \frac{R_C \parallel R_L}{R_E + r'_e} = \frac{212.9 \Omega}{103.25 \Omega} = \mathbf{2.06}$$

- 18.** $R_{in} = R_1 \parallel R_2 \parallel \beta_{ac} r'_e = 3.3 \text{ k}\Omega \parallel 12 \text{ k}\Omega \parallel 150(3.25 \Omega) = 410 \Omega$

Attenuation of the input network is

$$\frac{R_{in}}{R_{in} + R_s} = \frac{410 \Omega}{410 \Omega + 300 \Omega} = 0.578$$

$$A_v = \frac{R_c}{r'_e} = \frac{330 \Omega \parallel 1.0 \text{ k}\Omega}{3.25 \Omega} = 76.3$$

$$A'_v = 0.5777 A_v = 0.578(76.3) = \mathbf{44.1}$$

- 19.** See Figure 6-2.

$$r'_e \equiv \frac{25 \text{ mV}}{2.55 \text{ mA}} = 9.8 \Omega$$

$$R_e \geq 10r'_e$$

Set $R_e = 100 \Omega$.

The gain is reduced to

$$A_v = \frac{R_C}{R_e + r'_e} = \frac{3.3 \text{ k}\Omega}{109.8 \Omega} = 30.1$$

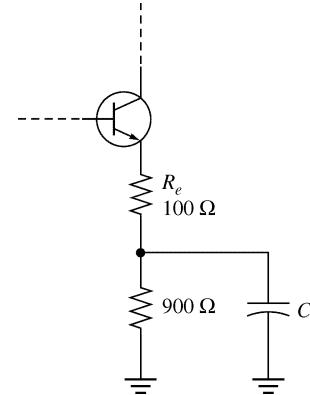


Figure 6-2

Chapter 6

Section 6-4 The Common-Collector Amplifier

20. $V_B = \left(\frac{R_2}{R_i + R_2} \right) V_{CC} = \left(\frac{4.7 \text{ k}\Omega}{14.7 \text{ k}\Omega} \right) 5.5 \text{ V} = 1.76 \text{ V}$

$$I_E = \frac{V_B - 0.7 \text{ V}}{R_E} = \frac{1.76 \text{ V} - 0.7 \text{ V}}{1.0 \text{ k}\Omega} = 1.06 \text{ mA}$$

$$r'_e \approx \frac{25 \text{ mV}}{1.06 \text{ mA}} = 23.6 \Omega$$

$$A_v = \frac{R_E}{R_E + r'_e} = \frac{1.0 \text{ k}\Omega}{1.0 \text{ k}\Omega + 23.6 \Omega} = \mathbf{0.977}$$

21. $R_{in} = R_i \parallel R_2 \parallel \beta_{ac}(r'_e + R_E) \approx R_i \parallel R_2 \parallel \beta_{ac}R_E = 10 \text{ k}\Omega \parallel 4.7 \text{ k}\Omega \parallel 100 \text{ k}\Omega = \mathbf{3.1 \text{ k}\Omega}$

$$V_{OUT} = V_B - 0.7 \text{ V} = \left(\frac{R_2}{R_i + R_2} \right) V_{CC} - 0.7 \text{ V} = \left(\frac{4.7 \text{ k}\Omega}{14.7 \text{ k}\Omega} \right) 5.5 \text{ V} - 0.7 \text{ V} = \mathbf{1.06 \text{ V}}$$

22. The voltage gain is **reduced** because $A_v = \frac{R_e}{R_e + r'_e}$.

23. $V_B = \left(\frac{R_2}{R_i + R_2} \right) V_{CC} = \left(\frac{4.7 \text{ k}\Omega}{14.7 \text{ k}\Omega} \right) 5.5 \text{ V} = 1.76 \text{ V}$

$$I_E = \frac{V_B - V_{BE}}{R_E} = \frac{1.76 \text{ V} - 0.7 \text{ V}}{1.0 \text{ k}\Omega} = 1.06 \text{ mA}$$

$$r'_e \approx \frac{25 \text{ mV}}{I_E} = \frac{25 \text{ mV}}{1.06 \text{ mA}} = 23.6 \Omega$$

$$A_v = \frac{R_E \parallel R_L}{r'_e + R_E \parallel R_L}$$

$$A_v(r'_e + R_E \parallel R_L) = R_E \parallel R_L$$

$$R_E \parallel R_L - A_v(R_E \parallel R_L) = A_v r'_e$$

$$(R_E \parallel R_L)(1 - A_v) = A_v r'_e$$

$$(R_E \parallel R_L) = \frac{A_v r'_e}{(1 - A_v)} = \frac{0.9(23.6 \Omega)}{1 - 0.9} = 212.4 \Omega$$

$$R_L R_E = 212.4 R_L + 212.4 R_E$$

$$R_L R_E - 212.4 R_L = 212.4 R_E$$

$$R_L = \frac{212.4 R_E}{R_E - 212.4} = \frac{(212.4 \Omega)(1000 \Omega)}{1000 \Omega - 212.4 \Omega} = \mathbf{270 \Omega}$$

24. (a) $V_{C1} = \mathbf{10 \text{ V}}$

$$V_{B1} = \left(\frac{R_2}{R_1 + R_2} \right) V_{CC} = \left(\frac{22 \text{ k}\Omega}{55 \text{ k}\Omega} \right) 10 \text{ V} = \mathbf{4 \text{ V}}$$

$$V_{E1} = V_{B1} - 0.7 \text{ V} = 4 \text{ V} - 0.7 \text{ V} = \mathbf{3.3 \text{ V}}$$

$$V_{C2} = \mathbf{10 \text{ V}}$$

$$V_{B2} = V_{E1} = \mathbf{3.3 \text{ V}}$$

$$V_{E2} = V_{B2} - 0.7 \text{ V} = 3.3 \text{ V} - 0.7 \text{ V} = \mathbf{2.6 \text{ V}}$$

$$(b) \beta'_{DC} = \beta_{DC1}\beta_{DC2} = (150)(100) = \mathbf{15,000}$$

$$(c) I_{E1} = \frac{V_{E1} - 0.7 \text{ V}}{\beta_{DC2} R_E} = \frac{2.6 \text{ V}}{100(1.5 \text{ k}\Omega)} = 17.3 \mu\text{A}$$

$$r'_{e1} \cong \frac{25 \text{ mV}}{I_{E1}} = \frac{25 \text{ mV}}{17.3 \mu\text{A}} = \mathbf{1.45 \text{ k}\Omega}$$

$$I_{E2} = \frac{V_{E2}}{R_E} = \frac{2.6 \text{ V}}{1.5 \text{ k}\Omega} = 1.73 \text{ mA}$$

$$r'_{e2} \cong \frac{25 \text{ mV}}{I_{E2}} = \frac{25 \text{ mV}}{1.73 \text{ mA}} = \mathbf{14.5 \Omega}$$

$$(d) R_{in} = R_1 \parallel R_2 \parallel R_{in(base1)}$$

$$R_{in(base1)} = \beta_{ac1}\beta_{ac2}R_E = (150)(100)(1.5 \text{ k}\Omega) = 22.5 \text{ M}\Omega$$

$$R_{in} = 33 \text{ k}\Omega \parallel 22 \text{ k}\Omega \parallel 22.5 \text{ M}\Omega = \mathbf{13.2 \text{ k}\Omega}$$

25. $R_{in(base)} = \beta_{ac1}\beta_{ac2}R_E = (150)(100)(1.5 \text{ k}\Omega) = 22.5 \text{ M}\Omega$

$$R_{in} = R_2 \parallel R_1 \parallel R_{in(base)} = 22 \text{ k}\Omega \parallel 33 \text{ k}\Omega \parallel 22.5 \text{ M}\Omega = 13.2 \text{ k}\Omega$$

$$I_{in} = \frac{V_{in}}{R_{in}} = \frac{1 \text{ V}}{13.2 \text{ k}\Omega} = 75.8 \mu\text{A}$$

$$I_{in(base1)} = \frac{V_{in}}{R_{in(base1)}} = \frac{1 \text{ V}}{22.5 \text{ M}\Omega} = 44.4 \text{ nA}$$

$$I_e \cong \beta_{ac1}\beta_{ac2}I_{in(base1)} = (150)(100)(44.4 \text{ nA}) = 667 \mu\text{A}$$

$$A'_i = \frac{I_e}{I_{in}} = \frac{667 \mu\text{A}}{75.8 \mu\text{A}} = \mathbf{8.8}$$

Section 6-5 The Common-Base Amplifier

26. The main disadvantage of a common-base amplifier is **low input impedance**. Another disadvantage is **unity current gain**.

Chapter 6

27. $V_E = \left(\frac{R_2}{R_1 + R_2} \right) V_{CC} - V_{BE} = \left(\frac{10 \text{ k}\Omega}{32 \text{ k}\Omega} \right) 24 \text{ V} - 0.7 \text{ V} = 6.8 \text{ V}$

$$I_E = \frac{6.8 \text{ V}}{620 \text{ }\Omega} = 10.97 \text{ mA}$$

$$R_{in(emitter)} = r'_e \cong \frac{25 \text{ mV}}{I_E} = \frac{25 \text{ mA}}{10.97 \text{ mA}} = 2.28 \text{ }\Omega$$

$$A_v = \frac{R_C}{r'_e} = \frac{1.2 \text{ k}\Omega}{2.28 \text{ }\Omega} = 526$$

$$A_i \cong 1$$

$$A_p = A_i A_v \cong 526$$

28. (a) Common-base (b) Common-emitter (c) Common-collector

Section 6-6 Multistage Amplifiers

29. $A'_v = A_{v1} A_{v2} = (20)(20) = 400$

30. $A'_{v(dB)} = 10 \text{ dB} + 10 \text{ dB} + 10 \text{ dB} = 30 \text{ dB}$

$$20 \log A'_v = 30 \text{ dB}$$

$$\log A'_v = \frac{30}{20} = 1.5$$

$$A'_v = 31.6$$

31. (a) $V_E = \left(\frac{R_2}{R_1 + R_2} \right) V_{CC} - V_{BE} = \left(\frac{8.2 \text{ k}\Omega}{33 \text{ k}\Omega + 8.2 \text{ k}\Omega} \right) 15 \text{ V} - 0.7 \text{ V} = 2.29 \text{ V}$

$$I_E = \frac{V_E}{R_E} = \frac{2.29 \text{ V}}{1.0 \text{ k}\Omega} = 2.29 \text{ mA}$$

$$r'_e \cong \frac{25 \text{ mV}}{I_E} = \frac{25 \text{ mV}}{2.29 \text{ mA}} = 10.9 \text{ }\Omega$$

$$R_{in(2)} = R_6 \parallel R_5 \parallel \beta_{ac} r'_e = 8.2 \text{ k}\Omega \parallel 33 \text{ k}\Omega \parallel 175(10.9 \text{ }\Omega) = 1.48 \text{ k}\Omega$$

$$A_{v1} = \frac{R_C \parallel R_{in(2)}}{r'_e} = \frac{3.3 \text{ k}\Omega \parallel 1.48 \text{ k}\Omega}{10.9 \text{ }\Omega} = 93.6$$

$$A_{v2} = \frac{R_C}{r'_e} = \frac{3.3 \text{ k}\Omega}{10.9 \text{ }\Omega} = 303$$

(b) $A'_v = A_{v1} A_{v2} = (93.6)(303) = 28,361$

(c) $A_{v1(dB)} = 20 \log(93.6) = 39.4 \text{ dB}$

$$A_{v2(dB)} = 20 \log(303) = 49.6 \text{ dB}$$

$$A'_{v(dB)} = 20 \log(28,361) = 89.1 \text{ dB}$$

32. (a) $A_{v1} = \frac{R_C \parallel R_{in(2)}}{r'_e} = \frac{3.3 \text{ k}\Omega \parallel 1.48 \text{ k}\Omega}{10.9 \Omega} = 93.6$

$$A_{v2} = \frac{R_C \parallel R_L}{r'_e} = \frac{3.3 \text{ k}\Omega \parallel 18 \text{ k}\Omega}{10.9 \Omega} = 256$$

(b) $R_{in(1)} = R_1 \parallel R_2 \parallel \beta_{ac} r'_e = 33 \text{ k}\Omega \parallel 8.2 \text{ k}\Omega \parallel 175(10.9 \Omega) = 1.48 \text{ k}\Omega$

Attenuation of the input network is

$$\frac{R_{in(1)}}{R_{in(1)} + R_s} = \frac{1.48 \text{ k}\Omega}{1.48 \text{ k}\Omega + 75 \Omega} = 0.95$$

$$A'_v = (0.95)A_{v1}A_{v2} = (0.95)(93.6)(256) = 22,764$$

(c) $A_{v1(\text{dB})} = 20 \log(93.6) = 39.4 \text{ dB}$
 $A_{v2(\text{dB})} = 20 \log(256) = 48.2 \text{ dB}$
 $A'_{v(\text{dB})} = 20 \log(22,764) = 87.1 \text{ dB}$

33. $V_{B1} = \left(\frac{R_2}{R_1 + R_2} \right) V_{CC} = \left(\frac{22 \text{ k}\Omega}{122 \text{ k}\Omega} \right) 12 \text{ V} = 2.16 \text{ V}$

$$V_{E1} = V_{B1} - 0.7 \text{ V} = 1.46 \text{ V}$$

$$I_{C1} \cong I_{E1} = \frac{V_{E1}}{R_4} = \frac{1.46 \text{ V}}{4.7 \text{ k}\Omega} = 0.311 \text{ mA}$$

$$V_{C1} = V_{CC} - I_{C1}R_3 = 12 \text{ V} - (0.311 \text{ mA})(22 \text{ k}\Omega) = 5.16 \text{ V}$$

$$V_{B2} = V_{C1} = 5.16 \text{ V}$$

$$V_{E2} = V_{B2} - 0.7 \text{ V} = 5.16 \text{ V} - 0.7 \text{ V} = 4.46 \text{ V}$$

$$I_{C2} \cong I_{E2} = \frac{V_{E2}}{R_6} = \frac{4.46 \text{ V}}{10 \text{ k}\Omega} = 0.446 \text{ mA}$$

$$V_{C2} = V_{CC} - I_{C2}R_5 = 12 \text{ V} - (0.446 \text{ mA})(10 \text{ k}\Omega) = 7.54 \text{ V}$$

$$r'_{e2} \cong \frac{25 \text{ mV}}{I_{E2}} = \frac{25 \text{ mV}}{0.446 \text{ mA}} = 56 \Omega$$

$$R_{in(2)} = \beta_{ac} r'_{e2} = (125)(56 \Omega) = 7 \text{ k}\Omega$$

$$r'_{e1} \cong \frac{25 \text{ mV}}{I_{E1}} = \frac{25 \text{ mV}}{0.311 \text{ mA}} = 80.4 \Omega$$

$$A_{v1} = \frac{R_3 \parallel R_{in(2)}}{r'_{e1}} = \frac{22 \text{ k}\Omega \parallel 7 \text{ k}\Omega}{80.4 \Omega} = 66$$

$$A_{v2} = \frac{R_5}{r'_{e2}} = \frac{10 \text{ k}\Omega}{56 \Omega} = 179$$

$$A'_v = A_v A_{v2} = (66)(179) = 11,814$$

- 34.** (a) $20 \log(12) = 21.6 \text{ dB}$
 (b) $20 \log(50) = 34.0 \text{ dB}$
 (c) $20 \log(100) = 40.0 \text{ dB}$
 (d) $20 \log(2500) = 68.0 \text{ dB}$

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35. (a) $20 \log\left(\frac{V_2}{V_1}\right) = 3 \text{ dB}$ (b) $20 \log\left(\frac{V_2}{V_1}\right) = 6 \text{ dB}$ (c) $20 \log\left(\frac{V_2}{V_1}\right) = 10 \text{ dB}$
- $$\log\left(\frac{V_2}{V_1}\right) = \frac{3}{20} = 0.15 \quad \log\left(\frac{V_2}{V_1}\right) = \frac{6}{20} = 0.3 \quad \log\left(\frac{V_2}{V_1}\right) = \frac{10}{20} = 0.5$$
- $$\frac{V_2}{V_1} = \mathbf{1.41} \quad \frac{V_2}{V_1} = \mathbf{2} \quad \frac{V_2}{V_1} = \mathbf{3.16}$$
- (d) $20 \log\left(\frac{V_2}{V_1}\right) = 20 \text{ dB}$ (e) $20 \log\left(\frac{V_2}{V_1}\right) = 40 \text{ dB}$
- $$\log\left(\frac{V_2}{V_1}\right) = \frac{20}{20} = 1 \quad \log\left(\frac{V_2}{V_1}\right) = \frac{40}{20} = 2$$
- $$\frac{V_2}{V_1} = \mathbf{10} \quad \frac{V_2}{V_1} = \mathbf{100}$$

Section 6-7 The Differential Amplifier

36. Determine I_E for each transistor:

$$I_{R_E} = \frac{V_{R_E}}{R_E} = \frac{14.3 \text{ V}}{2.2 \text{ k}\Omega} = 6.5 \text{ mA}$$

$$I_{E(Q1)} = I_{E(Q2)} = \frac{I_{R_E}}{2} = 3.25 \text{ mA}$$

Determine I_C for each transistor:

$$I_{C(Q1)} = \alpha_1 I_{E(Q1)} = 0.980(3.25 \text{ mA}) = 3.185 \text{ mA}$$

$$I_{C(Q2)} = \alpha_2 I_{E(Q2)} = 0.975(3.25 \text{ mA}) = 3.169 \text{ mA}$$

Calculate the collector voltages:

$$V_{C(Q1)} = 15 \text{ V} - (3.185 \text{ mA})(3.3 \text{ k}\Omega) = 4.49 \text{ V}$$

$$V_{C(Q2)} = 15 \text{ V} - (3.169 \text{ mA})(3.3 \text{ k}\Omega) = 4.54 \text{ V}$$

The differential output voltage is:

$$V_{\text{OUT}} = V_{C(Q2)} - V_{C(Q1)} = 4.54 \text{ V} - 4.49 \text{ V} = 0.05 \text{ V} = \mathbf{50 \text{ mV}}$$

37. V_1 measures the differential output voltage.
 V_2 measures the noninverting input voltage.
 V_3 measures the single-ended output voltage.
 V_4 measures the differential input voltage.
 I_1 measures the bias current.

- 38.** Calculate the voltage across each collector resistor:

$$V_{R_{C1}} = (1.35 \text{ mA})(5.1 \text{ k}\Omega) = 6.89 \text{ V}$$

$$V_{R_{C2}} = (1.29 \text{ mA})(5.1 \text{ k}\Omega) = 6.58 \text{ V}$$

The differential output voltage is:

$$V_{\text{OUT}} = V_{C(Q2)} - V_{C(Q1)} = (V_{CC} - V_{R_{C2}}) - (V_{CC} - V_{R_{C1}}) = V_{R_{C1}} - V_{R_{C2}}$$

$$= 6.89 \text{ V} - 6.58 \text{ V} = 0.31 \text{ V} = \mathbf{310 \text{ mV}}$$

- 39.**
- (a) Single-ended differential input, differential output
 - (b) Single-ended, differential input, single-ended output
 - (c) Double-ended differential input, single-ended output
 - (d) Double-ended differential input, differential output

Section 6-8 Troubleshooting

40. $V_E = \left(\frac{R_1}{R_1 + R_2} \right) 10 \text{ V} - 0.7 \text{ V} = \left(\frac{10 \text{ k}\Omega}{57 \text{ k}\Omega} \right) 10 \text{ V} - 0.7 \text{ V} = 1.05 \text{ V}$

$$I_E = \frac{V_E}{R_4} = \frac{1.05 \text{ V}}{1.0 \text{ k}\Omega} = 1.05 \text{ mA}$$

$$V_C = 10 \text{ V} - (1.05 \text{ mA})(4.7 \text{ k}\Omega) = 5.07 \text{ V}$$

$$V_{CE} = 5.07 \text{ V} - 1.05 \text{ V} = 4.02 \text{ V}$$

$$r'_{CE} \approx \frac{V_{CE}}{I_E} = \frac{4.02 \text{ V}}{1.05 \text{ mA}} = 3.83 \text{ k}\Omega$$

With C_2 shorted:

$$R_{IN(2)} = R_6 \parallel \beta_{DC} R_8 = 10 \text{ k}\Omega \parallel 125(1.0 \text{ k}\Omega) = 9.26 \text{ k}\Omega$$

Looking from the collector of Q_1 :

$$(r'_{CE} + R_4) \parallel R_{IN(2)} = (3.83 \text{ k}\Omega + 1.0 \text{ k}\Omega) \parallel 9.26 \text{ k}\Omega = 3.17 \text{ k}\Omega$$

$$V_{C1} = \left(\frac{3.17 \text{ k}\Omega}{3.17 \text{ k}\Omega + 4.7 \text{ k}\Omega} \right) 10 \text{ V} = \mathbf{4.03 \text{ V}}$$

- 41.** Q_1 is in **cutoff**. $I_C = 0 \text{ A}$, so $V_{C2} = \mathbf{10 \text{ V}}$.

- 42.**
- (a) Reduced gain
 - (b) No output signal
 - (c) Reduced gain
 - (d) Bias levels of first stage will change. I_C will increase and Q_1 will go into saturation.
 - (e) No signal at the Q_1 collector
 - (f) Signal at the Q_2 base. No output signal.

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43. $r'_e = 10.9 \Omega$ $R_{in} = 1.48 \text{ k}\Omega$
 $A_{v1} = 93.6$ $A_{v2} = 302$

Test Point	DC Volts	AC Volts (rms)
Input	0 V	$25 \mu\text{A}$
Q_1 base	2.99 V	$20.8 \mu\text{V}$
Q_1 emitter	2.29 V	0 V
Q_1 collector	7.44 V	1.95 mV
Q_2 base	2.99 V	1.95 mV
Q_2 emitter	2.29 V	0 V
Q_2 collector	7.44 V	589 mV
Output	0 V	589 mV

Application Activity Problems

44. For the block diagram of textbook Figure 6-46 with no output from the power amplifier or preamplifier and only one faulty block, the power amplifier must be ok because the fault must be one that affects the preamplifier's output prior to the power amplifier. Check the input to the preamplifier.
45. (a) No output signal
(b) Reduced output signal
(c) No output signal
(d) Reduced output signal
(e) No output signal
(f) Increased output signal (perhaps with distortion)
46. $R_7 = 220 \Omega$ will bias Q_2 off.
47. (a) Q_1 is in **cutoff**.
(b) $V_{C1} = V_{EE}$
(c) V_{C2} is unchanged and at **5.87 V**.

Datasheet Problems

- 48.** From the datasheet in textbook Figure 6-63:
- for a 2N3947, $\beta_{ac(min)} = h_{fe(min)} = 100$
 - For a 2N3947, $r'_{e(min)}$ cannot be determined since $h_{re(min)}$ is not given.
 - For a 2N3947, $r'_{c(min)}$ cannot be determined since $h_{re(min)}$ is not given.
- 49.** From the 2N3947 datasheet in Figure 6-63:
- For a 2N3947, $\beta_{ac(max)} = 700$
 - For a 2N3947, $r'_{e(max)} = \frac{h_{re}}{h_{oe}} = \frac{20 \times 10^{-4}}{50 \mu\text{S}} = 40 \Omega$
 - For a 2N3947, $r'_{c(max)} = \frac{h_{re} + 1}{h_{oe}} = \frac{20 \times 10^{-4} + 1}{50 \mu\text{S}} = 20 \text{ k}\Omega$
- 50.** For maximum current gain, a **2N3947** should be used.

Advanced Problems

- 51.** In the circuit of textbook Figure 6-62, a leaky coupling capacitor would affect the biasing of the transistors, attenuate the ac signal, and decrease the frequency response.
- 52.** See Figure 6-3.

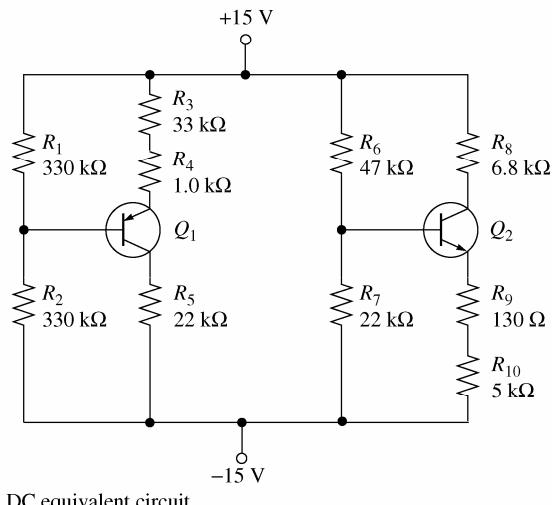
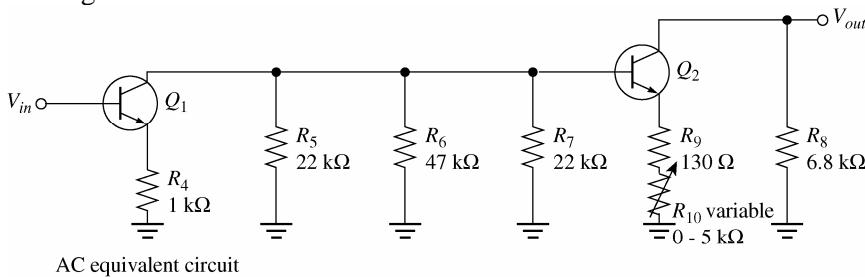


Figure 6-3

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53. For the 2nd stage:

$$I_{R6-7} = \frac{30 \text{ V}}{R_6 + R_7} = \frac{30 \text{ V}}{69 \text{ k}\Omega} = 435 \mu\text{A}$$

$$\begin{aligned} V_{B2} &= V_{CC} - I_{R6-7}R_6 = 15 \text{ V} - (435 \mu\text{A})(47 \text{ k}\Omega) \\ &= 15 \text{ V} - 20.5 \text{ V} = -5.5 \text{ V} \end{aligned}$$

$$I_{E2} = \frac{V_{E2}}{R_9 + R_{l0}} = \frac{-5.5 \text{ V} - 0.7 \text{ V}}{5.13 \text{ k}\Omega} = -1.21 \text{ mA}$$

$$r'_{e2} = \frac{25 \text{ mV}}{1.21 \text{ mA}} = 20.7 \Omega$$

With $R_{l0} = 0 \Omega$ for max gain:

$$A_{v(2)} = \frac{R_8}{R_9 + r'_{e2}} = \frac{6.8 \text{ k}\Omega}{150.7 \Omega} = 45.1 \text{ (unloaded)}$$

With a 10 kΩ load:

$$A_{v(2)} = \frac{R_8 \parallel R_L}{R_9 + r'_{e2}} = \frac{6.8 \text{ k}\Omega \parallel 10 \text{ k}\Omega}{150.7 \Omega} = \frac{4.05 \text{ k}\Omega}{150.7 \Omega} = 26.9$$

To keep unloaded gain:

$$\frac{4.05 \text{ k}\Omega}{R_9 + 20.7 \Omega} = 45.1$$

$$4.05 \text{ k}\Omega = 45.1(R_9 + 20.7 \Omega) = 45.1R_9 + 934 \Omega$$

$$R_9 = \frac{4.05 \text{ k}\Omega - 934 \Omega}{45.1} = 69.1 \Omega$$

54. $R_C > (100)(330 \Omega) = 33 \text{ k}\Omega$

To prevent cutoff, V_C must be no greater than

$$12 \text{ V} - (100)(1.414)(25 \text{ mV}) = 8.46 \text{ V}$$

In addition, V_C must fall no lower than $8.46 \text{ V} - 3.54 \text{ V} = 4.93 \text{ V}$ to prevent saturation.

$$R_C = 100(R_E + r'_e)$$

$$r'_e = \frac{25 \text{ mV}}{I_E}$$

$$12 \text{ V} - I_C R_C = 8.46 \text{ V}$$

$$I_C R_C = 3.54 \text{ V}$$

$$I_C (100(R_E + r'_e)) = 3.54 \text{ V}$$

$$I_C \left(100 \left(330 \Omega + \frac{25 \text{ mV}}{I_C} \right) \right) \cong 3.54 \text{ V}$$

$$(33 \text{ k}\Omega)I_C + 2.5 \text{ V} = 3.54 \text{ V}$$

$$I_C = 31.4 \mu\text{A}$$

$$r'_e \cong \frac{25 \text{ mV}}{31.4 \mu\text{A}} = 797 \Omega$$

$$R_C = 100(330 \Omega + 797 \Omega) = 113 \text{ k}\Omega$$

Let $R_C = 120 \text{ k}\Omega$.

$$V_C = 12 \text{ V} - (31.4 \mu\text{A})(120 \text{ k}\Omega) = 8.23 \text{ V}$$

$$V_{C(\text{sat})} = 8.23 \text{ V} - 3.54 \text{ V} = 4.69 \text{ V}$$

$$\frac{R_{E(\text{tot})}}{R_C} = \frac{4.69 \text{ V}}{7.31 \text{ V}}$$

$R_{E(\text{tot})} = (0.642)(120 \text{ k}\Omega) = 77 \text{ k}\Omega$. Let $R_E = 68 \text{ k}\Omega$.

$$V_E = (31.4 \mu\text{A})(68 \text{ k}\Omega) = 2.14 \text{ V}$$

$$V_B = 2.14 \text{ V} + 0.7 \text{ V} = 2.84 \text{ V}$$

$$\frac{R_2}{R_1} = \frac{2.84 \text{ V}}{9.16 \text{ V}} = 0.310$$

$R_2 = 0.310R_1$. If $R_1 = 20 \text{ k}\Omega$, $R_2 = 6.2 \text{ k}\Omega$.

The amplifier circuit is shown in Figure 6-4.

From the design:

$$V_B = \left(\frac{6.2 \text{ k}\Omega}{26.2 \text{ k}\Omega} \right) 12 \text{ V} = 2.84 \text{ V}$$

$$V_E = 2.14 \text{ V}$$

$$I_C \approx I_E = \frac{2.14 \text{ V}}{68.3 \text{ k}\Omega} = 31.3 \mu\text{A}$$

$$r'_e = \frac{25 \text{ mV}}{31.3 \mu\text{A}} = 798 \Omega$$

$$A_v = \frac{120 \text{ k}\Omega}{795 \Omega + 330 \Omega} = 106 \text{ or } 40.5 \text{ dB}$$

$$V_C = 12 \text{ V} - (31.3 \mu\text{A})(120 \text{ k}\Omega) = 8.24 \text{ V}$$

The design is a close fit.

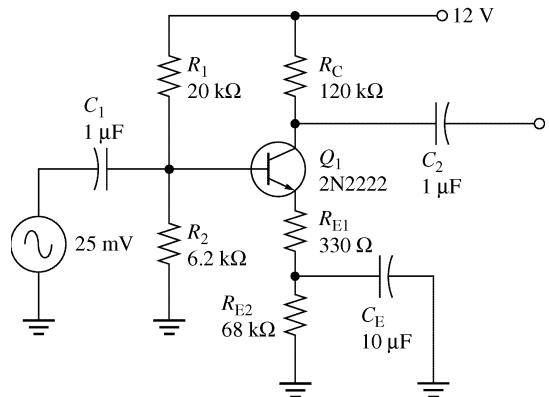


Figure 6-4

55. See Figure 6-5.

$$R_{in} = 120 \text{ k}\Omega \parallel 120 \text{ k}\Omega \parallel (100)(5.1 \text{ k}\Omega) = 53.6 \text{ k}\Omega \text{ minimum}$$

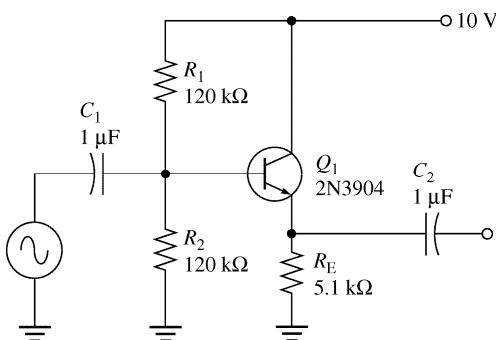


Figure 6-5

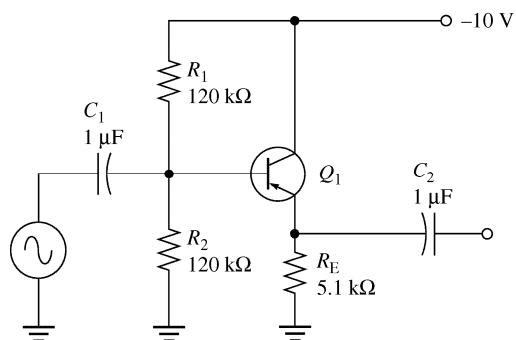


Figure 6-6

56. See Figure 6-6.

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- 57.** See Figure 6-7.

$$I_C = \frac{6 \text{ V} - 0.7 \text{ V}}{510 \Omega + 2 \text{ k}\Omega / 100} = 10 \text{ mA}$$

$$r'_e = \frac{25 \text{ mV}}{10 \text{ mA}} = 2.5 \text{ }\Omega$$

$$A_v = \frac{180 \text{ }\Omega}{2.5 \text{ }\Omega} = 72.4$$

This is reasonably close ($\approx 3.3\%$ off) and can be made closer by putting a $7.5 \text{ }\Omega$ resistor in series with the $180 \text{ }\Omega$ collector resistor.

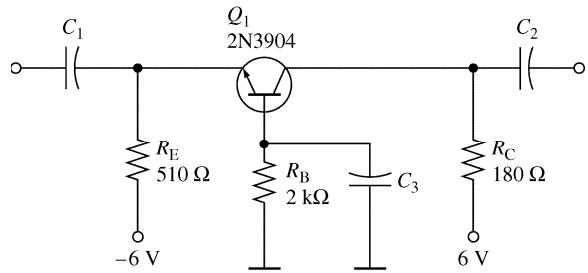


Figure 6-7

- 58.** Assuming $\beta_{ac} = 200$,

$$C_1 = \frac{1}{2\pi f_c R} = \frac{1}{2\pi(100 \text{ Hz})(330 \text{ k}\Omega \parallel 330 \text{ k}\Omega \parallel (200 \times 34 \text{ k}\Omega))}$$

$$= \frac{1}{2\pi(100 \text{ Hz})(161 \text{ k}\Omega)} = 0.01 \mu\text{F}$$

$$C_2 = \frac{1}{2\pi f_c R} = \frac{1}{2\pi(100 \text{ Hz})(22 \text{ k}\Omega + 47 \text{ k}\Omega \parallel 22 \text{ k}\Omega \parallel (200 \times 5.13 \text{ k}\Omega))}$$

$$= \frac{1}{2\pi(100 \text{ Hz})(36.98 \text{ k}\Omega)} = 0.043 \mu\text{F}$$

- 59.** $I_C \cong I_E$

$$A_v = \frac{R_C}{r'_e} \cong \frac{R_C}{25 \text{ mV}/I_E} \cong \frac{R_C}{25 \text{ mV}/I_C} = \frac{R_C I_C}{25 \text{ mV}} = \frac{V_{R_C}}{25 \text{ mV}} = 40 V_{R_C}$$

Multisim Troubleshooting Problems

The solutions showing instrument connections for Problems 60 through 65 are available from the Instructor Resource Center. See Chapter 1 for instructions. The faults in the circuit files may be accessed using the password *book* (all lowercase).

- 60.** C_2 open

- 61.** C_2 shorted

- 62.** R_E leaky

- 63.** C_1 open

- 64.** C_2 open

- 65.** C_3 open

Chapter 7

Power Amplifiers

Section 7-1 The Class A Power Amplifier

1. (a) $V_B = \left(\frac{R_2}{R_1 + R_2} \right) V_{CC} = \left(\frac{330 \Omega}{1.0 \text{ k}\Omega + 330 \text{ k}\Omega} \right) 15 \text{ V} = 3.72 \text{ V}$

$$V_E = V_B - V_{BE} = 3.72 - 0.7 \text{ V} = 3.02 \text{ V}$$

$$I_{CQ} \approx I_E = \frac{V_E}{R_{E1} + R_{E2}} = \frac{3.02 \text{ V}}{8.2 \Omega + 36 \Omega} = 68.4 \text{ mA}$$

$$\begin{aligned} V_{CEQ} &= V_{CC} - (I_C)(R_{E1} + R_{E2} + R_L) \\ &= 15 \text{ V} - (68.4 \text{ mA})(8.2 \Omega + 36 \Omega + 100 \Omega) = 5.14 \text{ V} \end{aligned}$$

(b) $A_v = \frac{R_L}{R_{E1} + r'_e} = \frac{100 \Omega}{8.2 \Omega + 0.37 \Omega} = 11.7$

$$\begin{aligned} R_{in} &= \beta_{ac}(R_{E1} + r'_e) \parallel R_1 \parallel R_2 \\ &= 100 (8.2 \Omega + 0.37 \Omega) \parallel 330 \Omega \parallel 1.0 \text{ k}\Omega = 192 \Omega \end{aligned}$$

$$A_p = A_v^2 \left(\frac{R_{in}}{R_L} \right) = 11.7^2 \left(\frac{192 \Omega}{100 \Omega} \right) = 263$$

The computed voltage and power gains are slightly higher if r'_e is ignored.

2. (a) If R_L is removed, there is no collector current; hence, the power dissipated in the transistor is **zero**.
- (b) Power is dissipated only in the bias resistors plus a small amount in R_{E1} and R_{E2} . Since the load resistor has been removed, the base voltage is altered. The base voltage can be found from the Thevenin equivalent drawn for the bias circuit in Figure 7-1.

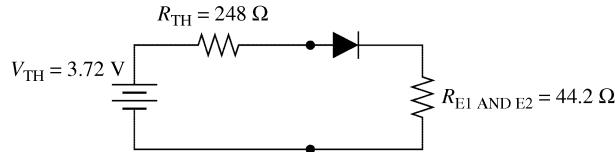


Figure 7-1

Applying the voltage-divider rule and including the base-emitter diode drop of 0.7 V result in a base voltage of 1.2 V. The power supply current is then computed as

$$I_{CC} = \frac{V_{CC} - 1.2 \text{ V}}{R_1} = \frac{15 \text{ V} - 1.2 \text{ V}}{1.0 \text{ k}\Omega} = 13.8 \text{ mA}$$

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Power from the supply is then computed as

$$P_T = I_{CC}V_{CC} = (13.8 \text{ mA})(15 \text{ V}) = 207 \text{ mW}$$

(c) $A_v = 11.7$ (see problem 1(b)). $V_{in} = 500 \text{ mV}_{pp} = 177 \text{ mV}_{rms}$.

$$V_{out} = A_v V_{in} = (11.7)(177 \text{ mV}) = 2.07 \text{ V}$$

$$P_{out} = \frac{V_{out}^2}{R_L} = \frac{2.07 \text{ V}^2}{100 \Omega} = 42.8 \text{ mW}$$

3. The changes are shown in Figure 7-2. The advantage of this arrangement is that the load resistor is referenced to ground.

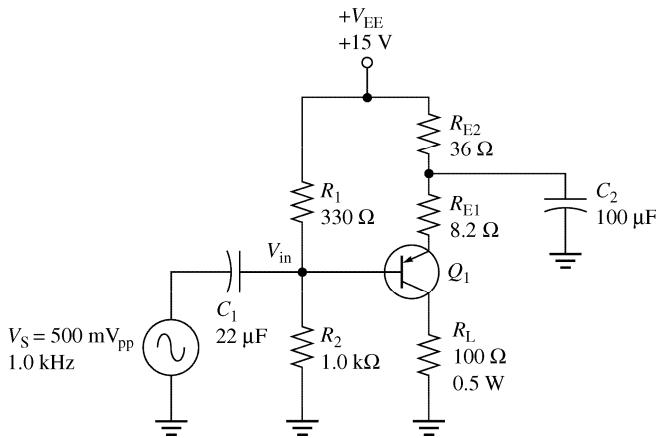


Figure 7-2

4. A CC amplifier has a voltage gain of approximately 1. Therefore,

$$A_p = \frac{R_{in}}{R_{out}} = \frac{2.2 \text{ k}\Omega}{50 \Omega} = 44$$

5. (a) Stiff voltage divider:

$$V_B = \left(\frac{R_2}{R_1 + R_2} \right) V_{CC} = \left(\frac{510 \Omega}{1190 \Omega} \right) 12 \text{ V} = 5.14 \text{ V}$$

$$V_E = V_B - 0.7 \text{ V} = 4.44 \text{ V}$$

$$I_E = \frac{V_E}{R_{E1} + R_{E2}} = \frac{4.44 \text{ V}}{79.7 \Omega} = 55.7 \text{ mA}$$

$$I_C \approx I_E = 55.7 \text{ mA}$$

$$V_C = V_{CC} - I_C R_C = 12 \text{ V} - (55.7 \text{ mA})(100 \Omega) = 6.43 \text{ V}$$

$$V_{CE} = V_C - V_E = 6.43 \text{ V} - 4.44 \text{ V} = 1.99 \text{ V}$$

- (b) Not stiff voltage divider:

$$R_{IN(BASE)} = \beta_{DC}(R_{E1} + R_{E2}) = 120(144 \Omega) = 17.0 \text{ k}\Omega$$

$$\begin{aligned} V_B &= \left(\frac{R_2 \parallel R_{IN(BASE)}}{R_1 + R_2 \parallel R_{IN(BASE)}} \right) V_{CC} = \left(\frac{4.7 \text{ k}\Omega \parallel 17.0 \text{ k}\Omega}{12 \text{ k}\Omega + 4.7 \text{ k}\Omega \parallel 17.0 \text{ k}\Omega} \right) 12 \text{ V} \\ &= \left(\frac{3.68 \text{ k}\Omega}{15.7 \text{ k}\Omega} \right) 12 \text{ V} = 2.8 \text{ V} \end{aligned}$$

$$V_E = V_B - 0.7 \text{ V} = 2.1 \text{ V}$$

$$I_E = \frac{V_E}{R_{E1} + R_{E2}} = \frac{2.1 \text{ V}}{144 \Omega} = 14.6 \text{ mA}$$

$$I_C \cong I_E = \mathbf{14.6 \text{ mA}}$$

$$V_C = V_{CC} - I_C R_C = 12 \text{ V} - (14.6 \text{ mA})(470 \Omega) = 5.14 \text{ V}$$

$$V_{CE} = V_C - V_E = 5.14 \text{ V} - 2.1 \text{ V} = \mathbf{3.04 \text{ V}}$$

6. The Q-point does not change because R_L is capacitively coupled and does not affect the DC values.

7. For the circuit in Figure 7-43(a):

$$R_{IN(BASE)} = \beta_{DC}(R_{E1} + R_{E2}) = (125)(79.7) = 9.96 \text{ k}\Omega$$

Since $R_{IN(BASE)} > 10R_2$, it can be neglected.

$$V_B = \left(\frac{R_2}{R_1 + R_2} \right) V_{CC} = \left(\frac{510 \Omega}{680 \Omega + 510 \Omega} \right) 12 \text{ V} = \left(\frac{510 \Omega}{1190 \Omega} \right) 12 \text{ V} = 5.14 \text{ V}$$

$$V_E = V_B - 0.7 \text{ V} = 5.14 \text{ V} - 0.7 \text{ V} = 4.44 \text{ V}$$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{4.44 \text{ V}}{79.7 \Omega} = 55.7 \text{ mA}$$

$$V_{CQ} = V_{CC} - I_{CQ} R_C = 12 \text{ V} - (55.7 \text{ mA})(100 \Omega) = 6.43 \text{ V}$$

$$V_{CEQ} = V_C - V_E = 6.43 \text{ V} - 4.44 \text{ V} = 1.99 \text{ V}$$

$$R_c = R_C \parallel R_L = 100 \Omega \parallel 100 \Omega = 50 \Omega$$

$$V_{ce(cutoff)} = V_{CEQ} + I_{CQ} R_c = 1.99 \text{ V} + 55.7 \text{ mA}(50 \Omega) = 4.78 \text{ V}$$

Since V_{CEQ} is closer to saturation, I_c is limited to

$$I_{c(p)} = \frac{V_{CEQ}}{R_c} = \frac{1.99 \text{ V}}{50 \Omega} = \mathbf{39.8 \text{ mA}}$$

V_{out} is limited to

$$V_{out(p)} = V_{CEQ} = \mathbf{1.99 \text{ V}}$$

For the circuit in 7-43(b):

$$R_{IN(BASE)} = \beta_{DC}(R_{E1} + R_{E2}) = (120)(142 \Omega) = 17 \text{ k}\Omega$$

Since $R_{IN(BASE)} < 10R_2$, it is taken into account.

$$V_B = \left(\frac{R_2 \parallel R_{IN(BASE)}}{R_1 + R_2 \parallel R_{IN(BASE)}} \right) V_{CC} = \left(\frac{4.7 \text{ k}\Omega \parallel 17 \text{ k}\Omega}{12 \text{ k}\Omega + 4.7 \text{ k}\Omega \parallel 17 \text{ k}\Omega} \right) 12 \text{ V} = \left(\frac{3.68 \text{ k}\Omega}{15.68 \text{ k}\Omega} \right) 12 \text{ V} = 2.82 \text{ V}$$

$$V_E = V_B - 0.7 \text{ V} = 2.82 \text{ V} - 0.7 \text{ V} = 2.12 \text{ V}$$

$$I_{CQ} \cong I_E = V_E/R_E = 2.12 \text{ V}/142 \Omega = 14.9 \text{ mA}$$

$$V_{CQ} = V_{CC} - I_{CQ} R_C = 12 \text{ V} - (14.9 \text{ mA})(470 \Omega) = 5.0 \text{ V}$$

$$V_{CEQ} = V_{CQ} - V_E = 5.0 \text{ V} - 2.12 \text{ V} = 2.88 \text{ V}$$

$$R_c = R_C \parallel R_L = 470 \Omega \parallel 470 \Omega = 235 \Omega$$

$$V_{ce(cutoff)} = V_{CEQ} + I_{CQ} R_c = 2.88 \text{ V} + 14.9 \text{ mA}(235 \Omega) = 6.38 \text{ V}$$

Since V_{CEQ} is closer to saturation, I_c is limited to

$$I_{c(p)} = \frac{V_{CEQ}}{R_c} = \frac{2.88 \text{ V}}{235 \Omega} = \mathbf{12.3 \text{ mA}}$$

V_{out} is limited to $V_{out(p)} = V_{CEQ} = \mathbf{2.88 \text{ V}}$

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8. (a) $A_p = A_v^2 \left(\frac{R_{in}}{R_L} \right)$

$$A_v \cong \frac{R_c}{R_{E1}} = \frac{R_C \parallel R_L}{R_{E1}} = \frac{100 \Omega \parallel 100 \Omega}{4.7 \Omega} = \frac{50 \Omega}{4.7 \Omega} = \mathbf{10.6}$$

$$R_{in} = R_1 \parallel R_2 \parallel R_{in(base)} = R_1 \parallel R_2 \parallel \beta_{ac} R_{E1}$$

$$R_{in} = 680 \Omega \parallel 510 \Omega \parallel (125)(4.7 \Omega) = 680 \Omega \parallel 510 \Omega \parallel 588 \Omega = 195 \Omega$$

$$A_p = (10.6)^2 \left(\frac{195 \Omega}{100 \Omega} \right) = \mathbf{219}$$

(b) $A_v \cong \frac{R_c}{R_{E1}} = \frac{R_C \parallel R_L}{R_{E1}} = \frac{470 \Omega \parallel 470 \Omega}{22 \Omega} = \frac{235 \Omega}{22 \Omega} = \mathbf{10.7}$

$$R_{in} = 12 \text{ k}\Omega \parallel 4.7 \text{ k}\Omega \parallel (120)(22 \Omega) = 12 \text{ k}\Omega \parallel 4.7 \text{ k}\Omega \parallel 2.64 \text{ k}\Omega = 1.48 \text{ k}\Omega$$

$$A_p = (10.7)^2 \left(\frac{1.48 \text{ k}\Omega}{470 \Omega} \right) = \mathbf{361}$$

9. $R_{IN(BASE)} = \beta_{DC} R_E = 90(130 \Omega) = 11.7 \text{ k}\Omega$

$$R_2 \parallel R_{IN(BASE)} = 1.0 \text{ k}\Omega \parallel 11.7 \text{ k}\Omega = 921 \Omega$$

$$V_B = \left(\frac{R_2 \parallel R_{IN(BASE)}}{R_1 + R_2 \parallel R_{IN(BASE)}} \right) V_{CC} = \left(\frac{921 \Omega}{5.62 \text{ k}\Omega} \right) 24 \text{ V} = 3.93 \text{ V}$$

$$V_E = V_B - 0.7 \text{ V} = 3.93 \text{ V} - 0.7 \text{ V} = 3.23 \text{ V}$$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{3.23 \text{ V}}{130 \Omega} = 24.8 \text{ mA}$$

$$V_C = V_{CC} - I_{CQ} R_C = 24 \text{ V} - (24.8 \text{ mA})(560 \Omega) = 10.1 \text{ V}$$

$$V_{CEQ} = V_C - V_E = 10.1 \text{ V} - 3.23 \text{ V} = 6.87 \text{ V}$$

$$P_{D(min)} = P_{DQ} = I_{CQ} V_{CEQ} = (24.8 \text{ mA})(6.87 \text{ V}) = \mathbf{170 \text{ mW}}$$

10. From Problem 9: $I_{CQ} = 24.8 \text{ mA}$ and $V_{CEQ} = 6.87 \text{ V}$

$$V_{ce(cutoff)} = V_{CEQ} + I_{CQ} R_c = 6.87 \text{ V} + (24.8 \text{ mA})(264 \Omega) = 13.4 \text{ V}$$

$$P_{out} = 0.5 I_{CQ}^2 R_c = 0.5(24.8 \text{ mA})^2(264 \Omega) = \mathbf{81.2 \text{ mW}}$$

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{P_{out}}{V_{CC} I_{CC}} = \frac{P_{out}}{V_{CC} I_{CQ}} = \frac{81.2 \text{ mW}}{(24 \text{ V})(24.8 \text{ mA})} = \mathbf{0.136}$$

Section 7-2 The Class B and Class AB Push-Pull Amplifiers

11. (a) $V_{B(Q1)} = 0 \text{ V} + 0.7 \text{ V} = \mathbf{0.7 \text{ V}}$

$$V_{B(Q2)} = 0 \text{ V} - 0.7 \text{ V} = \mathbf{-0.7 \text{ V}}$$

$$V_E = \mathbf{0 \text{ V}}$$

$$I_{CQ} = \frac{V_{CC} - (-V_{CC}) - 1.4 \text{ V}}{R_1 + R_2} = \frac{9 \text{ V} - (-9 \text{ V}) - 1.4 \text{ V}}{1.0 \text{ k}\Omega + 1.0 \text{ k}\Omega} = \mathbf{8.3 \text{ mA}}$$

$$V_{CEQ(Q1)} = \mathbf{9 \text{ V}}$$

$$V_{CEQ(Q2)} = \mathbf{-9 \text{ V}}$$

(b) $V_{out} = V_{in} = 5.0 \text{ V rms}$

$$P_{out} = \frac{(V_{out})^2}{R_L} = \frac{5.0 \text{ V}^2}{50 \Omega} = \mathbf{0.5 \text{ W}}$$

12. $I_{c(sat)} = \frac{V_{CC}}{R_L} = \frac{9.0 \text{ V}}{50 \Omega} = 180 \text{ mA}$

$$V_{ce(cutoff)} = 9 \text{ V}$$

These points define the ac load line as shown in Figure 7-3. The Q -point is at a collector current of 8.3 mA (see problem 11) and the dc load line rises vertically through this point.

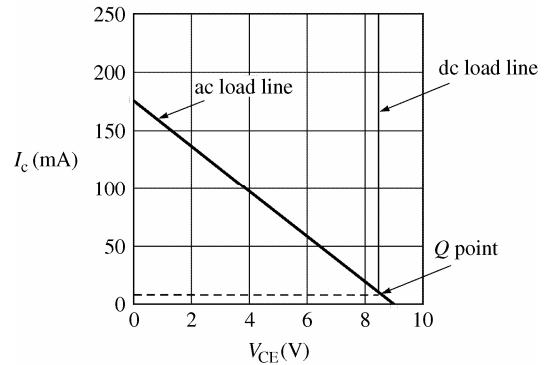


Figure 7-3

13. $R_{in} = \beta_{ac} (r'_e + R_L) \parallel R_1 \parallel R_2$

From Problem 11,

$$I_{CQ} = 8.3 \text{ mA}$$

$$\text{so, } I_E \approx 8.3 \text{ mA}$$

$$r'_e = \frac{25 \text{ mV}}{8.3 \text{ mA}} = 3 \Omega$$

$$R_{in} = 100(53 \Omega) \parallel 1.0 \text{ k}\Omega \parallel 1.0 \text{ k}\Omega$$

$$= 5300 \Omega \parallel 1.0 \text{ k}\Omega \parallel 1.0 \text{ k}\Omega = \mathbf{457 \Omega}$$

14. The DC voltage at the output becomes negative instead of 0 V.

15. (a) $V_{B(Q1)} = 7.5 \text{ V} + 0.7 \text{ V} = \mathbf{8.2 \text{ V}}$

$$V_{B(Q2)} = 7.5 \text{ V} - 0.7 \text{ V} = \mathbf{6.8 \text{ V}}$$

$$V_E = \frac{15 \text{ V}}{2} = \mathbf{7.5 \text{ V}}$$

$$I_{CQ} = \frac{V_{CC} - 1.4 \text{ V}}{R_1 + R_2} = \frac{15 \text{ V} - 1.4 \text{ V}}{1.0 \text{ k}\Omega + 1.0 \text{ k}\Omega} = \mathbf{6.8 \text{ mA}}$$

$$V_{CEQ(Q1)} = 15 \text{ V} - 7.5 \text{ V} = \mathbf{7.5 \text{ V}}$$

$$V_{CEQ(Q2)} = 0 \text{ V} - 7.5 \text{ V} = \mathbf{-7.5 \text{ V}}$$

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(b) $V_{in} = V_{out} = 10 \text{ V}_{\text{pp}} = 3.54 \text{ V rms}$

$$P_L = \frac{(V_L)^2}{R_L} = \frac{(3.54 \text{ V})^2}{75 \Omega} = \mathbf{167 \text{ mW}}$$

- 16.** (a) Maximum peak voltage = 7.5 V_p . $7.5 \text{ V}_p = 5.30 \text{ V rms}$

$$P_{L(\text{max})} = \frac{(V_L)^2}{R_L} = \frac{(5.30 \text{ V})^2}{75 \Omega} = \mathbf{375 \text{ mW}}$$

- (b) Maximum peak voltage = 12 V_p . $12 \text{ V}_p = 8.48 \text{ V rms}$

$$P_{L(\text{max})} = \frac{(V_L)^2}{R_L} = \frac{(8.48 \text{ V})^2}{75 \Omega} = \mathbf{960 \text{ mW}}$$

- 17.** (a) C_2 open or Q_2 open
 (b) power supply off, open R_1 , Q_1 base shorted to ground
 (c) Q_1 has collector-to-emitter short
 (d) one or both diodes shorted

18. $R_{in} = \beta_{ac}(r'_e + R_L) \parallel R_1 \parallel R_2$

From Problem 15:

$$I_{CQ} = 6.8 \text{ mA}$$

$$\text{so, } I_E \approx 6.8 \text{ mA}$$

$$r'_e = \frac{25 \text{ mV}}{I_E} = \frac{25 \text{ mV}}{6.8 \text{ mA}} = 3.68 \Omega$$

$$R_{in} = 200(78.7 \Omega) \parallel 1 \text{ k}\Omega \parallel 1 \text{ k}\Omega = 485 \Omega$$

$$V_b = \left(\frac{485 \Omega}{485 \Omega + 50 \Omega} \right) 1 \text{ V} = \mathbf{0.91 \text{ V rms}}$$

Section 7-3 The Class C Amplifier

19. $P_{D(\text{avg})} = \left(\frac{t_{on}}{T} \right) V_{CE(\text{sat})} I_{C(\text{sat})} = (0.1)(0.18 \text{ V})(25 \text{ mA}) = \mathbf{450 \mu W}$

20. $f_r = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{(10 \text{ mH})(0.001 \mu F)}} = \mathbf{50.3 \text{ kHz}}$

21. $V_{out(pp)} = 2V_{CC} = 2(12 \text{ V}) = \mathbf{24 \text{ V}}$

22. $P_{out} = \frac{0.5V_{CC}^2}{R_c} = \frac{0.5(15 \text{ V})^2}{50 \Omega} = 2.25 \text{ W}$

$$P_{D(\text{avg})} = \left(\frac{t_{on}}{T} \right) V_{CE(\text{sat})} I_{C(\text{sat})} = (0.1)(0.18 \text{ V})(25 \text{ mA}) = 0.45 \text{ mW}$$

$$\eta = \frac{P_{out}}{P_{out} + P_{D(\text{avg})}} = \frac{2.25 \text{ W}}{2.25 \text{ W} + 0.45 \text{ mW}} = \mathbf{0.9998}$$

Section 7-4 Troubleshooting

23. With C_1 open, only the negative half of the input signal appears across R_L .
24. One of the transistors is open between the collector and emitter or a coupling capacitor is open.
25.
 - (a) No dc supply voltage or R_1 open
 - (b) Diode D_2 open
 - (c) Circuit is OK
 - (d) Q_1 shorted from collector to emitter

Application Activity Problems

26. For the block diagram of textbook Figure 7-34 with no signal from the power amplifier or preamplifier, but with the microphone working, the problem is in the power amplifier or preamplifier. It must be assumed that the preamp is faulty, causing the power amp to have no signal.
27. For the circuit of Figure 7-35 with the base-emitter junction of Q_2 open, the dc output will be approximately -15 V with a signal output approximately equal to the input.
28. For the circuit of Figure 7-35 with the collector-emitter junction of Q_5 open, the dc output will be approximately $+15$ V with a signal output approximately equal to the input (some distortion possible).
29. On the circuit board of Figure 7-49, the vertically oriented diode has been installed backwards.

Datasheet Problems

30. From the BD135 datasheet of textbook Figure 7-50:
 - (a) $\beta_{DC(min)} = 40$ @ $I_C = 150$ mA, $V_{CE} = 2$ V
 $\beta_{DC(min)} = 25$ @ $I_C = 5$ mA, $V_{CE} = 2$ V
 - (b) For a BD135, $V_{CE(max)} = V_{CEO} = 45$ V
 - (c) $P_{D(max)} = 12.5$ W @ $T_C = 25^\circ\text{C}$
 - (d) $I_{C(max)} = 1.5$ A
31. $P_D = 10$ W @ 50°C from graph in Figure 7-50.
32. $P_D = 1$ W @ 50°C . Extrapolating from the case temperature graph in Figure 7-50, since $P_D = 1.25$ W @ 25°C ambient. This derating gives 1 W.
33. As I_C increases from 10 mA to approximately 125 mA, the dc current gain increases. As I_C increases above approximately 125 mA, the dc current gain decreases.
34. $h_{FE} \cong 89$ @ $I_C = 20$ mA

Chapter 7

Advanced Problems

35. T_C is much closer to the actual junction temperature than T_A . In a given operating environment, T_A is always less than T_C .

36. $I_{C(sat)} = \frac{24 \text{ V}}{330 \Omega + 100 \Omega} = \frac{24 \text{ V}}{430 \Omega} = 55.8 \text{ mA}$

$$V_{CE(cutoff)} = 24 \text{ V}$$

$$V_{BQ} = \left(\frac{1.0 \text{ k}\Omega}{1.0 \text{ k}\Omega + 4.7 \text{ k}\Omega} \right) 24 \text{ V} = 4.21 \text{ V}$$

$$V_{EQ} = 4.21 \text{ V} - 0.7 \text{ V} = 3.51 \text{ V}$$

$$I_{EQ} \cong I_{CQ} = \frac{3.51 \text{ V}}{100 \Omega} = 35.1 \text{ mA}$$

$$R_c = 330 \Omega \parallel 330 \Omega = 165 \Omega$$

$$V_{CQ} = 24 \text{ V} - (35.1 \text{ mA})(330 \Omega) = 12.4 \text{ V}$$

$$V_{CEQ} = 12.4 \text{ V} - 3.51 \text{ V} = 8.90 \text{ V}$$

$$I_{c(sat)} = 35.1 \text{ mA} + \frac{8.90 \text{ V}}{165 \Omega} = 89.1 \text{ mA}$$

$$V_{ce(cutoff)} = 8.90 \text{ V} + (35.1 \text{ mA})(165 \Omega) = 14.7 \text{ V}$$

See Figure 7-4.

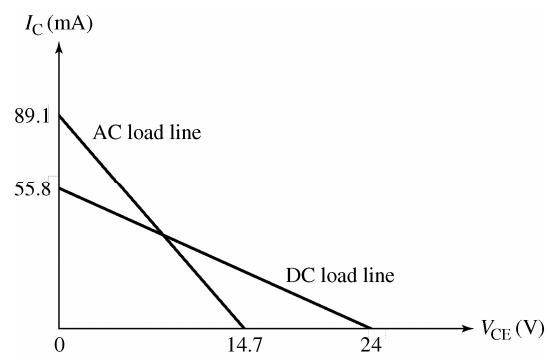


Figure 7-4

37. See Figure 7-5.

$$I_{R1} \cong I_{R2} = \frac{15 \text{ V}}{86 \Omega} = 174 \text{ mA}$$

$$V_B \cong \left(\frac{18 \Omega}{86 \Omega} \right) 15 \text{ V} = 3.14 \text{ V}$$

$$V_E = 3.14 \text{ V} - 0.7 \text{ V} = 2.44 \text{ V}$$

$$I_E \cong I_C = \frac{2.44 \text{ V}}{4.85 \Omega} = 503 \text{ mA}$$

$$V_C = 15 \text{ V} - (10 \Omega)(503 \text{ mA}) = 9.97 \text{ V}$$

$$V_{CE} = 7.53 \text{ V}$$

$$r'_e = \frac{25 \text{ mV}}{503 \text{ mA}} = 0.05 \Omega$$

The ac resistance affecting the load line is

$$R_c + R_e + r'_e = 10 \Omega$$

$$\beta_{ac} = \beta_{DC} \geq 100$$

$$I_{c(sat)} = 503 \text{ mA} + \frac{7.53 \text{ V}}{10.2 \Omega} = 1.24 \text{ A}$$

$$V_{ce(cutoff)} = 7.53 \text{ V} + (503 \text{ mA})(10.2 \Omega) = 12.7 \text{ V}$$

The Q -point is closer to cutoff so

$$P_{out} = (0.5)(503 \text{ mA})^2(10.2 \Omega) = 1.29 \text{ W}$$

As loading occurs, the Q -point will still be closer to cutoff. The circuit will have

$P_{out} \geq 1 \text{ W}$ for $R_L \geq 37.7 \Omega$. (39 Ω standard)

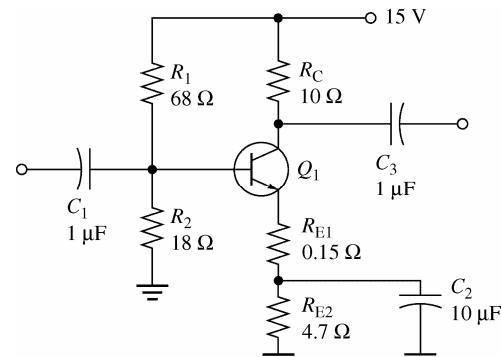


Figure 7-5

- 38.** Preamp quiescent current:

$$I_1 = I_2 = \frac{30 \text{ V}}{660 \text{ k}\Omega} = 45 \mu\text{A}$$

$$I_3 = I_4 = I_5 = \frac{15 \text{ V} - 0.7 \text{ V}}{34 \text{ k}\Omega} = 421 \mu\text{A}$$

$$I_6 = I_7 = \frac{30 \text{ V}}{69 \text{ k}\Omega} = 435 \mu\text{A}$$

$$V_{B2} = 15 \text{ V} - (435 \mu\text{A})(47 \text{ k}\Omega) = -5.45 \text{ V}$$

$$I_8 = I_9 = I_{10} = \frac{-15 \text{ V} - (-5.45 \text{ V} - 0.7 \text{ V})}{5.13 \text{ k}\Omega} = 1.73 \text{ mA}$$

$$I_{tot} = 45 \mu\text{A} + 421 \mu\text{A} + 435 \mu\text{A} + 1.73 \text{ mA} = 2.63 \text{ mA}$$

Power amp quiescent current:

$$I_{11} \approx 0$$

$$I_{12} = \frac{15.7 \text{ V} - 3(0.7 \text{ V})}{1.0 \text{ k}\Omega} = \frac{13.6 \text{ V}}{1.0 \text{ k}\Omega} = 13.6 \text{ mA}$$

$$I_{13} = \frac{-15 \text{ V} - (-0.7 \text{ V})}{220 \Omega} = \frac{-14.3 \text{ V}}{220 \Omega} = 65 \text{ mA}$$

$$I_{tot} = 13.6 \text{ mA} + 65 \text{ mA} = 78.6 \text{ mA}$$

Signal current to load:

Scope shows $\approx 9.8 \text{ V}$ peak output.

$$I_L = \frac{0.707(9.8 \text{ V})}{8 \Omega} = 866 \text{ mA}$$

$$I_{tot(sys)} = 2.63 \text{ mA} + 78.6 \text{ mA} + 866 \text{ mA} = 947 \text{ mA}$$

$$\text{Amp.} \times \text{hrs} = 947 \text{ mA} \times 4 \text{ hrs} = 3.79 \text{ Ah}$$

Multisim Troubleshooting Problems

The solutions showing instrument connections for Problems 39 through 43 are available from the Instructor Resource Center. See Chapter 1 for instructions. The faults in the circuit files may be accessed using the password *book* (all lowercase).

- 39.** C_{in} open

- 40.** R_{E2} open

- 41.** Q_1 collector-emitter open

- 42.** D_2 shorted

- 43.** Q_2 drain-source open

Chapter 8

Field-Effect Transistors (FETs)

Section 8-1 The JFET

1. (a) A greater V_{GS} **narrow**s the depletion region.
(b) The channel resistance **increas**e with increased V_{GS} .
2. The gate-to-source voltage of an *n*-channel JFET must be zero or negative in order to maintain the required reverse-bias condition.
3. See Figure 8-1.

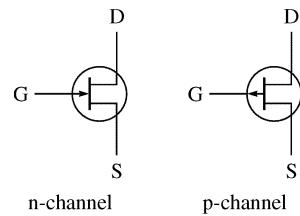


Figure 8-1

4. See Figure 8-2.

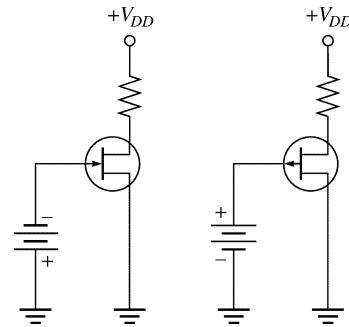


Figure 8-2

Section 8-2 JFET Characteristics and Parameters

5. $V_{DS} = V_P = 5 \text{ V}$ at point where I_D becomes constant.
6. $V_{GS(\text{off})} = -V_P = -6 \text{ V}$
The device is **on**, because $V_{GS} = -2 \text{ V}$.
7. By definition, $I_D = I_{DSS}$ when $V_{GS} = 0 \text{ V}$ for values of $V_{DS} > V_P$.
Therefore, $I_D = 10 \text{ mA}$.
8. Since $V_{GS} > V_{GS(\text{off})}$, the JFET is off and $I_D = 0 \text{ A}$.

9. $V_P = -V_{GS(\text{off})} = -(-4 \text{ V}) = 4 \text{ V}$

The voltmeter reads V_{DS} . As V_{DD} is increased, V_{DS} also increases. The point at which I_D reaches a constant value is $V_{DS} = V_P = 4 \text{ V}$.

10. $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}}\right)^2$

$$I_D = 5 \text{ mA} \left(1 - \frac{0 \text{ V}}{-8 \text{ V}}\right)^2 = 5 \text{ mA}$$

$$I_D = 5 \text{ mA} \left(1 - \frac{-1 \text{ V}}{-8 \text{ V}}\right)^2 = 3.83 \text{ mA}$$

$$I_D = 5 \text{ mA} \left(1 - \frac{-2 \text{ V}}{-8 \text{ V}}\right)^2 = 2.81 \text{ mA}$$

$$I_D = 5 \text{ mA} \left(1 - \frac{-3 \text{ V}}{-8 \text{ V}}\right)^2 = 1.95 \text{ mA}$$

$$I_D = 5 \text{ mA} \left(1 - \frac{-4 \text{ V}}{-8 \text{ V}}\right)^2 = 1.25 \text{ mA}$$

$$I_D = 5 \text{ mA} \left(1 - \frac{-5 \text{ V}}{-8 \text{ V}}\right)^2 = 0.703 \text{ mA}$$

$$I_D = 5 \text{ mA} \left(1 - \frac{-6 \text{ V}}{-8 \text{ V}}\right)^2 = 0.313 \text{ mA}$$

$$I_D = 5 \text{ mA} \left(1 - \frac{-7 \text{ V}}{-8 \text{ V}}\right)^2 = 0.078 \text{ mA}$$

$$I_D = 5 \text{ mA} \left(1 - \frac{-8 \text{ V}}{-8 \text{ V}}\right)^2 = 0 \text{ mA}$$

See Figure 8-3.

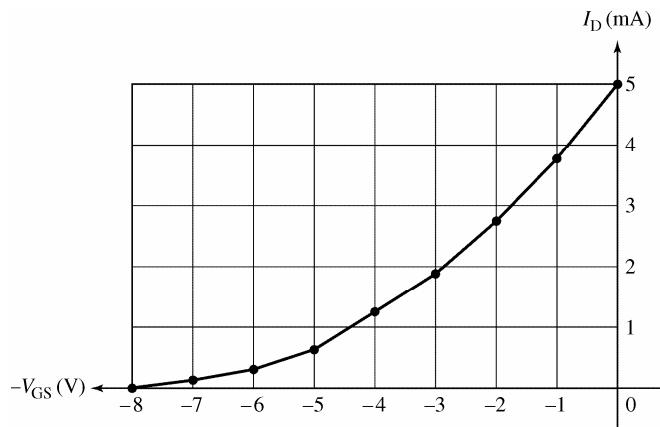


Figure 8-3

Chapter 8

11. $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$

$$1 - \frac{V_{GS}}{V_{GS(off)}} = \sqrt{\frac{I_D}{I_{DSS}}}$$

$$\frac{V_{GS}}{V_{GS(off)}} = 1 - \sqrt{\frac{I_D}{I_{DSS}}}$$

$$V_{GS} = V_{GS(off)} \left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$V_{GS} = -8 \text{ V} \left(1 - \sqrt{\frac{2.25 \text{ mA}}{5 \text{ mA}}}\right) = -8 \text{ V}(0.329) = \mathbf{-2.63 \text{ V}}$$

12. $g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) = 3200 \mu\text{S} \left(1 - \frac{-4 \text{ V}}{-8 \text{ V}}\right) = \mathbf{1600 \mu\text{S}}$

13. $g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) = 2000 \mu\text{S} \left(1 - \frac{-2 \text{ V}}{-7 \text{ V}}\right) = \mathbf{1429 \mu\text{S}}$

$$g_{fs} = g_m = \mathbf{1429 \mu\text{S}}$$

14. $R_{IN} = \frac{V_{GS}}{I_{GSS}} = \frac{10 \text{ V}}{5 \text{ nA}} = \mathbf{2000 \text{ M}\Omega}$

15. $V_{GS} = 0 \text{ V}: I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = 8 \text{ mA}(1 - 0)^2 = \mathbf{8 \text{ mA}}$

$$V_{GS} = -1 \text{ V}: I_D = 8 \text{ mA} \left(1 - \frac{-1 \text{ V}}{-5 \text{ V}}\right)^2 = 8 \text{ mA}(1 - 0.2)^2 = 8 \text{ mA}(0.8)^2 = \mathbf{5.12 \text{ mA}}$$

$$V_{GS} = -2 \text{ V}: I_D = 8 \text{ mA} \left(1 - \frac{-2 \text{ V}}{-5 \text{ V}}\right)^2 = 8 \text{ mA}(1 - 0.4)^2 = 8 \text{ mA}(0.6)^2 = \mathbf{2.88 \text{ mA}}$$

$$V_{GS} = -3 \text{ V}: I_D = 8 \text{ mA} \left(1 - \frac{-3 \text{ V}}{-5 \text{ V}}\right)^2 = 8 \text{ mA}(1 - 0.6)^2 = 8 \text{ mA}(0.4)^2 = \mathbf{1.28 \text{ mA}}$$

$$V_{GS} = -4 \text{ V}: I_D = 8 \text{ mA} \left(1 - \frac{-4 \text{ V}}{-5 \text{ V}}\right)^2 = 8 \text{ mA}(1 - 0.8)^2 = 8 \text{ mA}(0.2)^2 = \mathbf{0.320 \text{ mA}}$$

$$V_{GS} = -5 \text{ V}: I_D = 8 \text{ mA} \left(1 - \frac{-5 \text{ V}}{-5 \text{ V}}\right)^2 = 8 \text{ mA}(1 - 1)^2 = 8 \text{ mA}(0)^2 = \mathbf{0 \text{ mA}}$$

Section 8-3 JFET Biasing

16. $V_{GS} = -I_D R_S = -(12 \text{ mA})(100 \Omega) = -1.2 \text{ V}$

17. $R_S = \left| \frac{V_{GS}}{I_D} \right| = \left| \frac{-4 \text{ V}}{5 \text{ mA}} \right| = 800 \Omega$

18. $R_S = \left| \frac{V_{GS}}{I_D} \right| = \left| \frac{-3 \text{ V}}{2.5 \text{ mA}} \right| = 1.2 \text{ k}\Omega$

19. (a) $I_D = I_{DSS} = 20 \text{ mA}$
 (b) $I_D = 0 \text{ A}$
 (c) I_D increases

<p>20. (a) $V_S = (1 \text{ mA})(1.0 \text{ k}\Omega) = 1 \text{ V}$ $V_D = 12 \text{ V} - (1 \text{ mA})(4.7 \text{ k}\Omega) = 7.3 \text{ V}$ $V_G = 0 \text{ V}$ $V_{GS} = V_G - V_S = 0 \text{ V} - 1 \text{ V} = -1 \text{ V}$ $V_{DS} = 7.3 \text{ V} - 1 \text{ V} = 6.3 \text{ V}$</p> <p>(c) $V_S = (-3 \text{ mA})(470 \Omega) = -1.41 \text{ V}$ $V_D = -15 \text{ V} - (3 \text{ mA})(2.2 \text{ k}\Omega) = -8.4 \text{ V}$ $V_G = 0 \text{ V}$ $V_{GS} = V_G - V_S = 0 \text{ V} - (-1.41 \text{ V}) = 1.41 \text{ V}$ $V_{DS} = -8.4 \text{ V} - (-1.41 \text{ V}) = -6.99 \text{ V}$</p>	<p>(b) $V_S = (5 \text{ mA})(100 \Omega) = 0.5 \text{ V}$ $V_D = 9 \text{ V} - (5 \text{ mA})(470 \Omega) = 6.65 \text{ V}$ $V_G = 0 \text{ V}$ $V_{GS} = V_G - V_S = 0 \text{ V} - 0.5 \text{ V} = -0.5 \text{ V}$ $V_{DS} = 6.65 \text{ V} - 0.5 \text{ V} = 6.15 \text{ V}$</p>
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21. From the graph, $V_{GS} \approx -2 \text{ V}$ at $I_D = 9.5 \text{ mA}$.

$$R_S = \left| \frac{V_{GS}}{I_D} \right| = \left| \frac{-2 \text{ V}}{9.5 \text{ mA}} \right| = 211 \Omega$$

22. $I_D = \frac{I_{DSS}}{2} = \frac{14 \text{ mA}}{2} = 7 \text{ mA}$
 $V_{GS(\text{off})} = \frac{V_{GS(\text{off})}}{3.414} = \frac{-10 \text{ V}}{3.414} = -2.93 \text{ V}$
 $R_S = \left| \frac{V_{GS}}{I_D} \right| = \left| \frac{2.93 \text{ V}}{7 \text{ mA}} \right| = 419 \Omega$ (The nearest standard value is 430Ω).
 $R_D = \frac{V_{DD} - V_D}{I_D} = \frac{24 \text{ V} - 12 \text{ V}}{7 \text{ mA}} = 1.7 \text{ k}\Omega$ (The nearest standard value is $1.8 \text{ k}\Omega$.)

Select $R_G = 1.0 \text{ M}\Omega$. See Figure 8-4.

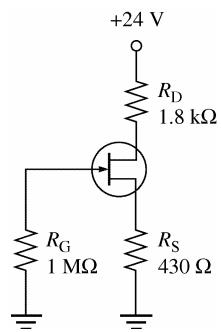


Figure 8-4

Chapter 8

23. $R_{IN(\text{total})} = R_G \parallel R_{IN}$

$$R_{IN} = \left| \frac{V_{GS}}{I_{GSS}} \right| = \left| \frac{-10 \text{ V}}{20 \text{ nA}} \right| = 500 \text{ M}\Omega$$
$$R_{IN(\text{total})} = 10 \text{ M}\Omega \parallel 500 \text{ M}\Omega = 9.8 \text{ M}\Omega$$

24. For $I_D = 0$,
 $V_{GS} = -I_D R_S = (0)(330 \text{ }\Omega) = 0 \text{ V}$
For $I_D = I_{DSS} = 5 \text{ mA}$
 $V_{GS} = -I_D R_S = -(5 \text{ mA})(330 \text{ }\Omega) = -1.65 \text{ V}$
From the graph in Figure 8-69 in the textbook, the Q -point is
 $V_{GS} \cong -0.95 \text{ V}$ and $I_D \cong 2.9 \text{ mA}$

25. For $I_D = 0$,
 $V_{GS} = 0 \text{ V}$
For $I_D = I_{DSS} = 10 \text{ mA}$,
 $V_{GS} = -I_D R_S = (10 \text{ mA})(390 \text{ }\Omega) = 3.9 \text{ V}$
From the graph in Figure 8-70 in the textbook, the Q -point is
 $V_{GS} \cong 2.1 \text{ V}$ and $I_D \cong 5.3 \text{ mA}$

26. Since $V_{R_D} = 9 \text{ V} - 5 \text{ V} = 4 \text{ V}$,
- $$I_D = \frac{V_{R_D}}{R_D} = \frac{4 \text{ V}}{4.7 \text{ k}\Omega} = 0.85 \text{ mA}$$
- $$V_S = I_D R_S = (0.85 \text{ mA})(3.3 \text{ k}\Omega) = 2.81 \text{ V}$$
- $$V_G = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD} = \left(\frac{2.2 \text{ M}\Omega}{12.2 \text{ M}\Omega} \right) 9 \text{ V} = 1.62 \text{ V}$$
- $$V_{GS} = V_G - V_S = 1.62 \text{ V} - 2.81 \text{ V} = -1.19 \text{ V}$$
- Q -point: $I_D = 0.85 \text{ mA}$, $V_{GS} = -1.19 \text{ V}$

27. For $I_D = 0$,
- $$V_{GS} = V_G = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD} = \left(\frac{2.2 \text{ M}\Omega}{5.5 \text{ M}\Omega} \right) 12 \text{ V} = 4.8 \text{ V}$$
- For $V_{GS} = 0 \text{ V}$, $V_S = 4.8 \text{ V}$
- $$I_D = \frac{V_S}{R_S} = \frac{|V_G - V_{GS}|}{R_S} = \frac{4.8 \text{ V}}{3.3 \text{ k}\Omega} = 1.45 \text{ mA}$$
- The Q -point is taken from the graph in Figure 8-72 in the textbook.
 $I_D \cong 1.9 \text{ mA}$, $V_{GS} = -1.5 \text{ V}$

Section 8-4 The Ohmic Region

28. $R_{DS} = \frac{V_{DS}}{I_D} = \frac{0.8 \text{ V}}{0.20 \text{ mA}} = 4 \text{ k}\Omega$

29. $R_{DS1} = \frac{0.4 \text{ V}}{0.15 \text{ mA}} = 2.67 \text{ k}\Omega$

$$R_{DS2} = \frac{0.6 \text{ V}}{0.45 \text{ mA}} = 1.33 \text{ k}\Omega$$

$$\Delta R_{DS} = 2.67 \text{ k}\Omega - 1.33 \text{ k}\Omega = \mathbf{1.34 \text{ k}\Omega}$$

30.
$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}}\right) = 1.5 \text{ mS} \left(1 - \frac{-1 \text{ V}}{-3.5 \text{ V}}\right)$$

$$= 1.5 \text{ mS}(0.714) = \mathbf{1.07 \text{ mS}}$$

31. $r_{ds} = \frac{1}{g_m} = \frac{1}{1.07 \text{ mS}} = \mathbf{935 \Omega}$

Section 8-5 The MOSFET

32. See Figure 8-5.

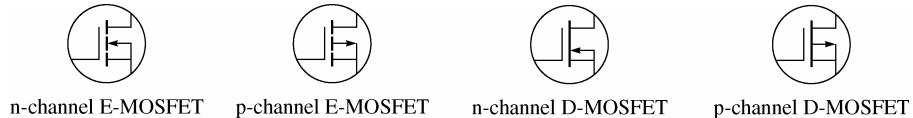


Figure 8-5

33. An *n*-channel D-MOSFET with a positive V_{GS} is operating in the **enhancement mode**.
34. An E-MOSFET has no physical channel or depletion mode. A D-MOSFET has a physical channel and can be operated in either depletion or enhancement modes.
35. MOSFETs have a very high input resistance because the gate is insulated from the channel by an SiO_2 layer.

Section 8-6 MOSFET Characteristics and Parameters

36. $K = \frac{I_{D(\text{on})}}{(V_{GS} - V_{GS(\text{th})})^2} = \frac{10 \text{ mA}}{(-12 \text{ V} + 3 \text{ V})^2} = 0.12 \text{ mA/V}^2$

$$I_D = K(V_{GS} - V_{GS(\text{off})})^2 = (0.12 \text{ mA/V}^2)(-6 \text{ V} + 3 \text{ V})^2 = \mathbf{1.08 \text{ mA}}$$

37. $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}}\right)^2$

$$I_{DSS} = \frac{I_D}{\left(1 - \frac{V_{GS}}{V_{GS(\text{off})}}\right)^2} = \frac{3 \text{ mA}}{\left(1 - \frac{-2 \text{ V}}{-10 \text{ V}}\right)^2} = \mathbf{4.69 \text{ mA}}$$

Chapter 8

38. (a) *n* channel

$$(b) \quad I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2$$

$$I_D = 8 \text{ mA} \left(1 - \frac{-4 \text{ V}}{-5 \text{ V}} \right)^2 = \mathbf{0.32 \text{ mA}}$$

$$I_D = 8 \text{ mA} \left(1 - \frac{-2 \text{ V}}{-5 \text{ V}} \right)^2 = \mathbf{2.88 \text{ mA}}$$

$$I_D = 8 \text{ mA} \left(1 - \frac{0 \text{ V}}{-5 \text{ V}} \right)^2 = \mathbf{8 \text{ mA}}$$

$$I_D = 8 \text{ mA} \left(1 - \frac{2 \text{ V}}{-5 \text{ V}} \right)^2 = \mathbf{15.7 \text{ mA}}$$

$$I_D = 8 \text{ mA} \left(1 - \frac{4 \text{ V}}{-5 \text{ V}} \right)^2 = \mathbf{25.9 \text{ mA}}$$

$$I_D = 8 \text{ mA} \left(1 - \frac{-5 \text{ V}}{-5 \text{ V}} \right)^2 = \mathbf{0 \text{ mA}}$$

$$I_D = 8 \text{ mA} \left(1 - \frac{-3 \text{ V}}{-5 \text{ V}} \right)^2 = \mathbf{1.28 \text{ mA}}$$

$$I_D = 8 \text{ mA} \left(1 - \frac{-1 \text{ V}}{-5 \text{ V}} \right)^2 = \mathbf{5.12 \text{ mA}}$$

$$I_D = 8 \text{ mA} \left(1 - \frac{1 \text{ V}}{-5 \text{ V}} \right)^2 = \mathbf{11.5 \text{ mA}}$$

$$I_D = 8 \text{ mA} \left(1 - \frac{3 \text{ V}}{-5 \text{ V}} \right)^2 = \mathbf{20.5 \text{ mA}}$$

$$I_D = 8 \text{ mA} \left(1 - \frac{5 \text{ V}}{-5 \text{ V}} \right)^2 = \mathbf{32 \text{ mA}}$$

(c) See Figure 8-6.

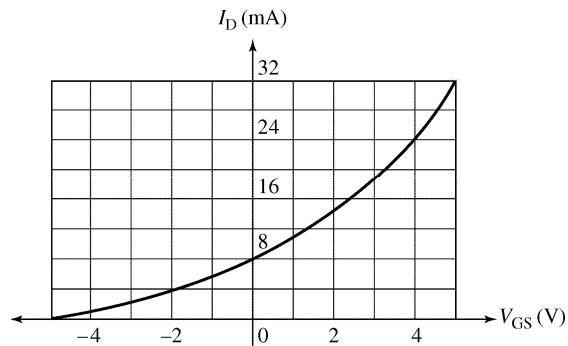


Figure 8-6

Section 8-7 MOSFET Biasing

- 39.** (a) Depletion
 (b) Enhancement
 (c) Zero bias
 (d) Depletion

40. (a) $V_{GS} = \left(\frac{10 \text{ M}\Omega}{14.7 \text{ M}\Omega} \right) 10 \text{ V} = 6.8 \text{ V}$ This MOSFET is **on**.

(b) $V_{GS} = \left(\frac{1.0 \text{ M}\Omega}{11 \text{ M}\Omega} \right) (-25 \text{ V}) = -2.27 \text{ V}$ This MOSFET is **off**.

- 41.** Since $V_{GS} = 0 \text{ V}$ for each circuit, $I_D = I_{DSS} = 8 \text{ mA}$.

- (a) $V_{DS} = V_{DD} - I_D R_D = 12 \text{ V} - (8 \text{ mA})(1.0 \text{ k}\Omega) = 4 \text{ V}$
 (b) $V_{DS} = V_{DD} - I_D R_D = 15 \text{ V} - (8 \text{ mA})(1.2 \text{ k}\Omega) = 5.4 \text{ V}$
 (c) $V_{DS} = V_{DD} - I_D R_D = -9 \text{ V} - (-8 \text{ mA})(560 \Omega) = -4.52 \text{ V}$

- 42.** (a) $I_{D(on)} = 3 \text{ mA} @ 4 \text{ V}, V_{GS(th)} = 2 \text{ V}$

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD} = \left(\frac{4.7 \text{ M}\Omega}{14.7 \text{ M}\Omega} \right) 10 \text{ V} = 3.2 \text{ V}$$

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{3 \text{ mA}}{(4 \text{ V} - 2 \text{ V})^2} = \frac{3 \text{ mA}}{(2 \text{ V})^2} = 0.75 \text{ mA/V}^2$$

$$I_D = K(V_{GS} - V_{GS(th)})^2 = (0.75 \text{ mA/V}^2)(3.2 \text{ V} - 2 \text{ V})^2 = 1.08 \text{ mA}$$

$$V_{DS} = V_{DD} - I_D R_D = 10 \text{ V} - (1.08 \text{ mA})(1.0 \text{ k}\Omega) = 10 \text{ V} - 1.08 \text{ V} = 8.92 \text{ V}$$

- (b) $I_{D(on)} = 2 \text{ mA} @ 3 \text{ V}, V_{GS(th)} = 1.5 \text{ V}$

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD} = \left(\frac{10 \text{ M}\Omega}{20 \text{ M}\Omega} \right) 5 \text{ V} = 2.5 \text{ V}$$

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{2 \text{ mA}}{(3 \text{ V} - 1.5 \text{ V})^2} = \frac{2 \text{ mA}}{(1.5 \text{ V})^2} = 0.89 \text{ mA/V}^2$$

$$I_D = K(V_{GS} - V_{GS(th)})^2 = (0.89 \text{ mA/V}^2)(2.5 \text{ V} - 1.5 \text{ V})^2 = 0.89 \text{ mA}$$

$$V_{DS} = V_{DD} - I_D R_D = 5 \text{ V} - (0.89 \text{ mA})(1.5 \text{ k}\Omega) = 5 \text{ V} - 1.34 \text{ V} = 3.66 \text{ V}$$

- 43.** (a) $V_{DS} = V_{GS} = 5 \text{ V}$

$$I_D = \frac{V_{DD} - V_{DS}}{R_D} = \frac{12 \text{ V} - 5 \text{ V}}{2.2 \text{ k}\Omega} = 3.18 \text{ mA}$$

- (b) $V_{DS} = V_{GS} = 3.2 \text{ V}$

$$I_D = \frac{V_{DD} - V_{DS}}{R_D} = \frac{8 \text{ V} - 3.2 \text{ V}}{4.7 \text{ k}\Omega} = 1.02 \text{ mA}$$

- 44.** $V_{DS} = V_{DD} - I_D R_D = 15 \text{ V} - (1 \text{ mA})(8.2 \text{ k}\Omega) = 6.8 \text{ V}$

$$V_{GS} = V_{DS} - I_G R_G = 6.8 \text{ V} - (50 \text{ pA})(22 \text{ M}\Omega) = 6.799 \text{ V}$$

Chapter 8

Section 8-8 The IGBT

- 45. The input resistance of an IGBT is very high because of the insulated gate structure.
- 46. With excessive collector current, the parasitic transistor turns on and the IGBT acts as a thyristor.

Section 8-9 Troubleshooting

- 47. When I_D goes to zero, the possible faults are:
 R_D or R_S open, JFET drain-to-source open, no supply voltage, or ground connection open.
- 48. If I_D goes to 16 mA, the possible faults are:
The JFET is shorted from drain-to-source or V_{DD} has increased.
- 49. If V_{DD} is changed to -20 V, I_D will change very little or none because the device is operating in the constant-current region of the characteristic curve.
- 50. The device is off. The gate bias voltage must be less than $V_{GS(th)}$. The gate could be shorted or partially shorted to ground.
- 51. The device is saturated, so there is very little voltage from drain-to-source. This indicates that V_{GS} is too high. The 1.0 MΩ bias resistor is probably **open**.

Application Activity Problems

- 52. (a) -500 mV
(b) -200 mV
(c) 0 mV
(d) 400 mV
- 53. At $V_{G2S} = 6$ V, $I_D \approx 10$ mA
At $V_{G2S} = 1$ V, $I_D \approx 5$ mA
- 54. $V_{GS1} = V_{\text{sensor}} = -400$ mV
 $V_{\text{OUT}} = 9.048$ V
 $I_D = \frac{V_{DD} - V_{\text{OUT}}}{R_3 + R_4} = \frac{12 \text{ V} - 9.048 \text{ V}}{1120 \Omega} = \mathbf{2.64 \text{ mA}}$

 $V_{GS1} = V_{\text{sensor}} = -300$ mV
 $V_{\text{OUT}} = 7.574$ V
 $I_D = \frac{12 \text{ V} - 7.574 \text{ V}}{1120 \Omega} = \mathbf{3.95 \text{ mA}}$

 $V_{GS1} = V_{\text{sensor}} = -200$ mV
 $V_{\text{OUT}} = 5.930$ V
 $I_D = \frac{12 \text{ V} - 5.930 \text{ V}}{1120 \Omega} = \mathbf{5.42 \text{ mA}}$

$$V_{GS1} = V_{\text{sensor}} = -100 \text{ mV}$$

$$V_{\text{OUT}} = 4.890 \text{ V}$$

$$I_D = \frac{12 \text{ V} - 4.890 \text{ V}}{1120 \Omega} = \mathbf{6.35 \text{ mA}}$$

$$V_{GS1} = V_{\text{sensor}} = 0 \text{ mV}$$

$$V_{\text{OUT}} = 4.197 \text{ V}$$

$$I_D = \frac{12 \text{ V} - 4.197 \text{ V}}{1120 \Omega} = \mathbf{6.97 \text{ mA}}$$

$$V_{GS1} = V_{\text{sensor}} = 100 \text{ mV}$$

$$V_{\text{OUT}} = 3.562 \text{ V}$$

$$I_D = \frac{12 \text{ V} - 3.562 \text{ V}}{1120 \Omega} = \mathbf{7.53 \text{ mA}}$$

$$V_{GS1} = V_{\text{sensor}} = 200 \text{ mV}$$

$$V_{\text{OUT}} = 2.960 \text{ V}$$

$$I_D = \frac{12 \text{ V} - 2.960 \text{ V}}{1120 \Omega} = \mathbf{8.07 \text{ mA}}$$

$$V_{GS1} = V_{\text{sensor}} = 300 \text{ mV}$$

$$V_{\text{OUT}} = 2.382 \text{ V}$$

$$I_D = \frac{12 \text{ V} - 2.382 \text{ V}}{1120 \Omega} = \mathbf{8.59 \text{ mA}}$$

See Figure 8-7.

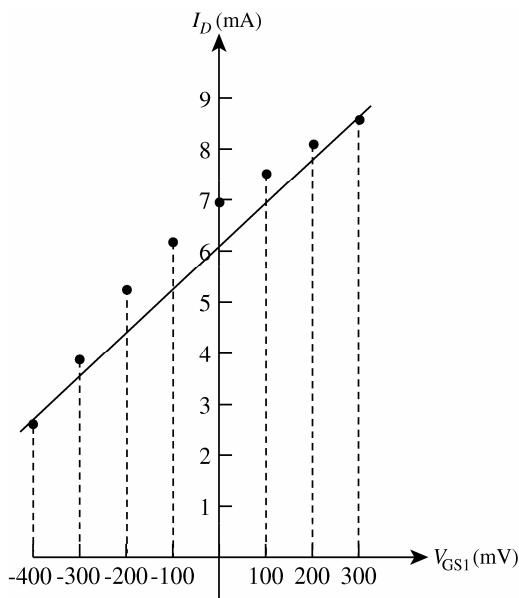


Figure 8-7

55.
$$V_{GS2} = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD} = \left(\frac{50 \text{ k}\Omega}{150 \text{ k}\Omega} \right) 12 \text{ V} = 4 \text{ V}$$

From the graph in Figure 8-79 in the textbook for $V_{G1S} = 0$ and $V_{G2S} = 4 \text{ V}$:

$$I_D \approx 8 \text{ mA}$$

$$V_{\text{OUT}} = 12 \text{ V} - (8 \text{ mA})(1120 \Omega) = \mathbf{3.04 \text{ V}}$$

Chapter 8

Datasheet Problems

56. The 2N5457 is an **n-channel JFET**.
57. From the datasheet in textbook Figure 8-14:
- (a) For a 2N5457, $V_{GS(off)} = -0.5 \text{ V}$ minimum
 - (b) For a 2N5457, $V_{DS(max)} = 25 \text{ V}$
 - (c) For a 2N5458 @ 25°C , $P_{D(max)} = 310 \text{ mW}$
 - (d) For a 2N5459, $V_{GS(rev)} = -25 \text{ V}$ maximum
58. $P_{D(max)} = 310 \text{ mW} - (2.82 \text{ mW}/\text{C})(65^\circ\text{C} - 25^\circ\text{C}) = 310 \text{ mW} - 113 \text{ mW} = 197 \text{ mW}$
59. $g_{m0(min)} = g_{fs} = 2000 \mu\text{s}$
60. Typical $I_D = I_{DSS} = 9 \text{ mA}$
61. From the datasheet graph in textbook Figure 8-80:
 $I_D \cong 1.4 \text{ mA}$ at $V_{GS} = 0$
62. For a 2N3796 with $V_{GS} = 6 \text{ V}$, $I_D = 15 \text{ mA}$
63. From the datasheet graph in textbook Figure 8-80:
At $V_{GS} = +3 \text{ V}$, $I_D \cong 13 \text{ mA}$
At $V_{GS} = -2 \text{ V}$, $I_D \cong 0.4 \text{ mA}$
64. $y_{fs} = 1500 \mu\text{s}$ at $f = 1 \text{ kHz}$ and at $f = 1 \text{ MHz}$ for both the 2N3796 and 2N3797.
There is **no change** in g_{fs} over the frequency range.
65. For a 2N3796, $V_{GS(off)} = -3.0 \text{ V}$ typical

Advanced Problems

66. For the circuit of textbook Figure 8-81:
- $$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2 \quad \text{where } V_{GS} = I_D R_S$$
- From the 2N5457 datasheet:
 $I_{DSS(min)} = 1.0 \text{ mA}$ and $V_{GS(off)} = -0.5 \text{ V}$ minimum
 $I_D = 66.3 \mu\text{A}$
 $V_{GS} = -(66.3 \mu\text{A})(5.6 \text{ k}\Omega) = -0.371 \text{ V}$
 $V_{DS} = 12 \text{ V} - (66.3 \mu\text{A})(10 \text{ k}\Omega + 5.6 \text{ k}\Omega) = 11.0 \text{ V}$

- 67.** For the circuit of textbook Figure 8-82:

$$V_C = \left(\frac{3.3 \text{ k}\Omega}{13.3 \text{ k}\Omega} \right) 9 \text{ V} = (0.248)(9 \text{ V}) = 2.23 \text{ V}$$

From the equation,

$$I_D = I_{DSS} \left(\frac{V_{GS}}{1 - V_{GS(\text{off})}} \right)^2 \text{ where } V_{GS} = V_G - I_D R_S$$

I_D is maximum for $I_{DSS(\text{max})}$ and $V_{GS(\text{off})}$ max, so that

$I_{DSS} = 16 \text{ mA}$ and $V_{GS(\text{off})} = -8.0 \text{ V}$

$I_D = 3.58 \text{ mA}$

$$V_{GS} = 2.23 \text{ V} - (3.58 \text{ mA})(1.8 \text{ k}\Omega) = 2.23 \text{ V} - 6.45 \text{ V} = -4.21 \text{ V}$$

- 68.** From the 2N5457 datasheet:

$I_{DSS(\text{min})} = 1.0 \text{ mA}$ and $V_{GS(\text{off})} = -0.5 \text{ minimum}$

$I_{D(\text{min})} = 66.3 \mu\text{A}$

$$V_{DS(\text{max})} = 12 \text{ V} - (66.3 \mu\text{A})(15.6 \text{ k}\Omega) = 11.0 \text{ V}$$

and

$I_{DSS(\text{max})} = 5.0 \text{ mA}$ and $V_{GS(\text{off})} = -6.0 \text{ maximum}$

$I_{D(\text{max})} = 677 \mu\text{A}$

$$V_{DS(\text{min})} = 12 \text{ V} - (677 \mu\text{A})(15.6 \text{ k}\Omega) = 1.4 \text{ V}$$

- 69.** $V_{pH} = +300 \text{ mV}$

$$I_D = (2.9 \text{ mA})(1 + 0.3 \text{ V}/5.0 \text{ V})^2 = (2.9 \text{ mA})(1.06)^2 = 3.26 \text{ mA}$$

$$V_{DS} = 15 \text{ V} - (3.26 \text{ mA})(2.76 \text{ k}\Omega) = 15 \text{ V} - 8.99 \text{ V} = +6.01 \text{ V}$$

70. $1 \text{ mA} = I_{DSS} \left(1 - \frac{(1 \text{ mA})R_S}{V_{GS(\text{off})}} \right)^2$

$$1 \text{ mA} = 2.9 \text{ mA} \left(1 - \frac{(1 \text{ mA})R_S}{-0.5 \text{ V}} \right)^2$$

$$0.345 = \left(1 - \frac{(1 \text{ mA})R_S}{-0.5 \text{ V}} \right)^2$$

$$0.587 = 1 - \frac{(1 \text{ mA})R_S}{-0.5 \text{ V}}$$

$$0.413 = \frac{(1 \text{ mA})R_S}{-0.5 \text{ V}}$$

$$R_S = 2.06 \text{ k}\Omega$$

Use $R_S = 2.2 \text{ k}\Omega$.

Then $I_D = 963 \mu\text{A}$

$$V_{GS} = V_S = (963 \mu\text{A})(2.2 \text{ k}\Omega) = 2.19 \text{ V}$$

$$\text{So, } V_D = 2.19 \text{ V} + 4.5 \text{ V} = 6.62 \text{ V}$$

$$R_D = \frac{9 \text{ V} - 6.62 \text{ V}}{963 \mu\text{A}} = 2.47 \text{ k}\Omega$$

Use $R_D = 2.4 \text{ k}\Omega$.

$$\text{So, } V_{DS} = 9 \text{ V} - (963 \mu\text{A})(4.6 \text{ k}\Omega) = 4.57 \text{ V}$$

Chapter 8

71. Let $I_D = 20 \text{ mA}$.

$$R_D = \frac{4 \text{ V}}{20 \text{ mA}} = 200 \Omega$$

Let $V_S = 2 \text{ V}$.

$$R_S = \frac{2 \text{ V}}{20 \text{ mA}} = 100 \Omega$$

$$K = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{th})})^2} = \frac{500 \text{ mA}}{(10 \text{ V} - 1 \text{ V})^2} = 6.17 \text{ mA/V}^2$$

Let $I_D = 20 \text{ mA}$.

$$(V_{GS} - 1 \text{ V})^2 = \frac{20 \text{ V}}{6.17 \text{ mA/V}^2} = 3.24$$

$$V_{GS} - 1 \text{ V} = 1.8 \text{ V}$$

$$V_{GS} = 2.8 \text{ V}$$

$$V_G = V_S + 2.8 \text{ V} = 4.8 \text{ V}$$

For the voltage divider:

$$\frac{R_1}{R_2} = \frac{7.2 \text{ V}}{4.8 \text{ V}} = 1.5$$

Let $R_2 = 10 \text{ k}\Omega$.

$$R_1 = (1.5)(10 \text{ k}\Omega) = 15 \text{ k}\Omega$$

See Figure 8-8.

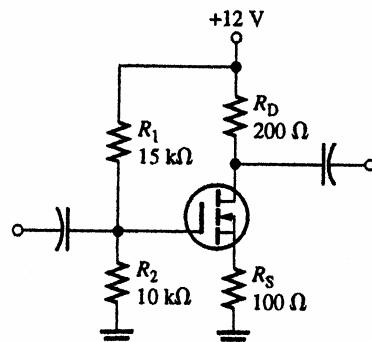


Figure 8-8

Multisim Troubleshooting Problems

The solutions showing instrument connections for Problems 72 through 80 are available from the Instructor Resource Center. See Chapter 1 for instructions. The faults in the circuit files may be accessed using the password *book* (all lowercase).

72. R_S shorted

73. R_D shorted

74. R_G shorted

75. R_1 open

76. Drain-source open

77. R_D open

78. R_2 shorted

79. Drain-source shorted

80. R_1 shorted

Chapter 9

FET Amplifiers and Switching Circuits

Section 9-1 The Common-Source Amplifier

1. (a) $I_d = g_m V_{gs} = (6000 \mu S)(10 \text{ mV}) = 60 \mu A$
 (b) $I_d = g_m V_{gs} = (6000 \mu S)(150 \text{ mV}) = 900 \mu A$
 (c) $I_d = g_m V_{gs} = (6000 \mu S)(0.6 \text{ V}) = 3.6 \text{ mA}$
 (d) $I_d = g_m V_{gs} = (6000 \mu S)(1 \text{ V}) = 6 \text{ mA}$

2. $A_v = g_m R_d$

$$R_d = \frac{A_v}{g_m} = \frac{20}{3500 \mu S} = 5.71 \text{ k}\Omega$$

3. $A_v = \left(\frac{R_D r'_{ds}}{R_D + r'_{ds}} \right) g_m = \left(\frac{(4.7 \text{ k}\Omega)(12 \text{ k}\Omega)}{16.7 \text{ k}\Omega} \right) 4.2 \text{ mS} = 14.2$

4. $R_d = R_D \parallel r'_{ds} = 4.7 \text{ k}\Omega \parallel 12 \text{ k}\Omega = 3.38 \text{ k}\Omega$

$$A_v = \frac{g_m R_d}{1 + g_m R_s} = \frac{(4.2 \text{ mS})(3.38 \text{ k}\Omega)}{1 + (4.2 \text{ mS})(1.0 \text{ k}\Omega)} = 2.73$$

5. (a) *N*-channel D-MOSFET with zero-bias.
 $V_{GS} = 0 \text{ V}$.
 (b) *P*-channel JFET with self-bias.
 $V_{GS} = -I_D R_S = (-3 \text{ mA})(330 \Omega) = -0.99 \text{ V}$
 (c) *N*-channel E-MOSFET with voltage-divider bias.

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD} = \left(\frac{4.7 \text{ k}\Omega}{14.7 \text{ k}\Omega} \right) 12 \text{ V} = 3.84 \text{ V}$$

6. (a) $V_G = 0 \text{ V}, \quad V_S = 0 \text{ V}$
 $V_D = V_{DD} - I_D R_D = 15 \text{ V} - (8 \text{ mA})(1.0 \text{ k}\Omega) = 7 \text{ V}$

- (b) $V_G = 0 \text{ V}$
 $V_S = -I_D R_D = -(3 \text{ mA})(330 \Omega) = -0.99 \text{ V}$
 $V_D = -V_{DD} + I_D R_D = -10 \text{ V} + (3 \text{ mA})(1.5 \text{ k}\Omega) = -5.5 \text{ V}$

(c) $V_G = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD} = \left(\frac{4.7 \text{ k}\Omega}{14.7 \text{ k}\Omega} \right) 12 \text{ V} = 3.84 \text{ V}$

$$V_S = 0 \text{ V}$$

 $V_D = V_{DD} - I_D R_D = 12 \text{ V} - (6 \text{ mA})(1.0 \text{ k}\Omega) = 6 \text{ V}$

Chapter 9

7. (a) *n*-channel D-MOSFET
 (b) *n*-channel JFET
 (c) *p*-channel E-MOSFET
8. From the curve in Figure 9-16(a) in the textbook:
 $I_{d(pp)} \cong 3.9 \text{ mA} - 1.3 \text{ mA} = \mathbf{2.6 \text{ mA}}$
9. From the curve in Figure 9-16(b) in the textbook:
 $I_{d(pp)} \cong 6 \text{ mA} - 2 \text{ mA} = \mathbf{4 \text{ mA}}$
 From the curve in Figure 9-16(c) in the textbook:
 $I_{d(pp)} \cong 4.5 \text{ mA} - 1.3 \text{ mA} = \mathbf{3.2 \text{ mA}}$
10. $V_D = V_{DD} - I_D R_D = 12 \text{ V} - (2.83 \text{ mA})(1.5 \text{ k}\Omega) = \mathbf{7.76 \text{ V}}$
 $V_S = I_D R_S = (2.83 \text{ mA})(1.0 \text{ k}\Omega) = \mathbf{2.83 \text{ V}}$
 $V_{DS} = V_D - V_S = 7.76 \text{ V} - 2.83 \text{ V} = \mathbf{4.93 \text{ V}}$
 $V_{GS} = V_G - V_S = 0 \text{ V} - 2.83 \text{ V} = \mathbf{-2.83 \text{ V}}$

11. $A_v = g_m R_d = g_m (R_D \parallel R_L) = 5000 \mu\text{S} (1.5 \text{ k}\Omega \parallel 10 \text{ k}\Omega) = 6.52$
 $V_{pp(out)} = (2.828)(50 \text{ mV})(6.52) = \mathbf{920 \text{ mV}}$

12. $A_v = g_m R_d$
 $R_d = 1.5 \text{ k}\Omega \parallel 1.5 \text{ k}\Omega = 750 \Omega$
 $A_v = (5000 \mu\text{S})(750 \Omega) = 3.75$
 $V_{out} = A_v V_{in} = (3.75)(50 \text{ mV}) = \mathbf{188 \text{ mV rms}}$

13. (a) $A_v = g_m R_d = g_m (R_D \parallel R_L) = 3.8 \text{ mS} (1.2 \text{ k}\Omega \parallel 22 \text{ k}\Omega) = 3.8 \text{ mS} (1138 \Omega) = \mathbf{4.32}$
 (b) $A_v = g_m R_d = g_m (R_D \parallel R_L) = 5.5 \text{ mS} (2.2 \text{ k}\Omega \parallel 10 \text{ k}\Omega) = 5.5 \text{ mS} (1.8 \text{ k}\Omega) = \mathbf{9.92}$

14. See Figure 9-1.

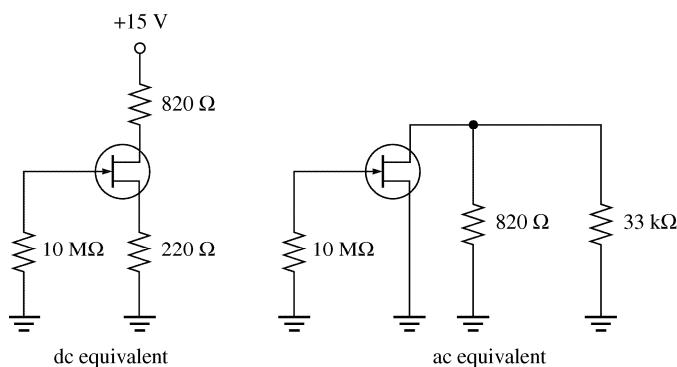


Figure 9-1

15. $I_D = \frac{I_{DSS}}{2} = \frac{15 \text{ mA}}{2} = \mathbf{7.5 \text{ mA}}$

16. $V_{GS} = (7.5 \text{ mA})(220 \Omega) = 1.65 \text{ V}$

$$g_{m0} = \frac{2I_{DSS}}{|V_{GS(\text{off})}|} = \frac{2(15 \text{ mA})}{4 \text{ V}} = 7.5 \text{ mS}$$

$$g_m = (7.5 \text{ mS})(1 - 1.65 \text{ V}/4 \text{ V}) = 4.41 \text{ mS}$$

$$A_v = \frac{g_m R_d}{1 + g_m R_S} = \frac{(4.41 \text{ mS})(820 \Omega \parallel 3.3 \text{ k}\Omega)}{1 + (4.41 \text{ mS})(220 \Omega)} = \frac{(4.41 \text{ mS})(657 \Omega)}{1 + 0.97} = \mathbf{1.47}$$

17. $A_v = g_m R_d = (4.41 \text{ mS})(820 \Omega \parallel 3.3 \text{ k}\Omega \parallel 4.7 \text{ k}\Omega) = (4.41 \text{ mS})(576 \Omega) = \mathbf{2.54}$

18. $I_D = \frac{I_{DSS}}{2} = \frac{9 \text{ mA}}{2} = \mathbf{4.5 \text{ mA}}$

$$V_{GS} = -I_D R_S = -(4.5 \text{ mA})(330 \Omega) = \mathbf{-1.49 \text{ V}}$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S) = 9 \text{ V} - (4.5 \text{ mA})(1.33 \text{ k}\Omega) = \mathbf{3 \text{ V}}$$

19. $A_v = g_m R_d = g_m (R_D \parallel R_L) = 3700 \mu\text{S} (1.0 \text{ k}\Omega \parallel 10 \text{ k}\Omega) = 3700 \mu\text{S} (909 \Omega) = 3.36$

$$V_{out} = A_v V_{in} = (3.36)(10 \text{ mV}) = \mathbf{33.6 \text{ mV rms}}$$

20. $V_{GS} = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD} = \left(\frac{6.8 \text{ k}\Omega}{24.8 \text{ k}\Omega} \right) 20 \text{ V} = \mathbf{5.48 \text{ V}}$

$$K = \frac{I_{D(\text{on})}}{(V_{GS} - V_{GS(\text{th})})^2} = \frac{18 \text{ mA}}{(10 \text{ V} - 2.5 \text{ V})^2} = 0.32 \text{ mA/V}^2$$

$$I_D = K(V_{GS} - V_{GS(\text{th})})^2 = 0.32 \text{ mA/V}^2 (5.48 \text{ V} - 2.5 \text{ V})^2 = \mathbf{2.84 \text{ mA}}$$

$$V_{DS} = V_{DD} - I_D R_D = 20 \text{ V} - (2.84 \text{ mA})(1.0 \text{ k}\Omega) = \mathbf{17.2 \text{ V}}$$

21. $R_{IN} = \left| \frac{V_{GS}}{I_{GSS}} \right| = \left| \frac{-15 \text{ V}}{25 \text{ nA}} \right| = 600 \text{ M}\Omega$

$$R_{in} = 10 \text{ M}\Omega \parallel 600 \text{ M}\Omega = \mathbf{9.84 \text{ M}\Omega}$$

22. $A_v = g_m R_d = 48 \text{ mS} (1.0 \text{ k}\Omega \parallel 10 \text{ M}\Omega) \approx 4.8$

$$V_{out} = A_v V_{in} = 4.8(10 \text{ mV}) = \mathbf{48 \text{ mV rms}}$$

$$I_D = I_{DSS} = 15 \text{ mA}$$

$$V_D = 24 \text{ V} - (15 \text{ mA})(1.0 \text{ k}\Omega) = \mathbf{9 \text{ V}}$$

See Figure 9-2.

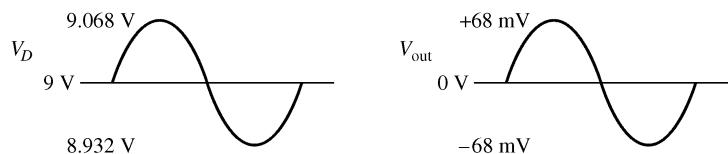


Figure 9-2

Chapter 9

23. $V_{GS} = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD} = \left(\frac{47 \text{ k}\Omega}{94 \text{ k}\Omega} \right) 18 \text{ V} = 9 \text{ V}$

$$K = \frac{I_{D(\text{on})}}{(V_{GS} - V_{GS(\text{th})})^2} = \frac{8 \text{ mA}}{(12 \text{ V} - 4 \text{ V})^2} = 0.125 \text{ mA/V}^2$$

$$I_{D(\text{on})} = K(V_{GS} - V_{GS(\text{th})})^2 = 0.125 \text{ mA/V}^2(9 \text{ V} - 4 \text{ V})^2 = 3.13 \text{ mA}$$

$$V_{DS} = V_{DD} - I_D R_D = 18 \text{ V} - (3.125 \text{ mA})(1.5 \text{ k}\Omega) = 13.3 \text{ V}$$

$$A_v = g_m R_D = 4500 \mu\text{S}(1.5 \text{ k}\Omega) = 6.75$$

$$V_{ds} = A_v V_{in} = 6.75(100 \text{ mV}) = 675 \text{ mV rms}$$

Section 9-2 The Common-Drain Amplifier

24. $R_s = 1.2 \text{ k}\Omega \parallel 1 \text{ k}\Omega \cong 545 \text{ }\Omega$

$$A_v = \frac{g_m R_s}{1 + g_m R_s} = \frac{(5500 \mu\text{S})(545 \text{ }\Omega)}{1 + (5500 \mu\text{S})(545 \text{ }\Omega)} = 0.750$$

$$R_{IN} = \left| \frac{V_{GS}}{I_{GSS}} \right| = \left| \frac{-15 \text{ V}}{50 \text{ pA}} \right| = 3 \times 10^{11} \text{ }\Omega$$

$$R_{in} = 10 \text{ M}\Omega \parallel 3 \times 10^{11} \text{ }\Omega \cong 10 \text{ M}\Omega$$

25. $R_s = 1.2 \text{ k}\Omega \parallel 1 \text{ k}\Omega \cong 545 \text{ }\Omega$

$$A_v = \frac{g_m R_s}{1 + g_m R_s} = \frac{(3000 \mu\text{S})(545 \text{ }\Omega)}{1 + (3000 \mu\text{S})(545 \text{ }\Omega)} = 0.620$$

$$R_{IN} = \left| \frac{V_{GS}}{I_{GSS}} \right| = \left| \frac{-15 \text{ V}}{50 \text{ pA}} \right| = 3 \times 10^{11} \text{ }\Omega$$

$$R_{in} = 10 \text{ M}\Omega \parallel 3 \times 10^{11} \text{ }\Omega \cong 10 \text{ M}\Omega$$

26. (a) $R_s = 4.7 \text{ k}\Omega \parallel 47 \text{ k}\Omega = 4.27 \text{ k}\Omega$

$$A_v = \frac{g_m R_s}{1 + g_m R_s} = \frac{(3000 \mu\text{S})(4.27 \text{ k}\Omega)}{1 + (3000 \mu\text{S})(4.27 \text{ k}\Omega)} = 0.928$$

(b) $R_s = 1.0 \text{ k}\Omega \parallel 100 \text{ }\Omega = 90.9 \text{ }\Omega$

$$A_v = \frac{g_m R_s}{1 + g_m R_s} = \frac{(4300 \mu\text{S})(90.9 \text{ }\Omega)}{1 + (4300 \mu\text{S})(90.9 \text{ }\Omega)} = 0.281$$

27. (a) $R_s = 4.7 \text{ k}\Omega \parallel 10 \text{ k}\Omega = 3.2 \text{ k}\Omega$

$$A_v = \frac{g_m R_s}{1 + g_m R_s} = \frac{(3000 \mu\text{S})(3.2 \text{ k}\Omega)}{1 + (3000 \mu\text{S})(3.2 \text{ k}\Omega)} = 0.906$$

(b) $R_s = 100 \text{ }\Omega \parallel 10 \text{ k}\Omega = 99 \text{ }\Omega$

$$A_v = \frac{g_m R_s}{1 + g_m R_s} = \frac{(4300 \mu\text{S})(99 \text{ }\Omega)}{1 + (4300 \mu\text{S})(99 \text{ }\Omega)} = 0.299$$

Section 9-3 The Common-Gate Amplifier

28. $A_v = g_m R_d = 4000 \mu\text{S} (1.5 \text{ k}\Omega) = \mathbf{6.0}$

29. $R_{in(source)} = \frac{1}{g_m} = \frac{1}{4000 \mu\text{S}} = \mathbf{250 \Omega}$

30. $A_v = g_m R_d = 3500 \mu\text{S} (10 \text{ k}\Omega) = \mathbf{35}$

$$R_{in} = R_S \parallel \left(\frac{1}{g_m} \right) = 2.2 \text{ k}\Omega \parallel \left(\frac{1}{3500 \mu\text{S}} \right) = \mathbf{253 \Omega}$$

31. $X_L = 2\pi fL = 2\pi(100 \text{ MHz})(1.5 \text{ mH}) = 943 \text{ k}\Omega$

$$A_v = g_{m(CG)} X_L = (2800 \mu\text{S})(943 \text{ k}\Omega) = \mathbf{2640}$$

$$R_{in} = R_3 \parallel \left(\frac{V_{GS}}{I_{GSS}} \right) = 15 \text{ M}\Omega \parallel \left(\frac{15 \text{ V}}{2 \text{ nA}} \right)$$

$$= 15 \text{ M}\Omega \parallel 500 \text{ M}\Omega = \mathbf{14.6 \text{ M}\Omega}$$

Section 9-4 The Class D Amplifier

32. $A_v = \frac{2(9 \text{ V})}{5 \text{ mV}} = \frac{18 \text{ V}}{5 \text{ mV}} = 3600$

33. $P_{out} = (12 \text{ V})(0.35 \text{ A}) = 4.2 \text{ W}$

$$P_{int} = (0.25 \text{ V})(0.35 \text{ A}) + 140 \text{ mW} \\ = 87.5 \text{ mW} + 140 \text{ mW} = 227.5 \text{ mW}$$

$$\eta = \frac{P_{out}}{P_{out} + P_{int}} = \frac{4.2 \text{ W}}{4.2 \text{ W} + 227.5 \text{ mW}} = \mathbf{0.95}$$

Section 9-5 MOSFET Analog Switching

34. $V_G - V_{p(out)} = V_{GS(\text{Th})}$
 $V_{p(out)} = V_G - V_{GS(\text{Th})} = 8 \text{ V} - 4 \text{ V} = 4 \text{ V}$
 $V_{pp(in)} = 2 V_{p(out)} = 2 \times 4 \text{ V} = \mathbf{8 \text{ V}}$

35. $f_{min} = 2 \times 15 \text{ kHz} = \mathbf{30 \text{ kHz}}$

36. $R = \frac{1}{fC}$

$$f = \frac{1}{RC} = \frac{1}{(10 \text{ k}\Omega)(10 \text{ pF})} = \mathbf{10 \text{ MHz}}$$

37. $R = \frac{1}{fC} = \frac{1}{(25 \text{ kHz})(0.001 \mu\text{F})} = \mathbf{40 \text{ k}\Omega}$

Chapter 9

Section 9-6 MOSFET Digital Switching

38. $V_{out} = +5\text{ V}$ when $V_{in} = 0$
 $V_{out} = 0\text{ V}$ when $V_{in} = +5\text{ V}$
39. (a) $V_{out} = 3.3\text{ V}$ (b) $V_{out} = 3.3\text{ V}$
(c) $V_{out} = 3.3\text{ V}$ (d) $V_{out} = 0\text{ V}$
40. (a) $V_{out} = 3.3\text{ V}$ (b) $V_{out} = 0\text{ V}$
(c) $V_{out} = 0\text{ V}$ (d) $V_{out} = 0\text{ V}$
41. The MOSFET has lower on-state resistance and can turn off faster.

Section 9-7 Troubleshooting

42. (a) $V_{D1} = V_{DD}$; No signal at Q_1 drain; No output signal
(b) $V_{D1} \geq 0\text{ V}$ (floating); No signal at Q_1 drain; No output signal
(c) $V_{GS1} = 0\text{ V}$; $V_S = 0\text{ V}$; V_{D1} less than normal; Clipped output signal
(d) Correct signal at Q_1 drain; No signal at Q_2 gate; No output signal
(e) $V_{D2} = V_{DD}$; Correct signal at Q_2 gate; No Q_2 drain signal or output signal
43. (a) $V_{out} = 0\text{ V}$ if C_1 is open.
(b) $A_{v1} = g_m R_d = 5000\text{ }\mu\text{S}(1.5\text{ k}\Omega) = 7.5$
$$A_{v2} = \frac{g_m R_d}{1 + g_m R_s} = \frac{7.5}{1 + (5000\text{ }\mu\text{S})(470\text{ }\Omega)} = 2.24$$

 $A_v = A_{v1}A_{v2} = (7.5)(2.24) = 16.8$
 $V_{out} = A_v V_{in} = (16.8)(10\text{ mV}) = 168\text{ mV}$
(c) V_{GS} for Q_2 is 0 V, so $I_D = I_{DSS}$. The output is clipped.
(d) No V_{out} because there is no signal at the Q_2 gate.

Datasheet Problems

44. The 2N3796 FET is an **n-channel D-MOSFET**.
45. (a) For a 2N3796, the typical $V_{GS(off)} = -3.0\text{ V}$
(b) For a 2N3797, $V_{DS(max)} = 20\text{ V}$
(c) At $T_A = 25^\circ\text{C}$, $P_{D(max)} = 200\text{ mW}$
(d) For a 2N3797, $V_{GS(max)} = \pm 10\text{ V}$
46. $P_D = 200\text{ mW} - (1.14\text{ mW}/^\circ\text{C})(55^\circ\text{C} - 25^\circ\text{C}) = 166\text{ mW}$
47. For a 2N3796 with $f = 1\text{ kHz}$, $g_{m0} = 900\text{ }\mu\text{S}$ minimum
48. At $V_{GS} = 3.5\text{ V}$ and $V_{DS} = 10\text{ V}$,
 $I_{D(min)} = 9.0\text{ mA}$, $I_{D(typ)} = 14\text{ mA}$, $I_{D(max)} = 18\text{ mA}$
49. For a zero-biased 2N3796, $I_{D(typ)} = 1.5\text{ mA}$

50. $A_{v(\max)} = (1800 \mu\text{S})(2.2 \text{ k}\Omega) = 3.96$

Advanced Problems

51. $R_{d(\min)} = 1.0 \text{ k}\Omega \parallel 4 \text{ k}\Omega = 800 \Omega$

$$A_{v(\min)} = (2.5 \text{ mS})(800 \Omega) = 2.0$$

$$R_{d(\max)} = 1.0 \text{ k}\Omega \parallel 10 \text{ k}\Omega = 909 \Omega$$

$$A_{v(\max)} = (7.5 \text{ mS})(909 \Omega) = 6.82$$

52. $I_{DSS(\text{typ})} = 2.9 \text{ mA}$

$$R_D + R_S = \frac{12 \text{ V}}{2.9 \text{ mA}} = 4.14 \text{ k}\Omega$$

$$\frac{1}{g_m} = \frac{1}{2300 \mu\text{S}} = 435 \Omega$$

If $R_S = 0 \Omega$, then $R_D \geq 4 \text{ k}\Omega$ (3.9 kΩ standard)

$$A_v = (2300 \mu\text{S})(3.9 \text{ k}\Omega) = 8.97$$

$$V_{DS} = 24 \text{ V} - (2.9 \text{ mA})(3.9 \text{ k}\Omega) = 24 \text{ V} - 11.3 \text{ V} = 12.7 \text{ V}$$

The circuit is a common-source zero-biased amplifier with a drain resistor of 3.9 kΩ.

53. To maintain $V_{DS} = 12 \text{ V}$ for the range of I_{DSS} values:

For $I_{DSS(\min)} = 2 \text{ mA}$

$$R_D = \frac{12 \text{ V}}{2 \text{ mA}} = 6 \text{ k}\Omega$$

For $I_{DSS(\max)} = 6 \text{ mA}$

$$R_D = \frac{12 \text{ V}}{6 \text{ mA}} = 2 \text{ k}\Omega$$

To maintain $A_v = 9$ for the range of $g_m(y_{fs})$ values:

For $g_{m(\min)} = 1500 \mu\text{S}$

$$R_D = \frac{9}{1500 \mu\text{S}} = 6 \text{ k}\Omega$$

For $g_{m(\max)} = 3000 \mu\text{S}$

$$R_D = \frac{9}{3000 \mu\text{S}} = 3 \text{ k}\Omega$$

A drain resistance consisting of a 2.2 kΩ fixed resistor in series with a 5 kΩ variable resistor will provide more than sufficient range to maintain a gain of 9 over the specified range of g_m values. The dc voltage at the drain will vary with adjustment and depends on I_{DSS} . The circuit cannot be modified to maintain both $V_{DS} = 12 \text{ V}$ and $A_v = 9$ over the full range of transistor parameter values. See Figure 9-3.

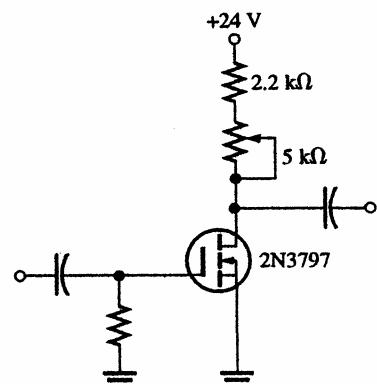


Figure 9-3

Chapter 9

Multisim Troubleshooting Problems

The solutions showing instrument connections for Problems 54 through 62 are available from the Instructor Resource Center. See Chapter 1 for instructions. The faults in the circuit files may be accessed using the password *book* (all lowercase).

54. Drain-source shorted

55. C_2 open

56. C_1 open

57. R_S shorted

58. Drain-source open

59. R_1 open

60. R_D open

61. R_2 open

62. C_2 open

Chapter 10

Amplifier Frequency Response

Section 10-1 Basic Concepts

1. If $C_1 = C_2$, the critical frequencies are equal, and they will both cause the gain to decrease at 40 dB/decade below f_c .
2. At sufficiently high frequencies, the reactances of the coupling capacitors become very small and the capacitors appear effectively as shorts; thus, negligible signal voltage is dropped across them.
3. BJT: C_{be} , C_{bc} , and C_{ce}
FET: C_{gs} , C_{gd} , and C_{ds}
4. Low-frequency response: C_1 , C_2 , and C_3
High-frequency response: C_{bc} , C_{be} , and C_{ce}

5. $V_E \approx \left(\frac{R_2}{R_1 + R_2} \right) V_{CC} - 0.7 \text{ V} = \left(\frac{4.7 \text{ k}\Omega}{37.7 \text{ k}\Omega} \right) 20 \text{ V} - 0.7 \text{ V} = 1.79 \text{ V}$

$$I_E = \frac{V_E}{R_E} = \frac{1.79 \text{ V}}{560 \Omega} = 3.2 \text{ mA}$$

$$r'_e = \frac{25 \text{ mV}}{3.2 \text{ mA}} = 7.8 \Omega$$

$$A_v = \frac{R_c}{r'_e} = \frac{2.2 \text{ k}\Omega \parallel 5.6 \text{ k}\Omega}{7.8 \Omega} = 202$$

$$C_{in(miller)} = C_{bc}(A_v + 1) = 4 \text{ pF}(202 + 1) = \mathbf{812 \text{ pF}}$$

6. $C_{out(miller)} = C_{bc} \left(\frac{A_v + 1}{A_v} \right) = 4 \text{ pF} \left(\frac{203}{202} \right) = \mathbf{4 \text{ pF}}$

7. $I_D = 3.36 \text{ mA}$ using Eq. 9-2 and a programmable calculator.

$$V_{GS} = -(3.36 \text{ mA})(1.0 \text{ k}\Omega) = -3.36 \text{ V}$$

$$g_{m0} = \frac{2(10 \text{ mA})}{8 \text{ V}} = 2.5 \text{ mS}$$

$$g_m = (2.5 \text{ mS}) \left(1 - \frac{3.36 \text{ V}}{8 \text{ V}} \right) = 1.45 \text{ mS}$$

$$A_v = g_m R_d = (1.45 \text{ mS})(1.0 \text{ k}\Omega \parallel 10 \text{ k}\Omega) = 1.32$$

$$C_{gd} = C_{rss} = 3 \text{ pF}$$

$$C_{in(miller)} = C_{gd}(A_v + 1) = 3 \text{ pF}(2.32) = \mathbf{6.95 \text{ pF}}$$

$$C_{out(miller)} = C_{gd} \left(\frac{A_v + 1}{A_v} \right) = 3 \text{ pF} \left(\frac{2.32}{1.32} \right) = \mathbf{5.28 \text{ pF}}$$

Chapter 10

Section 10-2 The Decibel

8. $A_p = \frac{P_{out}}{P_{in}} = \frac{5 \text{ W}}{0.5 \text{ W}} = 10$
 $A_{p(\text{dB})} = 10 \log\left(\frac{P_{out}}{P_{in}}\right) = 10 \log 10 = \mathbf{10 \text{ dB}}$

9. $V_{in} = \frac{V_{out}}{A_v} = \frac{1.2 \text{ V}}{50} = \mathbf{24 \text{ mV rms}}$
 $A_{v(\text{dB})} = 20 \log(A_v) = 20 \log 50 = \mathbf{34.0 \text{ dB}}$

10. The gain reduction is $20 \log\left(\frac{25}{65}\right) = \mathbf{-8.3 \text{ dB}}$

11. (a) $10 \log\left(\frac{2 \text{ mW}}{1 \text{ mW}}\right) = \mathbf{3.01 \text{ dBm}}$
(b) $10 \log\left(\frac{1 \text{ mW}}{1 \text{ mW}}\right) = \mathbf{0 \text{ dBm}}$
(c) $10 \log\left(\frac{4 \text{ mW}}{1 \text{ mW}}\right) = \mathbf{6.02 \text{ dBm}}$
(d) $10 \log\left(\frac{0.25 \text{ mW}}{1 \text{ mW}}\right) = \mathbf{-6.02 \text{ dBm}}$

12. $V_B = \left(\frac{4.7 \text{ k}\Omega}{37.7 \text{ k}\Omega}\right)20 \text{ V} = 1.79 \text{ V}$
 $I_E = \frac{1.79 \text{ V}}{560 \Omega} = 3.20 \text{ mA}$
 $r'_e = \frac{25 \text{ mV}}{3.2 \text{ mA}} = 7.81 \Omega$
 $A_v = \frac{5.6 \text{ k}\Omega \parallel 2.2 \text{ k}\Omega}{7.81 \Omega} = 202$

$A_{v(\text{dB})} = 20 \log(202) = \mathbf{46.1 \text{ dB}}$
At the critical frequencies,
 $A_{v(\text{dB})} = 46.1 \text{ dB} - 3 \text{ dB} = \mathbf{43.1 \text{ dB}}$

Section 10-3 Low-Frequency Amplifier Response

13. (a) $f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi(100 \Omega)(5 \mu\text{F})} = \mathbf{318 \text{ Hz}}$
(b) $f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi(1.0 \text{ k}\Omega)(0.1 \mu\text{F})} = \mathbf{1.59 \text{ kHz}}$

14. $R_{IN(BASE)} = \beta_{DC} R_E = 12.5 \text{ k}\Omega$

$$V_E = \left(\frac{R_2 \parallel R_{IN(BASE)}}{R_1 + R_2 \parallel R_{IN(BASE)}} \right) 9 \text{ V} - 0.7 \text{ V} = \left(\frac{4.7 \text{ k}\Omega \parallel 12.5 \text{ k}\Omega}{12 \text{ k}\Omega + 4.7 \text{ k}\Omega \parallel 12.5 \text{ k}\Omega} \right) 9 \text{ V} - 0.7 \text{ V} = 1.3 \text{ V}$$

$$I_E = \frac{V_E}{R_E} = \frac{1.3 \text{ V}}{100 \text{ }\Omega} = 13 \text{ mA}$$

$$r'_e = \frac{25 \text{ mV}}{13 \text{ mA}} = 1.92 \text{ }\Omega$$

$$R_{in(base)} = \beta_{ac} r'_e = (125)(1.92 \text{ }\Omega) = 240 \text{ }\Omega$$

$$R_{in} = 50 \text{ }\Omega + R_{in(base)} \parallel R_1 \parallel R_2 = 50 \text{ }\Omega + 240 \text{ }\Omega \parallel 12 \text{ k}\Omega \parallel 4.7 \text{ k}\Omega = 274 \text{ }\Omega$$

For the input circuit:

$$f_c = \frac{1}{2\pi R_{in} C_1} = \frac{1}{2\pi(274 \text{ }\Omega)(1 \text{ }\mu\text{F})} = 581 \text{ Hz}$$

For the output circuit:

$$f_c = \frac{1}{2\pi(R_C + R_L)C_3} = \frac{1}{2\pi(900 \text{ }\Omega)(1 \text{ }\mu\text{F})} = 177 \text{ Hz}$$

For the bypass circuit:

$$R_{TH} = R_1 \parallel R_2 \parallel R_s = 12 \text{ k}\Omega \parallel 4.7 \text{ k}\Omega \parallel 50 \text{ }\Omega \approx 49.3 \text{ }\Omega$$

$$f_c = \frac{1}{2\pi(r'_e + R_{TH}/\beta_{DC} \parallel R_E)C_2} = \frac{1}{2\pi(2.31 \text{ }\Omega)(10 \text{ }\mu\text{F})} = 6.89 \text{ kHz}$$

$$A_v = \frac{R_C \parallel R_L}{r'_e} = \frac{220 \text{ }\Omega \parallel 680 \text{ }\Omega}{1.92 \text{ }\Omega} = 86.6$$

$$A_{v(\text{dB})} = 20 \log(86.6) = 38.8 \text{ dB}$$

The **bypass circuit** produces the dominant low critical frequency. See Figure 10-1.

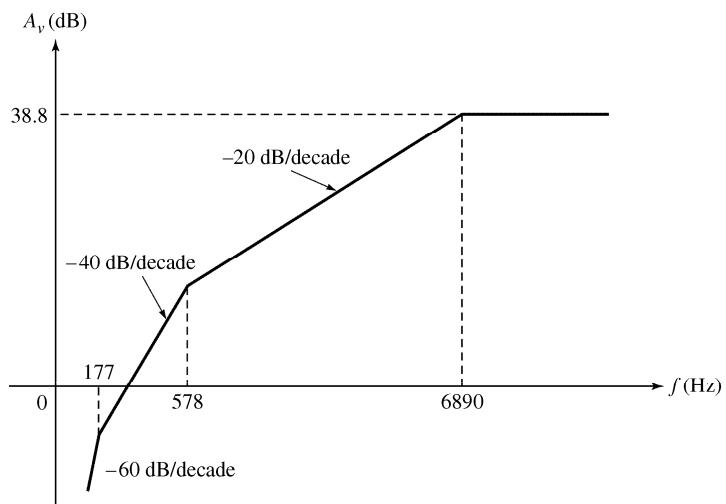


Figure 10-1

Chapter 10

15.

From Problem 14:

$$A_{v(mid)} = 86.6$$

$$A_{v(mid)} (\text{dB}) = 38.8 \text{ dB}$$

For the input RC circuit: $f_c = 578 \text{ Hz}$

For the output RC circuit: $f_c = 177 \text{ Hz}$

For the bypass RC circuit: $f_c = 6.89 \text{ kHz}$

The f_c of the bypass circuit is the dominant low critical frequency.

At $f = f_c = 6.89 \text{ kHz}$:

$$A_v = A_{v(mid)} - 3 \text{ dB} = 38.8 \text{ dB} - 3 \text{ dB} = \mathbf{35.8 \text{ dB}}$$

At $f = 0.1f_c$:

$$A_v = 38.8 \text{ dB} - 20 \text{ dB} = \mathbf{18.8 \text{ dB}}$$

At $10f_c$ (neglecting any high frequency effects):

$$A_v = A_{v(mid)} = \mathbf{38.8 \text{ dB}}$$

16.

At $f = f_c = X_C = R$

$$\theta = \tan^{-1}\left(\frac{X_C}{R}\right) = \tan^{-1}(1) = \mathbf{45^\circ}$$

At $f = 0.1f_c$, $X_C = 10R$.

$$\theta = \tan^{-1}(10) = \mathbf{84.3^\circ}$$

At $f = 10f_c$, $X_C = 0.1R$.

$$\theta = \tan^{-1}(0.1) = \mathbf{5.7^\circ}$$

17.

$$R_{in(gate)} = \left| \frac{V_{GS}}{I_{GSS}} \right| = \left| \frac{-10 \text{ V}}{50 \text{ nA}} \right| = 200 \text{ M}\Omega$$

$$R_{in} = R_G \parallel R_{in(gate)} = 10 \text{ M}\Omega \parallel 200 \text{ M}\Omega = 9.52 \text{ M}\Omega$$

For the input circuit:

$$f_c = \frac{1}{2\pi R_{in} C_1} = \frac{1}{2\pi(9.52 \text{ M}\Omega)(0.005 \mu\text{F})} = \mathbf{3.34 \text{ Hz}}$$

For the output circuit:

$$f_c = \frac{1}{2\pi(R_D + R_L)C_2} = \frac{1}{2\pi(560 \Omega + 10 \text{ k}\Omega)(0.005 \mu\text{F})} = \mathbf{3.01 \text{ kHz}}$$

The **output circuit is dominant**. See Figure 10-2. (A_v is determined in Problem 18.)

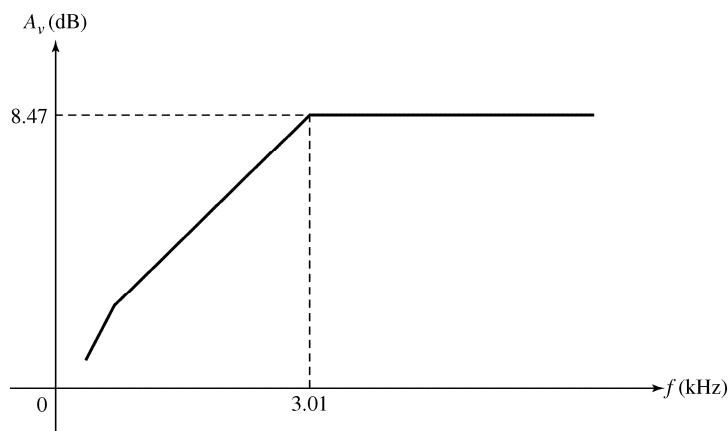


Figure 10-2

- 18.** $g_m = g_{m0} = \frac{2(15 \text{ mA})}{6 \text{ V}} = 5 \text{ mS}$
- $$A_{v(mid)} = g_m(R_D \parallel R_L) = 5 \text{ mS}(560 \Omega \parallel 10 \text{ k}\Omega) = 2.65$$
- $$A_{v(mid)} (\text{dB}) = 8.47 \text{ dB}$$
- At f_c :
- $$A_v = 8.47 \text{ dB} - 3 \text{ dB} = \mathbf{5.47 \text{ dB}}$$
- At $0.1f_c$:
- $$A_v = 8.47 \text{ dB} - 20 \text{ dB} = \mathbf{-11.5 \text{ dB}}$$
- At $10f_c$:
- $$A_v = A_{v(mid)} = \mathbf{8.47 \text{ dB}} \text{ (if } 10f_c \text{ is still in midrange)}$$

Section 10-4 High-Frequency Amplifier Response

- 19.** From Problems 14 and 15:
- $$r'_e = 1.92 \Omega \text{ and } A_{v(mid)} = 86.6$$
- Input circuit:
- $$C_{in(miller)} = C_{bc}(A_v + 1) = 10 \text{ pF}(87.6) = 876 \text{ pF}$$
- $$C_{tot} = C_{be} + C_{in(miller)} = 25 \text{ pF} + 876 \text{ pF} = 901 \text{ pF}$$
- $$f_c = \frac{1}{2\pi(R_s \parallel R_1 \parallel R_2 \parallel \beta_{ac} r'_e)C_{tot}} = \frac{1}{2\pi(50 \Omega \parallel 12 \text{ k}\Omega \parallel 4.7 \text{ k}\Omega \parallel 240 \Omega)901 \text{ pF}} = \mathbf{4.32 \text{ MHz}}$$
- Output circuit:
- $$C_{out(miller)} = C_{bc} \left(\frac{A_v + 1}{A_v} \right) = 10 \text{ pF} \left(\frac{87.6}{86.6} \right) = 10.1 \text{ pF}$$
- $$f_c = \frac{1}{2\pi R_c C_{out(miller)}} = \frac{1}{2\pi(166 \Omega)(10.1 \text{ pF})} = \mathbf{94.9 \text{ MHz}}$$

Therefore, the dominant high critical frequency is determined by the input circuit:
 $f_c = 4.32 \text{ MHz}$. See Figure 10-3.

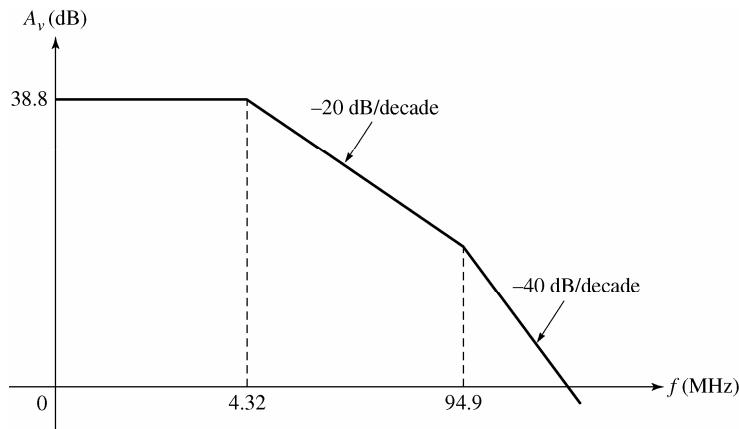


Figure 10-3

Chapter 10

20.

At $f = 0.1f_c = 458$ kHz:

$$A_v = A_{v(mid)} = \mathbf{38.8 \text{ dB}}$$

At $f = f_c = 4.58$ MHz:

$$A_v = A_{v(mid)} - 3 \text{ dB} = 38.8 \text{ dB} - 3 \text{ dB} = \mathbf{35.8 \text{ dB}}$$

At $f = 10f_c = 45.8$ MHz:

$$A_v = A_{v(mid)} - 20 \text{ dB} = 38.8 \text{ dB} - 20 \text{ dB} = \mathbf{18.8 \text{ dB}}$$

At $f = 100f_c = 458$ MHz:

The roll-off rate changes to -40 dB/decade at $f = 94.6$ MHz. So, for frequencies from 45.8 MHz to 94.6 MHz, the roll-off rate is -20 dB/decade and above 94.6 MHz it is -40 dB/decade.

The change in frequency from 45.8 MHz to 94.6 MHz represents

$$\frac{94.6 \text{ MHz} - 45.8 \text{ MHz}}{458 \text{ MHz} - 45.8 \text{ MHz}} \times 100\% = 11.8\%$$

So, for 11.8% of the decade from 45.8 MHz to 458 MHz, the roll-off rate is -20 dB/decade and for the remaining 88.2% of the decade, the roll-off rate is -40 dB/decade.

$$A_v = 18.8 \text{ dB} - (0.118)(20 \text{ dB}) - (0.882)(40 \text{ dB}) = 18.8 \text{ dB} - 2.36 \text{ dB} - 35.3 \text{ dB} = \mathbf{-18.9 \text{ dB}}$$

21.

$$C_{gd} = C_{rss} = 4 \text{ pF}$$

$$C_{gs} = C_{iss} - C_{rss} = 10 \text{ pF} - 4 \text{ pF} = 6 \text{ pF}$$

Input circuit:

$$C_{in(miller)} = C_{gd}(A_v + 1) = 4 \text{ pF}(2.65 + 1) = 14.6 \text{ pF}$$

$$C_{tot} = C_{gs} + C_{in(miller)} = 6 \text{ pF} + 14.6 \text{ pF} = 20.6 \text{ pF}$$

$$f_c = \frac{1}{2\pi R_s C_{tot}} = \frac{1}{2\pi(600 \Omega)(20.6 \text{ pF})} = \mathbf{12.9 \text{ MHz}}$$

Output circuit:

$$C_{out(miller)} = C_{gd} \left(\frac{A_v + 1}{A_v} \right) = 4 \text{ pF} \left(\frac{2.65 + 1}{2.65} \right) = 5.51 \text{ pF}$$

$$f_c = \frac{1}{2\pi R_d C_{out(miller)}} = \frac{1}{2\pi(530 \Omega)(5.51 \text{ pF})} = \mathbf{54.5 \text{ MHz}}$$

The input circuit is dominant.

22.

From Problem 21: For the input circuit, $f_c = 12.9$ MHz and for the output circuit, $f_c = 54.5$ MHz.

The dominant critical frequency is 12.9 MHz.

$$\text{At } f = 0.1f_c = 1.29 \text{ MHz: } A_v = A_{v(mid)} = \mathbf{8.47 \text{ dB}}, \theta = 0^\circ$$

$$\text{At } f = f_c = 12.9 \text{ MHz: } A_v = A_{v(mid)} - 3 \text{ dB} = 8.47 \text{ dB} - 3 \text{ dB} = \mathbf{5.47 \text{ dB}}, \theta = \tan^{-1}(1) = \mathbf{45^\circ}$$

$$\text{At } f = 10f_c = 129 \text{ MHz: }$$

From 12.9 MHz to 54.5 MHz the roll-off is -20 dB/decade. From 54.5 MHz to 129 MHz the roll-off is -40 dB/decade.

The change in frequency from 12.9 MHz to 54.5 MHz represents

$$\frac{54.5 \text{ MHz} - 12.9 \text{ MHz}}{129 \text{ MHz} - 12.9 \text{ MHz}} \times 100\% = 35.8\%$$

So, for 35.8% of the decade, the roll-off rate is -20 dB/decade and for 64.2% of the decade, the rate is -40 dB/decade.

$$A_v = 5.47 \text{ dB} - (0.358)(20 \text{ dB}) - (0.642)(40 \text{ dB}) = \mathbf{-27.4 \text{ dB}}$$

$$\text{At } f = 100f_c = 1290 \text{ MHz: } A_v = -27.4 \text{ dB} - 40 \text{ dB} = \mathbf{-67.4 \text{ dB}}$$

Section 10-5 Total Amplifier Frequency Response

23. $f_{cl} = 136 \text{ Hz}$
 $f_{cu} = 8 \text{ kHz}$

24. From Problems 14 and 19:
 $f_{cu} = 4.32 \text{ MHz}$ and $f_{cl} = 6.89 \text{ kHz}$
 $BW = f_{cu} - f_{cl} = 4.32 \text{ MHz} - 6.89 \text{ kHz} = 4.313 \text{ MHz}$

25. $f_{tot} = (BW)A_{v(mid)}$
 $BW = \frac{f_{tot}}{A_{v(mid)}} = \frac{200 \text{ MHz}}{38} = 5.26 \text{ MHz}$

Therefore, $f_{cu} \cong BW = 5.26 \text{ MHz}$

26. 6 dB/octave roll-off:
At $2f_{cu}$: $A_v = 50 \text{ dB} - 6 \text{ dB} = 44 \text{ dB}$
At $4f_{cu}$: $A_v = 50 \text{ dB} - 12 \text{ dB} = 38 \text{ dB}$
20 dB/decade roll-off:
At $10f_{cu}$: $A_v = 50 \text{ dB} - 20 \text{ dB} = 30 \text{ dB}$

Section 10-6 Frequency Response of Multistage Amplifiers

27. Dominant $f'_{cl} = 230 \text{ Hz}$
Dominant $f'_{cu} = 1.2 \text{ MHz}$

28. $BW = 1.2 \text{ MHz} - 230 \text{ Hz} \cong 1.2 \text{ MHz}$

29. $f'_{cl} = \frac{400 \text{ Hz}}{\sqrt{2^{1/2} - 1}} = \frac{400 \text{ Hz}}{0.643} = 622 \text{ Hz}$
 $f'_{cu} = (800 \text{ kHz})\sqrt{2^{1/2} - 1} = 0.643(800 \text{ kHz}) = 515 \text{ kHz}$
 $BW = 515 \text{ kHz} - 622 \text{ Hz} \cong 514 \text{ kHz}$

30. $f'_{cl} = \frac{50 \text{ Hz}}{\sqrt{2^{1/3} - 1}} = \frac{50 \text{ Hz}}{0.510} = 98.1 \text{ Hz}$

31. $f'_{cl} = \frac{125 \text{ Hz}}{\sqrt{2^{1/2} - 1}} = \frac{125 \text{ Hz}}{0.643} = 194 \text{ Hz}$
 $f'_{cu} 2.5 \text{ MHz}$
 $BW = 2.5 \text{ MHz} - 194 \text{ Hz} \cong 2.5 \text{ MHz}$

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Section 10-7 Frequency Response Measurements

32. $f_{cl} = \frac{0.35}{t_f} = \frac{0.35}{1 \text{ ms}} = 350 \text{ Hz}$

$$f_{cu} = \frac{0.35}{t_r} = \frac{0.35}{20 \text{ ns}} = 17.5 \text{ MHz}$$

33. Increase the frequency until the output voltage drops to 3.54 V (3 dB below the midrange output voltage). This is the upper critical frequency.

34. $t_r \equiv 3 \text{ div} \times 5 \mu\text{s/div} = 15 \mu\text{s}$

$$t_f \equiv 6 \text{ div} \times 0.1 \text{ ms/div} = 600 \mu\text{s}$$

$$f_{cl} = \frac{0.35}{t_f} = \frac{0.35}{600 \mu\text{s}} = 583 \text{ Hz}$$

$$f_{cu} = \frac{0.35}{t_r} = \frac{0.35}{15 \mu\text{s}} = 23.3 \text{ kHz}$$

$$BW = 23.3 \text{ kHz} - 583 \text{ Hz} = 22.7 \text{ kHz}$$

Application Activity Problems

35. Q_1 stage:

$$f_{cl(input)} = \frac{1}{2\pi(R_1 \parallel R_2 \parallel \beta_{ac}R_4)C_1} = \frac{1}{2\pi(90 \text{ k}\Omega)1 \mu\text{F}} = 1.77 \text{ Hz}$$

$$f_{cl(bypass)} = \frac{1}{2\pi R_4 C_2} = \frac{1}{2\pi(1 \text{ k}\Omega)10 \mu\text{F}} = 15.9 \text{ Hz}$$

$$f_{cl(output)} = \frac{1}{2\pi(R_5 + R_6 \parallel R_7 \parallel \beta_{ac}(R_9 + R_{10}))C_3} = \frac{1}{2\pi(36 \text{ k}\Omega)1 \mu\text{F}} = 4.42 \text{ Hz}$$

- Q_2 stage:

$$f_{cl(input)} = \frac{1}{2\pi(R_5 \parallel R_6 \parallel R_7 \parallel \beta_{ac}(R_9 + R_{10}))C_3} = \frac{1}{2\pi(36 \text{ k}\Omega)1 \mu\text{F}} = 4.42 \text{ Hz}$$

$$f_{cl(bypass)} = \frac{1}{2\pi\left(R_9 + \frac{R_6 \parallel R_7}{\beta_{ac}}\right)C_4} = \frac{1}{2\pi(205 \Omega)100 \mu\text{F}} = 7.76 \text{ Hz}$$

$$f_{cl(output)} = \frac{1}{2\pi(R_8 + R_L)C_5} = \frac{1}{2\pi(35.8 \text{ k}\Omega)1 \mu\text{F}} = 4.45 \text{ Hz}$$

The dominant critical frequency of **15.9 Hz** is set by the Q_1 bypass circuit.

36. Changing to 1 μF coupling capacitors does not significantly affect the overall bandwidth because the upper critical frequency is much greater than the dominant lower critical frequency.

- 37.** Increasing the load resistance on the output of the second stage has no effect on the dominant lower critical frequency because the critical frequency of the output circuit will decrease and the critical frequency of the first stage input circuit will remain dominant.

- 38.** The Q_1 stage bypass circuit set the dominant critical frequency.

$$f_{cl(bypass)} = \frac{1}{2\pi R_4 C_2} = \frac{1}{2\pi(1 \text{ k}\Omega)10 \mu\text{F}} = 15.9 \text{ Hz}$$

This frequency is not dependent on β_{ac} and is not affected.

Datasheet Problems

39. $C_{in(tot)} = (25 + 1)4 \text{ pF} + 8 \text{ pF} = 112 \text{ pF}$

40. $BW_{min} = \frac{f_T}{A_{v(mid)}} = \frac{300 \text{ MHz}}{50} = 6 \text{ MHz}$

41. $C_{gd} = C_{rss} = 1.3 \text{ pF}$

$$C_{gs} = C_{iss} - C_{rss} = 5 \text{ pF} - 1.3 \text{ pF} = 3.7 \text{ pF}$$

$$C_{ds} = C_d - C_{rss} = 5 \text{ pF} - 1.3 \text{ pF} = 3.7 \text{ pF}$$

Advanced Problems

- 42.** From Problem 12: $r'_e = 7.81 \Omega$ and $I_E = 3.2 \text{ mA}$

$$V_C \cong 20 \text{ V} - (3.2 \text{ mA})(2.2 \text{ k}\Omega) = 13 \text{ V dc}$$

The maximum peak output signal can be approximately 6 V.

The maximum allowable gain for the two stages is

$$A_{v(max)} = \frac{6 \text{ V}}{1.414(10 \text{ mV})} = 424$$

For stage 1:

$$R_c = 2.2 \text{ k}\Omega \parallel 33 \text{ k}\Omega \parallel 4.7 \text{ k}\Omega \parallel (150)(7.81 \Omega) = 645 \Omega$$

$$A_{v1} = \frac{645 \Omega}{7.81 \Omega} = 82.6$$

For stage 2:

$$R_c = 2.2 \text{ k}\Omega \parallel 5.6 \text{ k}\Omega = 1.58 \text{ k}\Omega$$

$$A_{v2} = \frac{1.58 \text{ k}\Omega}{7.81 \Omega} = 202$$

$$A_{v(tot)} = (82.6)(202) = 16,685$$

The amplifier will **not operate linearly** with a 10 mV rms input signal.

The gains of both stages can be reduced or the gain of the second stage only can be reduced.

Chapter 10

One approach is leave the gain of the first stage as is and bypass a portion of the emitter resistance in the second stage to achieve a gain of $424/82.6 = 5.13$.

$$A_v = \frac{R_c}{R_e + r'_e} = 5.13$$

$$R_e = \frac{R_c - 5.13r'_e}{5.13} = \frac{1.58 \text{ k}\Omega - 40.1 \Omega}{5.13} = 300 \Omega$$

Modification: Replace the 560Ω emitter resistor in the second stage with an unbypassed 300Ω resistor and a bypassed 260Ω resistor (closest standard value is 270Ω).

43. From Problems 17, 18, and 21:

$$C_{tot} = C_{gs} + C_{in(miller)} = 20.6 \text{ pF}$$

$$C_{out(miller)} = 4 \text{ pF} \left(\frac{2.65 + 1}{2.65} \right) = 5.51 \text{ pF}$$

Stage 1:

$$f_{cl(in)} = \frac{1}{2\pi R_{in} C_1} = \frac{1}{2\pi(9.52 \text{ M}\Omega)(0.005 \mu\text{F})} = 3.34 \text{ Hz}$$

$$f_{cl(out)} = \frac{1}{2\pi(9.52 \text{ M}\Omega)(0.005 \mu\text{F})} = 3.34 \text{ Hz} \text{ since } R_{in(2)} \gg 560 \Omega$$

$$f_{cu(in)} = \frac{1}{2\pi(600 \Omega)(20.6 \text{ pF})} = 12.9 \text{ MHz}$$

$$f_{cu(out)} = \frac{1}{2\pi(560 \Omega)(20.6 \text{ pF} + 5.51 \text{ pF})} = 10.9 \text{ MHz}$$

Stage 2:

$$f_{cl(in)} = \frac{1}{2\pi R_{in} C_1} = \frac{1}{2\pi(9.52 \text{ M}\Omega)(0.005 \mu\text{F})} = 3.34 \text{ Hz}$$

$$f_{cl(out)} = \frac{1}{2\pi(10.6 \text{ k}\Omega)(0.005 \mu\text{F})} = 3.01 \text{ kHz}$$

$$f_{cu(in)} = \frac{1}{2\pi(560 \Omega)(20.6 \text{ pF} + 5.51 \text{ pF})} = 10.9 \text{ MHz}$$

$$f_{cu(out)} = \frac{1}{2\pi(560 \Omega \parallel 10 \text{ k}\Omega)(5.51 \text{ pF})} = 54.5 \text{ MHz}$$

Overall:

$$f_{cl(in)} = 3.34 \text{ kHz} \text{ and } f_{cu(in)} = 10.9 \text{ MHz}$$

BW $\cong 10.9 \text{ MHz}$

44. $R_{in(1)} = 22 \text{ k}\Omega \parallel (100)(320 \text{ }\Omega) = 13 \text{ k}\Omega$

$$V_{B(1)} = \left(\frac{13 \text{ k}\Omega}{113 \text{ k}\Omega} \right) 12 \text{ V} = 1.38, V_{E(1)} = 0.681 \text{ V}$$

$$I_{E(1)} = \frac{0.681 \text{ V}}{320 \text{ }\Omega} = 2.13 \text{ mA}, r'_e = 11.7 \text{ }\Omega$$

$$R_{c(1)} = 4.7 \text{ k}\Omega \parallel 33 \text{ k}\Omega \parallel 22 \text{ k}\Omega \parallel (100)(100 \text{ }\Omega) = 2.57 \text{ k}\Omega$$

$$A_{v(1)} = \frac{2.57 \text{ k}\Omega}{112 \text{ }\Omega} = 23$$

$$R_{in(2)} = 22 \text{ k}\Omega \parallel (100)(1010 \text{ }\Omega) = 18 \text{ k}\Omega$$

$$V_{B(2)} = \left(\frac{18 \text{ k}\Omega}{51 \text{ k}\Omega} \right) 12 \text{ V} = 4.24, V_{E(1)} = 3.54 \text{ V}$$

$$I_{E(2)} = \frac{3.54 \text{ V}}{1.01 \text{ k}\Omega} = 3.51 \text{ mA}, r'_e = 7.13 \text{ }\Omega$$

$$R_{c(2)} = 3 \text{ k}\Omega \parallel 10 \text{ k}\Omega = 2.31 \text{ k}\Omega$$

$$A_{v(2)} = \frac{2.31 \text{ k}\Omega}{107.13 \text{ }\Omega} = 24 \text{ maximum}$$

$$A_{v(2)} = \frac{2.31 \text{ k}\Omega}{101 \text{ k}\Omega + 7.13 \text{ }\Omega} = 2.27 \text{ minimum}$$

$$A_{v(tot)} = (23)(24) = 552 \text{ maximum}$$

$$A_{v(tot)} = (23)(2.27) = 52.3 \text{ minimum}$$

This is a bit high, so adjust $R_{c(1)}$ to 3 kΩ, then

$$A_{v(1)} = \frac{3 \text{ k}\Omega \parallel 22 \text{ k}\Omega \parallel 33 \text{ k}\Omega \parallel 101 \text{ k}\Omega}{112 \text{ }\Omega} = 21.4$$

Now,

$$A_{v(tot)} = (21.3)(24) = 513 \text{ maximum}$$

$$A_{v(tot)} = (21.3)(2.27) = 48.5 \text{ minimum}$$

Thus, A_v is within 3% of the desired specifications.

Frequency response for stage 1:

$$R_{in} = 22 \text{ k}\Omega \parallel 100 \text{ k}\Omega \parallel 32 \text{ k}\Omega = 11.5 \text{ k}\Omega$$

$$f_{cl(in)} = \frac{1}{2\pi(11.5 \text{ k}\Omega)(10 \mu\text{F})} = 1.38 \text{ Hz}$$

$$R_{emitter} = 220 \text{ }\Omega \parallel (100 \text{ }\Omega + 11.7 \text{ }\Omega + (22 \text{ k}\Omega \parallel 100 \text{ k}\Omega/100)) = 125 \text{ }\Omega$$

$$f_{cl(bypass)} = \frac{1}{2\pi(125 \text{ }\Omega)(10 \mu\text{F})} = 12.7 \text{ Hz}$$

$$R_{out} = 3 \text{ k}\Omega + (33 \text{ k}\Omega \parallel 22 \text{ k}\Omega \parallel (100)(107 \text{ }\Omega)) = 8.91 \text{ k}\Omega$$

$$f_{cl(out)} = \frac{1}{2\pi(8.91 \text{ k}\Omega)(10 \mu\text{F})} = 1.79 \text{ Hz}$$

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Frequency response for stage 2:

$$f_{cl(in)} = 1.79 \text{ Hz} \text{ (same as } f_{cl(out)} \text{ for stage 1)}$$

$$R_{out} = 3 \text{ k}\Omega + 10 \text{ k}\Omega = 13 \text{ k}\Omega$$

$$f_{cl(out)} = \frac{1}{2\pi(13 \text{ k}\Omega)(10 \mu\text{F})} = 1.22 \text{ Hz}$$

This means that $C_{E(2)}$ is the frequency limiting capacitance.

$$R_{emitter} 910 \Omega \parallel (100 \Omega + 7 \Omega + (22 \text{ k}\Omega \parallel 33 \text{ k}\Omega \parallel 3 \text{ k}\Omega)/100) = 115 \Omega$$

For $f'_{cl} = 1 \text{ kHz}$:

$$C_{E(2)} = \frac{1}{2\pi(115 \Omega)(1 \text{ kHz})} = 1.38 \mu\text{F}$$

1.5 μF is the closest standard value and gives

$$f_{cl(bypass)} = \frac{1}{2\pi(115 \Omega)(1.5 \mu\text{F})} = 922 \text{ Hz}$$

This value can be moved closer to 1 kHz by using additional parallel bypass capacitors in stage 2 to fine-tune the response.

Multisim Troubleshooting Problems

The solutions showing instrument connections for Problems 45 through 48 are available from the Instructor Resource Center. See Chapter 1 for instructions. The faults in the circuit files may be accessed using the password *book* (all lowercase).

45. R_C open
46. Output capacitor open
47. R_2 open
48. Drain-source shorted

Chapter 11

Thyristors

Section 11-1 The Four-Layer Diode

1. $V_A = V_{BE} + V_{CE(sat)} = 0.7 \text{ V} + 0.2 \text{ V} = 0.9 \text{ V}$

$$V_{RS} = V_{BIAS} - V_A = 25 \text{ V} - 0.9 \text{ V} = 24.1 \text{ V}$$

$$I_A = \frac{V_{RS}}{R_S} = \frac{24.1 \text{ V}}{1.0 \text{ k}\Omega} = 24.1 \text{ mA}$$

2. (a) $R_{AK} = \frac{V_{AK}}{I_A} = \frac{15 \text{ V}}{1 \mu\text{A}} = 15 \text{ M}\Omega$

(b) From 15 V to 50 V for an increase of 35 V.

Section 11-2 The Silicon-Controlled Rectifier (SCR)

3. See Section 11-2 in the textbook.

4. Neglecting the SCR voltage drop,

$$R_{max} = \frac{30 \text{ V} - 0.7 \text{ V}}{10 \text{ mA}} = 2.93 \text{ k}\Omega$$

5. When the switch is closed, the battery V_2 causes illumination of the lamp. The light energy causes the LASCR to conduct and thus energize the relay. When the relay is energized, the contacts close and 115 V ac are applied to the motor.

6. See Figure 11-1.

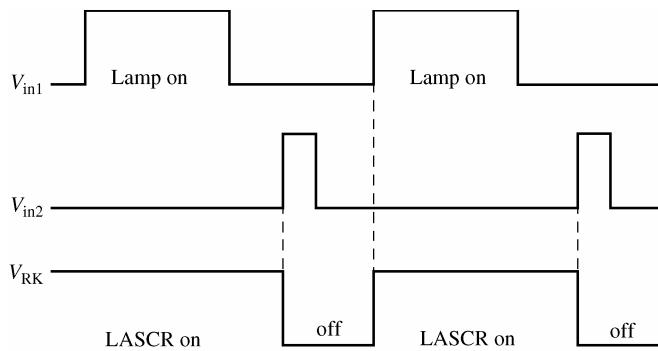


Figure 11-1

Chapter 11

Section 11-3 SCR Applications

7. Add a transistor to provide inversion of the negative half-cycle in order to obtain a positive gate trigger.
8. D_1 and D_2 are full-wave rectifier diodes.
9. See Figure 11-2.

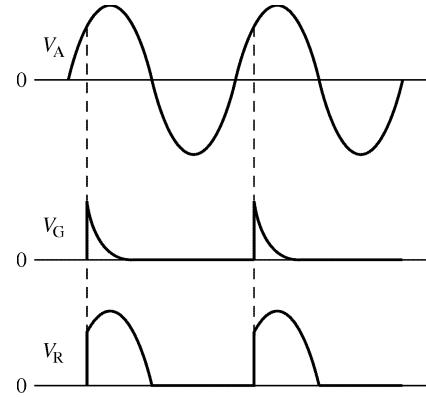


Figure 11-2

Section 11-4 The Diac and Triac

10. $V_{in(p)} = 1.414V_{in(rms)} = 1.414(25 \text{ V}) = 35.4 \text{ V}$

$$I_p = V_{in(p)} = \frac{35.35 \text{ V}}{1.0 \text{ k}\Omega} = 35.4 \text{ mA}$$

$$\text{Current at breakdown} = \frac{20 \text{ V}}{1.0 \text{ k}\Omega} = 20 \text{ mA}$$

See Figure 11-3.

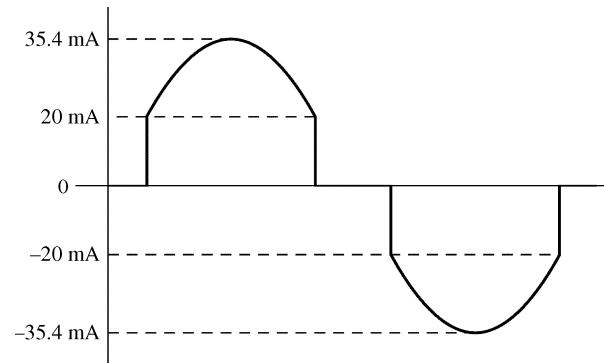


Figure 11-3

11. $I_p = \frac{15 \text{ V}}{4.7 \text{ k}\Omega} = 3.19 \text{ mA}$

See Figure 11-4.

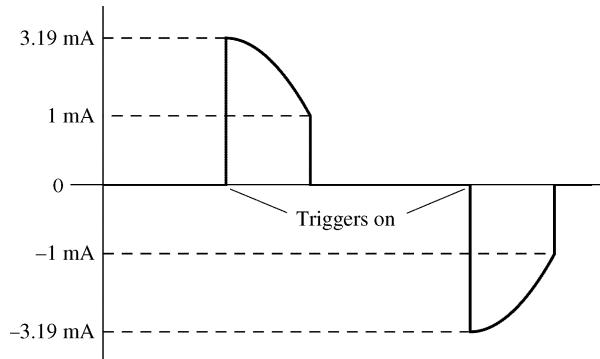


Figure 11-4

Section 11-5 The Silicon-Controlled Switch (SCS)

12. See Section 11-5 in the text.

13. Anode, cathode, anode gate, and cathode gate

Section 11-6 The Unijunction Transistor (UJT)

14. $\eta = \frac{r'_{B1}}{r'_{B1} + r'_{B2}} = \frac{2.5 \text{ k}\Omega}{2.5 \text{ k}\Omega + 4 \text{ k}\Omega} = 0.385$

15. $V_p = \eta V_{BB} + V_{pn} = 0.385(15 \text{ V}) + 0.7 \text{ V} = 6.48 \text{ V}$

16. $\frac{V_{BB} - V_v}{I_v} < R_1 < \frac{V_{BB} - V_p}{I_p}$
 $\frac{12 \text{ V} - 0.8 \text{ V}}{15 \text{ mA}} < R_1 < \frac{12 \text{ V} - 10 \text{ V}}{10 \mu\text{A}}$
 $747 \Omega < R_1 < 200 \text{ k}\Omega$

Section 11-7 The Programmable UJT (PUT)

17. (a) $V_A = \left(\frac{R_3}{R_2 + R_3} \right) V_B + 0.7 \text{ V} = \left(\frac{10 \text{ k}\Omega}{22 \text{ k}\Omega} \right) 20 \text{ V} + 0.7 \text{ V} = 9.79 \text{ V}$

(b) $V_A = \left(\frac{R_3}{R_2 + R_3} \right) V_B + 0.7 \text{ V} = \left(\frac{47 \text{ k}\Omega}{94 \text{ k}\Omega} \right) 9 \text{ V} + 0.7 \text{ V} = 5.2 \text{ V}$

Chapter 11

18. (a) From Problem 17(a), $V_A = 9.79$ V at turn on.

$$I = \frac{9.79 \text{ V}}{470 \Omega} = 20.8 \text{ mA at turn on}$$

$$I_p = \frac{10 \text{ V}}{470 \Omega} = 21.3 \text{ mA}$$

See Figure 11-5.

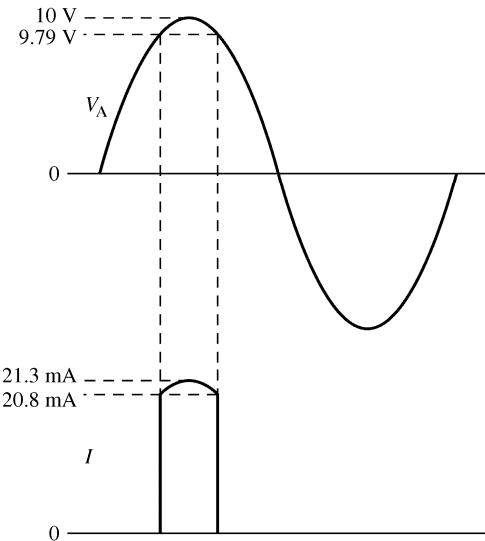


Figure 11-5

- (b) From Problem 17(b), $V_A = 5.2$ V at turn on.

$$I = \frac{5.2 \text{ V}}{330 \Omega} = 15.8 \text{ mA at turn on}$$

$$I_p = \frac{10 \text{ V}}{330 \Omega} = 30.3 \text{ mA}$$

See Figure 11-6.

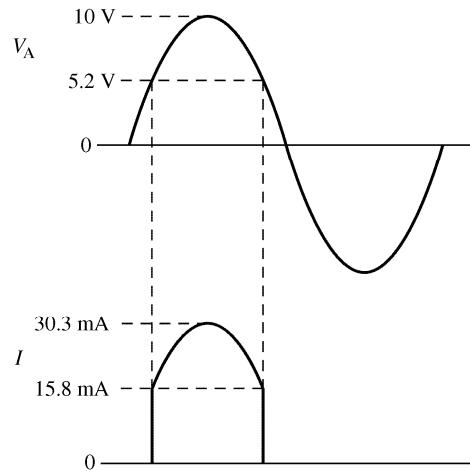


Figure 11-6

19. $V_A = \left(\frac{R_3}{R_2 + R_3} \right) 6 \text{ V} + 0.7 \text{ V} = \left(\frac{10 \text{ k}\Omega}{20 \text{ k}\Omega} \right) 6 \text{ V} + 0.7 \text{ V} = 3.7 \text{ V}$ at turn on

$V_{R1} \approx V_A = 3.7 \text{ V}$ at turn on.

See Figure 11-7.

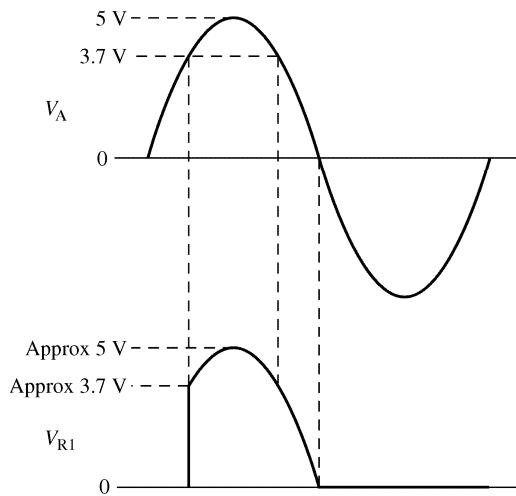


Figure 11-7

20. $V_A = \left(\frac{15 \text{ k}\Omega}{25 \text{ k}\Omega} \right) 6 \text{ V} + 0.7 \text{ V}$

= 4.3 V at turn on

$V_{R1} \approx V_A = 4.3 \text{ V}$

See Figure 11-8.

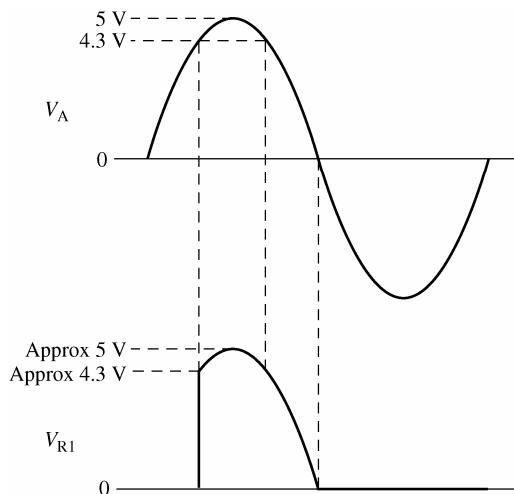


Figure 11-8

Application Activity Problems

21. The motor runs fastest at **0 V** for the motor speed control circuit.
22. If the rheostat resistance decreases, the SCR turns on **earlier** in the ac cycle.
23. As the PUT gate voltage increases in the circuit, the PUT triggers on later in the ac cycle causing the SCR to fire later in the cycle, conduct for a shorter time, and decrease the power to the motor.

Chapter 11

Advanced Problems

24. D_1 : 15 V zener (1N4744)

R_1 : 100 Ω , 1 W

R_2 : 100 Ω , 1 W

Q_1 : Any SCR with a 1 A minimum rating (1.5 A would be better)

R_3 : 150 Ω , 1 W

25. See Figure 11-9.

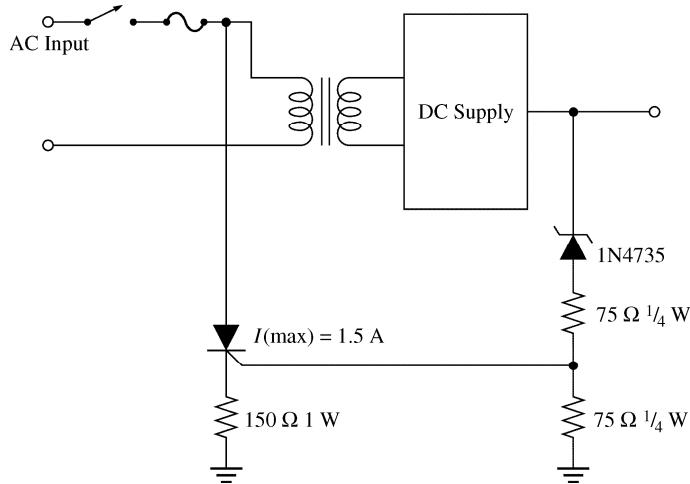


Figure 11-9

$$V_p = \eta V_{BB} + V_{pn} = (0.75)(12 \text{ V}) + 0.7 \text{ V} = 9.7 \text{ V}$$

$$I_v = 10 \text{ mA} \text{ and } I_p = 20 \mu\text{A}$$

$$R_1 < \frac{12 \text{ V} - 9.7 \text{ V}}{20 \mu\text{A}} = 115 \text{ k}\Omega$$

$$R_1 > \frac{12 \text{ V} - 1 \text{ V}}{10 \text{ mA}} = 1.1 \text{ k}\Omega$$

Select $R_1 = 51 \text{ k}\Omega$ as an intermediate value.

During the charging cycle:

$$V(t) = V_F - (V_F - V_0)e^{-t_1/R_1 C}$$

$$9.7 \text{ V} = 12 \text{ V} - (12 \text{ V} - 1 \text{ V})e^{-t_1/R_1 C}$$

$$-\frac{t_1}{R_1 C} = \ln\left(\frac{2.3 \text{ V}}{11 \text{ V}}\right)$$

$$t_1 = -R_1 C \ln\left(\frac{2.3 \text{ V}}{11 \text{ V}}\right) = 1.56 R_1 C = 79.8 \times 10^3 C$$

During the discharging cycle (assuming $R_2 \gg R_{B1}$):

$$V(t) = V_F - (V_F - V_0)e^{-t_2/R_2C}$$

$$1 \text{ V} = 0 \text{ V} - (0 \text{ V} - 9.3 \text{ V})e^{-t_2/R_2C}$$

$$-\frac{t_2}{R_2C} = \ln\left(\frac{1 \text{ V}}{9.3 \text{ V}}\right)$$

$$t_2 = -R_2C \ln\left(\frac{1 \text{ V}}{9.3 \text{ V}}\right) = 2.23R_2C$$

Let $R_2 = 100 \text{ k}\Omega$, so $t_2 = 223 \times 10^3 C$.

Since $f = 2.5 \text{ kHz}$, $T = 400 \mu\text{s}$

$$T = t_1 + t_2 = 79.8 \times 10^3 C + 223 \times 10^3 C = 303 \times 10^3 C = 400 \mu\text{s}$$

$$C = \frac{400 \mu\text{s}}{303 \times 10^3} = 0.0013 \mu\text{F}$$

See Figure 11-10.

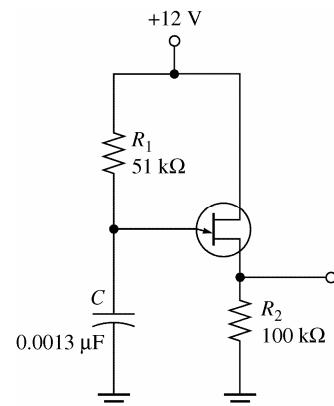


Figure 11-10

Multisim Troubleshooting Problems

The solutions showing instrument connections for Problems 27 through 29 are available from the Instructor Resource Center. See Chapter 1 for instructions. The faults in the circuit files may be accessed using the password *book* (all lowercase).

- 27. Cathode-anode shorted
- 28. Gate-cathode open
- 29. R_1 shorted

Chapter 12

The Operational Amplifier

Section 12-1 Introduction to Operational Amplifiers

1. *Practical op-amp:* High open-loop gain, high input impedance, low output impedance, and high CMRR.
Ideal op-amp: Infinite open-loop gain, infinite input impedance, zero output impedance, and infinite CMRR.
2. Op amp 2 is more desirable because it has a higher input impedance, a lower output impedance, and a higher open-loop gain.

Section 12-2 Op-Amp Input Modes and Parameters

3. (a) Single-ended differential input
(b) Double-ended differential input
(c) Common-mode
4. CMRR (dB) = $20 \log(250,000) = 108 \text{ dB}$
5. $\text{CMRR (dB)} = 20 \log\left(\frac{A_{ol}}{A_{cm}}\right) = 20 \log\left(\frac{175,000}{0.18}\right) = 120 \text{ dB}$
6. $\text{CMRR} = \frac{A_{ol}}{A_{cm}}$
 $A_{cm} = \frac{A_{ol}}{\text{CMRR}} = \frac{90,000}{300,000} = 0.3$
7. $I_{BIAS} = \frac{8.3 \mu\text{A} + 7.9 \mu\text{A}}{2} = 8.1 \mu\text{A}$
8. Input bias current is the average of the two input currents. Input offset current is the difference between the two input currents.
 $I_{OS} = |8.3 \mu\text{A} - 7.9 \mu\text{A}| = 400 \text{ nA}$
9. Slew rate = $\frac{24 \text{ V}}{15 \mu\text{s}} = 1.6 \text{ V}/\mu\text{s}$
10. $\Delta t = \frac{\Delta V_{out}}{\text{slew rate}} = \frac{20 \text{ V}}{0.5 \text{ V}/\mu\text{s}} = 40 \mu\text{s}$

Section 12-4 Op-Amps with Negative Feedback

- 11.** (a) Voltage-follower
 (b) Noninverting
 (c) Inverting

12. $B = \frac{R_i}{R_i + R_f} = \frac{1.0 \text{ k}\Omega}{101 \text{ k}\Omega} = 9.90 \times 10^{-3}$
 $V_f = BV_{out} = (9.90 \times 10^{-3})5 \text{ V} = 0.0495 \text{ V} = 49.5 \text{ mV}$

13. (a) $A_{cl(NI)} = \frac{1}{B} = \frac{1}{1.5 \text{ k}\Omega / 561.5 \text{ k}\Omega} = 374$
 (b) $V_{out} = A_{cl(NI)}V_{in} = (374)(10 \text{ mV}) = 3.74 \text{ V rms}$
 (c) $V_f = \left(\frac{1.5 \text{ k}\Omega}{561.5 \text{ k}\Omega} \right) 3.74 \text{ V} = 9.99 \text{ mV rms}$

14. (a) $A_{cl(NI)} = \frac{1}{B} = \frac{1}{4.7 \text{ k}\Omega / 51.7 \text{ k}\Omega} = 11$
 (b) $A_{cl(NI)} = \frac{1}{B} = \frac{1}{10 \text{ k}\Omega / 1.01 \text{ M}\Omega} = 101$
 (c) $A_{cl(NI)} = \frac{1}{B} = \frac{1}{4.7 \text{ k}\Omega / 224.7 \text{ k}\Omega} = 47.8$
 (d) $A_{cl(NI)} = \frac{1}{B} = \frac{1}{1.0 \text{ k}\Omega / 23 \text{ k}\Omega} = 23$

15. (a) $1 + \frac{R_f}{R_i} = A_{cl(NI)}$
 $R_f = R_i(A_{cl(NI)} - 1) = 1.0 \text{ k}\Omega(50 - 1) = 49 \text{ k}\Omega$
 (b) $\frac{R_f}{R_i} = A_{cl(I)}$
 $R_f = -R_i(A_{cl(I)}) = -10 \text{ k}\Omega(-300) = 3 \text{ M}\Omega$
 (c) $R_f = R_i(A_{cl(NI)} - 1) = 12 \text{ k}\Omega(7) = 84 \text{ k}\Omega$
 (d) $R_f = -R_i(A_{cl(I)}) = -2.2 \text{ k}\Omega(-75) = 165 \text{ k}\Omega$

16. (a) $A_{cl(VF)} = 1$
 (b) $A_{cl(I)} = -\left(\frac{R_f}{R_i} \right) = -\left(\frac{100 \text{ k}\Omega}{100 \text{ k}\Omega} \right) = -1$
 (c) $A_{cl(NI)} = \frac{1}{\left(\frac{R_i}{R_i + R_f} \right)} = \frac{1}{\left(\frac{47 \text{ k}\Omega}{47 \text{ k}\Omega + 1.0 \text{ M}\Omega} \right)} = 22$
 (d) $A_{cl(I)} = -\left(\frac{R_f}{R_i} \right) = -\left(\frac{330 \text{ k}\Omega}{33 \text{ k}\Omega} \right) = -10$

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17. (a) $V_{out} \cong V_{in} = 10 \text{ mV, in phase}$

(b) $V_{out} = A_{cl}V_{in} = -\left(\frac{R_f}{R_i}\right)V_{in} = -(1)(10 \text{ mV}) = -10 \text{ mV, } 180^\circ \text{ out of phase}$

(c) $V_{out} = V_{in} = \left(\frac{1}{\left(\frac{R_i}{R_i + R_f}\right)}\right)V_{in} = \left(\frac{1}{\left(\frac{47 \text{ k}\Omega}{1047 \text{ k}\Omega}\right)}\right)10 \text{ mV} = 223 \text{ mV, in phase}$

(d) $V_{out} = -\left(\frac{R_f}{R_i}\right)V_{in} = -\left(\frac{330 \text{ k}\Omega}{33 \text{ k}\Omega}\right)10 \text{ mV} = -100 \text{ mV, } 180^\circ \text{ out of phase}$

18. (a) $I_{in} = \frac{V_{in}}{R_{in}} = \frac{1 \text{ V}}{2.2 \text{ k}\Omega} = 455 \mu\text{A}$

(b) $I_f \cong I_{in} = 455 \mu\text{A}$

(c) $V_{out} = -I_f R_f = -(455 \mu\text{A})(22 \text{ k}\Omega) = -10 \text{ V}$

(d) $A_{cl(I)} = -\left(\frac{R_f}{R_i}\right) = -\left(\frac{22 \text{ k}\Omega}{2.2 \text{ k}\Omega}\right) = -10$

Section 12-5 Effects of Negative Feedback on Op-Amp Impedances

19. (a) $B = \frac{2.7 \text{ k}\Omega}{562.5 \text{ k}\Omega} = 0.0048$

$$Z_{in(NI)} = (1 + A_{ol})Z_{in} = [1 + (175,000)(0.0048)]10 \text{ M}\Omega = 8.41 \text{ G}\Omega$$

$$Z_{out(NI)} = \frac{Z_{out}}{1 + A_{ol}B} = \frac{75 \Omega}{1 + (175,000)(0.0048)} = 89.2 \text{ m}\Omega$$

(b) $B = \frac{1.5 \text{ k}\Omega}{48.5 \text{ k}\Omega} = 0.031$

$$Z_{in(NI)} = (1 + A_{ol}B)Z_{in} = [1 + (200,000)(0.031)]1 \text{ M}\Omega = 6.20 \text{ G}\Omega$$

$$Z_{out(NI)} = \frac{Z_{out}}{1 + A_{ol}B} = \frac{25 \Omega}{1 + (200,000)(0.031)} = 4.04 \text{ m}\Omega$$

(c) $B = \frac{56 \text{ k}\Omega}{1.056 \text{ M}\Omega} = 0.053$

$$Z_{in(NI)} = (1 + A_{ol}B)Z_{in} = [1 + (50,000)(0.053)]2 \text{ M}\Omega = 5.30 \text{ G}\Omega$$

$$Z_{out(NI)} = \frac{Z_{out}}{1 + A_{ol}B} = \frac{50 \Omega}{1 + (50,000)(0.053)} = 19.0 \text{ m}\Omega$$

20. (a) $Z_{in(VF)} = (1 + A_{ol})Z_{in} = (1 + 220,000)6 \text{ M}\Omega = 1.32 \times 10^{12} \Omega = 1.32 \text{ T}\Omega$

$$Z_{out(VF)} = \frac{Z_{out}}{1 + A_{ol}} = \frac{100 \Omega}{1 + 220,000} = 455 \mu\Omega$$

(b) $Z_{in(VF)} = (1 + A_{ol})Z_{in} = (1 + 100,000)5 \text{ M}\Omega = 5 \times 10^{11} \Omega = 500 \text{ G}\Omega$

$$Z_{out(VF)} = \frac{Z_{out}}{1 + A_{ol}} = \frac{60 \Omega}{1 + 100,000} = 600 \mu\Omega$$

(c) $Z_{in(VF)} = (1 + A_{ol})Z_{in} = (1 + 50,000)800 \text{ k}\Omega = 40 \text{ G}\Omega$

$$Z_{out(VF)} = \frac{Z_{out}}{1 + A_{ol}} = \frac{75 \Omega}{1 + 500,000} = 1.5 \text{ m}\Omega$$

21. (a) $Z_{in(I)} \cong R_i = 10 \text{ k}\Omega$

$$B = \frac{R_i}{R_i + R_f} = \frac{10 \text{ k}\Omega}{160 \text{ k}\Omega} = 0.0625$$

$$Z_{out(I)} = \frac{Z_{out}}{1 + A_{ol}B} = \frac{40 \Omega}{1 + (125,000)(0.0625)} = 5.12 \text{ m}\Omega$$

(b) $Z_{in(I)} \cong R_i = 100 \text{ k}\Omega$

$$B = \frac{100 \text{ k}\Omega}{1.1 \text{ M}\Omega} = 0.091$$

$$Z_{out(I)} = \frac{Z_{out}}{1 + A_{ol}B} = \frac{50 \Omega}{1 + (75,000)(0.91)} = 7.32 \text{ m}\Omega$$

(c) $Z_{in(I)} \cong R_i = 470 \Omega$

$$B = \frac{470 \Omega}{10,470 \Omega} = 0.045$$

$$Z_{out(I)} = \frac{Z_{out}}{1 + A_{ol}B} = \frac{70 \Omega}{1 + (250,000)(0.045)} = 6.22 \text{ m}\Omega$$

Section 12-6 Bias Current and Offset Voltage

22. (a) $R_{comp} = R_{in} = 75 \Omega$ placed in the feedback path.

$$I_{OS} = |42 \mu\text{A} - 40 \mu\text{A}| = 2 \mu\text{A}$$

(b) $V_{OUT(error)} = A_v I_{OS} R_{in} = (1)(2 \mu\text{A})(75 \Omega) = 150 \mu\text{V}$

23. (a) $R_c = R_i \parallel R_f = 2.7 \text{ k}\Omega \parallel 560 \text{ k}\Omega = 2.69 \text{ k}\Omega$

(b) $R_c = R_i \parallel R_f = 1.5 \text{ k}\Omega \parallel 47 \text{ k}\Omega = 1.45 \text{ k}\Omega$

(c) $R_c = R_i \parallel R_f = 56 \text{ k}\Omega \parallel 1.0 \text{ M}\Omega = 53 \text{ k}\Omega$

See Figure 12-1.

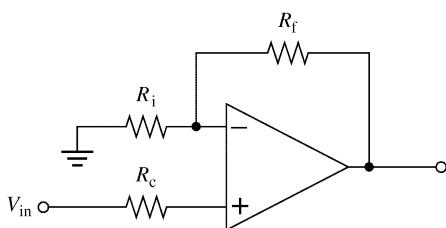


Figure 12-1

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24. $V_{\text{OUT(error)}} = A_v V_{\text{IO}} = (1)(2 \text{ nV}) = \mathbf{2 \text{ nV}}$

25. $V_{\text{OUT(error)}} = (1 + A_{ol})V_{\text{IO}}$
 $V_{\text{IO}} = \frac{V_{\text{OUT(error)}}}{A_{ol}} = \frac{35 \text{ mV}}{200,000} = \mathbf{175 \text{ nV}}$

Section 12-7 Open-Loop Response

26. $A_{cl} = 120 \text{ dB} - 50 \text{ dB} = \mathbf{70 \text{ dB}}$

27. The gain is ideally **175,000** at 200 Hz. The midrange dB gain is

$$20 \log(175,000) = 105 \text{ dB}$$

The actual gain at 200 Hz is

$$A_{v(\text{dB})} = 105 \text{ dB} - 3 \text{ dB} = 102 \text{ dB}$$

$$A_v = \log^{-1}\left(\frac{102}{20}\right) = \mathbf{125,892}$$

$$BW_{ol} = \mathbf{200 \text{ Hz}}$$

28. $\frac{f_c}{f} = \frac{X_C}{R}$

$$X_C = \frac{Rf_c}{f} = \frac{(1.0 \text{ k}\Omega)(5 \text{ kHz})}{3 \text{ kHz}} = \mathbf{1.67 \text{ k}\Omega}$$

29. (a) $\frac{V_{out}}{V_{in}} = \frac{1}{\sqrt{1 + \left(\frac{f}{f_c}\right)^2}} = \frac{1}{\sqrt{1 + \left(\frac{1 \text{ kHz}}{12 \text{ kHz}}\right)^2}} = \mathbf{0.997}$

(b) $\frac{V_{out}}{V_{in}} = \frac{1}{\sqrt{1 + \left(\frac{f}{f_c}\right)^2}} = \frac{1}{\sqrt{1 + \left(\frac{5 \text{ kHz}}{12 \text{ kHz}}\right)^2}} = \mathbf{0.923}$

(c) $\frac{V_{out}}{V_{in}} = \frac{1}{\sqrt{1 + \left(\frac{f}{f_c}\right)^2}} = \frac{1}{\sqrt{1 + \left(\frac{12 \text{ kHz}}{12 \text{ kHz}}\right)^2}} = \mathbf{0.707}$

(d) $\frac{V_{out}}{V_{in}} = \frac{1}{\sqrt{1 + \left(\frac{f}{f_c}\right)^2}} = \frac{1}{\sqrt{1 + \left(\frac{20 \text{ kHz}}{12 \text{ kHz}}\right)^2}} = \mathbf{0.515}$

(e) $\frac{V_{out}}{V_{in}} = \frac{1}{\sqrt{1 + \left(\frac{f}{f_c}\right)^2}} = \frac{1}{\sqrt{1 + \left(\frac{100 \text{ kHz}}{12 \text{ kHz}}\right)^2}} = \mathbf{0.119}$

30. (a) $A_{ol} = \frac{A_{ol(mid)}}{\sqrt{1 + \left(\frac{f}{f_{c(ol)}}\right)^2}} = \frac{80,000}{\sqrt{1 + \left(\frac{100 \text{ Hz}}{1 \text{ kHz}}\right)^2}} = 79,603$

(b) $A_{ol} = \frac{A_{ol(mid)}}{\sqrt{1 + \left(\frac{f}{f_{c(ol)}}\right)^2}} = \frac{80,000}{\sqrt{1 + \left(\frac{1 \text{ kHz}}{1 \text{ kHz}}\right)^2}} = 56,569$

(c) $A_{ol} = \frac{A_{ol(mid)}}{\sqrt{1 + \left(\frac{f}{f_{c(ol)}}\right)^2}} = \frac{80,000}{\sqrt{1 + \left(\frac{10 \text{ kHz}}{1 \text{ kHz}}\right)^2}} = 7960$

(d) $A_{ol} = \frac{A_{ol(mid)}}{\sqrt{1 + \left(\frac{f}{f_{c(ol)}}\right)^2}} = \frac{80,000}{\sqrt{1 + \left(\frac{1 \text{ MHz}}{1 \text{ kHz}}\right)^2}} = 80$

31. (a) $f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi(10 \text{ k}\Omega)(0.01 \mu\text{F})} = 1.59 \text{ kHz}; \theta = \tan^{-1}\left(\frac{f}{f_c}\right) = \tan^{-1}\left(\frac{2 \text{ kHz}}{1.59 \text{ kHz}}\right) = -51.5^\circ$

(b) $f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi(1.0 \text{ k}\Omega)(0.01 \mu\text{F})} = 15.9 \text{ kHz}; \theta = \tan^{-1}\left(\frac{f}{f_c}\right) = \tan^{-1}\left(\frac{2 \text{ kHz}}{15.9 \text{ kHz}}\right) = -7.17^\circ$

(c) $f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi(100 \text{ k}\Omega)(0.01 \mu\text{F})} = 159 \text{ Hz}; \theta = \tan^{-1}\left(\frac{f}{f_c}\right) = \tan^{-1}\left(\frac{2 \text{ kHz}}{159 \text{ Hz}}\right) = -85.5^\circ$

32. (a) $\theta = \tan^{-1}\left(\frac{f}{f_c}\right) = \tan^{-1}\left(\frac{100 \text{ Hz}}{8.5 \text{ kHz}}\right) = -0.674^\circ$

(b) $\theta = \tan^{-1}\left(\frac{f}{f_c}\right) = \tan^{-1}\left(\frac{400 \text{ Hz}}{8.5 \text{ kHz}}\right) = -2.69^\circ$

(c) $\theta = \tan^{-1}\left(\frac{f}{f_c}\right) = \tan^{-1}\left(\frac{850 \text{ Hz}}{8.5 \text{ kHz}}\right) = -5.71^\circ$

(d) $\theta = \tan^{-1}\left(\frac{f}{f_c}\right) = \tan^{-1}\left(\frac{8.5 \text{ kHz}}{8.5 \text{ kHz}}\right) = -45.0^\circ$

(e) $\theta = \tan^{-1}\left(\frac{f}{f_c}\right) = \tan^{-1}\left(\frac{25 \text{ kHz}}{8.5 \text{ kHz}}\right) = -71.2^\circ$

(f) $\theta = \tan^{-1}\left(\frac{f}{f_c}\right) = \tan^{-1}\left(\frac{85 \text{ kHz}}{8.5 \text{ kHz}}\right) = -84.3^\circ$

See Figure 12-2.

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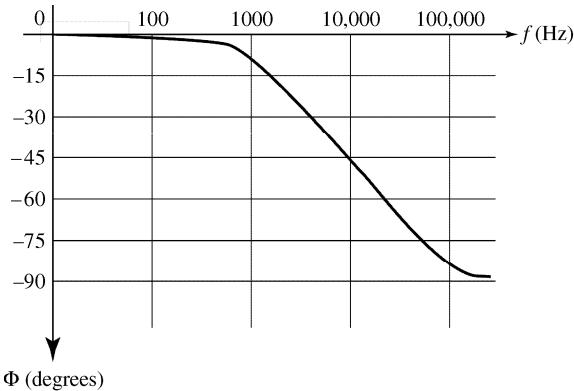


Figure 12-2

33. (a) $A_{ol(mid)} = 30 \text{ dB} + 40 \text{ dB} + 20 \text{ dB} = \mathbf{90 \text{ dB}}$

$$(b) \theta_1 = -\tan^{-1}\left(\frac{f}{f_c}\right) = -\tan^{-1}\left(\frac{10 \text{ kHz}}{600 \text{ Hz}}\right) = -86.6^\circ$$

$$\theta_2 = -\tan^{-1}\left(\frac{f}{f_c}\right) = -\tan^{-1}\left(\frac{10 \text{ kHz}}{50 \text{ kHz}}\right) = -11.3^\circ$$

$$\theta_3 = -\tan^{-1}\left(\frac{f}{f_c}\right) = -\tan^{-1}\left(\frac{10 \text{ kHz}}{200 \text{ kHz}}\right) = -2.86^\circ$$

$$\theta_{tot} = -86.6^\circ - 11.3^\circ - 2.86^\circ - 180^\circ = \mathbf{-281^\circ}$$

34. (a) 0 dB/decade
 (b) -20 dB/decade
 (c) -40 dB/decade
 (d) -60 dB/decade

Section 12-8 Closed-Loop Frequency Response

35. (a) $A_{cl(I)} = -\left(\frac{R_f}{R_i}\right) = -\left(\frac{68 \text{ k}\Omega}{2.2 \text{ k}\Omega}\right) = -30.9; \quad A_{cl(I)} (\text{dB}) = 20 \log(30.9) = \mathbf{29.8 \text{ dB}}$

$$(b) A_{cl(NI)} = \frac{1}{B} = \frac{1}{15 \text{ k}\Omega / 235 \text{ k}\Omega} = 15.7; \quad A_{cl(NI)} (\text{dB}) = 20 \log(15.7) = \mathbf{23.9 \text{ dB}}$$

(c) $A_{cl(VF)} = 1; A_{cl(VF)}(\text{dB}) = 20 \log(1) = \mathbf{0 \text{ dB}}$
 These are all closed-loop gains.

36. $BW_{cl} = BW_{ol}(1 + BA_{ol(mid)}) = 1500 \text{ Hz}[1 + (0.015)(180,000)] = \mathbf{4.05 \text{ MHz}}$

37. A_{ol} (dB) = 89 dB

$$A_{ol} = 28,184$$

$$A_c f_{c(cl)} = A_{ol} f_{c(ol)}$$

$$A_{cl} = \frac{A_{ol} f_{c(ol)}}{f_{c(cl)}} = \frac{(28,184)(750 \text{ Hz})}{5.5 \text{ kHz}} = 3843$$

$$A_{cl}$$
 (dB) = 20 log(3843) = **71.7 dB**

38. $A_{cl} = \frac{A_{ol} f_{c(ol)}}{f_{c(cl)}} = \frac{(28,184)(750 \text{ Hz})}{5.5 \text{ kHz}} = 3843$

$$f_T = A_c f_{c(cl)} = (3843)(5.5 \text{ kHz}) = **21.1 MHz**$$

39. (a) $A_{cl(VF)} = 1$

$$BW = f_{c(cl)} = \frac{f_T}{A_{cl}} = \frac{28 \text{ MHz}}{1} = **2.8 MHz**$$

(b) $A_{cl(I)} = -\frac{100 \text{ k}\Omega}{2.2 \text{ k}\Omega} = **-45.5**$

$$BW = \frac{2.8 \text{ MHz}}{45.5} = **61.6 kHz**$$

(c) $A_{cl(NI)} = 1 + \frac{12 \text{ k}\Omega}{1.0 \text{ k}\Omega} = **13**$

$$BW = \frac{2.8 \text{ MHz}}{13} = **215 kHz**$$

(d) $A_{cl(I)} = -\frac{1 \text{ M}\Omega}{5.6 \text{ k}\Omega} = **-179**$

$$BW = \frac{2.8 \text{ MHz}}{179} = **15.7 kHz**$$

40. (a) $A_{cl} = \frac{150 \text{ k}\Omega}{22 \text{ k}\Omega} = 6.8$

$$f_{c(cl)} = \frac{A_{ol} f_{c(ol)}}{A_{cl}} = \frac{(120,000)(150 \text{ Hz})}{6.8} = 2.65 \text{ MHz}$$

$$BW = f_{c(cl)} = **2.65 MHz**$$

(b) $A_{cl} = \frac{1.0 \text{ M}\Omega}{10 \text{ k}\Omega} = 100$

$$f_{c(cl)} = \frac{A_{ol} f_{c(ol)}}{A_{cl}} = \frac{(195,000)(50 \text{ Hz})}{100} = 97.5 \text{ kHz}$$

$$BW = f_{c(cl)} = **97.5 kHz**$$

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Section 12-9 Troubleshooting

41. (a) Faulty op-amp or open R_1
(b) R_2 open, forcing open-loop operation
42. (a) Circuit becomes a voltage-follower and the output replicates the input.
(b) Output will saturate.
(c) No effect on the ac; may add or subtract a small dc voltage to the output.
(d) The voltage gain will change from 10 to 0.1.
43. The gain becomes a fixed -100 with no effect as the potentiometer is adjusted.

Application Activity Problems

44. The push-pull stage will operate nonlinearly if a diode is shorted, a transistor is faulty, or the op-amp stage has excessive gain.
45. If a $100\text{ k}\Omega$ resistor is used for R_2 , the gain of the op amp will be reduced by a factor of 100.
46. If D_1 opens, the positive half of the signal will appear on the output through Q_3 and Q_4 . The negative half is missing due to the open diode.

Datasheet Problems

47. From the datasheet of textbook Figure 12-77:
$$B = \frac{470\text{ }\Omega}{47\text{ k}\Omega + 470\text{ }\Omega} = 0.0099$$

 $A_{ol} = 200,000$ (typical)
 $Z_{in} = 2.0\text{ M}\Omega$ (typical)
 $Z_{in(NI)} = (1 + 0.0099)(200,000)(2\text{ M}\Omega) = (1 + 1980)2\text{ M}\Omega = \mathbf{3.96\text{ G}\Omega}$
48. From the datasheet in Figure 12-77:
$$Z_{in(I)} = R_i = \frac{R_f}{A_{cl}} = \frac{100\text{ k}\Omega}{100} = \mathbf{1\text{ k}\Omega}$$
49. $A_{ol} = 50\text{ V/mV} = \frac{50\text{ V}}{1\text{ mV}} = \frac{50,000\text{ V}}{1\text{ V}} = \mathbf{50,000}$
50. Slew rate = $0.5\text{ V}/\mu\text{s}$
 $\Delta V = 8\text{ V} - (-8\text{ V}) = 16\text{ V}$
$$\Delta t = \frac{16\text{ V}}{0.5\text{ V}/\mu\text{s}} = \mathbf{32\text{ }\mu\text{s}}$$

Advanced Problems

- 51.** Using available standard values of $R_f = 150 \text{ k}\Omega$ and $R_i = 1.0 \text{ k}\Omega$,

$$A_v = 1 + \frac{150 \text{ k}\Omega}{1.0 \text{ k}\Omega} = 151$$

$$B = \frac{1.0 \text{ k}\Omega}{151 \text{ k}\Omega} = 6.62 \times 10^{-3}$$

$$Z_{in(\text{NI})} = (1 + (6.62 \times 10^{-3})(50,000))300 \text{ k}\Omega = 99.6 \text{ M}\Omega$$

The compensating resistor is

$$R_c = R_i \parallel R_f = 150 \text{ k}\Omega \parallel 1.0 \text{ k}\Omega = 993 \text{ }\Omega$$

See Figure 12-3.

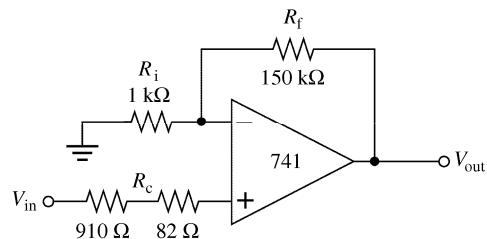


Figure 12-3

- 52.** See Figure 12-4. 2% tolerance resistors are used to achieve a 5% gain tolerance.

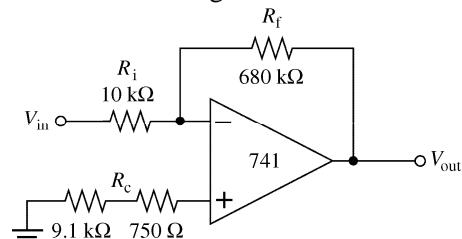


Figure 12-4

- 53.** From textbook Figure 12-78:

$$f_c = 10 \text{ kHz at } A_v = 40 \text{ dB} = 100$$

In this circuit

$$A_v = 1 + \frac{33 \text{ k}\Omega}{333 \text{ }\Omega} = 100.1 \approx 100$$

The compensating resistor is

$$R_c = 33 \text{ k}\Omega \parallel 333 \text{ }\Omega = 330 \text{ }\Omega$$

See Figure 12-5.

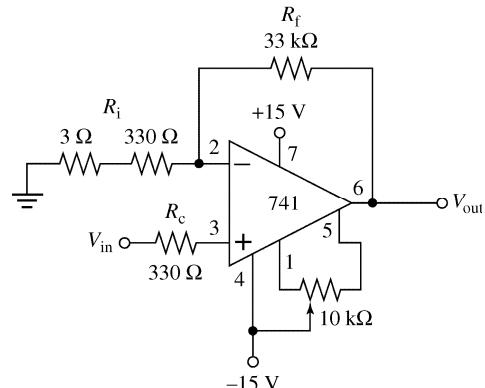


Figure 12-5

Chapter 12

54. From textbook Figure 12-79:

For a ± 10 V output swing minimum, the load must be 600Ω for a ± 10 V and $\approx 620 \Omega$ for -10 V. So, the minimum load is **620 Ω** .

55. For the amplifier,

$$A_v = -\frac{100 \text{ k}\Omega}{2 \text{ k}\Omega} = -50$$

The compensating resistor is

$$R_c = 100 \text{ k}\Omega \parallel 2 \text{ k}\Omega = 1.96 \text{ k}\Omega \approx 2 \text{ k}\Omega$$

See Figure 12-6.

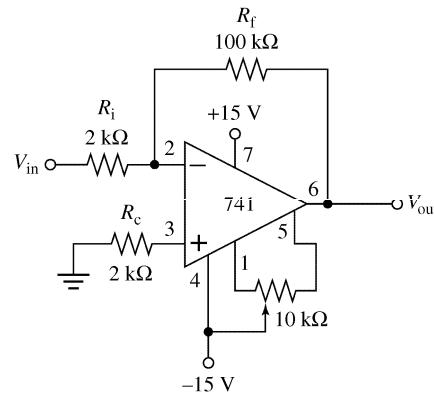


Figure 12-6

56. From textbook Figure 12-78 the maximum 741 closed loop gain with $BW = 5$ kHz is approximately $60 \text{ dB} - (20 \text{ dB})\log(5 \text{ kHz}/1 \text{ kHz}) = 60 \text{ dB} - (20 \text{ dB})(0.7) = \mathbf{46 \text{ dB}}$

$$A_{v(\text{dB})} = 20 \log A_v$$

$$A_v = \log^{-1}\left(\frac{A_{v(\text{dB})}}{20}\right) = \log^{-1}\left(\frac{46}{20}\right) = \mathbf{200}$$

Multisim Troubleshooting Problems

The solutions showing instrument connections for Problems 57 through 72 are available from the Instructor Resource Center. See Chapter 1 for instructions. The faults in the circuit files may be accessed using the password *book* (all lowercase).

57. R_f open

58. R_i open

59. R_f leaky

60. R_i shorted

61. R_f shorted

62. Op-amp input to output open

63. R_f leaky

64. R_i leaky

65. R_i shorted

66. R_i open

67. R_f open

68. R_f leaky

69. R_f open

70. R_f shorted

71. R_i open

72. R_i leaky

Chapter 13

Basic Op-Amp Circuits

Section 13-1 Comparators

1. $V_{out(p)} = A_{ol}V_{in} = (80,000)(0.15 \text{ mV})(1.414) = 17 \text{ V}$

Since 12 V is the peak limit, the op-amp saturates.

$V_{out(pp)} = 24 \text{ V}$ with distortion due to clipping.

2. (a) Maximum negative

- (b) Maximum positive

- (c) Maximum negative

3. $V_{UTP} = \left(\frac{R_2}{R_1 + R_2} \right) (+10 \text{ V}) = \left(\frac{18 \text{ k}\Omega}{65 \text{ k}\Omega} \right) 10 \text{ V} = 2.77 \text{ V}$

$$V_{LTP} = \left(\frac{R_2}{R_1 + R_2} \right) (-10 \text{ V}) = \left(\frac{18 \text{ k}\Omega}{65 \text{ k}\Omega} \right) (-10 \text{ V}) = -2.77 \text{ V}$$

4. $V_{HYS} = V_{UTP} - V_{LTP} = 2.77 \text{ V} - (-2.77 \text{ V}) = 5.54 \text{ V}$

5. See Figure 13-1.

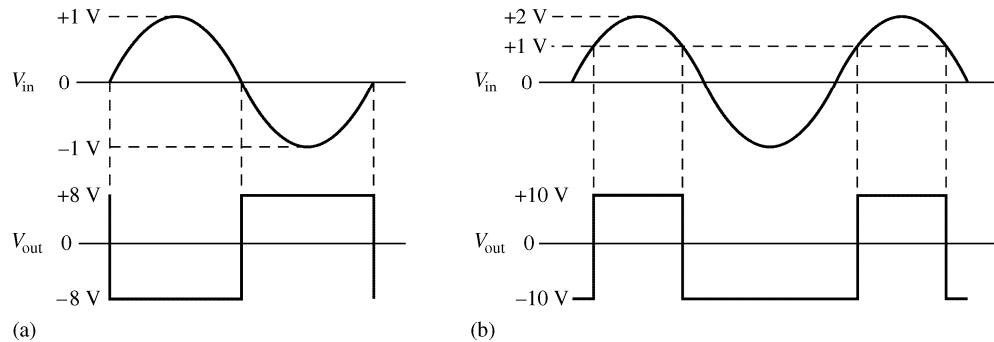


Figure 13-1

6. (a) $V_{\text{UTP}} = \left(\frac{R_2}{R_1 + R_2} \right) (+V_{\text{out(max)}}) = \left(\frac{18 \text{ k}\Omega}{51 \text{ k}\Omega} \right) 11 \text{ V} = 3.88 \text{ V}$

$$V_{\text{LTP}} = -3.88 \text{ V}$$

$$V_{\text{HYS}} = V_{\text{UTP}} - V_{\text{LTP}} = 3.88 \text{ V} - (-3.88 \text{ V}) = \mathbf{7.76 \text{ V}}$$

(b) $V_{\text{UTP}} = \left(\frac{R_2}{R_1 + R_2} \right) (+V_{\text{out(max)}}) = \left(\frac{68 \text{ k}\Omega}{218 \text{ k}\Omega} \right) 11 \text{ V} = 3.43 \text{ V}$

$$V_{\text{LTP}} = -3.43 \text{ V}$$

$$V_{\text{HYS}} = V_{\text{UTP}} - V_{\text{LTP}} = 3.43 \text{ V} - (-3.43 \text{ V}) = \mathbf{6.86 \text{ V}}$$

7. When the zener is forward-biased:

$$V_{\text{out}} = \left(\frac{18 \text{ k}\Omega}{18 \text{ k}\Omega + 47 \text{ k}\Omega} \right) V_{\text{out}} - 0.7 \text{ V}$$

$$V_{\text{out}} = (0.277)V_{\text{out}} - 0.7 \text{ V}$$

$$V_{\text{out}}(1 - 0.277) = -0.7 \text{ V}$$

$$V_{\text{out}} = \frac{-0.7 \text{ V}}{1 - 0.277} = \mathbf{-0.968 \text{ V}}$$

When the zener is reverse-biased:

$$V_{\text{out}} = \left(\frac{18 \text{ k}\Omega}{18 \text{ k}\Omega + 47 \text{ k}\Omega} \right) V_{\text{out}} + 6.2 \text{ V}$$

$$V_{\text{out}} = (0.277)V_{\text{out}} + 6.2 \text{ V}$$

$$V_{\text{out}}(1 - 0.277) = +6.2 \text{ V}$$

$$V_{\text{out}} = \frac{+6.2 \text{ V}}{1 - 0.277} = \mathbf{+8.57 \text{ V}}$$

8. $V_{\text{out}} = \left(\frac{10 \text{ k}\Omega}{10 \text{ k}\Omega + 47 \text{ k}\Omega} \right) V_{\text{out}} \pm (4.7 \text{ V} + 0.7 \text{ V})$

$$V_{\text{out}} = (0.175)V_{\text{out}} \pm 5.4 \text{ V}$$

$$V_{\text{out}} = \frac{\pm 5.4 \text{ V}}{1 - 0.175} = \pm 6.55 \text{ V}$$

$$V_{\text{UTP}} = (0.175)(+6.55 \text{ V}) = +1.15 \text{ V}$$

$$V_{\text{LTP}} = (0.175)(-6.55 \text{ V}) = -1.15 \text{ V}$$

See Figure 13-2.

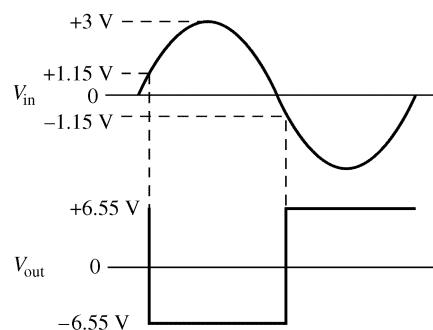


Figure 13-2

Chapter 13

Section 13-2 Summing Amplifiers

9. (a) $V_{\text{OUT}} = -\frac{R_f}{R_i}(+1 \text{ V} + 1.5 \text{ V}) = -1(1 \text{ V} + 1.5 \text{ V}) = -2.5 \text{ V}$

(b) $V_{\text{OUT}} = -\frac{R_f}{R_i}(0.1 \text{ V} + 1 \text{ V} + 0.5 \text{ V}) = -\frac{22 \text{ k}\Omega}{10 \text{ k}\Omega}(1.6 \text{ V}) = -3.52 \text{ V}$

10. (a) $V_{R1} = 1 \text{ V}$
 $V_{R2} = 1.8 \text{ V}$

(b) $I_{R1} = \frac{1 \text{ V}}{22 \text{ k}\Omega} = 45.5 \mu\text{A}$

$I_{R2} = \frac{1.8 \text{ V}}{22 \text{ k}\Omega} = 81.8 \mu\text{A}$

$I_f = I_{R1} + I_{R2} = 45.5 \mu\text{A} + 81.8 \mu\text{A} = 127 \mu\text{A}$

(c) $V_{\text{OUT}} = -I_f R_f = -(127 \mu\text{A})(22 \text{ k}\Omega) = -2.8 \text{ V}$

11. $5V_{in} = \left(\frac{R_f}{R}\right)V_{in}$

$\frac{R_f}{R} = 5$

$R_f = 5R = 5(22 \text{ k}\Omega) = 110 \text{ k}\Omega$

12. See Figure 13-3.

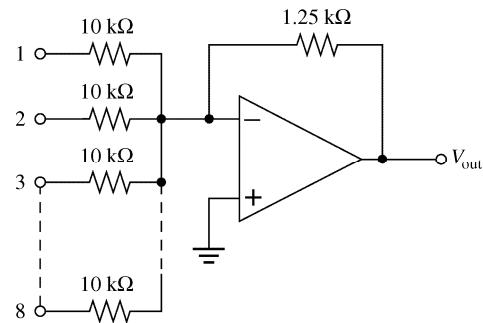


Figure 13-3

13. $V_{\text{OUT}} = -\left[\left(\frac{R_f}{R_1}\right)V_1 + \left(\frac{R_f}{R_2}\right)V_2 + \left(\frac{R_f}{R_3}\right)V_3 + \left(\frac{R_f}{R_4}\right)V_4\right]$
 $= -\left[\left(\frac{10 \text{ k}\Omega}{10 \text{ k}\Omega}\right)2 \text{ V} + \left(\frac{10 \text{ k}\Omega}{33 \text{ k}\Omega}\right)3 \text{ V} + \left(\frac{10 \text{ k}\Omega}{91 \text{ k}\Omega}\right)3 \text{ V} + \left(\frac{10 \text{ k}\Omega}{180 \text{ k}\Omega}\right)6 \text{ V}\right]$
 $= -(2 \text{ V} + 0.91 \text{ V} + 0.33 \text{ V} + 0.33 \text{ V}) = -3.57 \text{ V}$

$I_f = \frac{V_{\text{OUT}}}{R_f} = \frac{3.57 \text{ V}}{10 \text{ k}\Omega} = 357 \mu\text{A}$

14. $R_f = 100 \text{ k}\Omega$

Input resistors: $R_1 = 100 \text{ k}\Omega$, $R_2 = 50 \text{ k}\Omega$, $R_3 = 25 \text{ k}\Omega$, $R_4 = 12.5 \text{ k}\Omega$,
 $R_5 = 6.25 \text{ k}\Omega$, $R_6 = 3.125 \text{ k}\Omega$

Section 13-3 Integrators and Differentiators

15. $\frac{dV_{out}}{dt} = -\frac{V_{in}}{RC} = -\frac{5 \text{ V}}{(56 \text{ k}\Omega)(0.022 \mu\text{F})} = -4.06 \text{ mV}/\mu\text{s}$

16. See Figure 13-4.

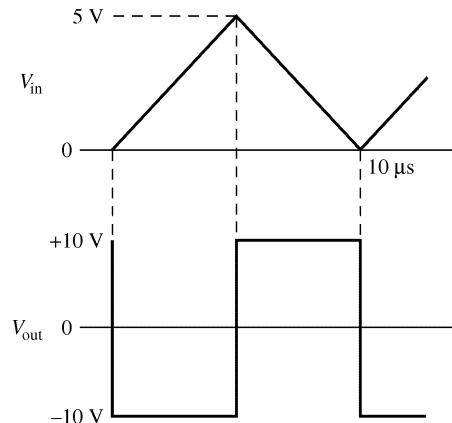


Figure 13-4

17. $I = \frac{CV_{pp}}{T/2} = \frac{(0.001 \mu\text{F})(5 \text{ V})}{10 \mu\text{s}/2} = 1 \text{ mA}$

18. $V_{out} = \pm RC \left(\frac{V_{pp}}{T/2} \right) = \pm(15 \text{ k}\Omega)(0.047 \mu\text{F}) \left(\frac{2 \text{ V}}{0.5 \text{ ms}} \right) = \pm 2.82 \text{ V}$

See Figure 13-5.

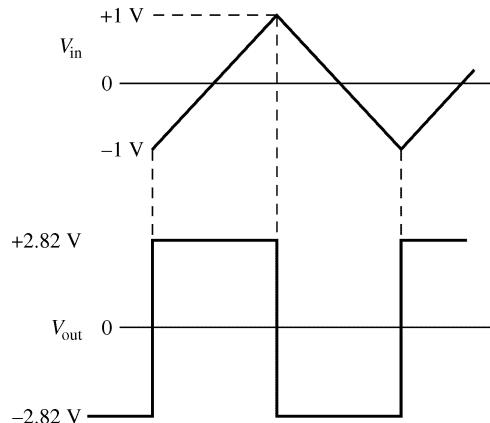


Figure 13-5

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19. For the 10 ms interval when the switch is in position 2:

$$\frac{\Delta V_{out}}{\Delta t} = -\frac{V_{IN}}{RC} = -\frac{5 \text{ V}}{(10 \text{ k}\Omega)(10 \mu\text{F})} = -\frac{5 \text{ V}}{0.1 \text{ s}} = -50 \text{ V/s} = -50 \text{ mV/ms}$$

$$\Delta V_{out} = (-50 \text{ mV/ms})(10 \text{ ms}) = -500 \text{ mV} = -0.5 \text{ V}$$

For the 10 ms interval when the switch is in position 1:

$$\frac{\Delta V_{out}}{\Delta t} = -\frac{V_{IN}}{RC} = -\frac{-5 \text{ V}}{(10 \text{ k}\Omega)(10 \mu\text{F})} = -\frac{-5 \text{ V}}{0.1 \text{ s}} = +50 \text{ V/s} = +50 \text{ mV/ms}$$

$$\Delta V_{out} = (+50 \text{ mV/ms})(10 \text{ ms}) = +500 \text{ mV} = +0.5 \text{ V}$$

See Figure 13-6.

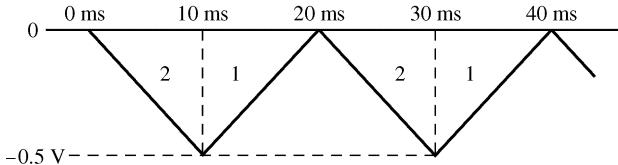


Figure 13-6

Section 13-4 Troubleshooting

20. $V_B = \left(\frac{R_2}{R_1 + R_2} \right) V_{out} \pm (V_Z + 0.7 \text{ V})$

$$V_B = \frac{\pm (V_Z + 0.7 \text{ V})}{1 - \left(\frac{R_2}{R_1 + R_2} \right)}$$

Normally, V_B should be

$$V_B = \frac{\pm (4.3 \text{ V} + 0.7 \text{ V})}{1 - 0.5} = \pm 10 \text{ V}$$

Since the negative portion of V_B is only -1.4 V , zener D_2 **must be shorted**:

$$V_B = \frac{-(0 \text{ V} + 0.7 \text{ V})}{1 - 0.5} = 1.4 \text{ V}$$

21. The output should be as shown in Figure 13-7. V_2 has no effect on the output. This indicates that R_2 is **open**.

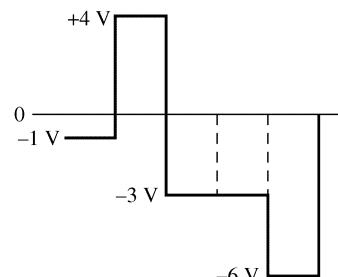


Figure 13-7

22. $A_v = \frac{2.5 \text{ k}\Omega}{10 \text{ k}\Omega} = 0.25$

The output should be as shown in Figure 13-8. An **open R_2** (V_2 is missing) will produce the observed output, which is incorrect.

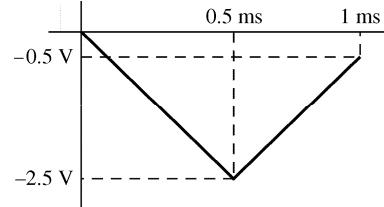


Figure 13-8

23. The D_2 input is missing (acts as a constant 0). This indicates an **open 50 k Ω resistor**.

Application Activity Problems

24. The first thing that you should always do is visually inspect the circuit for bad contacts or loose connections, shorts from solder splashes or wire clippings, incorrect components, and incorrectly installed components. After careful inspection, you have found nothing wrong. Measurements are now necessary to isolate a component's fault.
25. An open decoupling capacitor can make the circuit more susceptible to power line noise.
26. If a 1.0 k Ω resistor is used for R_1 , the inverting input would be increased, causing the pulse width to narrow for a given setting of the potentiometer.

Advanced Problems

27. $I_{R1-2-3} = \frac{24 \text{ V}}{612 \text{ k}\Omega} = 39.2 \mu\text{A}$

Minimum setting of R_2 :

$$V_{\text{INV}} = 12 \text{ V} - (39.2 \mu\text{A})(56 \text{ k}\Omega) = 9.8 \text{ V}$$

$$v = V_p \sin \theta$$

$$\sin \theta = \frac{v}{V_p} = \frac{9.8 \text{ V}}{10 \text{ V}} = 0.98$$

$$\theta = \sin^{-1} \left(\frac{v}{V_p} \right) = \sin^{-1}(0.98) = 78.5^\circ \text{ (on positive half cycle)}$$

Angle from 78.5° to 90°

$$\Delta\theta = 90^\circ - 78.5^\circ = 11.5^\circ$$

Angle from 90° to next point at which $v = 9.8 \text{ V}$:

$$\Delta\theta = 11.5^\circ$$

Angle from first point at which $v = 9.8 \text{ V}$ to second point at which $v = 9.8 \text{ V}$ on sine wave is
 $\theta = 11.5^\circ + 11.5^\circ = 23^\circ$

Chapter 13

$$\text{min. duty cycle} = \left(\frac{23^\circ}{360^\circ} \right) 100 = \mathbf{6.39\%}$$

See Figure 13.9(a).

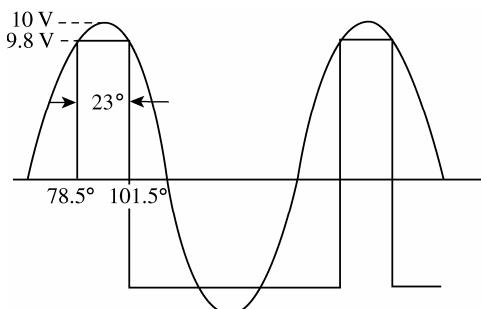
Maximum setting of R_2 :

$$V_{\text{INV}} = 12 \text{ V} - (39.2 \mu\text{A})(556 \text{ k}\Omega) = -9.8 \text{ V}$$

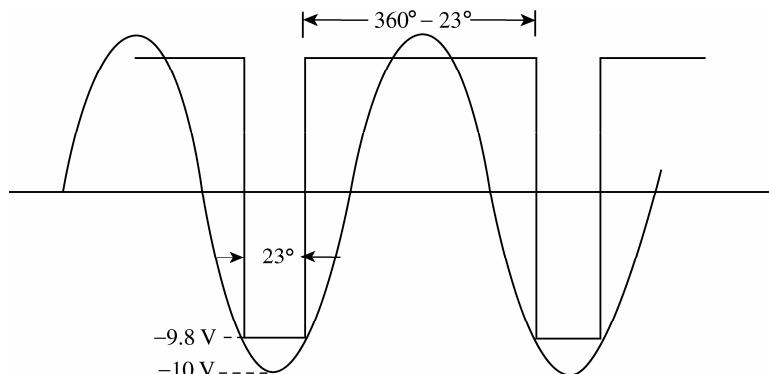
$$\sin \theta = \frac{v}{V_p} = \frac{-9.8 \text{ V}}{10 \text{ V}} = -0.98 \quad (\text{on negative half cycle})$$

$$\text{max. duty cycle} = \left(\frac{360^\circ - 23^\circ}{360^\circ} \right) 100 = \mathbf{93.6\%}$$

See Figure 13-9(b).



(a)



(b)

Figure 13-9

28. Let $V_{\text{INV}} = 4.8 \text{ V}$

Let $I_1 = 39.2 \mu\text{A}$

$$V_{\text{INV}} = 12 \text{ V} - I_1 R_1$$

$$-I_1 R_1 = 4.8 \text{ V} - 12 \text{ V}$$

$$I_1 R_1 = 7.2 \text{ V}$$

$$R_1 = \frac{7.2 \text{ V}}{39.2 \mu\text{A}} = 184 \text{ k}\Omega$$

Change R_1 and R_3 to $184 \text{ k}\Omega$.

29. $100 \text{ mV}/\mu\text{s} = 5 \text{ V}/R_i C$

$$R_i C = \frac{5 \text{ V}}{100 \text{ mV}/\mu\text{s}} = 50 \mu\text{s}$$

For $C = 3300 \text{ pF}$:

$$R_i = \frac{50 \mu\text{s}}{3300 \text{ pF}} = 15.15 \text{ k}\Omega = 15 \text{ k}\Omega + 150 \Omega$$

For a 5 V peak-peak triangle waveform:

$$t_{ramp\ up} = t_{ramp\ down} = \frac{5 \text{ V}}{100 \text{ mV}/\mu\text{s}} = 50 \mu\text{s}$$

$$\tau = 2(50 \mu\text{s}) = 100 \mu\text{s}$$

$$f_{in} = 1/100 \mu\text{s} = 100 \text{ kHz}$$

See Figure 13-10.

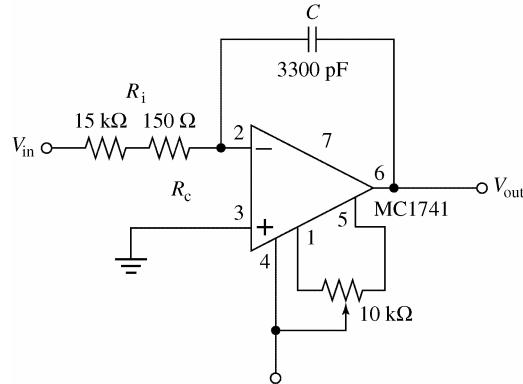


Figure 13-10

Multisim Troubleshooting Problems

The solutions showing instrument connections for Problems 30 through 39 are available from the Instructor Resource Center. See Chapter 1 for instructions. The faults in the circuit files may be accessed using the password *book* (all lowercase).

30. R_1 open

31. Op-amp inputs shorted together

32. Op-amp + input to output shorted

33. D_1 shorted

34. Top 10 kΩ resistor open

35. Middle 10 kΩ resistor shorted

36. R_f leaky

37. R_f open

38. C leaky

39. C open

Chapter 14

Special-Purpose Op-Amp Circuits

Section 14-1 Instrumentation Amplifiers

1. $A_{v(1)} = 1 + \frac{R_1}{R_G} = 1 + \frac{100 \text{ k}\Omega}{1.0 \text{ k}\Omega} = \mathbf{101}$

$$A_{v(2)} = 1 + \frac{R_2}{R_G} = 1 + \frac{100 \text{ k}\Omega}{1.0 \text{ k}\Omega} = \mathbf{101}$$

2. $A_{cl} = 1 + \frac{2R}{R_G} = 1 + \frac{200 \text{ k}\Omega}{1.0 \text{ k}\Omega} = \mathbf{201}$

3. $V_{out} = A_{cl}(V_{in(2)} - V_{in(1)}) = 202(10 \text{ mV} - 5 \text{ mV}) = \mathbf{1.005 \text{ V}}$

4. $A_v = 1 + \frac{2R}{R_G}$

$$\frac{2R}{R_G} = A_v - 1$$

$$R_G = \frac{2R}{A_v - 1} = \frac{2(100 \text{ k}\Omega)}{1000 - 1} = \frac{200 \text{ k}\Omega}{999} = 200.2 \Omega \cong \mathbf{200 \Omega}$$

5. $R_G = \frac{50.5 \text{ k}\Omega}{A_v - 1}$

$$A_v = \frac{50.5 \text{ k}\Omega}{1.0 \text{ k}\Omega} + 1 = \mathbf{51.5}$$

6. Using the graph in textbook Figure 14-6,
 $BW \cong \mathbf{300 \text{ kHz}}$

7. Change R_G to

$$R_G = \frac{50.5 \text{ k}\Omega}{A_v - 1} = \frac{50.5 \text{ k}\Omega}{24 - 1} \cong \mathbf{2.2 \text{ k}\Omega}$$

8. $R_G = \frac{50.5 \text{ k}\Omega}{A_v - 1} = \frac{50.5 \text{ k}\Omega}{20 - 1} \cong \mathbf{2.7 \text{ k}\Omega}$

Section 14-2 Isolation Amplifiers

9. $A_{v(tot)} = (30)(10) = 300$

10. (a) $A_{v1} = \frac{R_{f1}}{R_{i1}} + 1 = \frac{18 \text{ k}\Omega}{8.2 \text{ k}\Omega} + 1 = 3.2$

$$A_{v2} = \frac{R_{f2}}{R_{i2}} + 1 = \frac{150 \text{ k}\Omega}{15 \text{ k}\Omega} + 1 = 11$$

$$A_{v(tot)} = A_{v1}A_{v2} = (3.2)(11) = 35.2$$

(b) $A_{v1} = \frac{R_{f1}}{R_{i1}} + 1 = \frac{330 \text{ k}\Omega}{1.0 \text{ k}\Omega} + 1 = 331$

$$A_{v2} = \frac{R_{f2}}{R_{i2}} + 1 = \frac{47 \text{ k}\Omega}{15 \text{ k}\Omega} + 1 = 4.13$$

$$A_{v(tot)} = A_{v1}A_{v2} = (331)(4.13) = 1,367$$

11. $A_{v2} = 11$ (from Problem 10(a))

$$A_{v1}A_{v2} = 100$$

$$\frac{R_{f1}}{R_{i1}} + 1 = A_{v1} = \frac{100}{11} = 9.09$$

$$R_{f1} = (9.09 - 1)R_{i1} = (8.09)(8.2 \text{ k}\Omega) = 66 \text{ k}\Omega$$

Change R_f (18 kΩ) to 66 kΩ.

Use **68 kΩ ± 1%** standard value resistor.

12. $A_{v1} = 331$ (from Problem 10(b))

$$A_{v1}A_{v2} = 440$$

$$\frac{R_{f2}}{R_{i2}} + 1 = A_{v2} = \frac{440}{331} = 1.33$$

Change R_f (47 kΩ) to 3.3 kΩ.

Change R_i (15 kΩ) to 10 kΩ.

13. Connect pin 6 to pin 10 and pin 14 to pin 15. Make $R_f = 0$.

Section 14-3 Operational Transconductance Amplifiers (OTAs)

14. $g_m = \frac{I_{out}}{V_{in}} = \frac{10 \mu\text{A}}{10 \text{ mV}} = 1 \text{ mS}$

15. $I_{out} = g_m V_{in} = (5000 \mu\text{S})(100 \text{ mV}) = 500 \mu\text{A}$

$$V_{out} = I_{out} R_L = (500 \mu\text{A})(10 \text{ k}\Omega) = 5 \text{ V}$$

Chapter 14

16.
$$g_m = \frac{I_{out}}{V_{in}}$$

$$I_{out} = g_m V_{in} = (4000 \mu\text{S})(100 \text{ mV}) = 400 \mu\text{A}$$

$$R_L = \frac{V_{out}}{I_{out}} = \frac{3.5 \text{ V}}{400 \mu\text{A}} = 8.75 \text{ k}\Omega$$

17.
$$I_{BIAS} = \frac{+12 \text{ V} - (-12 \text{ V}) - 0.7 \text{ V}}{R_{BIAS}} = \frac{+12 \text{ V} - (-12 \text{ V}) - 0.7 \text{ V}}{220 \text{ k}\Omega} = \frac{23.3 \text{ V}}{220 \text{ k}\Omega} = 106 \mu\text{A}$$

From the graph in Figure 14-57:

$$g_m = K I_{BIAS} \cong (16 \mu\text{S}/\mu\text{A})(106 \mu\text{A}) = 1.70 \text{ mS}$$

$$A_v = \frac{V_{out}}{V_{in}} = \frac{I_{out} R_L}{V_{in}} = g_m R_L = (1.70 \text{ mS})(6.8 \text{ k}\Omega) = 11.6$$

18. The maximum voltage gain occurs when the 10 kΩ potentiometer is set to 0 Ω and was determined in Problem 17.

$$A_{v(max)} = 11.6$$

The minimum voltage gain occurs when the 10 kΩ potentiometer is set to 10 kΩ.

$$I_{BIAS} = \frac{+12 \text{ V} - (-12 \text{ V}) - 0.7 \text{ V}}{220 \text{ k}\Omega + 10 \text{ k}\Omega} = \frac{23.3 \text{ V}}{230 \text{ k}\Omega} = 101 \mu\text{A}$$

$$g_m \cong (16 \mu\text{S}/\mu\text{A})(101 \mu\text{A}) = 1.62 \text{ mS}$$

$$A_{v(min)} = g_m R_L = (1.62 \text{ mS})(6.8 \text{ k}\Omega) = 11.0$$

19. The V_{MOD} waveform is applied to the bias input.

The gain and output voltage for each value of V_{MOD} is determined as follows using $K = 16 \mu\text{S}/\mu\text{A}$. The output waveform is shown in Figure 14-1.

For $V_{MOD} = +8 \text{ V}$:

$$I_{BIAS} = \frac{+8 \text{ V} - (-9 \text{ V}) - 0.7 \text{ V}}{39 \text{ k}\Omega} = \frac{16.3 \text{ V}}{39 \text{ k}\Omega} = 418 \mu\text{A}$$

$$g_m = K I_{BIAS} \cong (16 \mu\text{S}/\mu\text{A})(418 \mu\text{A}) = 6.69 \text{ mS}$$

$$A_v = \frac{V_{out}}{V_{in}} = \frac{I_{out} R_L}{V_{in}} = g_m R_L = (6.69 \text{ mS})(10 \text{ k}\Omega) = 66.9$$

$$V_{out} = A_v V_{in} = (66.9)(100 \text{ mV}) = 6.69 \text{ V}$$

For $V_{MOD} = +6 \text{ V}$:

$$I_{BIAS} = \frac{+6 \text{ V} - (-9 \text{ V}) - 0.7 \text{ V}}{39 \text{ k}\Omega} = \frac{14.3 \text{ V}}{39 \text{ k}\Omega} = 367 \mu\text{A}$$

$$g_m = K I_{BIAS} \cong (16 \mu\text{S}/\mu\text{A})(367 \mu\text{A}) = 5.87 \text{ mS}$$

$$A_v = \frac{V_{out}}{V_{in}} = \frac{I_{out} R_L}{V_{in}} = g_m R_L = (5.87 \text{ mS})(10 \text{ k}\Omega) = 58.7$$

$$V_{out} = A_v V_{in} = (58.7)(100 \text{ mV}) = 5.87 \text{ V}$$

For $V_{\text{MOD}} = +4 \text{ V}$:

$$I_{\text{BIAS}} = \frac{+4 \text{ V} - (-9 \text{ V}) - 0.7 \text{ V}}{39 \text{ k}\Omega} = \frac{12.3 \text{ V}}{39 \text{ k}\Omega} = 315 \mu\text{A}$$

$$g_m = KI_{\text{BIAS}} \approx (16 \mu\text{S}/\mu\text{A})(315 \mu\text{A}) = 5.04 \text{ mS}$$

$$A_v = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{I_{\text{out}} R_L}{V_{\text{in}}} = g_m R_L = (5.04 \text{ mS})(10 \text{ k}\Omega) = 50.4$$

$$V_{\text{out}} = A_v V_{\text{in}} = (50.4)(100 \text{ mV}) = \mathbf{5.04 \text{ V}}$$

For $V_{\text{MOD}} = +2 \text{ V}$:

$$I_{\text{BIAS}} = \frac{+2 \text{ V} - (-9 \text{ V}) - 0.7 \text{ V}}{39 \text{ k}\Omega} = \frac{10.3 \text{ V}}{39 \text{ k}\Omega} = 264 \mu\text{A}$$

$$g_m = KI_{\text{BIAS}} \approx (16 \mu\text{S}/\mu\text{A})(264 \mu\text{A}) = 4.22 \text{ mS}$$

$$A_v = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{I_{\text{out}} R_L}{V_{\text{in}}} = g_m R_L = (4.22 \text{ mS})(10 \text{ k}\Omega) = 42.2$$

$$V_{\text{out}} = A_v V_{\text{in}} = (42.2)(100 \text{ mV}) = \mathbf{4.22 \text{ V}}$$

For $V_{\text{MOD}} = +1 \text{ V}$:

$$I_{\text{BIAS}} = \frac{+1 \text{ V} - (-9 \text{ V}) - 0.7 \text{ V}}{39 \text{ k}\Omega} = \frac{9.3 \text{ V}}{39 \text{ k}\Omega} = 238 \mu\text{A}$$

$$g_m = KI_{\text{BIAS}} \approx (16 \mu\text{S}/\mu\text{A})(238 \mu\text{A}) = 3.81 \text{ mS}$$

$$A_v = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{I_{\text{out}} R_L}{V_{\text{in}}} = g_m R_L = (3.81 \text{ mS})(10 \text{ k}\Omega) = 38.1$$

$$V_{\text{out}} = A_v V_{\text{in}} = (38.1)(100 \text{ mV}) = \mathbf{3.81 \text{ V}}$$

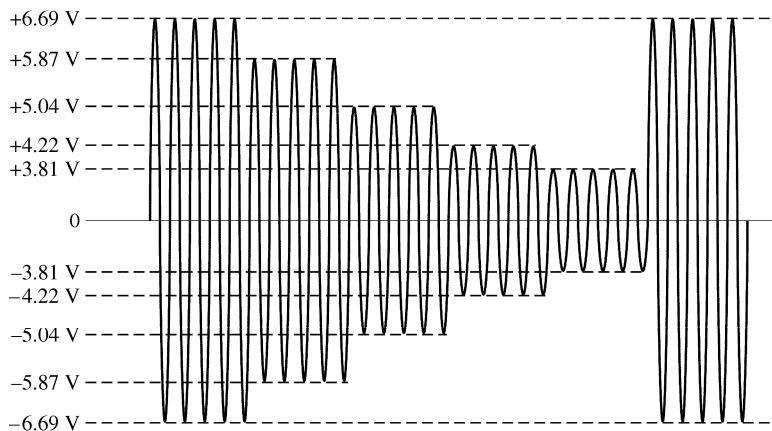


Figure 14-1

20. $I_{\text{BIAS}} = \frac{+9 \text{ V} - (-9 \text{ V}) - 0.7 \text{ V}}{39 \text{ k}\Omega} = \frac{17.3 \text{ V}}{39 \text{ k}\Omega} = 444 \mu\text{A}$

$$V_{\text{TRIG}(+)} = I_{\text{BIAS}} R_1 = (444 \mu\text{A})(10 \text{ k}\Omega) = \mathbf{+4.44 \text{ V}}$$

$$V_{\text{TRIG}(-)} = -I_{\text{BIAS}} R_1 = (-444 \mu\text{A})(10 \text{ k}\Omega) = \mathbf{-4.44 \text{ V}}$$

Chapter 14

21. See Figure 14-2.

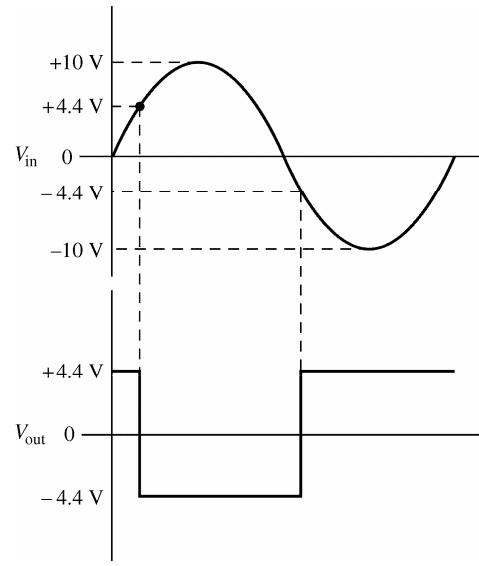


Figure 14-2

Section 14-4 Log and Antilog Amplifiers

22. (a) $\ln(0.5) = -0.693$

(b) $\ln(2) = 0.693$

(c) $\ln(50) = 3.91$

(d) $\ln(130) = 4.87$

23. (a) $\log_{10}(0.5) = -0.301$

(b) $\log_{10}(2) = 0.301$

(c) $\log_{10}(50) = 1.70$

(d) $\log_{10}(130) = 2.11$

24. Antilog $x = 10^x$ or e^x , depending on the base used.

INV $\ln = e^{1.6} = 4.95$

INV $\log = 10^{1.6} = 39.8$

25. The output of a log amplifier is limited to **0.7 V** because the output voltage is limited to the barrier potential of the transistor's *pn* junction.

26.
$$V_{out} \cong -(0.025 \text{ V})\ln\left(\frac{V_{in}}{I_s R_{in}}\right)$$
$$= -(0.025 \text{ V})\ln\left(\frac{3 \text{ V}}{(100 \text{ nA})(82 \text{ k}\Omega)}\right) = -(0.025 \text{ V})\ln(365.9) = -148 \text{ mV}$$

27.
$$V_{out} \cong -(0.025 \text{ V})\ln\left(\frac{V_{in}}{I_{EBO} R_{in}}\right)$$
$$= -(0.025 \text{ V})\ln\left(\frac{1.5 \text{ V}}{(60 \text{ nA})(47 \text{ k}\Omega)}\right) = -(0.025 \text{ V})\ln(531.9) = -157 \text{ mV}$$

28. $V_{out} = -R_f I_{EBO} \text{antilog}\left(\frac{V_{in}}{25 \text{ mV}}\right) = -R_f I_{EBO} e^{\left(\frac{V_{in}}{25 \text{ mV}}\right)}$

$$V_{out} = -(10 \text{ k}\Omega)(60 \text{ nA}) e^{\left(\frac{0.225 \text{ V}}{25 \text{ mV}}\right)} = -(10 \text{ k}\Omega)(60 \text{ nA})e^9 = -(10 \text{ k}\Omega)(60 \text{ nA})(8103) = \boxed{-4.86 \text{ V}}$$

29. $V_{out(max)} \cong -(0.025 \text{ V}) \ln\left(\frac{V_{in}}{I_{EBO} R_{in}}\right) = -(0.025 \text{ V}) \ln\left(\frac{1 \text{ V}}{(60 \text{ nA})(47 \text{ k}\Omega)}\right)$
 $= -(0.025 \text{ V}) \ln(354.6) = \boxed{-147 \text{ mV}}$

$$V_{out(min)} \cong -(0.025 \text{ V}) \ln\left(\frac{V_{in}}{I_{EBO} R_{in}}\right) = -(0.025 \text{ V}) \ln\left(\frac{100 \text{ mV}}{(60 \text{ nA})(47 \text{ k}\Omega)}\right)$$

 $= -(0.025 \text{ V}) \ln(35.5) = \boxed{-89.2 \text{ mV}}$

The signal compression allows larger signals to be reduced without causing smaller amplitudes to be lost (in this case, the 1 V peak is reduced 85% but the 100 mV peak is reduced only 10%).

Section 14-5 Converters and Other Op-Amp Circuits

30. (a) $V_{IN} = V_Z = 4.7 \text{ V}$
 $I_L = \frac{V_{IN}}{R_i} = \frac{4.7 \text{ V}}{1.0 \text{ k}\Omega} = \boxed{4.7 \text{ mA}}$

(b) $V_{IN} = \left(\frac{10 \text{ k}\Omega}{20 \text{ k}\Omega}\right)12 \text{ V} = 6 \text{ V}$
 $R_i = 10 \text{ k}\Omega \parallel 10 \text{ k}\Omega + 100 \Omega = 5.1 \text{ k}\Omega$
 $I_L = \frac{V_{IN}}{R_i} = \frac{6 \text{ V}}{5.1 \text{ k}\Omega} = \boxed{1.18 \text{ mA}}$

31. See Figure 14-3.

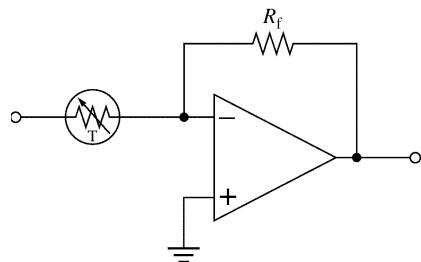


Figure 14-3

Chapter 14

Multisim Troubleshooting Problems

The solutions showing instrument connections for Problems 32 through 36 are available from the Instructor Resource Center. See Chapter 1 for instructions. The faults in the circuit files may be accessed using the password *book* (all lowercase).

- 32.** R_G leaky
- 33.** R open
- 34.** R_f open
- 35.** Zener diode open
- 36.** Lower 10 k Ω resistor open

Chapter 15

Active Filters

Section 15-1 Basic Filter Responses

1. (a) Band-pass

(b) High-pass

(c) Low-pass

(d) Band-stop

2. $BW = f_c = 800 \text{ Hz}$

3. $f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi(2.2 \text{ k}\Omega)(0.0015 \mu\text{F})} = 48.2 \text{ Hz}$

No, the upper response roll-off due to internal device capacitances is unknown.

4. The roll-off is **20 dB/decade** because this is a single-pole filter.

5. $BW = f_{c2} - f_{c1} = 3.9 \text{ kHz} - 3.2 \text{ kHz} = 0.7 \text{ kHz} = 700 \text{ Hz}$

$$f_0 = \sqrt{f_{c1}f_{c2}} = \sqrt{(3.2 \text{ kHz})(3.9 \text{ kHz})} = 3.53 \text{ kHz}$$

$$Q = \frac{f_0}{BW} = \frac{3.53 \text{ kHz}}{700 \text{ Hz}} = 5.04$$

6. $Q = \frac{f_0}{BW}$

$$f_0 = Q(BW) = 15(1 \text{ kHz}) = 15 \text{ kHz}$$

Section 15-2 Filter Response Characteristics

7. (a) 2nd order, 1 stage

$$DF = 2 - \frac{R_3}{R_4} = 2 - \frac{1.2 \text{ k}\Omega}{1.2 \text{ k}\Omega} = 2 - 1 = 1 \quad \text{Not Butterworth}$$

(b) 2nd order, 1 stage

$$DF = 2 - \frac{R_3}{R_4} = 2 - \frac{560 \Omega}{1.0 \text{ k}\Omega} = 2 - 0.56 = 1.44 \quad \text{Approximately Butterworth}$$

(c) 3rd order, 2 stages, 1st stage (2 poles):

$$DF = 2 - \frac{R_3}{R_4} = 2 - \frac{330 \Omega}{1.0 \text{ k}\Omega} = 1.67$$

2nd stage (1 pole):

$$DF = 2 - \frac{R_6}{R_7} = 1.67 \quad \text{Not Butterworth}$$

Chapter 15

8. (a) From Table 15-1 in the textbook, the damping factor must be 1.414; therefore,

$$\frac{R_3}{R_4} = 0.586$$

$$R_3 = 0.586R_4 = 0.586(1.2 \text{ k}\Omega) = 703 \text{ }\Omega$$

Nearest standard value: **720** Ω

(b) $\frac{R_3}{R_4} = 0.56$

This is an approximate Butterworth response
(as close as you can get using standard 5% resistors).

- (c) From Table 15-1, the damping factor of both stages must be 1, therefore

$$\frac{R_3}{R_4} = 1$$

$$R_3 = R_4 = R_6 = R_7 = 1 \text{ k}\Omega \text{ (for both stages)}$$

9. (a) Chebyshev
(b) Butterworth
(c) Bessel
(d) Butterworth

Section 15-3 Active Low-Pass Filters

10. High Pass

1st stage:

$$DF = 2 - \frac{R_3}{R_4} = 2 - \frac{1.0 \text{ k}\Omega}{6.8 \text{ k}\Omega} = 1.85$$

2nd stage:

$$DF = 2 - \frac{R_7}{R_8} = 2 - \frac{6.8 \text{ k}\Omega}{5.6 \text{ k}\Omega} = 0.786$$

From Table 15-1 in the textbook:

1st stage $DF = 1.848$ and 2nd stage $DF = 0.765$

Therefore, this filter is **approximately Butterworth**.

Roll-off rate = **80 dB/decade**

11. $f_c = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}} = \frac{1}{2\pi\sqrt{R_5R_6C_3C_4}} = \frac{1}{2\pi\sqrt{(4.7 \text{ k}\Omega)(6.8 \text{ k}\Omega)(0.22 \mu\text{F})(0.1 \mu\text{F})}} = 190 \text{ Hz}$

12. $R = R_1 = R_2 = R_5 = R_6$ and $C = C_1 = C_2 = C_3 = C_4$

Let $C = 0.22 \mu\text{F}$ (for both stages).

$$f_c = \frac{1}{2\pi\sqrt{R^2C^2}} = \frac{1}{2\pi RC}$$

$$R = \frac{1}{2\pi f_c C} = \frac{1}{2\pi(190 \text{ Hz})(0.22 \mu\text{F})} = 3.81 \text{ k}\Omega$$

Choose $R = 3.9 \text{ k}\Omega$ (for both stages)

13. See Figure 15-1.

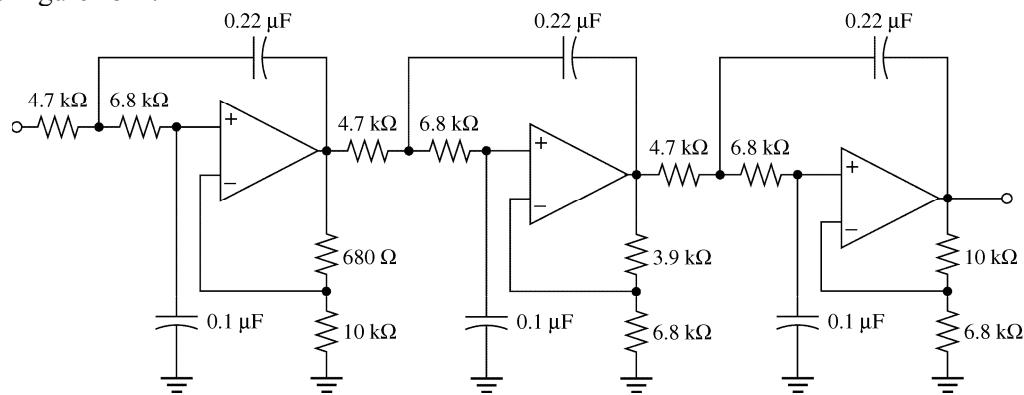


Figure 15-1

14. See Figure 15-2.

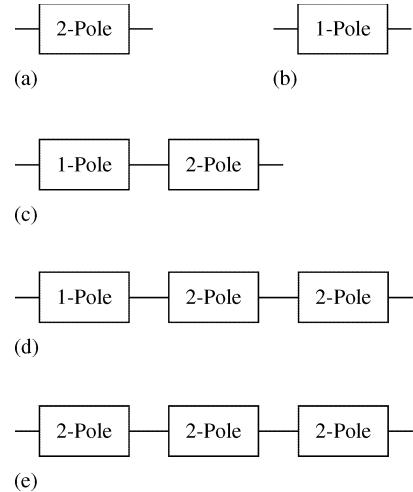


Figure 15-2

Section 15-4 Active High-Pass Filters

15. Exchange the positions of the resistors and the capacitors. See Figure 15-3.

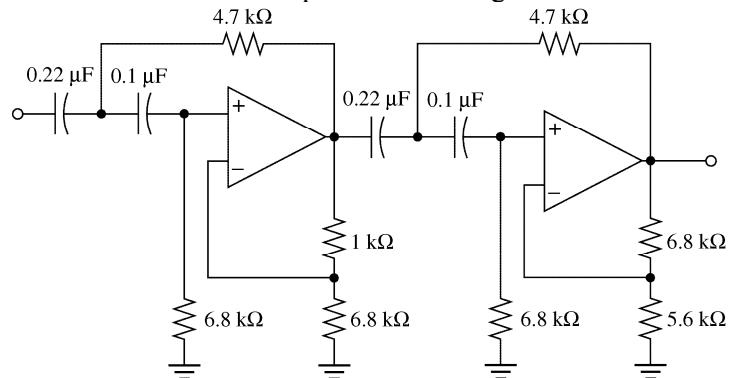


Figure 15-3

Chapter 15

16. $f_c = \frac{1}{2\pi RC}$

$$f_0 = \frac{190 \text{ Hz}}{2} = 95 \text{ Hz}$$

$$R = \frac{1}{2\pi f_c C} = \frac{1}{2\pi(95 \text{ Hz})(0.22 \mu\text{F})} = 7615 \Omega$$

Let $R = 7.5 \text{ k}\Omega$. Change R_1, R_2, R_5 and R_6 to **7.5 kΩ**.

17. (a) Decrease R_1 and R_2 or C_1 and C_2 .
(b) Increase R_3 or decrease R_4 .

Section 15-5 Active Band-Pass Filters

18. (a) Cascaded high-pass/low-pass filters
(b) Multiple feedback
(c) State variable

19. (a) 1st stage:

$$f_{c1} = \frac{1}{2\pi RC} = \frac{1}{2\pi(1.0 \text{ k}\Omega)(0.047 \mu\text{F})} = 3.39 \text{ kHz}$$

2nd stage:

$$f_{c2} = \frac{1}{2\pi RC} = \frac{1}{2\pi(1.0 \text{ k}\Omega)(0.022 \mu\text{F})} = 7.23 \text{ kHz}$$

$$f_0 = \sqrt{f_{c1}f_{c2}} = \sqrt{(3.39 \text{ kHz})(7.23 \text{ kHz})} = \mathbf{4.95 \text{ kHz}}$$

$$BW = 7.23 \text{ kHz} - 3.39 \text{ Hz} = \mathbf{3.84 \text{ kHz}}$$

(b) $f_0 = \frac{1}{2\pi C} \sqrt{\frac{R_1 + R_3}{R_1 R_3 R_2}} = \frac{1}{2\pi(0.022 \mu\text{F})} \sqrt{\frac{47 \text{ k}\Omega + 1.8 \text{ k}\Omega}{(47 \text{ k}\Omega)(1.8 \text{ k}\Omega)(150 \text{ k}\Omega)}} = \mathbf{449 \text{ Hz}}$

$$Q = \pi f_0 CR_2 = \pi(449 \text{ Hz})(0.022 \mu\text{F})(150 \text{ k}\Omega) = 4.66$$

$$BW = \frac{f_0}{Q} = \frac{449 \text{ Hz}}{4.66} = \mathbf{96.4 \text{ Hz}}$$

- (c) For each integrator:

$$f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi(10 \text{ k}\Omega)(0.001 \mu\text{F})} = 15.9 \text{ kHz}$$

$$f_0 = f_c = \mathbf{15.9 \text{ kHz}}$$

$$Q = \frac{1}{3} \left(\frac{R_5}{R_6} + 1 \right) = \frac{1}{3} \left(\frac{560 \text{ k}\Omega}{10 \text{ k}\Omega} + 1 \right) = \frac{1}{3} (56 + 1) = 19$$

$$BW = \frac{f_0}{Q} = \frac{15.9 \text{ kHz}}{19} = \mathbf{838 \text{ Hz}}$$

20.
$$Q = \frac{1}{3} \left(\frac{R_5}{R_6} + 1 \right)$$

Select $R_6 = 10 \text{ k}\Omega$.

$$Q = \frac{R_5}{3R_6} + \frac{1}{3} = \frac{R_5 + R_6}{3R_6}$$

$$3R_6Q = R_5 + R_6$$

$$R_5 = 3R_6Q - R_6 = 3(10 \text{ k}\Omega)(50) - 10 \text{ k}\Omega = 1500 \text{ k}\Omega - 10 \text{ k}\Omega = 1490 \text{ k}\Omega$$

$$f_0 = \frac{1}{2\pi(12 \text{ k}\Omega)(0.01 \mu\text{F})} = 1.33 \text{ kHz}$$

$$BW = \frac{f_0}{Q} = \frac{1.33 \text{ kHz}}{50} = 26.6 \text{ Hz}$$

Section 15-6 Active Band-Stop Filters

21. See Figure 15-4.

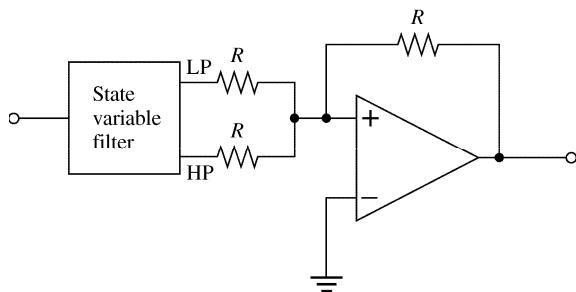


Figure 15-4

22.
$$f_0 = f_c = \frac{1}{2\pi RC}$$

Let C remain $0.01 \mu\text{F}$.

$$R = \frac{1}{2\pi f_0 C} = \frac{1}{2\pi(120 \text{ Hz})(0.01 \mu\text{F})} = 133 \text{ k}\Omega$$

Change R in the integrators from $12 \text{ k}\Omega$ to $133 \text{ k}\Omega$.

Multisim Troubleshooting Problems

The solutions showing instrument connections for Problems 23 through 31 are available from the Instructor Resource Center. See Chapter 1 for instructions. The faults in the circuit files may be accessed using the password *book* (all lowercase).

23. R_4 shorted

24. R_3 open

25. C_3 shorted

26. R_5 open

Chapter 15

- 27.** R_1 open
- 28.** R_2 shorted
- 29.** R_1 open
- 30.** C_2 open
- 31.** R_7 open

Chapter 16

Oscillators

Section 16-1 The Oscillator

1. An oscillator requires no input other than the dc supply voltage.
2. Amplifier and positive feedback circuit

Section 16-2 Feedback Oscillator Principles

3. Unity gain around the closed loop is required for sustained oscillation.

$$A_{cl} = A_v B = 1$$

$$B = \frac{1}{A_v} = \frac{1}{75} = 0.0133$$

4. To ensure startup:

$$A_{cl} > 1$$

since $A_v = 75$, B must be greater than 1/75 in order to produce the condition

$$A_v B > 1.$$

For example, if $B = 1/50$,

$$A_v B = 75 \left(\frac{1}{50} \right) = 1.5$$

Section 16-3 Oscillators with RC Feedback Circuits

5. $\frac{V_{out}}{V_{in}} = \frac{1}{3}$

$$V_{out} = \left(\frac{1}{3} \right) V_{in} = \frac{2.2 \text{ V}}{3} = 733 \text{ mV}$$

6. $f_r = \frac{1}{2\pi RC} = \frac{1}{2\pi(6.2 \text{ k}\Omega)(0.02 \mu\text{F})} = 1.28 \text{ kHz}$

7. $R_1 = 2R_2$

$$R_2 = \frac{R_1}{2} = \frac{100 \text{ k}\Omega}{2} = 50 \text{ k}\Omega$$

8. When dc power is first applied, both zener diodes appear as opens because there is insufficient output voltage. This places R_3 in series with R_1 , thus increasing the closed-loop gain to a value greater than unity to assure that oscillation will begin.

9. $R_f = (A_v - 1)(R_3 + r'_{ds}) = (3 - 1)(820 \Omega + 350 \Omega) = 2.34 \text{ k}\Omega$

Chapter 16

10. $f_r = \frac{1}{2\pi(1.0 \text{ k}\Omega)(0.015 \mu\text{F})} = \mathbf{10.6 \text{ kHz}}$

11. $B = \frac{1}{29}$

$$A_{cl} = \frac{1}{B} = 29$$

$$A_{cl} = \frac{R_f}{R_i}$$

$$R_f = A_{cl}R_i = 29(4.7 \text{ k}\Omega) = \mathbf{136 \text{ k}\Omega}$$

$$f_r = \frac{1}{2\pi\sqrt{6}(4.7 \text{ k}\Omega)(0.022 \mu\text{F})} = \mathbf{628 \text{ Hz}}$$

Section 16-4 Oscillators with LC Feedback Circuits

12. (a) *Colpitts*: C_1 and C_3 are the feedback capacitors.

$$f_r = \frac{1}{2\pi\sqrt{L_1C_T}}$$

$$C_T = \frac{C_1C_3}{C_1 + C_3} = \frac{(100 \mu\text{F})(1000 \text{ pF})}{1100 \text{ pF}} = 90.9 \text{ pF}$$

$$f_r = \frac{1}{2\pi\sqrt{(5 \text{ mH})(90.9 \text{ pF})}} = \mathbf{236 \text{ kHz}}$$

- (b) *Hartley*:

$$f_r = \frac{1}{2\pi\sqrt{L_TC_2}}$$

$$L_T = L_1 + L_2 = 1.5 \text{ mH} + 10 \text{ mH} = 11.5 \text{ mH}$$

$$f_r = \frac{1}{2\pi\sqrt{(11.5 \text{ mH})(470 \text{ pF})}} = \mathbf{68.5 \text{ kHz}}$$

13. $B = \frac{47 \text{ pF}}{470 \text{ pF}} = 0.1$

The condition for sustained oscillation is

$$A_v = \frac{1}{B} = \frac{1}{0.1} = \mathbf{10}$$

Section 16-5 Relaxation Oscillators

14. Triangular waveform.

$$f = \frac{1}{4R_1C} \left(\frac{R_2}{R_3} \right) = \frac{1}{4(22 \text{ k}\Omega)(0.022 \mu\text{F})} \left(\frac{56 \text{ k}\Omega}{18 \text{ k}\Omega} \right) = \mathbf{1.61 \text{ kHz}}$$

15. Change f to 10 kHz by changing R_1 :

$$f = \frac{1}{4R_1 C} \left(\frac{R_2}{R_3} \right)$$

$$R_1 = \frac{1}{4fC} \left(\frac{R_2}{R_3} \right) = \frac{1}{4(10 \text{ kHz})(0.022 \mu\text{F})} \left(\frac{56 \text{ k}\Omega}{18 \text{ k}\Omega} \right) = \mathbf{3.54 \text{ k}\Omega}$$

16. $T = \frac{V_p - V_F}{\left(\frac{|V_{IN}|}{RC} \right)}$

$$V_p = \left(\frac{R_5}{R_4 + R_5} \right) 12 \text{ V} = \left(\frac{47 \text{ k}\Omega}{147 \text{ k}\Omega} \right) 12 \text{ V} = 3.84 \text{ V}$$

PUT triggers at about +3.84 V (ignoring the 0.7 V drop)

Amplitude = +3.84 V – 1 V = **2.84 V**

$$V_{IN} = \left(\frac{R_2}{R_1 + R_2} \right) (-12 \text{ V}) = \left(\frac{22 \text{ k}\Omega}{122 \text{ k}\Omega} \right) (-12 \text{ V}) = -2.16 \text{ V}$$

$$T = \frac{3.84 \text{ V} - 1 \text{ V}}{\left(\frac{2.16 \text{ V}}{(100 \text{ k}\Omega)(0.0022 \mu\text{F})} \right)} = 289 \mu\text{s}$$

$$f = \frac{1}{T} = \frac{1}{289 \mu\text{s}} = \mathbf{3.46 \text{ kHz}}$$

See Figure 16-1.

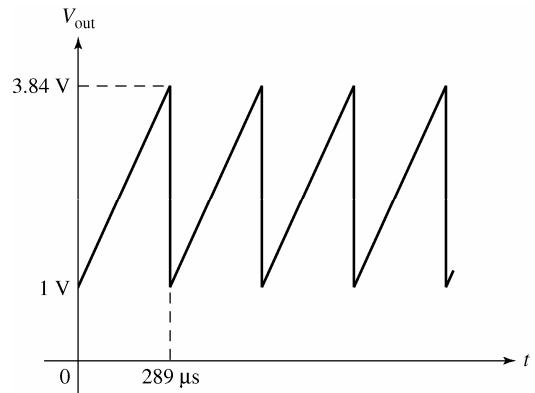


Figure 16-1

Chapter 16

17. $V_G = 5 \text{ V}$. Assume $V_{AK} = 1 \text{ V}$.

$$R_5 = 47 \text{ k}\Omega$$

$$V_G = \left(\frac{R_5}{R_4 + R_5} \right) 12 \text{ V}$$

Change R_4 to get $V_G = 5 \text{ V}$.

$$5 \text{ V}(R_4 + 47 \text{ k}\Omega) = (47 \text{ k}\Omega)12 \text{ V}$$

$$R_4(5 \text{ V}) = (47 \text{ k}\Omega)12 \text{ V} - (47 \text{ k}\Omega)5 \text{ V}$$

$$R_4 = \frac{(12 \text{ V} - 5 \text{ V})47 \text{ k}\Omega}{5 \text{ V}} = \mathbf{65.8 \text{ k}\Omega}$$

18. $T = \frac{V_p - V_F}{\left(\frac{V_{IN}}{RC} \right)}$

$$V_p = \left(\frac{V_{IN}}{RC} \right) T + V_F = \left(\frac{3 \text{ V}}{(4.7 \text{ k}\Omega)(0.001 \mu\text{F})} \right) 10 \mu\text{s} + 1 \text{ V} = 7.38 \text{ V}$$

$$V_{pp(out)} = V_p - V_F = 7.38 \text{ V} - 1 \text{ V} = \mathbf{6.38 \text{ V}}$$

Section 16-6 The 555 Timer as an Oscillator

19. $\frac{1}{3}V_{CC} = \frac{1}{3}(10 \text{ V}) = \mathbf{3.33 \text{ V}}$

$$\frac{2}{3}V_{CC} = \frac{2}{3}(10 \text{ V}) = \mathbf{6.67 \text{ V}}$$

20. $f = \frac{1.44}{(R_1 + 2R_2)C_{ext}} = \frac{1.44}{(1.0 \text{ k}\Omega + 6.6 \text{ k}\Omega)(0.047 \mu\text{F})} = \mathbf{4.03 \text{ kHz}}$

21. $f = \frac{1.44}{(R_1 + 2R_2)C_{ext}}$

$$C_{ext} = \frac{1.44}{(R_1 + 2R_2)f} = \frac{1.44}{(1.0 \text{ k}\Omega + 6.6 \text{ k}\Omega)(25 \text{ kHz})} = \mathbf{0.0076 \mu\text{F}}$$

22. Duty cycle (dc) = $\frac{R_1 + R_2}{R_1 + 2R_2} \times 100\%$

$$dc(R_1 + 2R_2) = (R_1 + R_2)100$$

$$75(3.3 \text{ k}\Omega + 2R_2) = (3.3 \text{ k}\Omega + R_2)100$$

$$75(3.3 \text{ k}\Omega) + 150R_2 = 100(3.3 \text{ k}\Omega) + 100R_2$$

$$150R_2 - 100R_2 = 100(3.3 \text{ k}\Omega) - 75(3.3 \text{ k}\Omega)$$

$$50R_2 = 25(3.3 \text{ k}\Omega)$$

$$R_2 = \frac{25(3.3 \text{ k}\Omega)}{50} = \mathbf{1.65 \text{ k}\Omega}$$

Multisim Troubleshooting Problems

The solutions showing instrument connections for Problems 23 through 28 are available from the Instructor Resource Center. See Chapter 1 for instructions. The faults in the circuit files may be accessed using the password *book* (all lowercase).

- 23.** Drain-to-source shorted
- 24.** C_3 open
- 25.** Collector-to-emitter shorted
- 26.** R_1 open
- 27.** R_2 open
- 28.** R_1 leaky

Chapter 17

Voltage Regulators

Section 17-1 Voltage Regulation

1. Percent line regulation = $\left(\frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{IN}}} \right) 100\% = \left(\frac{2 \text{ mV}}{6 \text{ V}} \right) 100\% = \mathbf{0.0333\%}$
2. Percent line regulation = $\left(\frac{\Delta V_{\text{OUT}} / V_{\text{OUT}}}{\Delta V_{\text{IN}}} \right) 100\% = \left(\frac{2 \text{ mV}/8 \text{ V}}{6 \text{ V}} \right) 100\% = \mathbf{0.00417\%/V}$
3. Percent load regulation = $\left(\frac{V_{\text{NL}} / V_{\text{FL}}}{\Delta V_{\text{FL}}} \right) 100\% = \left(\frac{10 \text{ V} - 9.90 \text{ V}}{9.90 \text{ V}} \right) 100\% = \mathbf{1.01\%}$
4. From Problem 3, the percent load regulation is 1.01%. For a full load current of 250 mA, this can be expressed as
$$\frac{1.01\%}{250 \text{ mA}} = \mathbf{0.00404\%/mA}$$

Section 17-2 Basic Linear Series Regulators

5. See Figure 17-1.

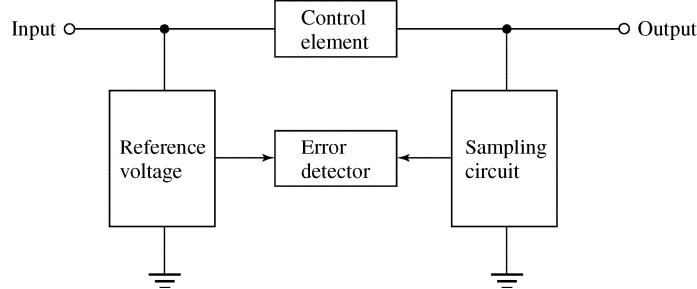


Figure 17-1

6. $V_{\text{OUT}} = \left(1 + \frac{R_2}{R_3} \right) V_{\text{REF}} = \left(1 + \frac{33 \text{ k}\Omega}{10 \text{ k}\Omega} \right) 2.4 \text{ V} = \mathbf{10.3 \text{ V}}$
7. $V_{\text{OUT}} = \left(1 + \frac{R_2}{R_3} \right) V_{\text{REF}} = \left(1 + \frac{5.6 \text{ k}\Omega}{2.2 \text{ k}\Omega} \right) 2.4 \text{ V} = \mathbf{8.51 \text{ V}}$

8. For $R_3 = 2.2 \text{ k}\Omega$:

$$V_{\text{OUT}} = \left(1 + \frac{R_2}{R_3}\right)V_{\text{REF}} = \left(1 + \frac{5.6 \text{ k}\Omega}{2.2 \text{ k}\Omega}\right)2.4 \text{ V} = 8.5 \text{ V}$$

For $R_3 = 4.7 \text{ k}\Omega$:

$$V_{\text{OUT}} = \left(1 + \frac{R_2}{R_3}\right)V_{\text{REF}} = \left(1 + \frac{5.6 \text{ k}\Omega}{4.7 \text{ k}\Omega}\right)2.4 \text{ V} = 5.26 \text{ V}$$

The output voltage **decreases by 3.24 V** when R_3 is changed from $2.2 \text{ k}\Omega$ to $4.7 \text{ k}\Omega$.

9. $V_{\text{OUT}} = \left(1 + \frac{R_2}{R_3}\right)V_{\text{REF}} = \left(1 + \frac{5.6 \text{ k}\Omega}{2.2 \text{ k}\Omega}\right)2.7 \text{ V} = \mathbf{9.57 \text{ V}}$

10. $I_{L(\text{max})} = \frac{0.7 \text{ V}}{R_4}$

$$R_4 = \frac{0.7 \text{ V}}{I_{L(\text{max})}} = \frac{0.7 \text{ mA}}{250 \text{ mA}} = \mathbf{2.8 \Omega}$$

$$P = I_{L(\text{max})}^2 R_4 = (250 \text{ mA})^2 2.8 \Omega = \mathbf{0.175 \text{ W}}, \text{ Use a } 0.25 \text{ W.}$$

11. $R_4 = \frac{2.8 \Omega}{2} = 1.4 \Omega$

$$I_{L(\text{max})} = \frac{0.7 \text{ V}}{R_4} = \frac{0.7 \text{ V}}{1.4 \Omega} = \mathbf{500 \text{ mA}}$$

Section 17-3 Basic Linear Shunt Regulators

12. Q_1 conducts more when the load current increases, assuming that the output voltage attempts to increase. When the output voltage tries to increase due to a change in load current, the attempted increase is sensed by R_3 and R_4 and a proportional voltage is applied to the op-amp's noninverting input. The resulting difference voltage increases the op-amp output, driving Q_1 more and thus increasing its collector current.

13. $\Delta I_C = \frac{\Delta V_{R1}}{R_1} = \frac{1 \text{ V}}{100 \Omega} = \mathbf{10 \text{ mA}}$

14. $V_{\text{OUT}} = \left(1 + \frac{R_3}{R_4}\right)V_{\text{REF}} = \left(1 + \frac{10 \text{ k}\Omega}{3.9 \text{ k}\Omega}\right)5.1 \text{ V} = \mathbf{18.2 \text{ V}}$

$$I_{L1} = \frac{V_{\text{OUT}}}{R_{L1}} = \frac{18.2 \text{ V}}{1 \text{ k}\Omega} = 18.2 \text{ mA}$$

$$I_{L2} = \frac{V_{\text{OUT}}}{R_{L2}} = \frac{18.2 \text{ V}}{1.2 \text{ k}\Omega} = 15.2 \text{ mA}$$

$$\Delta I_L = 15.2 \text{ mA} - 18.2 \text{ mA} = -3.0 \text{ mA}$$

$$\Delta I_S = -\Delta I_L = \mathbf{3.0 \text{ mA}}$$

Chapter 17

15. $I_{L(\max)} = \frac{V_{IN}}{R_1} = \frac{25\text{ V}}{100\Omega} = 250\text{ mA}$

$$P_{R1} = I_{L(\max)}^2 R_1 = (250\text{ mA})^2 100\Omega = 6.25\text{ W}$$

Section 17-4 Basic Switching Regulators

16. $V_{OUT} = \left(\frac{t_{on}}{T} \right) V_{IN}$

$$t_{on} = T - t_{off}$$
$$T = \frac{1}{f} = \frac{1}{100\text{ Hz}} = 0.01\text{ s} = 10\text{ ms}$$
$$V_{OUT} = \left(\frac{4\text{ ms}}{10\text{ ms}} \right) 12\text{ V} = 4.8\text{ V}$$

17. $f = 100\text{ Hz}, t_{off} = 6\text{ ms}$

$$T = \frac{1}{f} = \frac{1}{100\text{ Hz}} = 10\text{ ms}$$
$$t_{on} = T - t_{off} = 10\text{ ms} - 6\text{ ms} = 4\text{ ms}$$
$$\text{duty cycle} = \frac{t_{on}}{T} = \frac{4\text{ ms}}{10\text{ ms}} = 0.4$$
$$\text{percent duty cycle} = 0.4 \times 100\% = 40\%$$

18. The diode D_1 becomes forward-biased when Q_1 turns off.
19. The output voltage **decreases**.

Section 17-5 Integrated Circuit Voltage Regulators

20. (a) 7806: **+6 V**
(b) 7905.2: **-5.2 V**
(c) 7818: **+18 V**
(d) 7924: **-24 V**

21. $V_{OUT} = \left(1 + \frac{R_2}{R_1} \right) V_{REF} + I_{ADJ} R_2 = \left(1 + \frac{10\text{ k}\Omega}{1.0\text{ k}\Omega} \right) 1.25\text{ V} + (50\text{ }\mu\text{A})(10\text{ k}\Omega)$
$$= 13.7\text{ V} + 0.5\text{ V} = 14.3\text{ V}$$

22.
$$V_{\text{OUT(min)}} = - \left[\left(1 + \frac{R_{2(\min)}}{R_1} \right) V_{\text{REF}} + I_{\text{ADJ}} R_{2(\min)} \right]$$

$$R_{2(\min)} = 0 \Omega$$

$$V_{\text{OUT(min)}} = - (1.25 \text{ V}(1+0) + 0) = -1.25 \text{ V}$$

$$V_{\text{OUT(max)}} = - \left[\left(1 + \frac{R_{2(\max)}}{R_1} \right) V_{\text{REF}} + I_{\text{ADJ}} R_{2(\max)} \right] = - \left[1.25 \text{ V} \left(1 + \frac{10 \text{ k}\Omega}{470 \Omega} \right) + (50 \mu\text{A})(10 \text{ k}\Omega) \right]$$

$$= - (1.25 \text{ V}(22.28) + 0.5 \text{ V}) = -28.4 \text{ V}$$

23. The regulator current equals the current through $R_1 + R_2$.

$$I_{\text{REG}} \cong \frac{V_{\text{OUT}}}{R_1 + R_2} = \frac{14.3 \text{ V}}{11 \text{ k}\Omega} = 1.3 \text{ mA}$$

24. $V_{\text{IN}} = 18 \text{ V}$, $V_{\text{OUT}} = 12 \text{ V}$

$$I_{\text{REG(max)}} = 2 \text{ mA}$$
, $V_{\text{REF}} = 1.25 \text{ V}$

$$R_1 = \frac{V_{\text{REF}}}{I_{\text{REG}}} = \frac{1.25 \text{ V}}{2 \text{ mA}} = 625 \Omega$$

Neglecting I_{ADJ} :

$$V_{R2} = 12 \text{ V} - 1.25 \text{ V} = 10.8 \text{ V}$$

$$R_2 = \frac{V_{R2}}{I_{\text{REG}}} = \frac{10.8 \text{ V}}{2 \text{ mA}} = 5.4 \text{ k}\Omega$$

For R_1 use **620 Ω** and for R_2 use either **5600 Ω** or a 10 kΩ potentiometer for precise adjustment to 12 V.

Section 17-6 Applications of IC Voltage Regulators

25. $V_{R_{\text{ext(min)}}} = 0.7 \text{ V}$

$$R_{\text{ext}} = \frac{0.7 \text{ V}}{I_{\text{max}}} = \frac{0.7 \text{ V}}{250 \text{ mA}} = 2.8 \Omega$$

26. $V_{\text{OUT}} = +12 \text{ V}$

$$I_L = \frac{12 \text{ V}}{10 \Omega} = 1200 \text{ mA} = 1.2 \text{ A}$$

$$I_{\text{ext}} = I_L - I_{\text{max}} = 1.2 \text{ A} - 0.5 \text{ A} = 0.7 \text{ A}$$

$$P_{\text{ext}} = I_{\text{ext}}(V_{\text{IN}} - V_{\text{OUT}}) = 0.7 \text{ A}(15 \text{ V} - 12 \text{ V}) = 0.7 \text{ A}(3 \text{ V}) = 2.1 \text{ W}$$

27. $V_{R_{\text{lim(min)}}} = 0.7 \text{ V}$

$$R_{\text{lim(min)}} = \frac{0.7 \text{ V}}{I_{\text{ext}}} = \frac{0.7 \text{ V}}{2 \text{ A}} = 0.35 \Omega$$

See Figure 17-2.

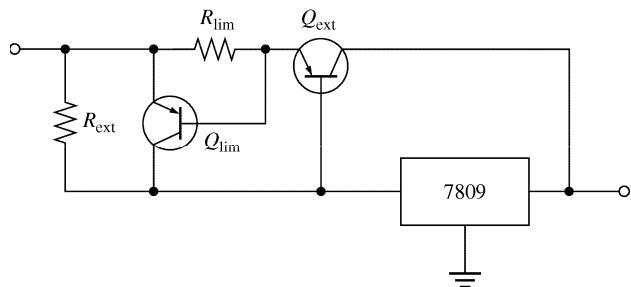


Figure 17-2

Chapter 17

28. $R = \frac{1.25 \text{ V}}{500 \text{ mA}} = 2.5 \Omega$

See Figure 17-3.

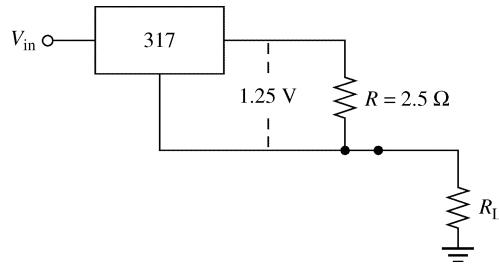


Figure 17-3

29. $I = 500 \text{ mA}$

$$R = \frac{8 \text{ V}}{500 \text{ mA}} = 16 \Omega$$

See Figure 17-4.

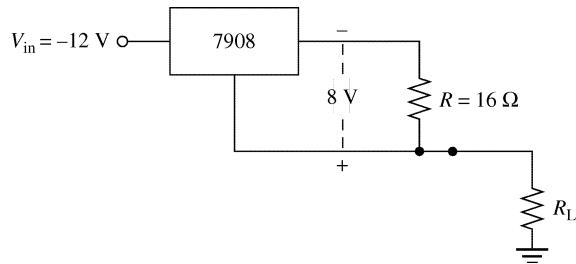


Figure 17-4

30. $V_{\text{REF}} = 1.25 \text{ V}$

The voltage divider must reduce the output voltage (12 V) down to the reference voltage (1.25 V). See Figure 17-38 in the text.

$$V_{\text{REF}} = \left(\frac{R_1}{R_1 + R_2} \right) V_{\text{OUT}}$$

$$\frac{R_1}{R_1 + R_2} = \frac{V_{\text{REF}}}{V_{\text{OUT}}}$$

$$R_1 = R_1(V_{\text{REF}}/V_{\text{OUT}}) + R_2(V_{\text{REF}}/V_{\text{OUT}})$$

$$R_2 = \frac{R_1 - R_1(V_{\text{REF}}/V_{\text{OUT}})}{(V_{\text{REF}}/V_{\text{OUT}})} = \frac{R_1(1 + V_{\text{REF}}/V_{\text{OUT}})}{(V_{\text{REF}}/V_{\text{OUT}})}$$

Let $R_1 = 10 \text{ k}\Omega$.

$$R_2 = \frac{10 \text{ k}\Omega(1 - 1.25 \text{ V}/12 \text{ V})}{(1.25 \text{ V}/12 \text{ V})} = 86 \text{ k}\Omega$$

Multisim Troubleshooting Problems

The solutions showing instrument connections for Problems 31 through 34 are available from the Instructor Resource Center. See Chapter 1 for instructions. The faults in the circuit files may be accessed using the password *book* (all lowercase).

31. R_2 leaky
32. Zener diode open
33. Q_2 collector-to-emitter open
34. R_1 open

Chapter 18

Communications

Section 18-1 Basic Receivers

1. See Figure 18-1.

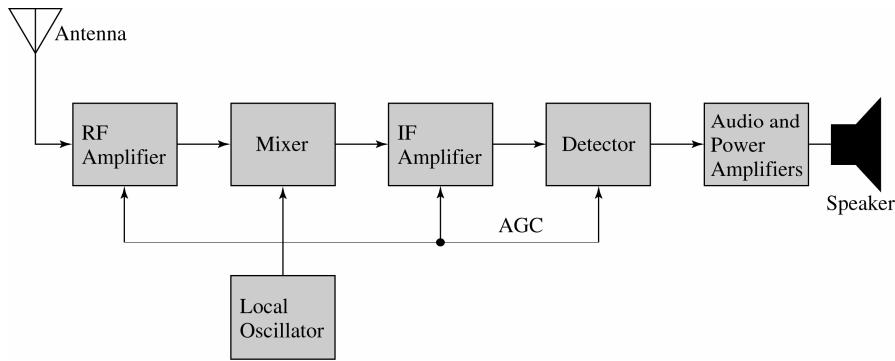


Figure 18-1

2. See Figure 18-2.

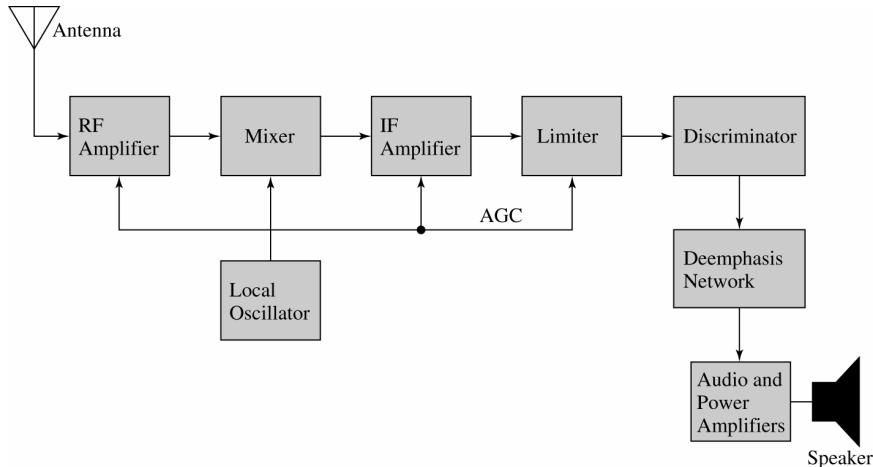


Figure 18-2

3. $f_{LO} = 680 \text{ kHz} + 455 \text{ kHz} = \mathbf{1135 \text{ kHz}}$
4. $f_{LO} = 97.2 \text{ MHz} + 10.7 \text{ MHz} = \mathbf{107.9 \text{ MHz}}$
5. $f_{RF} = 101.9 \text{ MHz} - 10.7 \text{ MHz} = \mathbf{91.2 \text{ MHz}}$
 $f_{IF} = \mathbf{10.7 \text{ MHz}}$ (always)

Section 18-2 The Linear Multiplier

6. (a) $V_{out} \cong -2.5 \text{ V}$
 (b) $V_{out} \cong -1.6 \text{ V}$
 (c) $V_{out} \cong +1.0 \text{ V}$
 (d) $V_{out} \cong +10 \text{ V}$
7. $V_{out} = KV_X V_Y = 0.125(+3.5 \text{ V})(-2.9 \text{ V}) = -1.27 \text{ V}$
8. Connect the two inputs together.
9. (a) $V_{out} = KV_1 V_2 = (0.1)(+2 \text{ V})(+1.4 \text{ V}) = +0.28 \text{ V}$
 (b) $V_{out} = KV_1 V_2 = KV_1^2 (0.1)(-3.2 \text{ V})^2 = +1.024 \text{ V}$
 (c) $V_{out} = \frac{-V_1}{V_2} = \frac{-(6.2 \text{ V})}{-3 \text{ V}} = +2.07 \text{ V}$
 (d) $V_{out} = \sqrt{V_1} = \sqrt{6.2 \text{ V}} = +2.49 \text{ V}$

Section 18-3 Amplitude Modulation

10. $f_{diff} = f_1 - f_2 = 100 \text{ kHz} - 30 \text{ kHz} = 70 \text{ kHz}$
 $f_{sum} = f_1 + f_2 = 100 \text{ kHz} + 30 \text{ kHz} = 130 \text{ kHz}$
11. $f_1 = \frac{9 \text{ cycles}}{1 \text{ ms}} = 9000 \text{ cycles/s} = 9 \text{ kHz}$
 $f_2 = \frac{1 \text{ cycle}}{1 \text{ ms}} = 1000 \text{ cycles/s} = 1 \text{ kHz}$
 $f_{diff} = f_1 - f_2 = 9 \text{ kHz} - 1 \text{ kHz} = 8 \text{ kHz}$
 $f_{sum} = f_1 + f_2 = 9 \text{ kHz} + 1 \text{ kHz} = 10 \text{ kHz}$
12. $f_c = 1000 \text{ kHz}$
 $f_{diff} = 1000 \text{ kHz} - 3 \text{ kHz} = 997 \text{ kHz}$
 $f_{sum} = 1000 \text{ kHz} + 3 \text{ kHz} = 1003 \text{ kHz}$
13. $f_1 = \frac{18 \text{ cycles}}{10 \mu\text{s}} = 1.8 \text{ MHz}$
 $f_2 = \frac{1 \text{ cycle}}{10 \mu\text{s}} = 100 \text{ kHz}$
 $f_{diff} = f_1 - f_2 = 1.8 \text{ MHz} - 100 \text{ kHz} = 1.7 \text{ MHz}$
 $f_{sum} = f_1 + f_2 = 1.8 \text{ MHz} + 100 \text{ kHz} = 1.9 \text{ MHz}$
 $f_c = 1.8 \text{ MHz}$
14. $f_c = 1.2 \text{ MHz}$ by inspection
 $f_m = f_c - f_{diff} = 1.2 \text{ MHz} - 1.1955 \text{ MHz} = 4.5 \text{ kHz}$

Chapter 18

15. $f_c = \frac{f_{diff} + f_{sum}}{2} = \frac{8.47 \text{ kHz} + 853 \text{ KHz}}{2} = 850 \text{ kHz}$

$$f_m = f_c - f_{diff} = 850 \text{ kHz} - 847 \text{ kHz} = 3 \text{ kHz}$$

16. $f_{diff(min)} = 600 \text{ kHz} - 3 \text{ kHz} = 597 \text{ kHz}$
 $f_{diff(max)} = 600 \text{ kHz} - 300 \text{ Hz} = 599.7 \text{ kHz}$
 $f_{sum(min)} = 600 \text{ kHz} + 300 \text{ kHz} = 600.3 \text{ kHz}$
 $f_{sum(max)} = 600 \text{ kHz} + 3 \text{ kHz} = 603 \text{ kHz}$
See Figure 18-3.

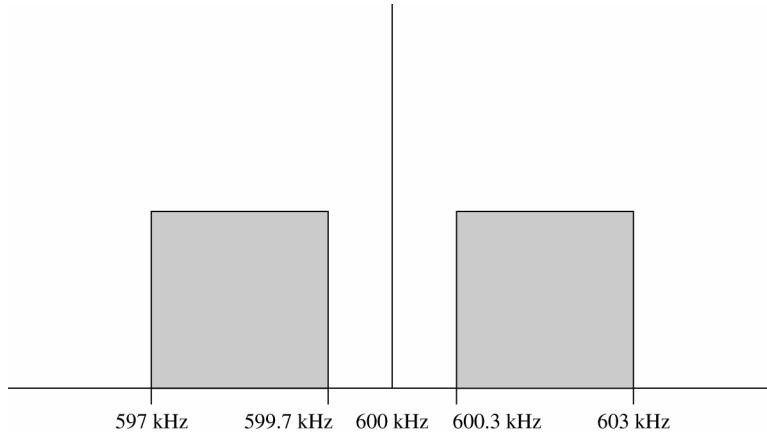


Figure 18-3

Section 18-4 The Mixer

17. $(\sin A)(\sin B) = \frac{1}{2}[\cos(A - B) - \cos(A + B)]$

$$V_{in(1)} = 0.2 \text{ V} \sin [2\pi(2200 \text{ kHz})t]$$
$$V_{in(2)} = 0.15 \text{ V} \sin [2\pi(3300 \text{ kHz})t]$$
$$V_{in(1)}V_{in(2)} = (0.2 \text{ V})(0.15 \text{ V}) \sin [2\pi(2200 \text{ kHz})t] \sin [2\pi(3300 \text{ kHz})t]$$
$$V_{out} = \frac{(0.2 \text{ V})(0.15 \text{ V})}{2} [\cos 2\pi(3300 \text{ kHz} - 2200 \text{ kHz})t - \cos 2\pi(3300 \text{ kHz} + 2200 \text{ kHz})t]$$
$$V_{out} = 15 \text{ mV} \cos [2\pi(1100 \text{ kHz})t] - 15 \text{ mV} \cos [2\pi(5500 \text{ kHz})t]$$

18. $f_{IF} = f_{LO} - f_c = 986.4 \text{ kHz} - 980 \text{ kHz} = 6.4 \text{ kHz}$

Section 18-5 AM Demodulation

19. See Figure 18-4.

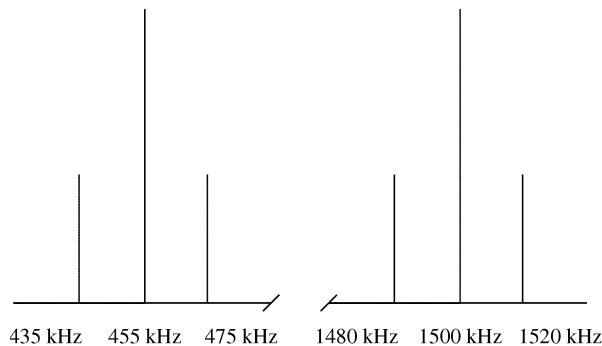


Figure 18-4

20. See Figure 18-5.

21. See Figure 18-6.

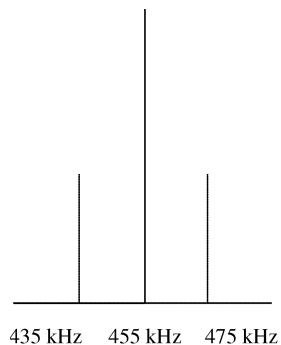


Figure 18-5

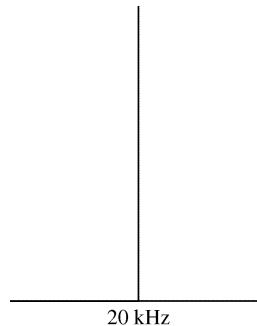


Figure 18-6

Section 18-6 IF and Audio Amplifiers

22. $f_c - f_m = 1.2 \text{ MHz} - 8.5 \text{ kHz} = 1.1915 \text{ MHz}$
 $f_c + f_m = 1.2 \text{ MHz} + 8.5 \text{ kHz} = 1.2085 \text{ MHz}$
 $f_c = 1.2 \text{ MHz}$
 $f_{\text{LO}} - f_m = 455 \text{ kHz} - 8.5 \text{ kHz} = 446.5 \text{ kHz}$
 $f_{\text{LO}} + f_m = 455 \text{ kHz} + 8.5 \text{ kHz} = 463.5 \text{ kHz}$
 $f_{\text{LO}} = 455 \text{ kHz}$

23. The **IF amplifier** has a 450 kHz to 460 kHz passband.
The **audio/power amplifiers** have a 10 Hz to 5 kHz bandpass.

Chapter 18

24. C_4 between pins 1 and 8 makes the gain 200.
With R_1 set for minimum input, $V_{in} = 0 \text{ V}$.
 $V_{out(min)} = A_v V_{in(min)} = 200(0 \text{ V}) = 0 \text{ V}$
With R_1 set for maximum input, $V_{in} = 10 \text{ mV rms}$.
 $V_{out(max)} = A_v V_{in(max)} = 200(10 \text{ mV}) = 2 \text{ V rms}$

Section 18-7 Frequency Modulation

25. The modulating input signal is applied to the control voltage terminal of the VCO. As the input signal amplitude varies, the output frequency of the VCO varies proportionately.
26. An FM signal differs from an AM signal in that the information is contained in frequency variations of the carrier rather than amplitude variations.
27. Varactor

Section 18-8 The Phase-Locked Loop (PLL)

28. See Figure 18-7.

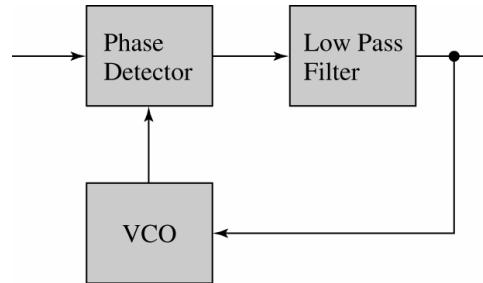


Figure 18-7

29. (a) The VCO signal is locked onto the incoming signal and therefore its frequency is equal to the incoming frequency of **10 MHz**.

(b) $V_c = \frac{V_i V_o}{2} \cos \theta_e \frac{(250 \text{ mV})(400 \text{ mV})}{2} \cos(30^\circ - 15^\circ) = (0.050)(0.966) = 48.3 \text{ mV}$

30. $\Delta f_o = +3.6 \text{ kHz}, \quad \Delta V_c = +0.5 \text{ V}$

$$K = \frac{\Delta f_o}{\Delta V_c} = \frac{+3.6 \text{ kHz}}{+0.5 \text{ V}} = 7.2 \text{ kHz/V}$$

31. $K = 1.5 \text{ kHz/V}, \quad \Delta V_c = +0.67 \text{ V}$

$$K = \frac{\Delta f_o}{\Delta V_c}$$

$$\Delta f_o = K \Delta V_c = (1.5 \text{ kHz/V})(+0.67 \text{ V}) = 1005 \text{ Hz}$$

- 32.** For a PLL to acquire lock the following conditions are needed:
- (1) The difference frequency, $f_0 - f_i$ must fall within the filter's bandwidth.
 - (2) The maximum frequency deviation of the VCO frequency, Δf_{max} , must be sufficient to permit f_0 to change to equal f_i .

- 33.** The free-running frequency:

$$f_o = \frac{1.2}{4R_1C_1} = \frac{1.2}{4(3.9\text{ k}\Omega)(330\text{ pF})} = 233\text{ kHz}$$

The lock range:

$$f_{lock} = \pm \frac{8f_o}{V_{CC}} = \pm \frac{8(233\text{ kHz})}{18\text{ V}} = \pm \frac{1.864\text{ MHz}}{18\text{ V}} = \pm 104\text{ kHz}$$

The capture range:

$$\begin{aligned} f_{cap} &= \pm \frac{1}{2\pi} \sqrt{\left(\frac{2\pi f_{lock}}{3600 \times C_2} \right)} \\ &= \pm \frac{1}{2\pi} \sqrt{\left(\frac{2\pi(103.6\text{ kHz})}{3600 \times 0.22\text{ }\mu\text{F}} \right)} = \pm \frac{1}{2\pi} \sqrt{\left(\frac{650.9\text{ kHz}}{792\text{ }\mu\text{F}} \right)} = \pm 4.56\text{ kHz} \end{aligned}$$

Section 18-9 Fiber Optics

- 34.** The light ray will be **reflected** because the angle of incidence (30°) is greater than the critical angle (15°).
- 35.** $\theta_C = \cos^{-1}(n_2/n_1) = \cos^{-1}(1.25/1.55) = 36.2^\circ$

There are no Multisim Troubleshooting Problems in this chapter.

Application Activity

Results

Chapter 2

1. A comparison of Equations 2-5 and 2-7 shows that the output voltage of a bridge rectifier is nearly twice that of a center-tapped rectifier. Also, two diode drops contribute to the bridge output voltage, but only one diode drop contributes to the center-tapped output voltage.
2. A comparison of Equations 2-6 and 2-8 shows that the PIV of a bridge rectifier is nearly half that of a center-tapped rectifier.
3. $V_{p(out)} = V_{p(sec)} - 1.4 \text{ V}$
 $V_{p(sec)} = V_{p(out)} + 1.4 \text{ V} = 16 \text{ V} + 1.4 \text{ V} = 17.4 \text{ V peak} = 12.3 \text{ V rms}$
4. Minimum VA = (12.3 V)(250 mA) = 3.075 VA
Use the 12 V CT rated at 6 VA.
The 12 V rms secondary voltage is within 10% of the specified 12.3 V determined in 3.
5. The primary current is determined as follows:
$$\frac{I_{p(pri)}}{I_{p(sec)}} = \frac{V_{sec}}{V_{pri}}$$
$$I_{p(pri)} = \left(\frac{V_{sec}}{V_{pri}} \right) I_{p(sec)} = \left(\frac{12 \text{ V}}{120 \text{ V}} \right) 354 \text{ mA} = 35.4 \text{ mA}$$

The fuse rating should be at least 20% greater than $I_{p(pri)}$.
6. $r = \frac{V_{r(pp)}}{V_{DC}}$
 $V_{r(pp)} = rV_{DC} = 0.03(16 \text{ V}) = 480 \text{ mV}$
7. $V_{r(pp)} = \left(\frac{1}{fR_L C} \right) V_{p(rectified)}$
 $C = \left(\frac{1}{fR_L V_{r(pp)}} \right) V_{p(rectified)} = \left(\frac{1}{\sqrt{(120 \text{ Hz})(64 \Omega)(480 \text{ mV})}} \right) 17 \text{ V} = 0.004612 \text{ F}$

Use 4700 μF .
8. $P_L = V_L I_L = (16 \text{ V})(258 \text{ mA}) = 4.13 \text{ W}$
The rating should be at least 5 W.

Application Activity Results

Troubleshooting

- (a) Open capacitor. Circuit is operating as full-wave rectifier with no filter.
- (b) No fault
- (c) Rectifier diode open. Circuit is operating as a half-wave rectifier.
- (d) Diode and filter capacitor open. Circuit is operating as a half-wave rectifier with no filter.

Chapter 3

1. $V_{\text{OUT(max)}} = 12 \text{ V} + 120 \text{ mV} = 12.12 \text{ V}$ (typical)
2. $\Delta V_{\text{OUT}} = 5 \text{ mV}$
3. $V_F = 1.9 \text{ V}$
 $R_{\text{limit}} = \frac{12 \text{ V} - 1.9 \text{ V}}{20 \text{ mA}} = 505 \text{ W}$
 $P = (10.1 \text{ V})20 \text{ mA} = 202 \text{ mW}$. Use 0.25 W rating.
4. $I_{\text{pri}} = \left(\frac{V_{\text{sec}}}{V_{\text{pri}}} \right) I_{\text{sec}} = \left(\frac{12.6 \text{ V}}{120 \text{ V}} \right) 250 \text{ mA} = 26.3 \text{ mA}$
Use the next highest standard fuse rating.
5. $P_L = \frac{(12 \text{ V})^2}{47 \Omega} = 3.06 \text{ W}$
6. The printed circuit board and the schematic agree.
7. $I_{\text{reg}} = I_{\text{LED}} + I_L = 20 \text{ mA} + 250 \text{ mA} = 270 \text{ mA}$
 $P_{\text{reg}} = (16 \text{ V} - 12 \text{ V})270 \text{ mA} = 1.08 \text{ W}$

Chapter 4

1. From the datasheet, $V_{\text{CE(sat)}} = 0.3 \text{ V}$.
 $R_3 = \frac{V_{\text{CC}} - V_{\text{CE(sat)}}}{I_{C1}} = \frac{12 \text{ V} - 0.3 \text{ V}}{10 \text{ mA}} = 1170 \Omega$ (use std. 1.2 kΩ)
2. From the datasheet, $\beta_{\text{DC(min)}} = h_{\text{FE(min)}} = 75$.
 $I_{B1} = \frac{I_{C1}}{\beta_{\text{DC(min)}}} = \frac{10 \text{ mA}}{75} = 133 \mu\text{A}$
3. $R_1 = \frac{V_{\text{sensor}} - V_{\text{BE}}}{I_{B1}} = \frac{12 \text{ V} - 0.7 \text{ V}}{133 \mu\text{A}} = 85 \Omega$ (use std. 75 Ω)

Application Activity Results

4. $I_{C2} = \frac{V_{CC} - V_{CE(sat)}}{R_L} = \frac{12 \text{ V} - 0.3 \text{ V}}{620 \Omega} = 18.9 \text{ mA}$

$$I_{B2} = \frac{I_{C2}}{\beta_{DC(min)}} = \frac{18.9 \text{ mA}}{75} = 252 \mu\text{A}$$

$$I_{B2} = \frac{V_{CC} - V_{BE}}{R_3 + R_4}$$

$$R_3 + R_4 = \frac{V_{CC} - V_{BE}}{I_{B2}} = \frac{12 \text{ V} - 0.7 \text{ V}}{252 \mu\text{A}} = 44.8 \text{ k}\Omega$$

$R_4 = 44.8 \text{ k}\Omega - 1.2 \text{ k}\Omega = 43.6 \text{ k}\Omega$ (use lower std. value 39 kΩ or even 36 kΩ to ensure saturation)

5. The value of $V_{CE(sat)}$ in the simulation is 0.126 V. The datasheet shows a value of 0.3 V at 150 mA. The simulated value is less because the collector current is much less than the current at which the datasheet value of 0.3 V is specified.

6. Each circuit on the printed circuit board is in agreement with the schematic. See Figure AA-1 for the component identification.

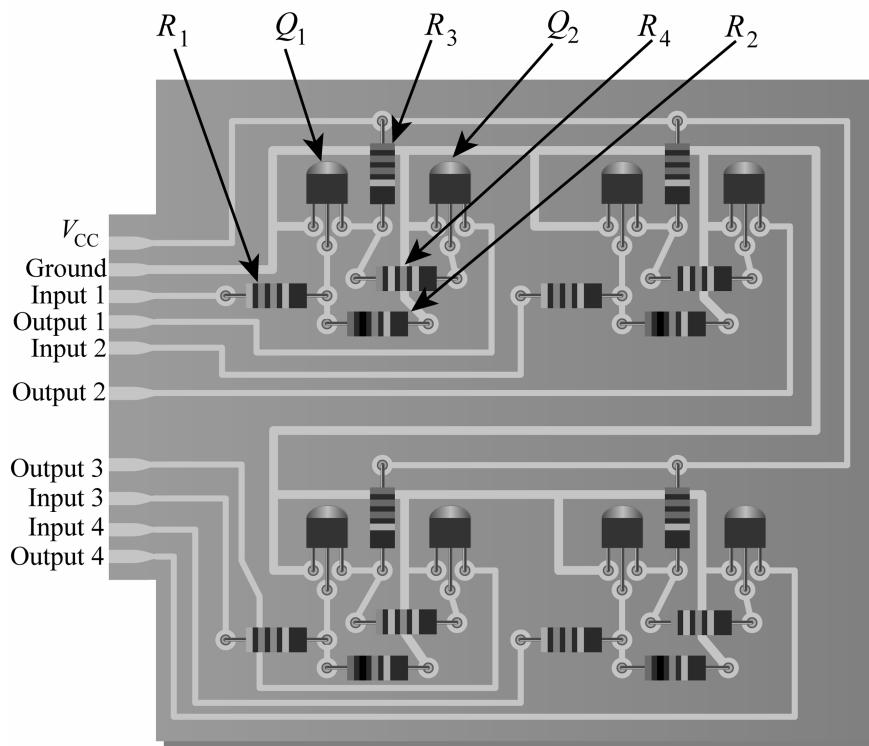


Figure AA-1 Each of the four circuits is identical.

7. The resistor values are in close agreement.

8. See Figure AA-1 for pin labels.

Application Activity Results

9. Connect V_{CC} and ground. Apply +12V to input 1. Check output 1 for +12 V. Apply 0 V to input 1. Check output 1 for approximately 0 V ($V_{CE(sat)}$). Repeat for each of the four circuits using the inputs 2-4 and outputs 2-4.
10. Add a second circuit board with only two circuits installed for zones 5 and 6. The outputs are externally connected to the circuit outputs of the other board to form a single output to the alarm.

Chapter 5

1. See Figure AA-2.

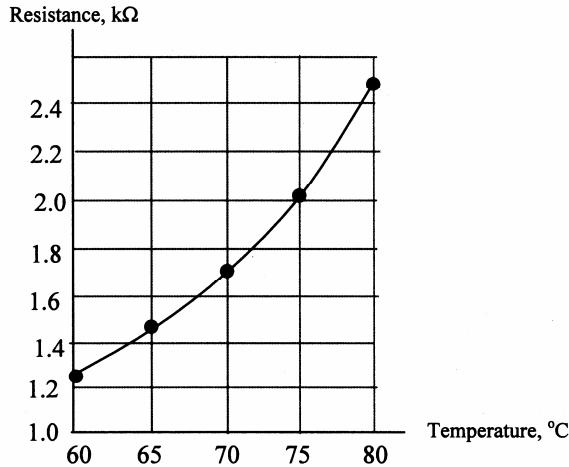


Figure AA-2

2. $R_{IN(BASE)} = \beta_{DC} R_E = 300(470 \Omega) = 141 \text{ k}\Omega$
The voltage divider is stiff for all values of R_{Therm} .

$$\text{At } 60^\circ\text{C: } V_B = \left(\frac{R_{Therm}}{R_1 + R_{Therm}} \right) V_{CC} = \left(\frac{1.256 \text{ k}\Omega}{5.965 \text{ k}\Omega} \right) 9 \text{ V} = 1.9 \text{ V}$$

$$I_E = \frac{V_B - V_{BE}}{R_E} = \frac{1.9 \text{ V} - 0.7 \text{ V}}{470 \Omega} = 2.6 \text{ mA}$$

$$I_C = I_E = 2.6 \text{ mA}$$

$$\text{At } 65^\circ\text{C: } V_B = \left(\frac{R_{Therm}}{R_1 + R_{Therm}} \right) V_{CC} = \left(\frac{1.481 \text{ k}\Omega}{6.181 \text{ k}\Omega} \right) 9 \text{ V} = 2.16 \text{ V}$$

$$I_E = \frac{V_B - V_{BE}}{R_E} = \frac{2.16 \text{ V} - 0.7 \text{ V}}{470 \Omega} = 3.1 \text{ mA}$$

$$I_C = I_E = 3.1 \text{ mA}$$

$$\text{At } 70^\circ\text{C: } V_B = \left(\frac{R_{Therm}}{R_1 + R_{Therm}} \right) V_{CC} = \left(\frac{1.753 \text{ k}\Omega}{6.453 \text{ k}\Omega} \right) 9 \text{ V} = 2.44 \text{ V}$$

$$I_E = \frac{V_B - V_{BE}}{R_E} = \frac{2.44 \text{ V} - 0.7 \text{ V}}{470 \Omega} = 3.7 \text{ mA}$$

$$I_C = I_E = 3.7 \text{ mA}$$

Application Activity Results

$$\text{At } 75^\circ\text{C: } V_B = \left(\frac{R_{\text{Therm}}}{R_i + R_{\text{Therm}}} \right) V_{\text{CC}} = \left(\frac{2.084 \text{ k}\Omega}{6.784 \text{ k}\Omega} \right) 9 \text{ V} = 2.76 \text{ V}$$

$$I_E = \frac{V_B - V_{\text{BE}}}{R_E} = \frac{2.76 \text{ V} - 0.7 \text{ V}}{470 \text{ }\Omega} = 4.4 \text{ mA}$$

$$I_C = I_E = 4.4 \text{ mA}$$

$$\text{At } 80^\circ\text{C: } V_B = \left(\frac{R_{\text{Therm}}}{R_i + R_{\text{Therm}}} \right) V_{\text{CC}} = \left(\frac{2.490 \text{ k}\Omega}{7.19 \text{ k}\Omega} \right) 9 \text{ V} = 3.12 \text{ V}$$

$$I_E = \frac{V_B - V_{\text{BE}}}{R_E} = \frac{3.12 \text{ V} - 0.7 \text{ V}}{470 \text{ }\Omega} = 5.1 \text{ mA}$$

$$I_C = I_E = 5.1 \text{ mA}$$

3. At 60°C : $V_{\text{OUT}} = V_{\text{CC}} - I_C R_2 = 9 \text{ V} - (2.6 \text{ mA})(1.0 \text{ k}\Omega) = 6.4 \text{ V}$

At 65°C : $V_{\text{OUT}} = V_{\text{CC}} - I_C R_2 = 9 \text{ V} - (3.1 \text{ mA})(1.0 \text{ k}\Omega) = 5.9 \text{ V}$

At 70°C : $V_{\text{OUT}} = V_{\text{CC}} - I_C R_2 = 9 \text{ V} - (3.7 \text{ mA})(1.0 \text{ k}\Omega) = 5.3 \text{ V}$

At 75°C : $V_{\text{OUT}} = V_{\text{CC}} - I_C R_2 = 9 \text{ V} - (4.4 \text{ mA})(1.0 \text{ k}\Omega) = 4.6 \text{ V}$

At 80°C : $V_{\text{OUT}} = V_{\text{CC}} - I_C R_2 = 9 \text{ V} - (5.1 \text{ mA})(1.0 \text{ k}\Omega) = 3.9 \text{ V}$

4. The calculated values agree reasonably well with the values measured in the simulation.

Chapter 6

1. Second stage is set for maximum gain when R_{10} is completely bypassed and equal to 0Ω .

$$R_{c1} = R_5 \parallel R_6 \parallel R_7 \parallel \beta_{\text{DC}} R_9 = 22 \text{ k}\Omega \parallel 47 \text{ k}\Omega \parallel 22 \text{ k}\Omega \parallel 200(130 \text{ }\Omega) = 6.6 \text{ k}\Omega$$

$$A_{v1} = \frac{R_{c1}}{R_4} = \frac{6.6 \text{ k}\Omega}{1.0 \text{ k}\Omega} = 6.6$$

2. $A_{v2} = \frac{R_8}{R_9} = \frac{6.8 \text{ k}\Omega}{130 \text{ }\Omega} = 52.3$

3. $A_{v(tot)} = A_{v1} A_{v2} = (6.6)(52.3) = 345$ (This exceeds the specified maximum gain)

4. $I_1 = I_2 = \frac{30 \text{ V}}{660 \text{ k}\Omega} = 45.5 \mu\text{A}$

$$I_{E1} = I_{C1} = \frac{14.3 \text{ V}}{34 \text{ k}\Omega} = 421 \mu\text{A}$$

$$I_6 = I_7 = \frac{30 \text{ V}}{69 \text{ k}\Omega} = 435 \mu\text{A}$$

$$V_{B2} = V_{\text{CC}} - I_6 R_6 = 15 \text{ V} - 20.4 \text{ V} = -5.4 \text{ V}$$

$$I_{E2} = I_{C2} = \frac{-15 \text{ V} - (-5.4 \text{ V} - 0.7 \text{ V})}{130 \text{ }\Omega + 5 \text{ k}\Omega} = 1.7 \text{ mA}$$

$$I_{\text{TOT}} = 45.5 \mu\text{A} + 421 \mu\text{A} + 435 \mu\text{A} + 1.7 \text{ mA} = 2.6 \text{ mA}$$

$$P_D = 30 \text{ V} (2.6 \text{ mA}) = 78 \text{ mW}$$

Application Activity Results

5. $V_{in(p)} = 45 \text{ mV}$
From the scope display, $V_{out(p)} = 5.5 \text{ V}$.
 $A_v = \frac{5.5 \text{ V}}{45 \text{ mV}} = 122$
6. The calculated maximum voltage gain is 345. The amplifier is not adjusted for maximum gain, but the value of 122 is within the specified range (90 to 170).
7. The pc board agrees with the schematic.
8. See Figure AA-3.

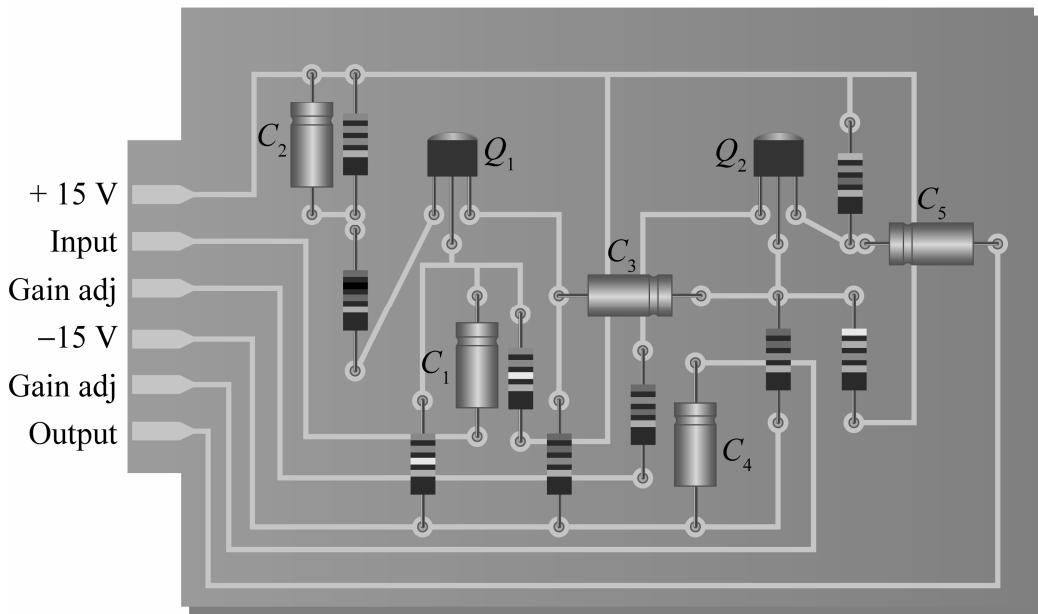


Figure AA-3

9. There is a 400 mV peak signal at the collector of Q_1 and the same signal appears at the base of Q_2 . There is no output signal. Either Q_2 is faulty or C_5 (the output coupling capacitor) is open.
10. There is a 50 mV peak signal at the base of Q_1 and a 300 mV peak signal at the collector of Q_1 . There is no signal at the base of Q_2 . The coupling capacitor C_3 is open.

Chapter 7

1. Assuming β_{DC} for Q_5 is 200,
 $R_{IN(BASE)} = \beta_{DC}R_4 = 200(220 \Omega) = 44 \text{ k}\Omega$
 $R_{IN} = R_{IN(BASE)} = 44 \text{ k}\Omega$
2. $A_v = \frac{R_3}{R_4} = \frac{1.0 \text{ k}\Omega}{220 \Omega} = 4.5$

Application Activity Results

3. The output waveform has a peak of approximately 10 V.

$$V_{out(rms)} = 0.707(10 \text{ V}) = 7.07 \text{ V}$$

$$P_{out} = \frac{V_{out(rms)}^2}{R_L} = \frac{(7.07 \text{ V})^2}{8.2 \Omega} = 6.1 \text{ W}$$

4. $A_v = \frac{10.5 \text{ V}}{2.5} = 4.2$

5. The calculated gain is 4.5 and the measured gain is 4.2. They are close within less than 10%.

6. The scope display shows the peak output of the power amplifier is approximately 9.8 V.

$$P_{out} = \frac{V_{out(rms)}^2}{R_L} = \frac{(6.93 \text{ V})^2}{8.2 \Omega} = 5.86 \text{ W}$$

7. From the scope display, $V_{in(peak)} = 2 \text{ V}$ and $V_{out(peak)} = 9.8 \text{ V}$.

$$A_v = \frac{9.8 \text{ V}}{2 \text{ V}} = 4.9$$

8. $A_v = \frac{9.8 \text{ V}}{40 \text{ mV}} = 245$

9. The pc board agrees with the schematic.

10. See Figure AA-4.

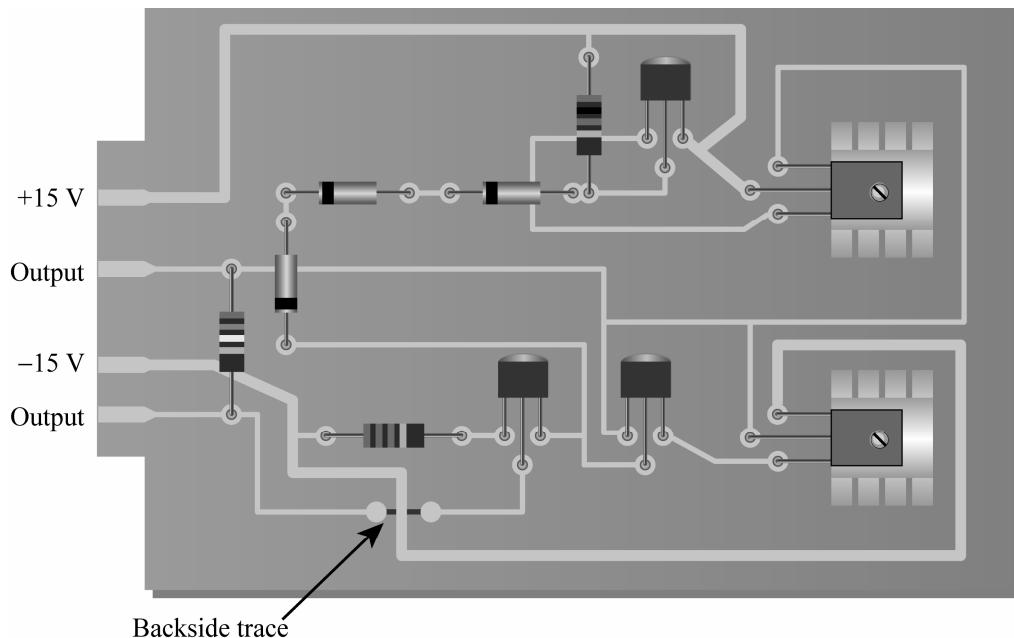


Figure AA-4

Application Activity Results

11. An output transistor is faulty.
12. The interconnections are correct.

Chapter 8

1. From the graph, $V_{\text{sensor}} = 100 \text{ mV}$ for a pH of 8.
2. From the graph, $V_{\text{sensor}} = -400 \text{ mV}$ for a pH of 3.
3. From the datasheet $y_{21s} = g_{fs} = 24 \text{ mS}$
4. The maximum drain current is specified to be 30 mA regardless of V_{DS} .
5. From the datasheet graph, with $V_{G2S} = 1 \text{ V}$ and $V_{G1S} = 0 \text{ V}$, I_D is approximately 4.5 mA.
6. For $V_{\text{OUT}} = 7 \text{ V}$, V_{sensor} is between -200 mV and -300 mV so the pH is between 4 and 5, making the solution acidic.
7. See Figure AA-5.

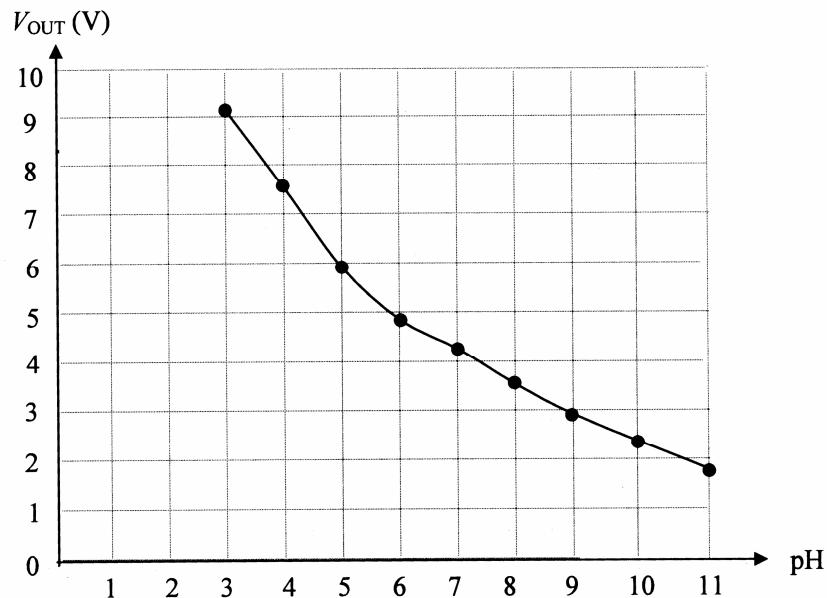


Figure AA-5

8. The pc board agrees with the schematic.

Application Activity Results

9. See Figure AA-6.

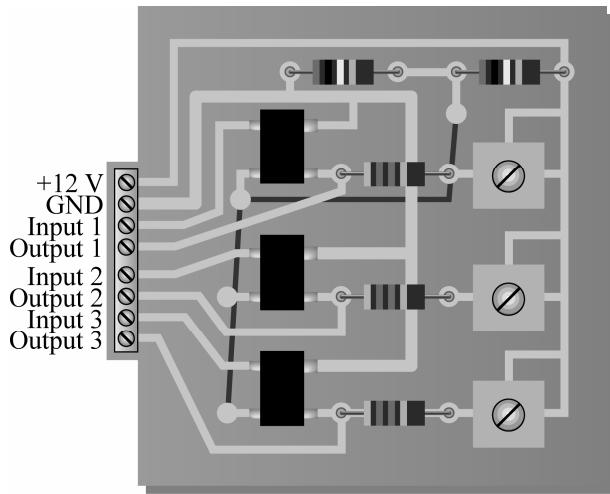


Figure AA-6

10. See Figure AA-6.

Chapter 9

1. Channel 7: 174-180 MHz
Channel 8: 180-186 MHz
Channel 9: 186-192 MHz
Channel 10: 192-198 MHz
Channel 11: 198-204 MHz
Channel 12: 204-210 MHz
Channel 13: 210-216 MHz
2. 824-896 MHz and 1850-1990 MHz
3. C_2 provides an ac ground for the gate of Q_1 (common gate).
4. $R_{IN(gate)} = \frac{V_{GS}}{I_{GSS}} = \frac{20 \text{ V}}{1 \text{ nA}} = 20 \times 10^9 \Omega$
5. $R_{in} = R_3 \parallel R_{IN(gate)} = 10 \text{ M}\Omega \parallel 20 \times 10^9 \Omega = 10 \text{ M}\Omega$
6. From the datasheet, $g_{fs} = 3000 \mu\text{mhos} = 3000 \mu\text{S}$
7. 88 MHz is the lower end of the FM band.

Application Activity Results

8. (b) $V_{out(rms)} = 0.707 V_{out(p)} = 0.707(21 \text{ mV}) = 14.8 \text{ mV}$

$$A_v = \frac{21 \text{ mV}}{10 \mu\text{V}} = 2100$$

(c) $V_{out(rms)} = 0.707 V_{out(p)} = 0.707(100 \text{ mV}) = 70.7 \text{ mV}$

$$A_v = \frac{70.7 \text{ mV}}{10 \mu\text{V}} = 7070$$

9. The pc board agrees with the schematic.

10. It is a decoupling capacitor connected to the dc supply line for noise elimination.

11. See Figure AA-7.

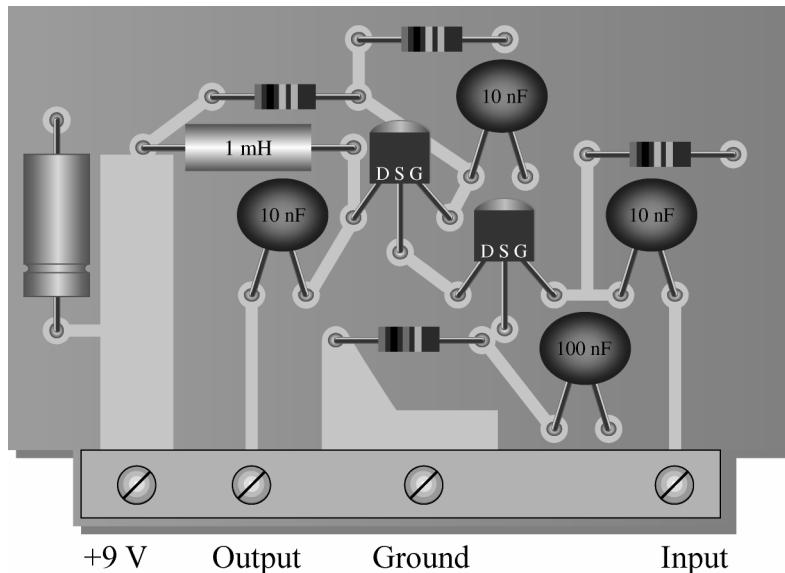


Figure AA-7

Chapter 10

1. For stage 1 input circuit:

$$f_{cl(input)} = \frac{1}{2\pi(R_1 \parallel R_2 \parallel \beta_{ac}R_4)C_1}$$

$$C_1 = \frac{1}{2\pi(R_1 \parallel R_2 \parallel \beta_{ac}R_4)f_{cl(input)}} = \frac{1}{2\pi(330 \text{ k}\Omega \parallel 330 \text{ k}\Omega \parallel 100(1.0 \text{ k}\Omega))193 \text{ Hz}} = 13.2 \text{ nF}$$

2. For stage 2 input circuit:

$$f_{cl(input)} = \frac{1}{2\pi(R_5 + R_6 \parallel R_7 \parallel \beta_{ac}(R_9 + R_{10}))C_3}$$

$$C_3 = \frac{1}{2\pi(R_5 + R_6 \parallel R_7 \parallel \beta_{ac}(R_9 + R_{10}))f_{cl(input)}} = \frac{1}{2\pi(35.2 \text{ k}\Omega)193 \text{ Hz}} = 23.4 \text{ nF}$$

Application Activity Results

3. Midrange gain is 33.4 dB. Gain at 60 Hz is 9.7 dB.
$$33.4 \text{ dB} - 9.7 \text{ dB} = 23.7 \text{ dB}$$
4. At 5 kHz from scope display: $V_{out} = 0.707(2.6 \text{ V}) = 1.84 \text{ V}$
5. At 60 Hz from scope display: $V_{out} = 0.707(240 \text{ mV}) = 170 \text{ mV}$
6. At 300 Hz: $V_{out} = 0.707(1.84 \text{ V}) = 1.30 \text{ V}$
7. $A_v = \frac{2.6 \text{ V}}{45 \text{ mV}} = 57.8$
$$A_v (\text{dB}) = 20 \log A_v = 20 \log(57.8) = 35.2 \text{ dB}$$
8. $A_v = \frac{170 \text{ mV}}{45 \text{ mV}} = 3.78$
$$A_v (\text{dB}) = 20 \log A_v = 20 \log(3.78) = 11.6 \text{ dB}$$

Chapter 11

1. From the datasheet, $V_{PRM} = 400 \text{ V}$ for the 2N6397.
2. From the datasheet, the maximum on-state rms current is 12 A.
3. $V_{on(max)} = 1.5 \text{ V}$
 $I_F = 50 \text{ mA}$
 $P_{max} = V_{on(max)}I_F = (1.5 \text{ V})(50 \text{ mA}) = 750 \text{ mW}$
4. The SCR conducts during the flat portion of the waveform.
5. The SCR will conduct more if the control voltage is reduced.
6. The motor speed will increase when the SCR conducts more as a result of a reduced control voltage.
7. The pc board agrees with the schematic.

Application Activity Results

8. See Figure AA-8.

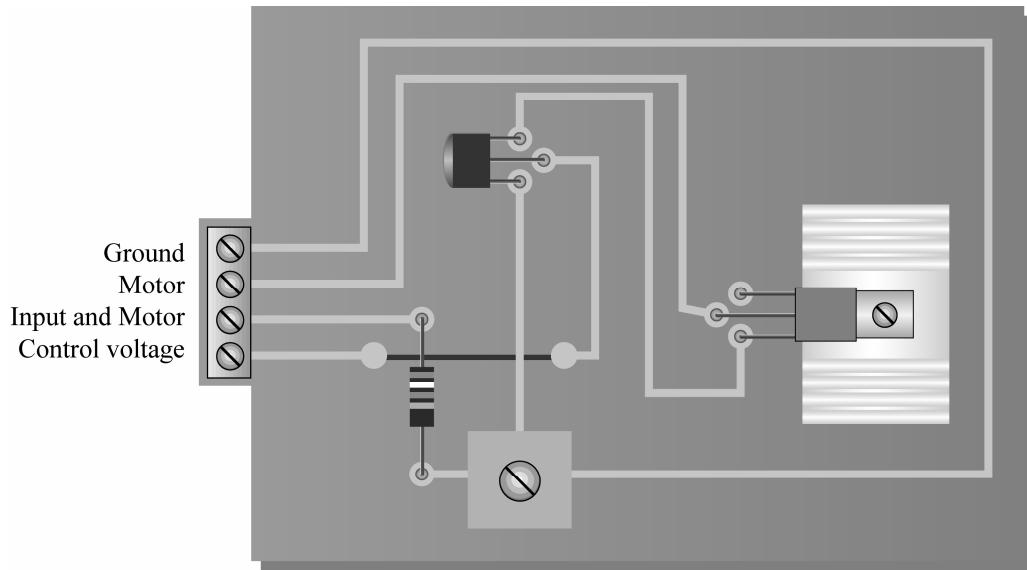


Figure AA-8

9. (a) Test of board 1: Working properly
(b) Test of board 2: SCR is not triggering on.
(c) Test of board 3: SCR continuously on
10. (a) No problem
(b) PUT faulty or SCR gate open
(c) SCR shorted

Chapter 12

1. The op-amp configuration is a noninverting amplifier.
2. The maximum and minimum gains of the op-amp stage are

$$A_v = 1 + \frac{R_f}{R_i}$$

$$A_{v(\max)} = 1 + \frac{150 \text{ k}\Omega}{1 \text{ k}\Omega} = 151$$

$$A_{v(\min)} = 1 + \frac{150 \text{ k}\Omega}{2 \text{ k}\Omega} = 75$$

3. Maximum output voltage of the op-amp stage is
 $V_{out(\max)} = A_{v(\max)} V_{in} = (150)(50 \text{ mV}) = 7.5 \text{ V}$

Application Activity Results

4. The ideal maximum power to the speaker is

$$V_{out(rms)} = 7.5 \text{ V}$$

$$P_{\max} = \frac{V_{out(rms)}^2}{R_{speaker}} = \frac{(7.5 \text{ V})^2}{8 \Omega} = 7.03 \text{ W}$$

5. Noninverting input: pin 3; inverting input: pin 2; output: pin 6; $\pm 15 \text{ V}$: pin 7; -15 V pin 4.

6. From the datasheet: Maximum power consumption @ $+15 \text{ V}$ is 85 mW.

7. From the datasheet, the typical output voltage swing is $+14 \text{ V}$.

8. $V_{1(rms)} = 50 \text{ mV}$ input voltage

$$V_{2(rms)} = 0.707(10 \text{ V}) = 7.07 \text{ V}$$
 output of op-amp

$$V_{3(rms)} = 0.707(9 \text{ V}) = 6.36 \text{ V}$$
 voltage across the load

9. Voltage gain of op-amp stage:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{V_2}{V_1} = \frac{7.07 \text{ V}}{50 \text{ mV}} = 141.4$$

10. Overall voltage gain:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{V_3}{V_1} = \frac{6.36 \text{ V}}{50 \text{ mV}} = 127.2$$

11. The pc board agrees with the schematic.

12. See Figure AA-9.

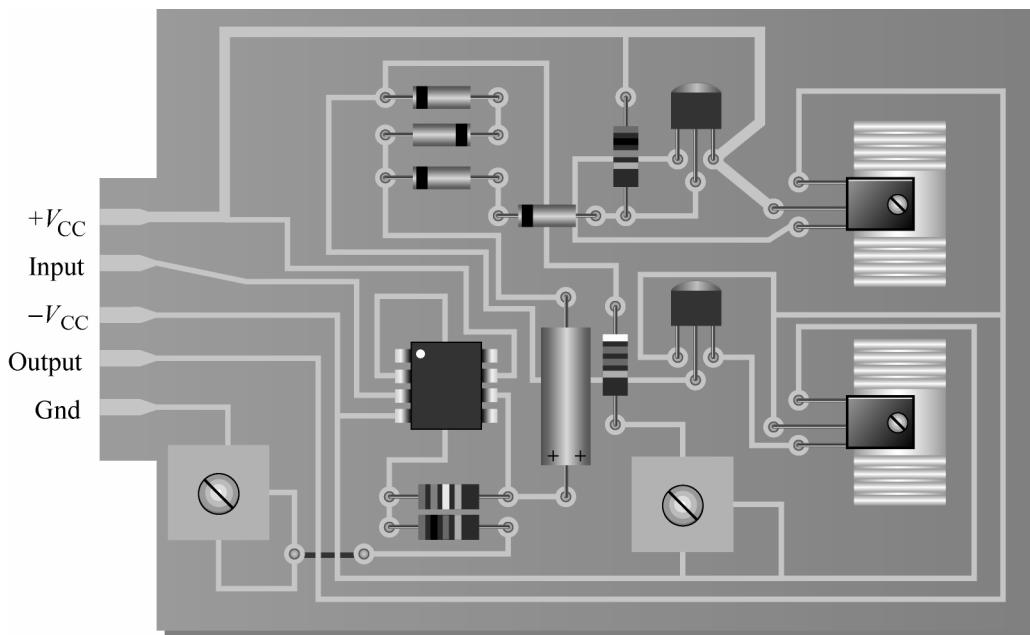


Figure AA-9

Application Activity Results

13. (a) Working properly
(b) No signal at C_1 .
(c) Top half of output clipped.
(d) Bottom half of output clipped.
14. (a) No problem
(b) Op-amp or C_1 faulty.
(c) Q_3 or Q_4 faulty.
(d) Q_1 or Q_2 faulty.

Chapter 13

1. R_1 , R_2 , and R_3 determine the reference voltage.
2. $I_{R1} = I_{R2} = I_{R3} = \frac{24 \text{ V}}{R_1 + R_2 + R_3} = \frac{24 \text{ V}}{612 \text{ k}\Omega} = 39 \mu\text{A}$
 $V_{R3} = I_{R3}R_3 = 39 \mu\text{A}(56 \text{ k}\Omega) = 2.18 \text{ V}$
 $V_{\text{REF(min)}} = -12 \text{ V} + V_{R3} = -12 \text{ V} + 2.18 \text{ V} = -9.82 \text{ V}$
3. $V_{R2/R3} = I_{R3}(R_2 + R_3) = 39 \mu\text{A}(556 \text{ k}\Omega) = 21.7 \text{ V}$
 $V_{\text{REF(max)}} = -12 \text{ V} + 21.7 \text{ V} = +9.7 \text{ V}$
4. The output pulse amplitude is limited to +5 V and 0 V by the +5V supply voltage.
5. As R_2 is adjusted, the reference voltage at which the comparator is triggered is varied from a maximum of +9.82 V to a minimum of -9.7 V. This changes the point on the input sine wave where the comparator changes state. The higher up on the sine wave that the trigger point occurs, the smaller the duty cycle.
6. Noninverting input: pin 2; inverting input: pin 3; output: pin 7; +12 V: pin 8; -12 V: pin 4.
7. $V_p = 10 \text{ V}$
 $V_{rms} = 0.707(10 \text{ V}) = 7.07 \text{ V}$
8. $V_{\text{pulse}} = 5 \text{ V}$
9. $T = (2 \text{ div})(50 \mu\text{s}/\text{div}) = 100 \mu\text{s}$
 $f = \frac{1}{T} = \frac{1}{100 \mu\text{s}} = 10 \text{ kHz}$
10. (a) Each small division = $40 \mu\text{s}$
Pulse width = $1.5(40 \mu\text{s}) = 60 \mu\text{s}$
Period = $5 \text{ div}(200 \mu\text{s}/\text{div}) = 1000 \mu\text{s}$
% Duty cycle = $\left(\frac{60 \mu\text{s}}{1000 \mu\text{s}}\right)100 = 6\%$ (exceeds specs)

Application Activity Results

- (b) Pulse width = $4.6 \text{ div}(200 \mu\text{s}) = 920 \mu\text{s}$
Period = $5 \text{ div}(200 \mu\text{s/div}) = 1000 \mu\text{s}$
 $\% \text{ Duty cycle} = \left(\frac{920 \mu\text{s}}{1000 \mu\text{s}} \right) 100 = 92\% \text{ (exceeds spec)}$
- (c) Each small division = $4 \mu\text{s}$
Pulse width = $2(4 \mu\text{s}) = 8 \mu\text{s}$
Period = $5 \text{ div}(20 \mu\text{s/div}) = 100 \mu\text{s}$
 $\% \text{ Duty cycle} = \left(\frac{8 \mu\text{s}}{100 \mu\text{s}} \right) 100 = 8\% \text{ (exceeds spec)}$
- (d) Pulse width = $4.6(20 \mu\text{s}) = 92 \mu\text{s}$
Period = $5 \text{ div}(20 \mu\text{s/div}) = 100 \mu\text{s}$
 $\% \text{ Duty cycle} = \left(\frac{92 \mu\text{s}}{100 \mu\text{s}} \right) 100 = 92\% \text{ (exceeds spec)}$

11. The pc board agrees with the schematic.

12. See Figure AA-10.

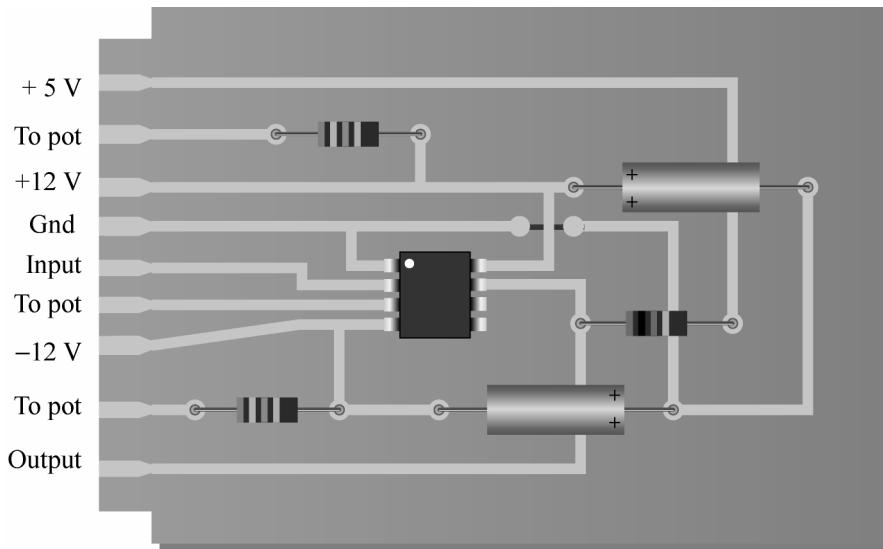


Figure AA-10

13. The connections are correct.

Chapter 14

1. Pin 3 is connected to pin 11. From Table 1 on the on-line datasheet, the gain is 500.

Application Activity Results

2. Table 1 in the on-line datasheet shows pin connections for various fixed gains. Also, the formula can be applied for pins 3 and 16, as shown in Figure AA-11.

Table I.

Gain (Nominal)	Temperature Coefficient (Nominal)	Pin 3 to Pin	Connect Pins
1	-0 ppm/ $^{\circ}\text{C}$	—	—
100	-1.5 ppm/ $^{\circ}\text{C}$	13	—
125	-5 ppm/ $^{\circ}\text{C}$	13	11 to 16
137	-5.5 ppm/ $^{\circ}\text{C}$	13	11 to 12
186.5	-6.5 ppm/ $^{\circ}\text{C}$	13	11 to 12 to 16
200	-3.5 ppm/ $^{\circ}\text{C}$	12	—
250	-5.5 ppm/ $^{\circ}\text{C}$	12	11 to 13
333	-15 ppm/ $^{\circ}\text{C}$	12	11 to 16
375	-0.5 ppm/ $^{\circ}\text{C}$	12	13 to 16
500	-10 ppm/ $^{\circ}\text{C}$	11	—
624	-5 ppm/ $^{\circ}\text{C}$	11	13 to 16
688	-1.5 ppm/ $^{\circ}\text{C}$	11	11 to 12; 13 to 16
831	+4 ppm/ $^{\circ}\text{C}$	11	16 to 12
1000	0 ppm/ $^{\circ}\text{C}$	11	16 to 12; 13 to 11

Pins 3 and 16 program the gain according to the formula

$$R_G = \frac{40k}{G - 1}$$

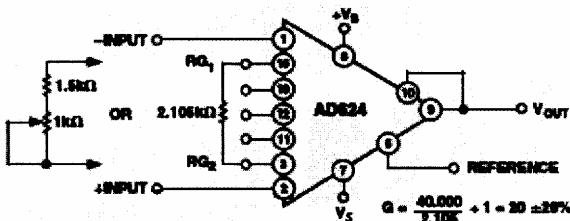


Figure AA-11 Operating connections for $G = 20$.

3. From the scope, $V_{out(pp)} = (2.9 \text{ div})(50 \text{ mV/div}) = 145 \text{ mV}$

$$V_{out(rms)} = 0.707 \left(\frac{145 \text{ mV}}{2} \right) = 52.1 \text{ mV}$$

$$A_v = \frac{V_{out(rms)}}{V_{in(rms)}} = \frac{51.2 \text{ mV}}{100 \mu\text{V}} = 512$$

The gain indicated by the pin connections is 500.

4. The hysteresis is approximately 50 mV.

5. The shield-guard driver output on the scope display is approximately 100 mV rms. This is the same as the common-mode signal.

6. The pc board agrees with the schematic.

7. See Figure AA-12.

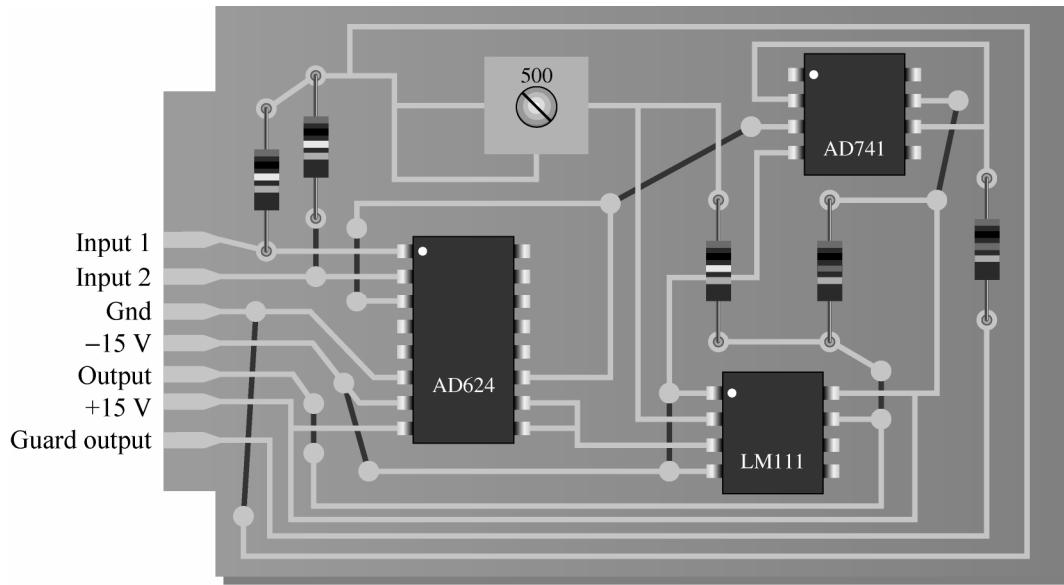


Figure AA-12

Chapter 15

1. RFID systems are used for tracking and identification of objects.
2. The basic RFID system components are tag, reader, and processor.
3. The tag stores an identification code and other information which it transmits to a reader in the form of a modulated signal.
4. The reader receives the transmitted information from the tag and converts it to digital form.
5. The band-pass filter eliminates frequencies other than the frequency transmitted by the tag.
6. The low-pass filter eliminates the carrier frequency and passes only the modulating signal frequency.
7. Gain of amplifier U2 and U3:

$$A_v = 1 + \frac{R_5}{R_6} = 1 + \frac{R_7}{R_8} = 1 + \frac{100 \text{ k}\Omega}{2.2 \text{ k}\Omega} = 46.5$$

$$8. f_o = \frac{1}{2\pi C} = \sqrt{\frac{R_1 + R_3}{R_1 R_2 R_3}} = \frac{1}{2\pi(200 \text{ pF})} \sqrt{\frac{15 \text{ k}\Omega + 1 \text{ k}\Omega}{(15 \text{ k}\Omega)(39 \text{ k}\Omega)(1 \text{ k}\Omega)}} = 132 \text{ kHz}$$

This is within 6% of the measured center frequency.

Application Activity Results

9. The low-pass filter is set for an approximate Butterworth response since the damping factor is

$$DF = 2 - \left(\frac{R_{12}}{R_{11}} \right) = 2 - \left(\frac{560 \Omega}{1000 \Omega} \right) = 1.44$$

10. $f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi(1 \text{ k}\Omega)(10 \text{ nF})} = 15.9 \text{ kHz}$

11. $V_{\text{REF}} = \left(\frac{R_{15}}{R_{14} + R_{15}} \right) V_{CC} = \left(\frac{15 \text{ k}\Omega}{115 \text{ k}\Omega} \right) 15 \text{ V} = 1.96 \text{ V}$

A positive reference is required because the output of the LP filter is a positive signal.

12. The pc board agrees with the schematic.

13. See Figure AA-13.

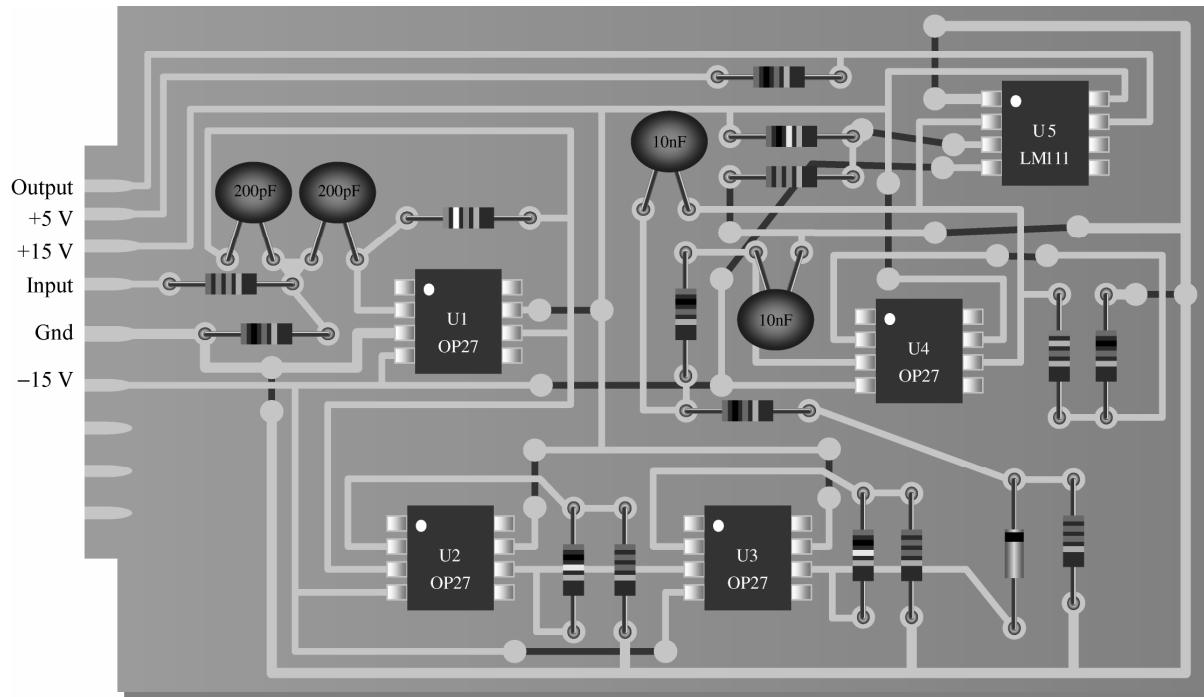


Figure AA-13

Chapter 16

$$1. \quad A_v = \frac{C_1}{C_2} = \frac{C_4}{C_5} = \frac{100 \text{ nF}}{10 \text{ nF}} = 10$$

$$2. \quad C_T = \frac{C_4 C_5}{C_4 + C_5} = \frac{(100 \text{ nF})(10 \text{ nF})}{110 \text{ nF}} = 9.1 \text{ nF}$$

$$f_r = \frac{1}{2\pi\sqrt{L_1 C_T}} = \frac{1}{2\pi\sqrt{(150 \mu\text{H})(9.1\text{nF})}} = 136 \text{ kHz}$$

This calculated frequency is within 10% of the 125 kHz measured frequency.

$$3. \quad f_r = \frac{1.44}{(R_7 + R_8)C_3} = \frac{1.44}{(6.2 \text{ k}\Omega + 6.2 \text{ k}\Omega)10\text{nF}} = 11.6 \text{ kHz}$$

The measured frequency is 10 kHz. The calculated value differs by 16%.

4. The forward resistance of the diode is a possible factor in the difference between the calculated and measured values in 2 and 3.
5. Q_2 operates as an analog switch that turns the carrier signal (125 kHz) on and off.
6. First waveform: Output of ASK generator containing bursts of the 125 kHz carrier signal at 10 kHz.

Second waveform: output of the RFID rectifier.

Third waveform: The rectified signal after filtering out the 125 kHz carrier.

Fourth waveform: Pulse output of the RFID reader.

7. The pc board agrees with the schematic of the ASK test generator.

Application Activity Results

8. See Figure AA-14.

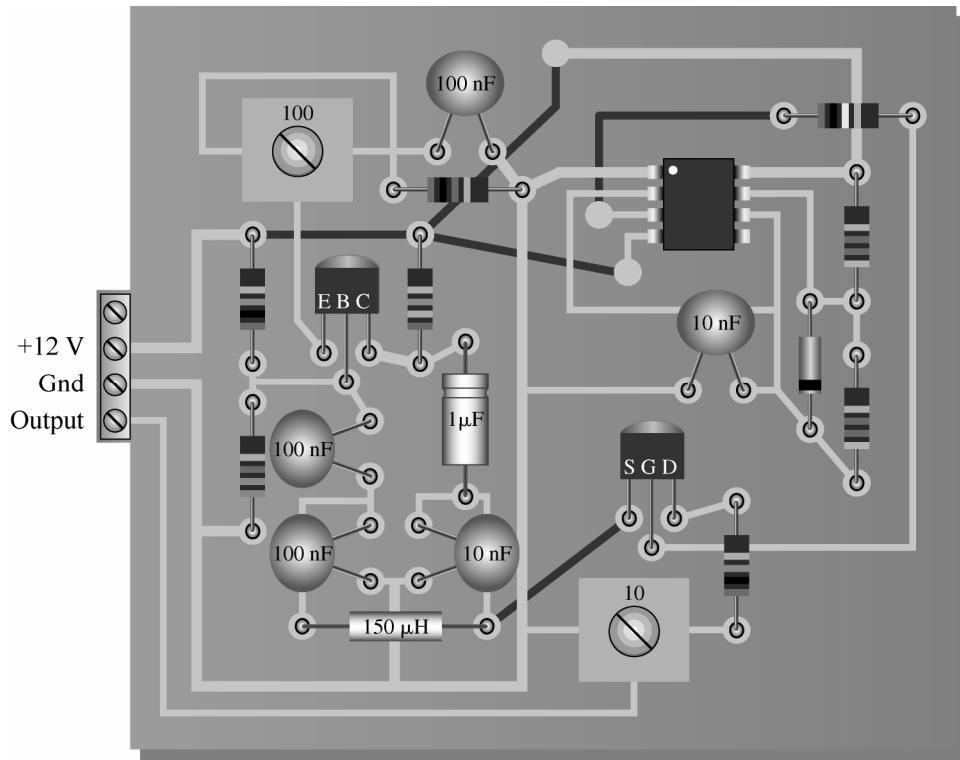


Figure AA-14

Chapter 17

1. From the datasheet, $V_{O(\min)} = 8.65 \text{ V}$ and $V_{O(\max)} = 9.35 \text{ V}$.
2. From the datasheet, the output voltage can change a maximum of 180 mV.

$$3. I_{L(\max)} = \frac{V_{O(\max)}}{R_L} = \frac{9.4 \text{ V}}{330 \Omega} = 28.3 \text{ mA}$$

$$P_{D(\max)} = (28.3 \text{ mA})^2 330 \Omega = 265 \text{ mW}$$

$$4. V_{R2(\max)} = \left(\frac{1 \text{ k}\Omega}{1330 \Omega} \right) 9.4 \text{ V} = 7.07 \text{ V}$$

$$P_{D(\max)} = \frac{(7.07 \text{ V})^2}{1 \text{ k}\Omega} = 50 \text{ mW}$$

$$5. \frac{I_{pri}}{I_{sec}} = \frac{V_{sec}}{V_{pri}}$$
$$I_{pri} = \left(\frac{(0.707)(34 \text{ V})}{120 \text{ V}} \right) 100 \text{ mA} = 20 \text{ mA}$$

Fuse rating should exceed 20 mA.

Application Activity Results

6. The pc board agrees with the schematic.
7. $P_D = (32.6 \text{ V} - 9 \text{ V})100 \text{ mA} = 2.36 \text{ W}$
8. $P_D = (32.6 \text{ V} - 30 \text{ V})100 \text{ mA} = 236 \text{ mW}$

Summary of MultiSIM Circuit Files

Chapter 1:

Circuit	MultiSIM
E01-01	$V_R(1) = 9.29 \text{ V}$ $V_D(1) = 0.713 \text{ V}$ $V_R(2) = 4.99 \text{ V}$ $V_D(2) = 4.99 \text{ V}$
F01-40a	$V_R = 0.020 \text{ nV}$
F01-40b	$V_R = 99.151 \text{ V}$
F01-40c	$V_R = 14.01 \text{ V}$
F01-40d	$V_D = 0.651 \text{ V}$
F01-41a	$V_D = 25.000 \text{ V}$
F01-41b	$V_D = 15.000 \text{ V}$
F01-41c	$V_D = 2.500 \text{ V}$
F01-41d	$V_R = 11.285 \text{ nV}$
F01-42	$V_A = 25.00 \text{ V}$ $V_B = 24.255 \text{ V}$ $V_C = 8.746 \text{ V}$ $V_D = 8.000 \text{ V}$
TSP01-22	$V_R = 3.000 \text{ V}$
TSP01-23	$V_D = 99.994 \text{ V}$
TSP01-24	$V_D = 32.434$
TSP01-25	$V_D = -1.000 \text{ pV}$
TSP01-26	$V_D = 0.668 \text{ V}$
TSP01-27	$V_D = 0.192 \text{ nV}$
TSP01-28	$V_D = 2.577 \text{ V}$
TSP01-29	$V_D = 11.994 \text{ V}$
TSP01-30	$V_A = 25.00 \text{ V}$ $V_B = 24.253 \text{ V}$ $V_C = 8.000 \text{ V}$ $V_D = 8.000 \text{ V}$

Chapter 2:

Circuit	MultiSIM
E02-02a	Half-wave $V_P = 4.3 \text{ V}$
E02-02b	Half-wave $V_P = 99.2 \text{ V}$
E02-03	Half-wave $V_P = 84.2 \text{ V}$
E02-05	Full-wave $V_P = 24.3 \text{ V}$
E02-06	Full-wave $V_P = 15.74 \text{ V}$
E02-07	$V_L(\max) = 14.7 \text{ V}$ $V_L(\min) = 13.8 \text{ V}$
E02-09	Half-wave $V_P(\max) = 9.1 \text{ V}$ $V_P(\min) = 779.1 \text{ mV}$

Summary of MultiSIM Files

Circuit	MultiSIM
E02-10	Clipped $V_p(\max) = 5.7 \text{ V}$ $V_p(\min) = -5.7 \text{ V}$
E02-11	Negative Clamp $V_p(\max) = 9.0 \text{ V}$ $V_p(\min) = -18.0 \text{ V}$
E02-12	Clipped $V_p(\max) = 729 \text{ mV}$ $V_p(\min) = -45.5 \text{ V}$
F02-73a	Half-wave $V_p = 4.2 \text{ V}$
F02-73b	Half-wave $V_p = -49.3 \text{ V}$
F02-74	Half-wave $V_p = 83.964 \text{ V}$
F02-76	Full-wave $V_p = 20.476 \text{ V}$
F02-77	Full-wave $V_p = 32.296 \text{ V}$
F02-78	$V_L(\max) = 47.6 \text{ V}$ $V_L(\min) = 46.6 \text{ V}$
F02-79	Half-wave $V_p(\max) = 712.7 \text{ mV}$ $V_p(\min) = -10.0 \text{ V}$
F02-83a	Clipped $V_p(\max) = 721.9 \text{ mV}$ $V_p(\min) = -722.0 \text{ mV}$
F02-83b	Clipped $V_p(\max) = 722.0 \text{ mV}$ $V_p(\min) = -722.0 \text{ mV}$
F02-86	$V_{\text{SEC}} = 119.812 \text{ V}_{\text{AC}}$ $V_{\text{REC}} = 0.2 \text{ V}$ $V_L = 59.1 \text{ V}$
F02-88	Full-wave $V_p = 16.211 \text{ V}$
TSE02-01	$V_{\text{FUSE}} = 0 \text{ V}$
TSE02-02	$V_{\text{SURGE}} = 0 \text{ V}$
TSE02-03	Not implemented
TSP02-52	Unrectified AC $10.0 \text{ V}_{\text{PP}}$
TSP02-53	$V_L(\max) = 38.4 \text{ V}$ $V_L(\min) = -49.3 \text{ V}$
TSP02-54	$V_L = 0 \text{ V}$
TSP02-55	Half-wave $V_p = 19.6 \text{ V}$
TSP02-56	Clipped Full-wave $V_p(\max) = 59.8 \text{ V}$ $V_p(\min) = 1.6 \text{ V}$
TSP02-57	Full-wave $V_p(\max) = 49.1 \text{ V}$ $V_p(\min) = 784.1 \text{ mV}$
TSP02-58	Positive Clipped $V_p(\max) = 679.1 \text{ mV}$ $V_p(\min) = -909.1 \text{ mV}$
TSP02-59	Half-wave $V_p(\min) = -30.0 \text{ V}$

Summary of MultiSIM Files

Circuit	MultiSIM
TSP02-60	Half-wave $V_P(\max) = 16.0 \text{ V}$ $V_P(\min) = 480.1 \text{ mV}$

Chapter 3:

Circuit	MultiSIM
E03-05	$I_D(1) = 4.749 \mu\text{A}$ $V_D(1) = 4.860 \text{ V}$ $I_D(2) = 206 \text{ mA}$ $V_D(2) = 5.137 \text{ V}$
E03-06	$I_D = 1.330 \text{ mA}$ $V_R = 0.024 \text{ A}$ $V_D = 11.930 \text{ V}$
E03-08	Clipped $V_P(\max)(1) = 5.6 \text{ V}$ $V_P(\min)(1) = -3.8 \text{ V}$ $V_P(\max)(2) = 6.7 \text{ V}$ $V_P(\min)(1) = -15.5 \text{ V}$
F03-70	$I_R(1) = 150 \text{ mA}$ $V_R(1) = 4.692 \text{ V}$ $I_R(2) = 40 \text{ mA}$ $V_R(2) = 5.116 \text{ V}$
F03-73	$I_D = 34 \text{ mA}$
F03-77	$V_{\text{OUT}} = 11.002 \text{ V}$
TSE03-01	$V_{\text{OUT}} = 10.439 \text{ V}$
TSE03-02	$V_C = 0 \text{ V}_{\text{DC}}$ $V_{\text{OUT}} = 0.000 \text{ V}_{\text{DC}}$
TSE03-03	$V_D = 15.0 \text{ V}_{\text{DC}}$ with ripple $V_{\text{OUT}} = 15.0 \text{ V}_{\text{DC}}$
TSE03-04	$V_D = 0 \text{ V}$ Blown fuse
TSP03-47	$V_{\text{OUT}} = 8.000 \text{ V}_{\text{DC}}$
TSP03-48	Spikey output $V_{\text{OUT}} = 12.0 \text{ V}$ $V_{\text{SPIKE}} = 9.0 \text{ V}$
TSP03-49	$V_R > 26 \text{ V}_{\text{DC}}$ $V_{\text{OUT}} = 0.079 \text{ nV}_{\text{DC}}$
TSP03-50	$V_R = 22.243 \text{ V}$

Chapter 4:

Circuit	MultiSIM
E04-02	$I_B = 412 \mu\text{A}$ $I_C = 62 \text{ mA}$ $I_E = 62 \text{ mA}$ $V_{CB} = 2.94 \text{ V}$ $V_{CE} = 3.821 \text{ V}$

Summary of MultiSIM Files

Circuit	MultiSIM
E04-04	$I_B = 217 \mu A$ $I_C = 9.838 mA$
E04-11	$I_C(1) = 16 mA$ $V_{CE}(1) = 2.952 V$ $I_C(2) = 13 mA$ $V_{CE}(2) = 3.709 V$
F04-54	$I_B = 667 \mu A$ $I_C = 32 mA$ $I_E = 33 mA$
F04-55a	$V_{BC} = -4.608 V$ $V_{BE} = 877 mV$ $V_{CE} = 5.458 V$
F04-55b	$V_{BC} = 3.254 V$ $V_{BE} = -0.834 V$ $V_{CE} = -4.088 V$
F04-56	$I_B = 24 \mu A$ $I_C = 1.197 mA$ $I_E = 1.221 mA$
F04-57	$V_B(1) = 10.000 V$ $V_C(1) = 20.000 V$ $V_E(1) = 9.228 V$ $V_B(2) = -4.000 V$ $V_C(2) = -12.000 V$ $V_E(2) = -3.216 V$
F04-58	$V_C = 222 mV$
F04-59	$V_B = 0.798 V$ $V_C = 0.389 V$
TSE04-01	$V_B = 0.716 V$ $V_C = 5.172 V$
TSE04-02	$V_B = 0.598 V$ $V_C = 0.022 V$
TSE04-03	$V_B = 2.998 V$ $V_C = 9.000 V$
TSP04-55	$V_{RB} = 2.471 V$
TSP04-56	$V_{RC} = 14.982 V$
TSP04-57	$V_{CE} = -0.021 nV$
TSP04-58	$V_{CE} = 10.0 V$
TSP04-59	$V_B = 10.00 V$ $V_C = 20.00 V$ $I_C = 91 mA$
TSP04-60	$I_C = 5.456 mA$
TSP04-61	$I_B = 0.444 pA$ $V_C = 4.999 V$
TSP04-62	$I_B = 4.350 \mu A$ $I_C = -0.021 pA$

Summary of MultiSIM Files

Chapter 5:

Circuit	MultiSIM
E05-01	$V_{BE} = 869 \text{ mV}$ $V_{CE} = 7.187 \text{ V}$ $I_C = 39 \text{ mA}$
E05-02	$V_{BE} = 814 \text{ mV}$ $V_{CE} = 2.775 \text{ V}$ $I_C = 4.615 \text{ mA}$
E05-04	$V_{BE} = -794 \text{ mV}$ $V_{CE} = -3.082 \text{ V}$ $I_C = 2.155 \text{ mA}$
E05-08a	$V_{BE} = 0.802 \text{ V}$ $V_{CE} = 10.385 \text{ V}$ $I_C = 2.884 \text{ mA}$
E05-08b	$V_{BE} = 0.806 \text{ V}$ $V_{CE} = 10.101 \text{ V}$ $I_C = 3.391 \text{ mA}$
E05-10	$V_{BE} = 0.767 \text{ V}$ $V_{CE} = 2.366 \text{ V}$ $I_C = 763 \mu\text{A}$
F05-34	$V_{CE} = 10.771 \text{ V}$ $I_C = 923 \mu\text{A}$
F05-35	$V_{CE} = 6.001 \text{ V}$ $I_C = 5.126 \text{ mA}$
F05-38	$V_B = 2.047 \text{ V}$ $V_C = 6.237 \text{ V}$ $V_E = 1.267 \text{ V}$
F05-39	$V_B = -1.666 \text{ V}$ $V_C = -9.197 \text{ V}$ $V_E = -0.881 \text{ V}$
F05-41	$V_{BE} = -0.846 \text{ V}$ $V_{CE} = -7.182 \text{ V}$ $I_C = 16 \text{ mA}$
F05-42	$V_{BE} = 0.774 \text{ V}$ $V_{CE} = 1.169 \text{ V}$ $I_C = 1.017 \text{ mA}$
TSE05-01	$V_B = 0.047 \mu\text{V}$ $V_C = 10.000 \text{ V}$ $V_E = 4.700 \text{ nV}$
TSE05-02	$V_B = 3.197 \text{ V}$ $V_C = 10.000 \text{ V}$ $V_E = 0.000 \text{ V}$
TSE05-03	$V_B = 3.145 \text{ V}$ $V_C = 5.061 \text{ V}$ $V_E = 2.329 \text{ V}$
TSE05-04	$V_B = 3.197 \mu\text{V}$ $V_C = 10.000 \text{ V}$ $V_E = 2.695 \text{ V}$

Summary of MultiSIM Files

Circuit	MultiSIM
TSP05-55	$V_B = 669 \text{ mV}$ $V_C = 18 \text{ mV}$
TSP05-56	$I_B = -0.444 \text{ pA}$
TSP05-57	$V_B = 3.664 \text{ V}$
TSP05-58	$V_C = -2.846 \text{ V}$
TSP05-59	$V_C = -10.000 \text{ V}$ $V_E = 2.438 \text{ V}$
TSP05-60	$V_B = 2.999 \text{ V}$

Chapter 6:

Circuit	MultiSIM
E06-08	$V_C = 5.530 \text{ V}_{\text{DC}}$ $V_b = 26.1 \text{ mV}_{\text{PP}}$ $V_c = 221.9 \text{ mV}_{\text{PP}}$ DC values off, gain is OK
E06-09	$V_b = 2.8 \text{ V}_{\text{PP}}$ $V_c = 2.8 \text{ V}_{\text{PP}}$ DC values off, gain is OK
E06-11	$V_b = 14.0 \text{ mV}_{\text{PP}}$ $V_c = 930.5 \text{ mV}_{\text{PP}}$
F06-51	$V_B = 2.570 \text{ V}_{\text{DC}}$ $V_b = 99 \text{ mV}_{\text{AC}}$ $V_{\text{OUT}} \approx 0 \text{ V}_{\text{DC}}$ $V_{\text{out}} = 216 \text{ mV}_{\text{AC}}$
F06-52	$V_B = 1.593 \text{ V}_{\text{DC}}$ $V_b = 100 \text{ mV}_{\text{AC}}$ $V_{\text{OUT}} = 7.990 \text{ mV}_{\text{DC}}$ $V_{\text{out}} = 395 \text{ mV}_{\text{AC}}$
F06-53	$V_B = 1.593 \text{ V}_{\text{DC}}$ $V_b = 100 \text{ mV}_{\text{AC}}$ $V_{\text{OUT}} = 7.990 \text{ mV}_{\text{DC}}$ $V_{\text{out}} = 395 \text{ mV}_{\text{AC}}$
F06-54	$V_B = 1.741 \text{ V}_{\text{DC}}$ $V_b = 1.01 \text{ V}_{\text{AC}}$ $V_{\text{OUT}} = 88 \text{ mV}_{\text{DC}}$ $V_{\text{out}} = 881 \text{ mV}_{\text{AC}}$
F06-57	$V_{C1} = 7.097 \text{ V}_{\text{DC}}$ $V_{B1} = 2.859 \text{ V}_{\text{DC}}$ $V_{b1} = 0.051 \text{ V}_{\text{AC}}$ $V_{E1} = 2.106 \text{ V}_{\text{DC}}$ $V_{C2} = 6.204 \text{ V}_{\text{DC}}$ $V_{B2} = 1.657 \text{ V}_{\text{DC}}$ $V_{\text{OUT2}} = -1.862 \text{ V}_{\text{DC}}$ $V_{\text{out2}} = 5.949 \text{ V}_{\text{AC}}$
F06-62	$V_{\text{in}} = 0.100 \text{ V}$ $V_{\text{out}} = 3.28 \text{ V}$

Summary of MultiSIM Files

Circuit	MultiSIM
TSE06-01	$V_B(1) = 1.680 \text{ V}_{\text{DC}}$ $V_C(1) = 5.772 \text{ V}_{\text{DC}}$ $V_E(1) = 908 \text{ mV}_{\text{DC}}$ $V_b(1) = 0.100 \text{ V}_{\text{AC}}$ $V_c(1) = 5.117 \text{ mV}_{\text{AC}}$ $V_e(1) = 0.473 \mu\text{V}_{\text{AC}}$ $V_B(2) = 1.680 \text{ V}_{\text{DC}}$ $V_C(2) = 5.732 \text{ V}_{\text{DC}}$ $V_E(2) = 908 \text{ mV}_{\text{DC}}$ $V_b(2) = 5.132 \text{ V}_{\text{AC}}$ $V_c(2) = 832 \text{ mV}_{\text{AC}}$ $V_e(2) = 908 \text{ mV}_{\text{AC}}$ $V_{\text{OUT}} = -0.040 \text{ V}_{\text{DC}}$ $V_{\text{out}} = 832 \text{ mV}_{\text{AC}}$
TSE06-02	$V_B(1) = 1.680 \text{ V}_{\text{DC}}$ $V_C(1) = 5.772 \text{ V}_{\text{DC}}$ $V_E(1) = 908 \text{ mV}_{\text{DC}}$ $V_b(1) = 0.100 \text{ V}_{\text{AC}}$ $V_c(1) = 0.016 \text{ V}_{\text{AC}}$ $V_e(1) = 0.469 \mu\text{V}_{\text{AC}}$ $V_B(2) = 1.680 \text{ V}_{\text{DC}}$ $V_C(2) = 5.772 \text{ V}_{\text{DC}}$ $V_E(2) = 908 \text{ mV}_{\text{DC}}$ $V_b(2) = 0.010 \text{ pV}_{\text{AC}}$ $V_c(2) = 0.047 \text{ pV}_{\text{AC}}$ $V_e(2) = 0.000 \text{ V}_{\text{AC}}$ $V_{\text{OUT}} = 1.721 \text{ pV}_{\text{DC}}$ $V_{\text{out}} = 2.658 \text{ pV}_{\text{AC}}$
TSE06-03	$V_B(1) = 1.680 \text{ V}_{\text{DC}}$ $V_C(1) = 5.772 \text{ V}_{\text{DC}}$ $V_E(1) = 908 \text{ mV}_{\text{DC}}$ $V_b(1) = 0.100 \text{ V}_{\text{AC}}$ $V_c(1) = 5.117 \text{ mV}_{\text{AC}}$ $V_e(1) = 0.473 \mu\text{V}_{\text{AC}}$ $V_B(2) = 1.680 \text{ V}_{\text{DC}}$ $V_C(2) = 5.772 \text{ V}_{\text{DC}}$ $V_E(2) = 908 \text{ mV}_{\text{DC}}$ $V_b(2) = 0.010 \text{ V}_{\text{AC}}$ $V_c(2) = 0.046 \text{ mV}_{\text{AC}}$ $V_e(2) = 9.838 \text{ mV}_{\text{AC}}$ $V_{\text{OUT}} = -0.097 \text{ mV}_{\text{DC}}$ $V_{\text{out}} = 0.046 \text{ V}_{\text{AC}}$

Summary of MultiSIM Files

Circuit	MultiSIM
TSE06-04	$V_B(1) = 1.680 \text{ V}_{\text{DC}}$ $V_C(1) = 5.772 \text{ V}_{\text{DC}}$ $V_E(1) = 908 \text{ mV}_{\text{DC}}$ $V_b(1) = 0.100 \text{ V}_{\text{AC}}$ $V_c(1) = 0.010 \text{ V}_{\text{AC}}$ $V_e(1) = 0.473 \mu\text{V}_{\text{AC}}$ $V_B(2) = 1.754 \text{ V}_{\text{DC}}$ $V_C(2) = 9.999 \text{ V}_{\text{DC}}$ $V_E(2) = 0.000 \text{ V}_{\text{DC}}$ $V_b(2) = 0.010 \text{ V}_{\text{AC}}$ $V_c(2) = 0.041 \text{ pV}_{\text{AC}}$ $V_e(2) = 0.000 \text{ V}_{\text{AC}}$ $V_{\text{OUT}} = 0.012 \text{ nV}_{\text{DC}}$ $V_{\text{out}} = 0.016 \text{ nV}_{\text{AC}}$
TSP06-60	$V_b = 0.100 \text{ V}_{\text{AC}}$ $V_c = 0.215 \text{ V}_{\text{AC}}$ $V_{\text{out}} = 0.000 \text{ V}_{\text{AC}}$
TSP06-61	$V_b = 0.099 \text{ V}_{\text{AC}}$ $I_E = 0.000 \text{ A}_{\text{DC}}$
TSP06-62	$V_b = 0.100 \text{ V}_{\text{AC}}$ $V_{\text{out}} = 0.926 \text{ V}_{\text{AC}}$
TSP06-63	$V_{\text{in}} = 0.100 \text{ V}_{\text{AC}}$ $V_b = 0.090 \text{ pV}$ $V_{\text{out}} = 0.000 \text{ V}$
TSP06-64	$V_b = 0.100 \text{ V}_{\text{AC}}$ $V_c = 0.114 \text{ V}_{\text{AC}}$
TSP06-65	$V_c(1) = 2.764 \text{ V}_{\text{AC}}$ $V_b(2) = 0.013 \text{ pV}_{\text{AC}}$

Chapter 7:

Circuit	MultiSIM
E07-03 Lower than 40 V_{PP}	$V_{\text{out}} = 37.9 \text{ V}_{\text{PP}}$
E07-04 Lower than 20 V_{PP}	$V_{\text{out}} = 13.733 \text{ V}_{\text{PP}}$
F07-42	$V_{\text{CE}} = 6.296 \text{ V}_{\text{DC}}$ $I_C = 0.060 \text{ A}$
F07-44	$V_{\text{out}} = 6.295 \text{ V}_{\text{PP}}$ for $V_{\text{in}} = 100 \text{ mV}_{\text{rms}}$
F07-45	$V_{\text{out}} = 13.641 \text{ V}_{\text{PP}}$
F07-46	$V_{\text{out}} = 13.759 \text{ V}_{\text{PP}}$
TSE07-01	$V_B = 2.596 \text{ V}_{\text{PP}}$ with output clipped on bottom
TSE07-02	$V_B = 0.839 \text{ V}_{\text{DC}}$ $V_{\text{out(max)}} = 2.173 \text{ V}_P$ $V_{\text{out(min)}} = -1.816 \text{ V}_P$
TSE07-03	$V_{\text{out}} = 2.043 \text{ V}_{\text{PP}}$ with nonlinear distortion

Summary of MultiSIM Files

Circuit	MultiSIM
TSP07-39	$I_C = 0.060 \text{ A}_{\text{DC}}$ $V_{CE} = 6.281 \text{ V}_{\text{DC}}$ $V_B = 0.021 \text{ pV}_{\text{rms}}$
TSP07-40	$V_B = 4.204 \text{ V}_{\text{DC}}$ $V_{RE2} = 3.715 \text{ V}_{\text{DC}}$ V_{out} is negative pulses
TSP07-41	$V_{out} = -6.820 \text{ V}_{\text{PP}}$ half-wave output
TSP07-42	$V_{D2} = 6.885 \text{ pV}_{\text{DC}}$ $V_{out} = 13.060 \text{ V}_{\text{PP}}$
TSP07-43	V_{OUT} is a 12.039 V_P positive half-wave output

Chapter 8:

Circuit	MultiSIM
E08-06	$I_D = 8.078 \text{ mA}_{\text{DC}}$ $V_D = 5.053 \text{ V}_{\text{DC}}$ $V_{GS} = -3.116 \text{ V}_{\text{DC}}$ $V_S = 3.147 \text{ V}_{\text{DC}}$
E08-09	$I_D = 4.827 \text{ mA}_{\text{DC}}$ $V_D = 7.706 \text{ V}_{\text{DC}}$ $V_{GS} = -2.700 \text{ V}_{\text{DC}}$
E08-12	$I_D = 1.281 \text{ mA}_{\text{DC}}$ $V_D = 7.129 \text{ V}_{\text{DC}}$ $V_{GS} = -2.020 \text{ V}_{\text{DC}}$
F08-66a	$V_{GS} = -0.997 \text{ V}_{\text{DC}}$ $V_{DS} = 6.262 \text{ V}_{\text{DC}}$ $I_D = 1.007 \text{ mA}_{\text{DC}}$
F08-66b	$V_{GS} = -0.497 \text{ V}_{\text{DC}}$ $V_{DS} = 6.139 \text{ V}_{\text{DC}}$ $I_D = 5.020 \text{ mA}_{\text{DC}}$
F08-66c	$V_{GS} = -1.408 \text{ V}_{\text{DC}}$ $V_{DS} = 6.922 \text{ V}_{\text{DC}}$ $I_D = 3.025 \text{ mA}_{\text{DC}}$
F08-69	$I_D = 2.854 \text{ mA}_{\text{DC}}$ $V_{GS} = -0.856 \text{ V}_{\text{DC}}$
F08-70	$I_D = 3.356 \text{ mA}_{\text{DC}}$ $V_{GS} = 1.190 \text{ V}_{\text{DC}}$
F08-71	$I_D = 0.857 \text{ mA}_{\text{DC}}$ $V_{GS} = -1.186 \text{ V}_{\text{DC}}$
F08-72	$I_D = 1.917 \text{ mA}_{\text{DC}}$ $V_{GS} = -1.508 \text{ V}_{\text{DC}}$
F08-75a	$I_S = 8.000 \text{ mA}_{\text{DC}}$ $V_{DS} = 4.000 \text{ V}_{\text{DC}}$
F08-75b	$I_S = 8.000 \text{ mA}_{\text{DC}}$ $V_{DS} = 5.400 \text{ V}_{\text{DC}}$
F08-75c	$I_S = -8.000 \text{ mA}_{\text{DC}}$ $V_{DS} = -4.520 \text{ V}_{\text{DC}}$

Summary of MultiSIM Files

Circuit	MultiSIM
F08-76a	$I_D = 0.904 \text{ mA}_{\text{DC}}$ $V_{GS} = 3.098 \text{ V}_{\text{DC}}$
F08-76b	$I_D = 5.316 \text{ mA}_{\text{DC}}$ $V_{GS} = 4.762 \text{ V}_{\text{DC}}$
F08-81	$V_{DS} = 10.940 \text{ V}_{\text{DC}}$ $V_{GS} = -0.381 \text{ V}_{\text{DC}}$
TSE08-01	$V_{GS} = -0.080 \text{ V}_{\text{DC}}$ $V_D = 14.631 \text{ V}_{\text{DC}}$ $V_S = 0.081 \text{ V}_{\text{DC}}$ $I_D = 0.368 \text{ mA}_{\text{DC}}$
TSE08-02	$V_{GS} = 0.000 \text{ V}_{\text{DC}}$ $V_D = 0.000 \text{ V}_{\text{DC}}$ $V_S = 0.000 \text{ V}_{\text{DC}}$ $I_D = 0.000 \text{ A}_{\text{DC}}$
TSE08-03	$V_{GS} = -1.994 \text{ V}_{\text{DC}}$ $V_D = 14.999 \text{ V}_{\text{DC}}$ $V_S = 2.014 \text{ V}_{\text{DC}}$ $I_D = -1.776 \mu\text{A}_{\text{DC}}$
TSP08-72	$V_D = 0.031 \text{ V}_{\text{DC}}$ $V_S = 2.547 \text{ pV}_{\text{DC}}$ $V_G = 0.345 \mu\text{V}_{\text{DC}}$
TSP08-73	$V_D = 6.000 \text{ V}_{\text{DC}}$ $V_S = 0.906 \text{ V}_{\text{DC}}$ $V_G = 0.063 \text{ mV}_{\text{DC}}$
TSP08-74	$V_D = -2.988 \text{ V}_{\text{DC}}$ $V_S = -1.303 \text{ V}_{\text{DC}}$ $V_G = 0.000 \text{ V}_{\text{DC}}$
TSP08-75	$V_D = 7.166 \text{ V}_{\text{DC}}$ $V_S = 1.287 \text{ V}_{\text{DC}}$ $V_G = 0.018 \text{ mV}_{\text{DC}}$
TSP08-76	$V_D = 12.000 \text{ V}_{\text{DC}}$ $V_S = 0.000 \text{ V}_{\text{DC}}$ $V_G = 4.737 \text{ V}_{\text{DC}}$
TSP08-77	$V_D = 0.000 \text{ V}_{\text{DC}}$ $V_G = 0.000 \text{ V}_{\text{DC}}$
TSP08-78	$V_D = 10.000 \text{ V}_{\text{DC}}$ $V_G = 1.000 \text{ V}_{\text{DC}}$
TSP08-79	$V_D = 4.307 \text{ V}_{\text{DC}}$ $V_S = 4.307 \text{ V}_{\text{DC}}$ $V_G = 0.000 \text{ V}_{\text{DC}}$
TSP08-80	$V_D = 8.352 \text{ V}_{\text{DC}}$ $V_S = 8.311 \text{ V}_{\text{DC}}$ $V_G = 9.000 \text{ V}_{\text{DC}}$

Summary of MultiSIM Files

Chapter 9:

Circuit	MultiSIM
E09-08	$I_S = 2.633 \text{ mA}_{\text{DC}}$ $V_D = 6.318 \text{ V}_{\text{DC}}$ $V_{RL} = 1.712 \text{ V}_{\text{rms}}$
E09-09	$V_{GS} = -0.623 \text{ V}_{\text{DC}}$ $V_{in} = 9.998 \text{ mV}_{\text{rms}}$ $V_{out} = 9.142 \text{ mV}_{\text{rms}}$
E09-10	$V_{in} = 9.998 \text{ mV}_{\text{rms}}$ $V_{out} = 0.096 \text{ V}_{\text{rms}}$
F09-56	$I_D = 2.834 \text{ mA}_{\text{DC}}$ $V_{DS} = 4.914 \text{ V}_{\text{DC}}$ $V_S = 2.834 \text{ V}_{\text{DC}}$
F09-57a	$I_D = 1.843 \text{ mA}_{\text{DC}}$ $V_{in} = 0.050 \text{ V}_{\text{rms}}$ $V_{out} = 0.215 \text{ V}_{\text{rms}}$
F09-57b	$I_D = 1.016 \text{ mA}_{\text{DC}}$ $V_{in} = 0.050 \text{ V}_{\text{rms}}$ $V_{out} = 0.496 \text{ V}_{\text{rms}}$
F09-58	$I_D = 5.847 \text{ mA}_{\text{DC}}$ $V_{in} = 0.050 \text{ V}_{\text{rms}}$ $V_{out} = 0.141 \text{ V}_{\text{rms}}$
F09-59	$I_D = 4.463 \text{ mA}_{\text{DC}}$ $V_{DS} = 3.065 \text{ V}_{\text{DC}}$ $V_G = -1.458 \text{ V}_{\text{DC}}$
F09-60	$V_D = 17.151 \text{ V}_{\text{DC}}$ $V_G = 5.484 \text{ V}_{\text{DC}}$ $I_S = 2.849 \text{ mA}_{\text{DC}}$
F09-62	$I_S = 0.015 \text{ mA}_{\text{DC}}$ $V_D = 9.000 \text{ V}_{\text{DC}}$ $V_d = 0.048 \text{ V}_{\text{rms}}$ $V_{in} = 9.996 \text{ mV}_{\text{rms}}$
F09-65a	$I_D = 0.279 \text{ mA}_{\text{DC}}$ $V_{in} = 0.050 \text{ V}_{\text{rms}}$ $V_{out} = 0.046 \text{ V}_{\text{rms}}$
F09-65b	$I_D = 6.615 \text{ mA}_{\text{DC}}$ $V_{in} = 0.050 \text{ V}_{\text{rms}}$ $V_{out} = 0.014 \text{ V}_{\text{rms}}$
TSE09-01	$V_{in} = 9.998 \text{ mV}_{\text{rms}}$ $I_D(1) = 3.125 \text{ mA}_{\text{DC}}$ $V_D(1) = 7.313 \text{ V}_{\text{DC}}$ $V_G(2) = -0.135 \text{ mV}_{\text{DC}}$ $V_g(2) = 0.075 \text{ V}_{\text{rms}}$ $I_D(2) = 3.135 \text{ mA}_{\text{DC}}$ $V_{out}(2) = 0.562 \text{ V}_{\text{rms}}$

Summary of MultiSIM Files

Circuit	MultiSIM
TSE09-02	$V_{in} = 9.998 \text{ mV}_{\text{rms}}$ $I_D(1) = 6.092 \text{ mA}_{\text{DC}}$ $V_D(1) = 2.863 \text{ V}_{\text{DC}}$ $V_G(2) = 2.863 \text{ mV}_{\text{DC}}$ $V_g(2) = 0.433 \text{ V}_{\text{rms}}$ $I_D(2) = 6.115 \text{ mA}_{\text{DC}}$ $V_{out}(2) = 0.128 \text{ mV}_{\text{rms}}$
TSE09-03	$V_{in} = 9.997 \text{ mV}_{\text{rms}}$ $I_D(1) = 1.776 \mu\text{A}_{\text{DC}}$ $V_D(1) = 12.001 \text{ V}_{\text{DC}}$ $V_G(2) = 0.067 \text{ mV}_{\text{DC}}$ $V_g(2) = 0.000 \text{ V}_{\text{rms}}$ $I_D(2) = 3.125 \text{ mA}_{\text{DC}}$ $V_{out}(2) = 0.000 \text{ V}_{\text{rms}}$
TSE09-04	$V_{in} = 9.998 \text{ mV}_{\text{rms}}$ $I_D(1) = 3.125 \text{ mA}_{\text{DC}}$ $V_D(1) = 7.313 \text{ V}_{\text{DC}}$ $V_G(2) = -0.199 \text{ mV}_{\text{DC}}$ $V_g(2) = 0.075 \text{ V}_{\text{rms}}$ $I_D(2) = 0.000 \text{ A}_{\text{DC}}$ $V_{out}(2) = 0.026 \text{ nV}_{\text{rms}}$
TSP09-54	$I_D = 4.800 \text{ mA}_{\text{DC}}$ $V_{DS} = 4.801 \text{ pV}_{\text{DC}}$ $V_S = 4.800 \text{ V}_{\text{DC}}$
TSP09-55	$I_D = 1.842 \text{ mA}_{\text{DC}}$ $V_S = 0.034 \text{ V}_{\text{DC}}$ $V_{in} = 0.050 \text{ V}_{\text{rms}}$ $V_{out} = 0.069 \text{ V}_{\text{rms}}$
TSP09-56	$I_D = 1.000 \text{ A}_{\text{DC}}$ $V_G = 0.000 \text{ V}_{\text{DC}}$ $V_{in} = 0.050 \text{ V}_{\text{rms}}$ $V_{out} = 6.203 \text{ pV}_{\text{rms}}$
TSP09-57	$I_D = 0.013 \text{ A}_{\text{DC}}$ $V_{GS} = 0.080 \text{ mV}_{\text{DC}}$ $V_{in} = 0.050 \text{ V}_{\text{rms}}$ $V_{out} = 0.208 \text{ V}_{\text{rms}}$
TSP09-58	$I_D = 9.008 \text{ nA}_{\text{DC}}$ $V_{DS} = 9.000 \text{ V}_{\text{DC}}$ $V_{GS} = -2.941 \mu\text{V}_{\text{DC}}$
TSP09-59	$V_{R1} = 20.000 \text{ V}_{\text{DC}}$ $V_G = 0.136 \text{ mV}_{\text{DC}}$ $V_D = 20.000 \text{ V}_{\text{DC}}$ $I_D = 0.028 \text{ nA}_{\text{DC}}$
TSP09-60	$V_{RD} = 24.00 \text{ V}_{\text{DC}}$ $V_{in} = 0.010 \text{ V}_{\text{rms}}$ $I_C = 0.240 \mu\text{A}_{\text{DC}}$ $V_D = 0.050 \text{ mV}_{\text{DC}}$ $V_d = 0.080 \mu\text{V}_{\text{rms}}$ $V_{out} = 0.080 \mu\text{V}_{\text{rms}}$

Summary of MultiSIM Files

Circuit	MultiSIM
TSP09-61	$I_D = 9.876 \text{ mA}_{\text{DC}}$ $V_{DS} = 3.186 \text{ V}_{\text{DC}}$ $V_{GS} = 17.991 \text{ V}_{\text{DC}}$ $V_{\text{out}} = 0.024 \text{ V}_{\text{rms}}$
TSP09-62	$I_D = 0.279 \text{ mA}_{\text{DC}}$ $V_s = 0.047 \text{ V}_{\text{rms}}$ $V_{\text{in}} = 0.050 \text{ V}_{\text{rms}}$ $V_{\text{out}} = 0.000 \text{ V}_{\text{rms}}$

Chapter 10:

Circuit	MultiSIM
E10-03	$f_C \approx 209 \text{ Hz}$
E10-05	$f_C \approx 50 \text{ Hz}$
E10-06	$f_C \approx 30 \text{ Hz}$
E10-07	$f_C \approx 16 \text{ Hz}$
E10-08	$f_C \approx 17 \text{ Hz}$
E10-11	$f_C \approx 1.78 \text{ MHz}$
F10-56	$f_C(1) \approx 3.1 \text{ kHz}$ $f_C(2) \approx 25.0 \text{ kHz}$
F10-57	$f_C \approx 93 \text{ kHz}$
F10-60	$f_C \approx 2.95 \text{ kHz}$
TSP10-45	$V_{RC} = 19.765 \text{ V}_{\text{DC}}$
TSP10-46	$V_d = 202 \text{ mV}_{\text{PP}}$ $V_{\text{out}} = 0.0 \text{ V}_{\text{rms}}$
TSP10-47	$V_B = 2.589 \text{ V}_{\text{DC}}$
TSP10-48	$V_{RD} = 10.00 \text{ V}_{\text{DC}}$ $I_D = 0.018 \text{ A}_{\text{DC}}$

Chapter 11:

Circuit	MultiSIM
E11-03	$I_{\text{SCR}} = 0.436 \text{ A}$ Expected SCR operation
E11-04	Sine wave with missing piece from 90° to 180° with $R_{\text{POT}} = 82\%$
F11-53	Expected SCR operation
TSP11-27	Cathode-anode shorted
TSP11-28	SCR never fires
TSP11-29	$V_{R1} = 0.074 \text{ nV}$ V_{out} is half-wave output

Chapter 12:

Circuit	MultiSIM
E12-03	$V_{\text{in}} = 0.100 \text{ V}_{\text{rms}}$ $V_{\text{out}} = 2.227 \text{ V}_{\text{rms}}$

Summary of MultiSIM Files

Circuit	MultiSIM
E12-04	$V_{in} = 0.100 \text{ V}_{\text{rms}}$ $V_{out} = 9.997 \text{ V}_{\text{rms}}$
E12-05	$V_{in} = 0.100 \text{ V}_{\text{rms}}$ $V_{out} = 2.299 \text{ V}_{\text{rms}}$
E12-07	$V_{in} = 0.010 \text{ V}_{\text{rms}}$ $V_{out} = 9.997 \text{ V}_{\text{rms}}$
E12-12	$\text{BW}(1) \approx 48.9 \text{ kHz}$ $\text{BW}(2) \approx 70.0 \text{ kHz}$
F12-63	$V_{in} = 10.000 \text{ mV}_{\text{rms}}$ $V_{out} = 3.742 \text{ V}_{\text{rms}}$
F12-64a	$V_{in} = 10.000 \text{ mV}_{\text{rms}}$ $V_{out} = 0.110 \text{ V}_{\text{rms}}$
F12-64b	$V_{in} = 10.000 \text{ mV}_{\text{rms}}$ $V_{out} = 1.010 \text{ V}_{\text{rms}}$
F12-64c	$V_{in} = 10.000 \text{ mV}_{\text{rms}}$ $V_{out} = 0.478 \text{ V}_{\text{rms}}$
F12-64d	$V_{in} = 10.000 \text{ mV}_{\text{rms}}$ $V_{out} = 10.003 \text{ V}_{\text{rms}}$
F12-66a	$V_{in} = 1.000 \text{ V}_{\text{rms}}$ $V_{out} = 1.000 \text{ V}_{\text{rms}}$
F12-66b	$V_{in} = 1.000 \text{ V}_{\text{rms}}$ $V_{out} = 1.000 \text{ V}_{\text{rms}}$
F12-66c	$V_{in} = 1.000 \text{ V}_{\text{rms}}$ $V_{out} = 0.223 \text{ V}_{\text{rms}}$
F12-66d	$V_{in} = 10.000 \text{ mV}_{\text{rms}}$ $V_{out} = 9.998 \text{ V}_{\text{rms}}$
F12-67	$V_{in} = 10.000 \text{ mV}_{\text{rms}}$ $I_s = 0.030 \text{ mA}_{\text{rms}}$ $V_{out} = 10.004 \text{ V}_{\text{rms}}$ $I_f = 0.030 \text{ mA}_{\text{rms}}$
F12-68a	$V_{in} = 10.000 \text{ mV}_{\text{rms}}$ $I_s = 0.100 \text{ nA}_{\text{rms}}$ $V_{out} = 2.084 \text{ V}_{\text{rms}}$ $I_f = 3.726 \mu\text{A}_{\text{rms}}$
F12-68b	$V_{in} = 10.000 \text{ mV}_{\text{rms}}$ $I_s = 0.100 \text{ nA}_{\text{rms}}$ $V_{out} = 0.323 \text{ V}_{\text{rms}}$ $I_f = 6.685 \mu\text{A}_{\text{rms}}$
F12-68c	$V_{in} = 10.000 \text{ mV}_{\text{rms}}$ $I_s = 0.100 \text{ nA}_{\text{rms}}$ $V_{out} = 0.189 \text{ V}_{\text{rms}}$ $I_f = 0.181 \mu\text{A}_{\text{rms}}$
F12-70a	$V_{in} = 10.000 \text{ mV}_{\text{rms}}$ $I_s = 1.000 \mu\text{A}_{\text{rms}}$ $V_{out} = 0.150 \text{ V}_{\text{rms}}$ $I_f = 1.001 \mu\text{A}_{\text{rms}}$

Summary of MultiSIM Files

Circuit	MultiSIM
F12-70b	$V_{in} = 10.000 \text{ mV}_{rms}$ $I_s = 0.100 \mu\text{A}_{rms}$ $V_{out} = 1.000 \text{ V}_{rms}$ $I_f = 0.110 \mu\text{A}_{rms}$
F12-70c	$V_{in} = 10.000 \text{ mV}_{rms}$ $I_s = 0.021 \text{ mA}_{rms}$ $V_{out} = 0.213 \text{ V}_{rms}$ $I_f = 0.021 \text{ mA}_{rms}$
TSE12-01	$V_{in} = 0.100 \text{ V}_{rms}$ $V_{out} = 2.227 \text{ V}_{rms}$
TSE12-02	$V_{in} = 0.047 \mu\text{V}_{rms}$ $V_{out} \text{ is railed}$
TSE12-03	$V_{in} = 0.100 \text{ V}_{rms}$ $V_{out} = 9.997 \text{ V}_{rms}$
TSE12-04	$V_{in} = 0.100 \text{ V}_{rms}$ $V_{out} = 0.000 \text{ V}_{rms}$
TSP12-57	$V_{in} = 28.3 \text{ V}_{pp}$ $V_{out} \text{ is railed}$
TSP12-58	$V_{in} = 2.83 \text{ V}_{pp}$ $V_{out} = 2.83 \text{ V}_{pp}$
TSO12-59	$V_{in} = 28.3 \text{ mV}_{pp}$ $V_{out} = 28.5 \text{ mV}_{pp}$
TSP12-60	$V_{out} \text{ is railed}$ $V_{Ri} \approx 0 \text{ V}_{pp}$
TSP12-61	$V_{in} = 28.3 \text{ mV}_{pp}$ $V_{out} = 28.3 \text{ mV}_{pp}$
TSP12-62	$V_{in} = 2.83 \text{ V}_{pp}$ $V_{out} \approx 0 \text{ V}_{pp}$
TSP12-63	$V_{in} = 14.1 \text{ V}_{pp}$ $V_{out} = 14.1 \text{ mV}_{pp}$
TSP12-64	$V_{in} = 2.83 \text{ V}_{pp}$ $V_{out} = 28.0 \text{ V}_{pp}$
TSP12-65	$V_{in} = 2.83 \text{ mV}_{pp}$ $V_{out} \text{ is railed}$
TSP12-66	$V_{in} = 2.83 \text{ V}_{pp}$ $V_{out} \approx 0 \text{ V}_{pp}$
TSP12-67	$V_{in} = 2.83 \text{ V}_{pp}$ $V_{out} \text{ is railed}$
TSP12-68	$V_{in} = 2.83 \text{ V}_{pp}$ $V_{out} = 3.02 \text{ V}_{pp}$
TSP12-69	$V_{in} = 28.3 \text{ V}_{pp}$ $V_{out} \text{ is railed}$
TSP12-70	$V_{in} = 2.83 \text{ V}_{pp}$ $V_{out} \approx 0 \text{ V}_{pp}$
TSP12-71	$V_{in} = 2.83 \text{ V}_{pp}$ $V_{out} \approx 0 \text{ V}_{pp}$
TSP12-72	$V_{in} = 28.3 \text{ mV}_{pp}$ $V_{out} = 3.43 \text{ V}_{pp}$

Summary of MultiSIM Files

Chapter 13:

Circuit	MultiSIM
E13-01	$V_{LTP} = +1.627 \text{ V}$ $V_{UTP} = +1.627 \text{ V}$
E13-02	$V_{LTP} = -2.551 \text{ V}$ $V_{UTP} = +2.468 \text{ V}$
E13-03	$V_{UTP} = -2.391 \text{ V}$ $V_{LTP} = +2.391 \text{ V}$ $V_{out} = -7.722 \text{ V}, +7.684 \text{ V}$
E13-05	$V_{OUT} = -12 \text{ V}$
E13-06	$V_{OUT} = -7 \text{ V}$
E13-07	$V_{OUT} = -2.5 \text{ V}$
E13-08	$V_1 = 3.000 \text{ V}$ $V_2 = 2.000 \text{ V}$ $V_3 = 8.000 \text{ V}$ $V_{OUT} = -8.838 \text{ V}$
E13-10	Integrator output $\Delta V/\Delta t = -4.816 \text{ V}/200 \mu\text{s}$
F13-61	$V_{LTP} = -2.637 \text{ V}$ $V_{UTP} = +2.574 \text{ V}$
F13-63a	$V_{LTP} = -3.848 \text{ V}$ $V_{UTP} = +3.817 \text{ V}$
F13-63b	$V_{LTP} = -3.628 \text{ V}$ $V_{UTP} = +3.411 \text{ V}$
F13-64	$V_{UTP} = -1.206 \text{ V}$ $V_{LTP} = +1.206 \text{ V}$ $V_{out} = -6.144 \text{ V}, +6.142 \text{ V}$
F13-65a	$V_{OUT} = -2.500 \text{ V}$
F13-65b	$V_{OUT} = -3.520 \text{ V}$
F13-66	$V_{OUT} = -14.00 \text{ V}$
F13-67	$V_{OUT} = -3.572 \text{ V}$
F13-68	Integrator output $\Delta V/\Delta t = -4.058 \text{ V}/1.0 \text{ ms}$
F13-69	$V_{OUT} = 20 \text{ V}_{PP}$ square wave
TSE13-01	$V(-) = 2.000 \text{ V}$ V_{OUT} is railed
TSE13-02	$V_{IN} = 3 \text{ V}, 2 \text{ V}, 8 \text{ V}$ $V(-) = 6.682 \text{ V}$ $V_{OUT} = 6.682 \text{ V}$
TSE13-03	$V_{in} = 0 \text{ V}$ to 5 V square wave $V_{out} = 0 \text{ V}$
TSE13-04	$V_{in} = 10 \text{ V}_{PP}$ triangle wave $V_{out} = 0 \text{ V}$
TSE13-05	$V_{out(min)} = -898 \text{ mV}$ $V_{out(max)} = 6.908 \text{ V}$
TSE13-06	0 V output
TSE13-07	$V_{UTP} = -4.589 \text{ V}$ $V_{LTP} = +4.589 \text{ V}$ $V_{out} = -7.806 \text{ V}, +7.804 \text{ V}$

Summary of MultiSIM Files

Circuit	MultiSIM
TSE13-08	$V_{in} = 1 \text{ V}, 0.5 \text{ V}, 0.2 \text{ V}, 0.1 \text{ V}$ $V(-) = 0.450 \text{ V}$ V_{out} is railed negative
TSE13-09	$V_{in} = 1 \text{ V}, 0.5 \text{ V}, 0.2 \text{ V}, 0.1 \text{ V}$ $V(-) = 0.500 \text{ V}$ V_{out} is railed negative
TSP13-30	$V_{LTP} = -5.137 \text{ V}$ $V_{UTP} = +10.649 \text{ V}$ V_{out} is railed
TSP13-31	$V_{LTP} = -6.135 \text{ V}$ $V_{UTP} = -9.472 \text{ V}$ $V_{out} = \pm 10 \text{ V}_p$ square wave
TSP13-32	$V_{in} = 2.0 \text{ V}_p$ $V_{out} = 2.0 \text{ V}_p$
TSP13-33	$V_{out}(\min) = -711.0 \text{ mV}$ $V_{out}(\max) = +5.700 \text{ V}$
TSP13-34	$V_{OUT} = -1.500 \text{ V}$
TSP13-35	$V(-) = 1.000 \text{ V}$ V_{out} is railed negative
TSP13-36	$V_{OUT} = -0.013 \text{ V}$
TSP13-37	$V(-) = 2.432 \text{ V}$ V_{out} is railed negative
TSP13-38	$V_{out} = 2.804 \text{ V}$
TSP13-39	$V_{out} = 8.928 \text{ mV}_{pp}$ square wave

Chapter 14:

Circuit	MultiSIM
E14-08	$V_{OUT} = -153.926 \text{ mV}$
F14-53	$V_{in}(1) = 1.005 \text{ V}_{rms}$ $V_{in}(2) = 1.005 \text{ V}_{rms}$ $V_{out} = 2.010 \text{ V}_{rms}$
F14-60	$V_{OUT} = -162.307 \text{ mV}$
F14-62a	$I_L = 4.659 \text{ mA}$
F14-62b	$I_L = 1.176 \text{ mA}$
TSP14-32	$V_{out} = 21.958 \text{ V}_{rms}$
TSP14-33	$I_Q = 0 \text{ A}$
TSP14-34	$I_Q = 27.756 \text{ nA}$
TSP14-35	$I_L = 6 \text{ mA}$
TSP14-36	$I_L = 594.058 \mu\text{A}$

Chapter 15:

Circuit	MultiSIM
E15-03	$f_C \approx 7.1 \text{ kHz}$
E15-06	$f_C(1) \approx 634 \text{ Hz}$ $f_C(2) \approx 854 \text{ Hz}$

Summary of MultiSIM Files

Circuit	MultiSIM
E15-07	$f_C(1) \approx 7.1 \text{ kHz}$ $f_C(2) \approx 7.3 \text{ kHz}$
E15-08	$f_C \approx 60.1 \text{ Hz}$
F15-43a	$f_C \approx 11.2 \text{ kHz}$
F15-43b	$f_C \approx 162 \text{ kHz}$
F15-43c	$f_C \approx 49 \text{ kHz}$
F15-45	$f_C(1) \approx 174 \text{ Hz}$ $f_C(2) \approx 200 \text{ Hz}$
F15-46	$f_C \approx 1.27 \text{ kHz}$
F15-47a	$f_1 \approx 116 \text{ Hz}$ $f_2 \approx 218 \text{ Hz}$ $f_C \approx 159 \text{ Hz}$
F15-47b	$f_1 \approx 402 \text{ Hz}$ $f_2 \approx 500 \text{ Hz}$ $f_C \approx 445 \text{ Hz}$
F15-47c	$f_1 \approx 15.7 \text{ kHz}$ $f_2 \approx 16.2 \text{ kHz}$ $f_{\text{PEAK}} \approx 15.8 \text{ kHz}$
F15-48	$f_1 \approx 1.3 \text{ kHz}$ $f_2 \approx 1.75 \text{ kHz}$ $f_{\text{NOTCH}} \approx 1.32 \text{ kHz}$
TSP15-23	$I_{R4} = 0.000 \text{ A}$ $V_{R4} = 0.432 \text{ V}$
TSP15-24	$I_{R3} = 0 \text{ A}$
TSP15-25	$V+(2) = 1.321 \text{ pV}_{\text{rms}}$
TSP15-26	$f_C \approx 270 \text{ Hz}$
TSP15-27	$f_C \approx 2.5 \text{ kHz}$
TSP15-28	$V+(1) = 2.950 \text{ pV}$ $I_{R2} = 1.475 \text{ mA}$
TSP15-29	$V_S = 0.100 \text{ V}_{\text{rms}}$ $V \text{ on end of R1} = 0 \text{ V}$
TSP15-30	$V_{C2} = 0.100 \text{ V}_{\text{rms}}$ $I_{C2} = 0.017 \mu\text{A}_{\text{rms}}$
TSP15-31	$V_{\text{out}}(2) = 36.7 \text{ mV}_{\text{PP}}$ $V-(3) = 0 \text{ V}$

Chapter 16:

Circuit	MultiSIM
E16-01	$V_{\text{out}} = 2.2 \text{ V}_{\text{PP}} @ 1.6 \text{ kHz}$
E16-02	$V_{\text{out}} = 16.6 \text{ V}_{\text{PP}} @ 6.37 \text{ kHz}$
F16-58	$V_{\text{out}} = 2.2 \text{ V}_{\text{PP}} @ 9.81 \text{ kHz}$
F16-59	$V_{\text{out}} = 8.1 \text{ V}_{\text{PP}} @ 692 \text{ Hz}$
F16-60a	$V_{\text{out}} = 386 \text{ mV}_{\text{PP}} @ 264 \text{ kHz}$ (Tank circuit is loaded)
F16-60b	$V_{\text{out}} = 4.02 \text{ V}_{\text{PP}} @ 58.9 \text{ kHz}$
F16-62	$V_{\text{out}} = 11.7 \text{ V}_{\text{PP}} @ 1.56 \text{ kHz}$

Summary of MultiSIM Files

Circuit	MultiSIM
F16-64	$t_H = 139 \mu s$ $t_L = 109 \mu s$ $f_{osc} = 4.02 \text{ kHz}$
TSP16-23	$R_{DS} = 0 \Omega$
TSP16-24	V_{C3} open from oscilloscope trace
TSP16-25	$V_{CE} \approx 2.557 \text{ pV}$
TSP16-26	$V_{R1} = 661.758 \text{ mV}$
TSP16-27	Resistance of R2 out of range
TSP16-28	$t_H = 110.5 \mu s$ $t_L = 110.5 \mu s$

Chapter 17:

Circuit	MultiSIM
E17-03	$V_{OUT} = 10.340 \text{ V}_{DC}$
E17-05	$V_{OUT} = 10.340 \text{ V}_{DC}$
F17-45	$V_{OUT} = 10.625 \text{ V}_{DC}$
F17-46	$V_{OUT} = 8.752 \text{ V}_{DC}$
F17-47	$V_{R4} = 0.529 \text{ V}_{DC}$ $I_{R4} = 0.189 \text{ A}_{DC}$ $I_{Q2} = 0.191 \text{ mA}_{DC}$ $I_L = 0.188 \text{ A}_{DC}$ $V_{OUT} = 9.419 \text{ V}_{DC}$
F17-48	$I_L = 0.037 \text{ A}$
TSP17-31	$V_{R3} = 2.496 \text{ V}_{DC}$ $V_{OUT} = 2.471 \text{ V}_{DC}$
TSP17-32	$V_Z = 11.881 \text{ V}_{DC}$ $V_{OUT} = 11.999 \text{ V}_{DC}$
TSP17-33	$V_{R4} = 0.353 \text{ V}_{DC}$ $I_{R4} = 0.126 \text{ A}_{DC}$ $I_{Q2} < 2 \mu A_{DC}$ $I_L = 0.126 \text{ A}_{DC}$ $V_{OUT} = 9.419 \text{ V}_{DC}$
TSP17-34	$V_{R1} = 24.99 \text{ V}_{DC}$ $I_L = 0.019 \text{ mA}_{DC}$

Solutions Manual Laboratory Exercises for Electronic Devices

Eighth Edition

**David M. Buchla
Steven Wetterling**

Instructor note: The B experiments include useful notes regarding the Anadigm Signal Processor (ASP) and the Programmable Analog Module (PAM). These are presented on an “as needed” basis with the heading *Instructor note*::.

Experiment 1: The Diode Characteristic

Part 1: The Diode Characteristic Curve

Step 1: Answers depend on the meter. A meter with a diode test will typically show about 0.6 V in one direction and an open in the other direction.

Table 1-1

Component	Listed Value	Measured Value
R_1	330 Ω	331 Ω
R_2	1.0 M Ω	1.05 MΩ

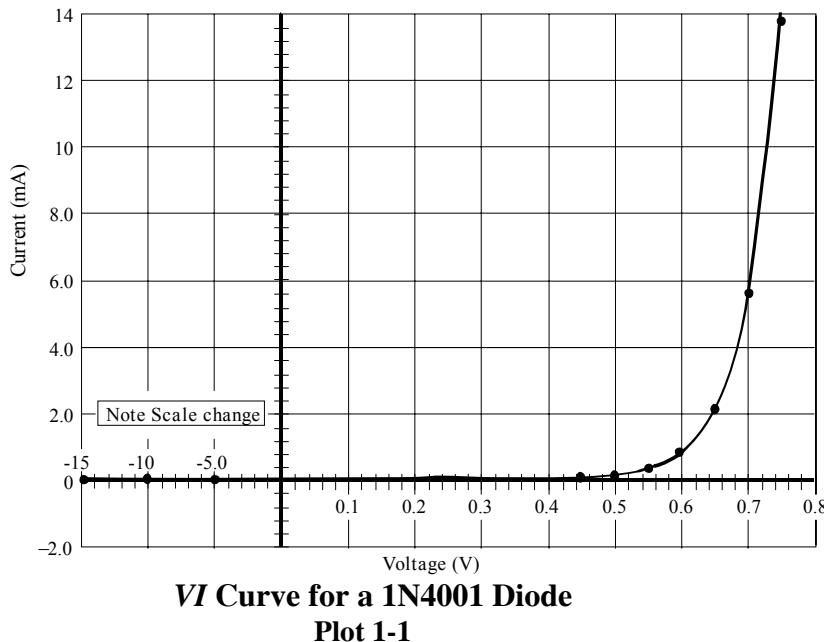
Table 1-2

V_F	V_{R1} (measured)	I_F (computed)
0.45 V	3.8 mV	11 μA
0.50 V	16.3 mV	49 μA
0.55 V	83 mV	250 μA
0.60 V	230 mV	695 μA
0.65 V	690 mV	2.08 mA
0.70 V	1.85 V	5.59 mA
0.75 V	4.58 V	13.8 mA

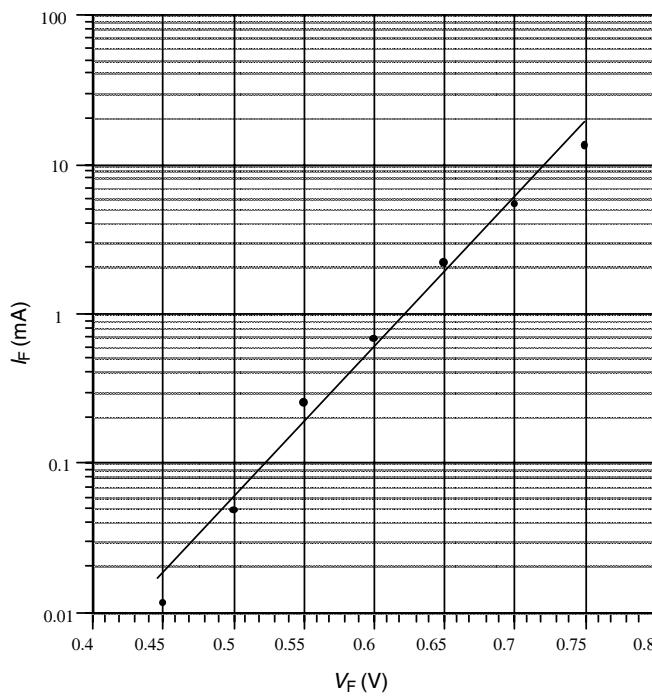
Table 1-3

V_S (measured)	V_{R2} (measured)	I_R (computed)
5.0 V	454 mV	0.43 μA
10.0 V	890 mV	0.85 μA
15.0 V	1.3 V	1.24 μA

Step 8: Plot of the diode curve:



Step 9: The semilog plot shows that logarithm of forward current is proportional to the diode drop.



Questions: Part 1

1. The input impedance is equal to the series $1 \text{ M}\Omega$ resistor, which can be seen from the voltage: divider rule.
2. The larger resistor is needed to develop enough voltage to be easily measured.

Part 2: Plotting Diode Curves with an Oscilloscope

Step 3: The barrier potential is reduced by the addition of heat, causing current to increase for a given voltage.

Step 4: The threshold is about 1.5 V for a red LED.

Step 5: The threshold is about 1.8 V for a green LED.

Step 6: The zener forward voltage is about 0.7 V; the breakdown is at 5.0 V.

Questions: Part 2

1. The dynamic resistance is measured by observing a small voltage change in the characteristic curve at the point it is being measured and dividing by a corresponding current change.
2. The setup can be used to measure any two-terminal device because it enables a plot of current versus voltage.

Experiment 2 Diode Applications

Part 1: Diode Rectifiers

Step 1: Waveforms:

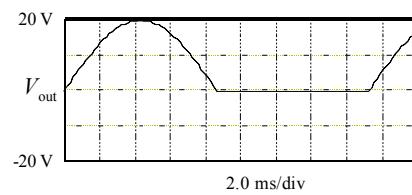
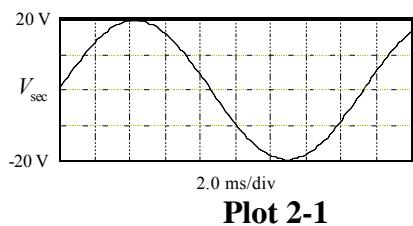


Table 2-1 Half-wave rectifier.

Without Filter Capacitor				With Filter Capacitor		
Computed	Measured	Compute	Measured	Measured		
$V_{sec(rms)}$	$V_{sec(rms)}$	$V_{out(p)}$	$V_{out(p)}$	$V_{OUT(DC)}$	$V_{r(pp)}$	Ripple Frequency
12.6 V ac	14.4 V rms	20.3 V_p	20.0 V_p	19.1 V dc	1.4 V_{pp}	60 Hz

Step 4: Waveforms:

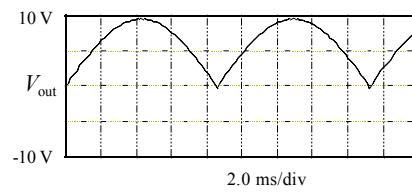
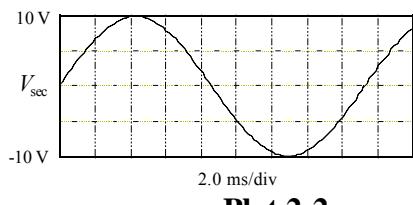


Table 2-2 Full-wave rectifier circuit.

Without Filter Capacitor				With Filter Capacitor		
Computed	Measured	Computed	Measured	Measured		
V _{sec(rms)}	V _{sec(rms)}	V _{out(p)}	V _{out(p)})	V _{OUT(DC)}	V _{r(pp)}	Ripple Frequency
6.3 V ac	7.3 Vrms	10.2 V_p	9.8 V_p	9.5 V dc	0.35 V_{pp}	120 Hz

Step 7: A second parallel load resistor increases the load current and the ripple voltage.

Table 2-3 Bridge rectifier circuit.

Without Filter Capacitor				With Filter Capacitor		
Computed	Measured	Computed	Measured	Measured		
V _{sec(rms)}	V _{sec(rms)}	V _{out(p)}	V _{out(p)})	V _{OUT(DC)}	V _{r(pp)}	Ripple Frequency
12.6 V ac	14.5 Vrms	20.5 V_p	19.5 V_p	19.0 V dc	0.65 V_{pp}	120 Hz

Step 10: The output voltage drops; ripple voltage is doubled; ripple frequency is 60 Hz.

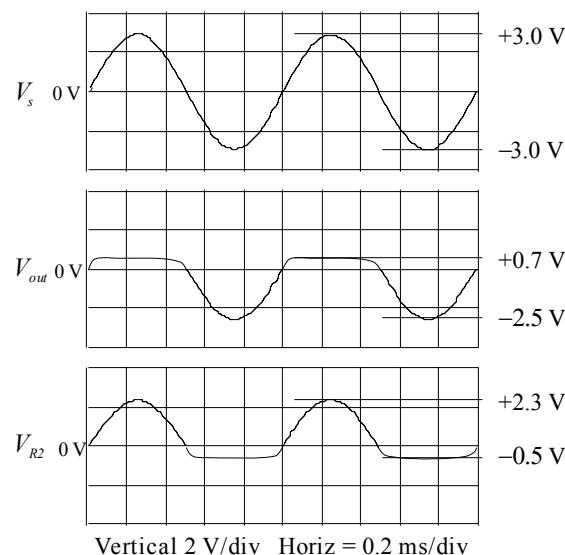
Questions: Part 1

1. The scope ground connection, if common with the circuit, will short the secondary if it is connected to one side, so two channels are necessary.
2. An open diode will cause the ripple frequency to drop to 60 Hz (instead of 120 Hz).

Part 2: Diode Clipping Circuits

Step 1: R_2 and R_L form a voltage divider; the voltage across R_L is only slightly less than V_S .

Step 2: Waveforms:

**Plot 2-3**

Step 3: The load has a waveform with a minimum of -2.72 V and a maximum of 0.68 V similar to the second waveform in Plot 2-3. The change in the lower part of the waveform is due to loading effects.

Step 4: The positive clipping level follows changes in the power supply voltage. As the supply is increased, the positive clipping level moves up from about 0.7 V to the peak of the input waveform.

Step 5: The negative portion of the waveform is clipped. The power supply controls the level, which varies from -0.7 V to the positive peak.

Step 6: Reversing the power supply voltage moves the clipping level to negative voltages.

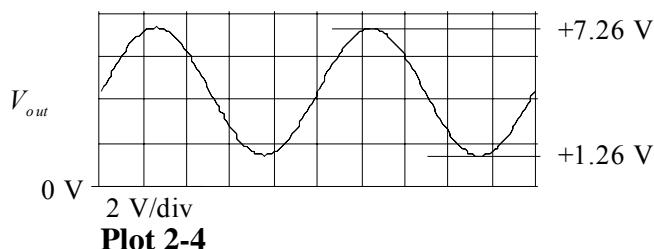
Questions: Part 2

1. The clipping level stays the same when the load is reduced but the lower level of the waveform changes due to loading effects.
2. At all times, the algebraic sum of the voltages around a closed path is zero. The voltage across R_2 can be found directly by subtracting the load voltage from the source voltage.

Part 3: Diode Clamping Circuits

Step 1: The output is an ac waveform that varies from approximately -0.6 V to +5.4 V. The output tracks changes in the input amplitude but the lower peak remains at -0.6 V (after a short delay for settling to the new level).

Step 2: The power supply voltage adds to the output. See Plot 2-4 for output waveform.



Step 3: The circuit is now a negative clamping circuit. The peak is at approximately 0.6 V when the dc supply is zero and the clamping point moves more negative as the dc voltage increases.

Questions: Part 3

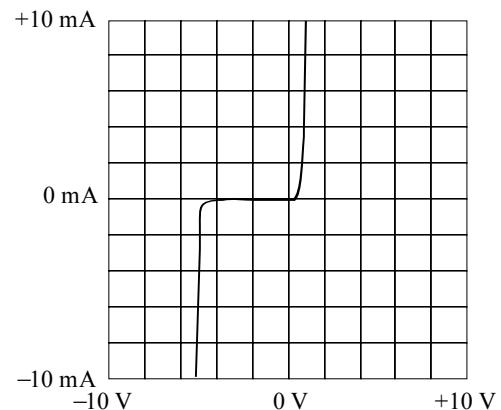
1. The capacitor is polarized, so how it charges needs to be considered in placing it in the circuit.
2. The output will “settle” faster due to the decreased time constant. There is also a small additional distortion on the bottom of the waveform when the diode conducts.

Experiment 3 Special-Purpose Diodes

Part 1: The Zener Diode and Regulator

Table 3-1

Resistor	Listed Value	Measured Value
R_1	220 Ω	219 Ω
R_2	1.0 k Ω	1.00 kΩ
R_L	2.2 k Ω	2.22 kΩ



Plot 3-1

Table 3-2

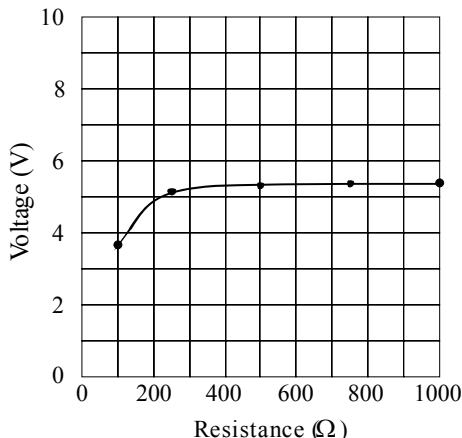
V_s	V_{out} (measured)	I_L (computed)	V_{R1} (computed)	I_s (computed)	I_Z (computed)
2.0 V	1.82 V	0.82 mA	0.18 V	0.82 mA	0.0 mA
4.0 V	3.60 V	1.62 mA	0.40 V	1.81 mA	0.19 mA
6.0 V	4.70 V	2.12 mA	1.30 V	5.90 mA	3.78 mA
8.0 V	5.07 V	2.28 mA	2.93 V	13.3 mA	11.0 mA
10.0 V	5.24 V	2.26 mA	4.76 V	21.6 mA	19.3 mA

Step 4: As shown in Table 3-2, zener current increases for increasing source voltage.

Table 3-3

R_L	V_{out} (measured)	I_L (computed)	V_{R1} (computed)	I_s (computed)	I_Z (computed)
1.0 k Ω	5.32 V	5.32 mA	6.68 V	30.4 mA	28.0 mA
750 Ω	5.31 V	7.08 mA	6.69 V	30.4 mA	28.0 mA
500 Ω	5.26 V	10.5 mA	6.72 V	30.5 mA	28.1 mA
250 Ω	5.08 V	20.3 mA	6.92 V	31.5 mA	29.2 mA
100 Ω	3.75 V	37.5 mA	8.25 V	37.5 mA	0.0 mA*

* out of regulation with this load.



Plot 3-2

Step 9: From the data taken, the zener was able to regulate as long as the load was at least $250\ \Omega$.

Step 11: The regulated output had approximately 1 mV of ripple. The ripple waveform showed only the tip of the positive waveform. Noise level was less than 1 mV. Although this circuit had the advantage of a larger filter capacitor, the ripple is hundreds of times smaller than the unregulated supply in step 9 of Experiment 2 (see Table 2-3 for a comparison.)

Questions: Part 1

1. (a) The region between zener breakdown and 0.7 V is approximated by an open circuit.
 (b) Both the forward-bias region and the reverse-bias region are approximated by a short.
2. Percent line regulation = $\frac{\Delta V_{\text{out}}}{\Delta V_{\text{in}}} \times 100\% = \frac{5.24\ \text{V} - 5.07\ \text{V}}{10\ \text{V} - 8.0\ \text{V}} \times 100\% = 8.5\%$
3. For the worst case ($1\ \text{k}\Omega$ and $100\ \Omega$ loads) the percentage load regulation was poor since the zener carried no current for the $100\ \Omega$ load.

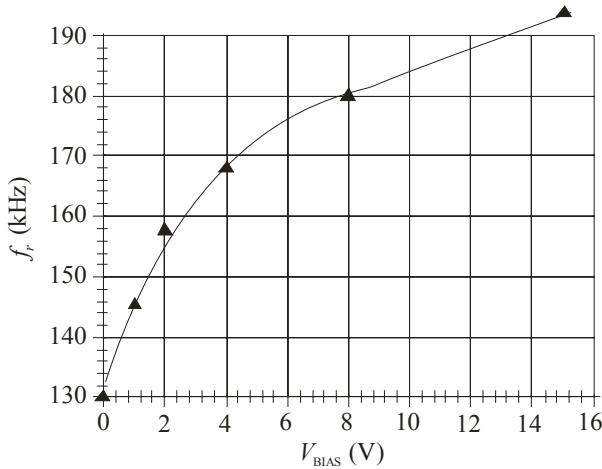
$$\text{Percent load regulation} = \frac{V_{\text{NL}} - V_{\text{FL}}}{V_{\text{FL}}} = \frac{5.32\ \text{V} - 3.75\ \text{V}}{3.75\ \text{V}} \times 100\% = 42\%$$

Part 2: The Varactor Diode

Step 1. *Note:* Measured resonant frequencies are shown in Table 3-4. Three varactor diodes were tested, all from the same manufacturer, with consistently lower than calculated resonant frequencies. The lower measured frequencies may be due to stray capacitance acting to reduce the measured frequency. With no stray capacitance, the calculated f_r should be approximately 226 kHz with $-4\ \text{V}$ of bias.

Table 3-4

V_{BIAS}	Resonant Frequency, f_r
0.0 V	130 kHz
1.0 V	146 kHz
2.0 V	158 kHz
4.0 V	168 kHz
8.0 V	180 kHz
15.0 V	195 kHz

**Table 3-5**

Parameter	Measured Value
Resonant frequency, f_r	194.7 kHz
Upper critical frequency, f_{cu}	196.2 kHz
Lower critical frequency, f_{cl}	192.5 kHz
Bandwidth, BW	3.7 kHz
Q	52

Questions: Part 2

- Answers will vary. For the varactors tested, the resonant frequency was 168 kHz at 4 V of bias. This implies the total capacitance is

$$C = \frac{1}{(2\pi f_r)^2 L} = \frac{1}{(2\pi(168 \text{ kHz}))^2 15 \text{ mH}} = 60 \text{ pF}$$

Note: This is larger than the varactor capacitance alone. The reason is likely due to stray capacitance as discussed in step 1. (Typical varactor capacitance is 33 pF at -4 V).

2. The higher resonant frequency that was observed with increasing bias implies a smaller capacitance with increasing bias.
3. (a) It would have very little effect on the resonant frequency because the resonant frequency is primarily determined by the LC circuit.
- (b) It will affect the Q because R_1 acts as a resistive load on the resonant circuit.

Part 3: Light-Emitting Diode and Photodiode

Step 1: The red LED drops approximately 1.65 V when forward-biased (measured at 10 mA of current) and has the smallest ac resistance (approximately $50\ \Omega$ in the region tested). The yellow LED drops approximately 1.9 V when forward-biased. The green LED drops approximately 2.0 V and has the highest ac resistance (approximately $100\ \Omega$ in the region tested).

Step 2: The reverse curve drops as light is increased. (*Note:* The optimum value of R_1 depends on the diode and lighting conditions).

Step 4: Measured data for a green LED is shown in the table and plot.

Angle	Voltage
-90°	0.56 V
-75°	0.90 V
-60°	1.1 V
-45°	1.5 V
-30°	3.5 V
-15°	5.6 V
0°	6.0 V
+15°	5.3 V
+30°	2.3 V
+45°	1.1 V
+60°	0.85 V
+75°	0.69 V
+90°	0.29 V

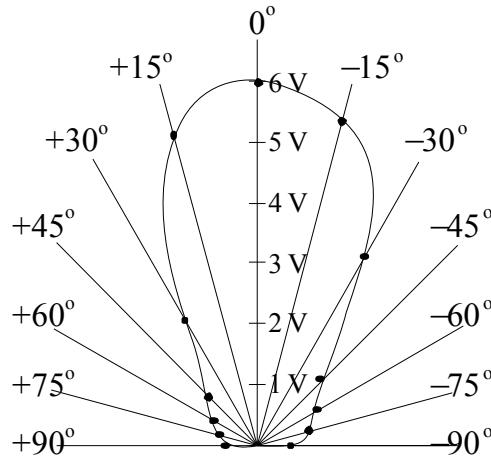


Figure 3-9 Directional data for a green LED

Questions: Part 3

1. (a) $I = \frac{18.0\text{ V} - 2.0\text{ V}}{680\ \Omega} = 23.5\text{ mA}$ (b) $R = \frac{18.0\text{ V} - 2.0\text{ V}}{30\text{ mA}} = 533\ \Omega$
2. *Electrical:* forward voltage drop at a specified forward current, reverse leakage current I_R , and reverse breakdown voltage $V_{(BR)R}$.
Optical: peak emission wavelength (in nm), power output (in milliwatts or microwatts) P_O , and spectral output.
3. The photodiode is a current source; a larger resistor develops more voltage for a given current, making the circuit more sensitive to light.

Experiment 4: Bipolar Junction Transistors

Part 1: The BJT Characteristic Curve

Values shown are for a 2N3904 transistor:

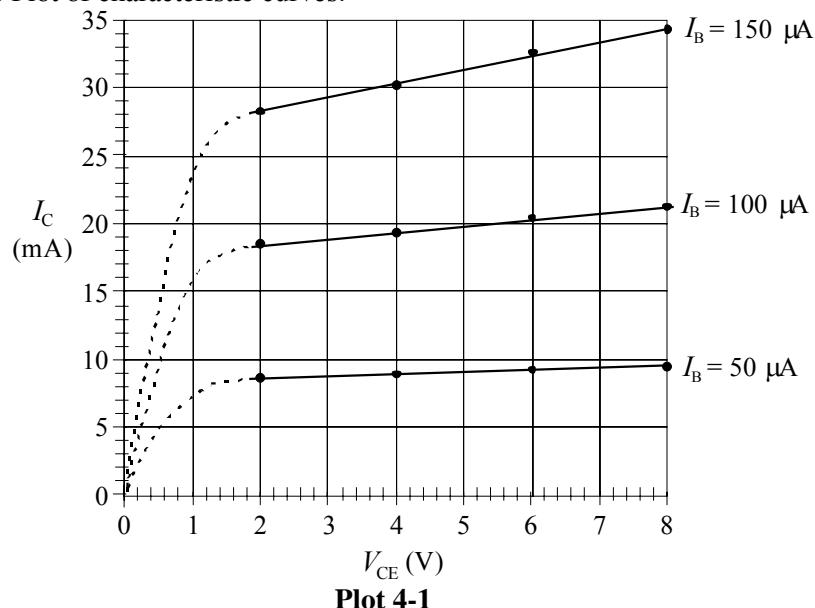
Table 4-1

Resistor	Listed Value	Measured Value
R_1	33 kΩ	32.8 kΩ
R_2	100 Ω	104 Ω

Table 4-2

V_{CE} (measured)	Base Current = 50 μA		Base Current = 100 μA		Base Current = 150 μA	
	V_{R2} (measured)	I_C (computed)	V_{R2} (measured)	I_C (computed)	V_{R2} (measured)	I_C (computed)
2.0 V	0.900 V	8.65 mA	1.91 V	18.4 mA	2.93 V	28.2 mA
4.0 V	0.931 V	8.95 mA	2.01 V	19.3 mA	3.14 V	30.2 mA
6.0 V	0.955 V	9.18 mA	2.13 V	20.5 mA	3.38 V	32.5 mA
8.0 V	0.992 V	9.54 mA	2.23 V	21.4 mA	3.58 V	34.4 mA

Step 11: Plot of characteristic curves:



Plot 4-1

Table 4-3

V_{CE}	Current Gain, β_{DC}		
	$I_B = 50 \mu A$	$I_B = 100 \mu A$	$I_B = 150 \mu A$
3.0 V	176	189	193
5.0 V	192	200	209

Questions: Part 1

1. For the test transistor, the β_{dc} was not constant at all points (see Plot 4-1). This has an effect on linearity as the gain will change as the operating point changes.
2. It would raise all of the curves.
3. Answers vary. For the test transistor, maximum power dissipated was $8\text{ V} \times 34\text{ mA} = 272\text{ mW}$.
4. (a)

$$\beta = \frac{I_C}{I_B}$$

$$\alpha = \frac{I_C}{I_E} = \frac{I_C}{I_C + I_B} = \frac{I_C/I_B}{I_C/I_B + I_B/I_B} = \frac{\beta_{dc}}{\beta_{dc} + 1}$$
- (b) Answers vary. The alpha for the test transistor was approximately 0.995.
5. V_{CE} would equal V_{CC} . Without base current, there would be no collector current and the supply voltage would appear across the transistor.

Part 2: BJT Switching Circuits

Table 4-4

Resistor	Listed Value	Measured Value
R_B	10 k Ω	9.88 kΩ
R_C	1.0 k Ω	1.00 kΩ
R_{C1}	10 k Ω	9.86 kΩ
R_E	330 Ω	327 Ω

Table 4-5

Quantity	Computed Value	Measured Value
$V_{CE(\text{cutoff})}$	12.0 V	10.45 V*
$V_{CE(\text{sat})}$	0.1 V	0.08 V
$V_{RC(\text{sat})}$	9.9 V	9.87 V
I_{sat}	9.9 mA	

* The LED and transistor appear to be open; thus the measurement is affected by meter loading. Answers vary.

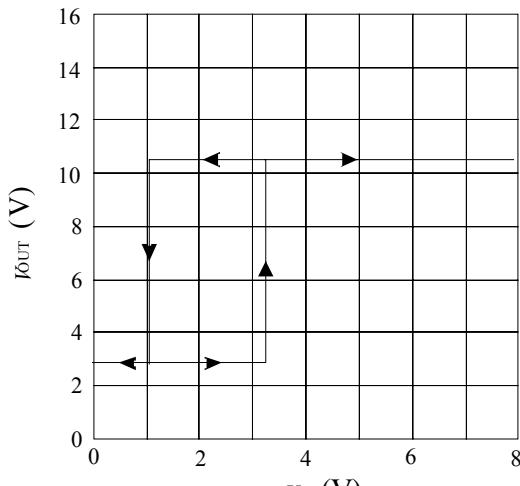
Table 4-6

Quantity	Measured Value
V_{IN} (LED on)	0.0 V
V_{OUT} (LED on)	0.080 V
V_{IN} (threshold)	0.645 V
V_{OUT} (threshold)	10.47 V*

Table 4-7

Quantity	Measured Value
V_{IN} (LED on)	0.0 V
V_{OUT} (LED on)	2.735 V
V_{IN} (upper threshold)	3.16 V
V_{OUT} (upper threshold)	10.47 V
V_{IN} (lower threshold)	1.03 V
V_{OUT} (lower threshold)	2.735 V

Step 8: Transfer curve:



Plot 4-2

Questions: Part 2

1. Some advantages of transistor switching circuits:
 - (1) Very fast
 - (2) Electrically controlled with a low voltage or current
 - (3) Reliable
 - (4) Low cost
 - (5) Can be adopted to interface high current loads with low current circuits.
2. R_B limits current to the base-emitter diode of Q_1 . Without it, current could destroy the transistor when the potentiometer is set near maximum.
3. Measure the voltage drop across R_B and apply Ohm's law.
4. The collector resistances are different for the two transistors.

Experiment 5 Transistor Bias Circuits

Part 1: Three Bias Circuits

Table 5-1

Resistor	Listed Value	Measured Value
R_B	1.0 MΩ	994 kΩ
R_C	2.0 kΩ	1.97 kΩ
R_E	1.5 kΩ	1.47 kΩ

Table 5-2

DC Parameter	Computed Value	Measured Value		
		Q_1	Q_2	Q_3
V_{RB}	11.3 V	11.4 V	11.3 V	11.3 V
I_B	11.37 μA			
I_C	2.27 mA			
V_{RC}	4.48 V	3.79 V	3.25 V	5.08 V
V_C	7.52 V	8.18 V	8.74 V	6.91 V

Table 5-3

DC Parameter	Computed Value	Measured Value		
		Q_1	Q_2	Q_3
V_{RB}	8.67 V	8.99	9.21	8.27
I_B	8.73 μA			
I_C	1.75 mA			
V_{RC}	3.44 V	2.86	2.56	3.79
V_C	8.56 V	9.11	9.42	8.21

Table 5-4

Resistor	Listed Value	Measured Value
R_1	33 k Ω	32.96 kΩ
R_2	6.8 k Ω	6.70 kΩ
R_E	680 Ω	676 Ω
R_C	2.0 k Ω	1.97 kΩ

Table 5-5

DC Parameter	Computed Value	Measured Value		
		Q_1	Q_2	Q_3
V_B	2.03 V	1.97 V	1.96 V	1.98 V
V_E	1.33 V	1.33 V	1.29 V	1.34 V
$I_E \approx I_C$	1.99 mA			
V_{RC}	3.97 V	3.86 V	3.74 V	3.88 V
V_C	8.03 V	8.14 V	8.25 V	8.12 V

Table 5-6

Resistor	Listed Value	Measured Value
R_B	360 k Ω	363 kΩ
R_C	2.0 k Ω	1.97 kΩ

Table 5-7

DC Parameter	Computed Value	Measured Value		
		Q_1	Q_2	Q_3
I_C	3.07 mA			
V_{RC}	6.13 V	5.73 V	5.23 V	6.27 V
V_C	5.87 V	6.26 V	6.76 V	5.73 V

Questions: Part 1

1. The data for voltage-divider bias shows the least variation between the transistors.
2. An emitter resistor will improve bias stability as it is a form of negative feedback.

Part 2: Emitter Bias and Two-Supply Voltage-Divider Bias**Table 5-8**

Resistor	Listed Value	Measured Value
R_B	4.7 k Ω	4.62 kΩ
R_C	330 Ω	329 Ω
R_E	470 Ω	477 Ω
R_2	4.7 k Ω	4.60 kΩ

Table 5-9

Quantity	Computed Value	Measured Value		
		Q_1	Q_2	Q_3
V_E	-1 V	-1.33 V	-1.10 V	-1.24 V
$I_E \approx I_C$	17.0 mA			
V_C	3.39 V	3.74 V	3.57 V	3.67 V

Table 5-10

Quantity	Computed Value	Measured Value		
		Q_1	Q_2	Q_3
V_E	-0.7 V	-1.05V	-0.93 V	-1.02 V
$I_E \approx I_C$	17.7 mA			
V_C	3.16 V	3.55 V	3.45V	3.52 V

Step 8: The LED fades out as the thermistor warms. The decrease in resistance as it warms causes the base voltage to drop and the transistor stops conducting.

Questions: Part 2

1. An advantage to emitter bias is great stability. A disadvantage is the requirement for both a positive and negative supply voltage.
2. For most troubleshooting work, it is valid to assume the emitter should be near -1 V. For precise design work, it is better to apply KVL.
3. The thermistor can be moved to the other side of the voltage-divider (in series with R_1). Alternatively, the thermistor could be changed for a positive temperature coefficient type

Experiment 6 BJT Amplifiers

Part 1: The Common-Emitter Amplifier

Table 6-1

Resistor	Listed Value	Measured Value
R_1	10 kΩ	9.87 kΩ
R_2	4.7 kΩ	4.66 kΩ
R_{E1}	100 Ω	100 Ω
R_{E2}	330 Ω	333 Ω
R_C	1.0 kΩ	1.00 kΩ
R_L	10 kΩ	10.1 kΩ

Table 6-2

DC Quantity	Computed Value	Measured Value
V_B	3.85 V	3.74 V
V_E	3.15 V	3.04 V
I_E	7.02 mA	
V_C	4.98 V	4.87 V
V_{CE}	1.83 V	1.93 V

Table 6-3

AC Quantity	Computed Value	Measured Value
$V_{in} = V_b$	300 mV _{pp}	300 mV_{pp}
V_e	290 mV_{pp}	280 mV_{pp}
r_e	3.6 Ω	
$V_{out} = V_c$	8.8	8.43
A_v	2.63 V_{pp}	2.53 V_{pp}
$R_{in(tot)}$	2.9 kΩ*	2.89 kΩ
β_{ac}	300 mV _{pp}	300 mV_{pp}

* Measured β_{ac} of 300 used for calculation

Step 8: The gain drops to 2.2 when C_2 is opened.

Step 9: The gain drops to 4.5 when R_L is replaced with a 1.0 kΩ resistor.

Step 10: Transistor is cutoff since there is no path for base current. (Note that a measurement of V_{CE} could mislead student to thinking transistor is near saturation; however, the power supply voltage is across the reverse-biased base-collector junction, not across R_C).

Step 11: Transistor is saturated. V_C and V_E are nearly the same and current is limited only by R_C and R_E . Maximum current is in the collector circuit.

Questions: Part 1

- Monitoring the output voltage ensures that the amplifier is performing normally during the test. If the output is clipped or distorted, the measurement is invalid.
- The load resistor has no effect on the input resistance because it is an isolated transistor, which looks like a current source.

3. The unbypassed emitter resistor is used for gain stability and makes gain much less dependent on the particular transistor that is used. It also increases the input resistance of the amplifier.
4. The gain is inversely proportional to the ac emitter resistance. When the bypass capacitor is open, the ac emitter resistance increases, and the gain goes down.

Part 2: The Common-Collector Amplifier

Table 6-4

	Listed Value	Measured Value
R_1	33 kΩ	32.5 kΩ
R_2	10 kΩ	9.98 kΩ
R_E	1.0 kΩ	1.00 kΩ
R_L	1.0 kΩ	1.01 kΩ

Table 6-6

AC Quantity	Computed Value	Measured Value
V_b	1.0 V _{pp} *	1.0 V_{pp}
V_e	298 mV_{pp}	298 mV_{pp}
r_e	3.0 Ω	
A_v	0.99	0.99
$R_{in(tot)}$	6.63 kΩ	7.03 kΩ
A_p	6.5	6.9

Table 6-5

DC Quantity	Computed Value	Measured Value
V_B	2.82 V	3.08 V
V_E	3.52 V	3.77 V
I_E	8.48 mA	
V_{CE}	-3.52 V	-3.77 V

Step 6: There is no phase shift between the input and output signal.

Table 6-7

Trouble	DC Predictions			DC Measurements			Effect of Trouble V_{out}
	V_B	V_E	V_{CE}	V_B	V_E	V_{CE}	
R_1 open	0.69 V	1.39 V	-1.39 V	0.66 V	1.37 V	-1.37 V	See note 1.
R_2 open	12.0 V	12.0 V	-12.0 V	12.0 V	12.0 V	-12.0 V	No output.
R_1 shorted	12.0 V	12.0 V	-12.0 V	12.0 V	12.0 V	-12.0 V	No output.
R_E open	2.82 V	0.0 V	0.0 V	12.0 V	0.0 V	0.0 V	No output.
open collector	10.2 V	10.9 V	-10.9 V	10.3 V	11.0 V	-11.0 V	See note 2.
open emitter	2.82 V	12.0 V	-12.0 V	2.82 V	12.0 V	-12.0 V	No output.

Note 1: Little effect. The dc conditions can be computed by assuming base bias; however, these conditions change when an ac signal is applied due to clamping action of the transistor and input coupling capacitor. The output ac signal is maintained as a result.

Note 2: Output reduced. The input impedance drops significantly when the collector is open. Although the voltage gain drops slightly (to about 0.88), the power gain drops significantly (measured = 0.38)

Step 8: Cutoff clipping is observed first.

Step 9: As the resistance increases, the clipping level is observed to rise.

Questions: Part 2

1. In the equivalent *npn* circuit, positive clipping occurs when the transistor has maximum conduction, hence it is saturation clipping.
2. The output voltage is always smaller than the input voltage but the output current is larger than the input current, hence there is power gain.

Part 3: Multistage Amplifiers

Table 6-8

Resistor	Listed Value	Measured Value
R_A	100 kΩ	100 kΩ
R_B	2.0 kΩ	1.98 kΩ
R_1	330 kΩ	322 kΩ
R_2	330 kΩ	321 kΩ
R_{E1}	33 kΩ	32.5 kΩ
R_{E2}	1.0 kΩ	1.00 kΩ
R_{C1}	22 kΩ	21.8 kΩ
R_3	47 kΩ	46.7 kΩ
R_4	22 kΩ	21.6 kΩ
R_{E3}	4.7 kΩ	4.68 kΩ
R_{E4}	220 Ω	219 Ω
R_{C2}	6.8 kΩ	6.71 kΩ
R_L	10 kΩ	10.0 kΩ

Table 6-9

DC Parameter	Computed Value	Measured Value
$V_{B(Q1)}$	0.0 V	0.46 V
$V_{E(Q1)}$	0.70 V	1.10 V
$I_{E(Q1)}$	0.43 mA	
$V_{C(Q1)}$	-5.69 V	-6.02 V
$V_{CE(Q1)}$	-6.39 V	-7.12 V
$V_{B(Q2)}$	-5.43 V	-5.83 V
$V_{E(Q2)}$	-6.13 V	-6.39 V
$I_{E(Q2)}$	1.80 mA	
$V_{C(Q2)}$	2.74 V	3.31 V
$V_{CE(Q2)}$	8.87 V	9.70 V

Table 6-10

AC Parameter	Computed Value
$r_{e'(Q1)}$	58.1 Ω
$r_{e'(Q2)}$	13.9 Ω
$R_{out(Q1)}$	21.8 kΩ
$R_{in(Q2)}$	9.1 kΩ
$A_v(NL)(Q1)$	20.4*
$A_v(NL)(Q2)$	28.0*

Table 6-11

AC Parameter	Computed Value	Measured Value
A_v'	78*	82
$R_{in(Q1)}$	63.8 kΩ	68.6 kΩ
$R_{out(Q2)}$	6.71 kΩ	6.71 kΩ
$V_{in(Q1)}$	10 mV	
$V_{out(Q2)}$	780 mV_{pp}	820 mV_{pp}

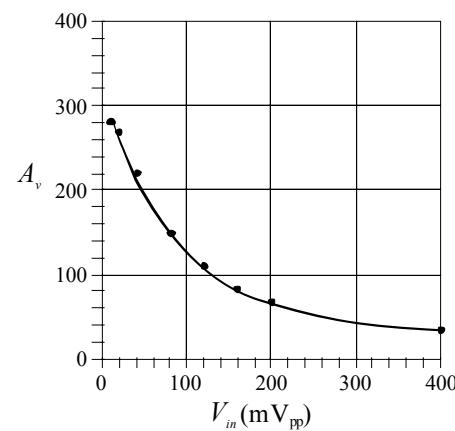
* calculated with 10 kΩ load resistor.

$$A_v' = 20.4 \times (9.1 \text{ kΩ}/39.9 \text{ kΩ}) \times 28.0 \times (10 \text{ kΩ}/16.7 \text{ kΩ}) = 78$$

Table 6-12

Generator Setting	V_{in}	V_{out}	A_v
0.5 V	10 mV*	2.8 V	280
1.0 V	20 mV	5.4 V	270
2.0 V	40 mV	9.1 V	220
4.0 V	80 mV	12.0 V	150
6.0 V	120 mV	12.8 V	107
8.0 V	160 mV	13.2 V	82.5
10.0 V	200 mV	13.2 V	66
20.0 V	400 mV	12.0 V	36

* V_{in} should be 2% of the generator setting. All voltages shown are peak-to-peak values. Some distortion is observed on the output for $V_{in} = 20$ V

**Plot 6-1****Questions: Part 3**

1. The input and output impedances are ac quantities. The input impedance is determined, in part, by r_e' , a quantity that can not be measured directly.
2. Capacitors can be considered “shorts” to ac for frequencies for which the reactance is small compared to the circuit impedance.
3. “Looking” back from the load resistor, the circuit can be considered to be a current source (the transistor) in parallel with the collector resistor. Assuming the current source is an open, the ac and dc resistances are equivalent and are represented by the collector resistor.
4. (a) Base bias is formed by removing R_4 and increasing the value of R_3 (the base resistor). To find the appropriate value, divide the emitter current (1.80 mA) by β ; this is the desired base current and current in R_3 . Find the resistance value by dividing the desired voltage across it (20.4 V) by the base current. For a β of 100, the computed base resistor is 1.1 MΩ.
 (b) The disadvantage of this is that the amplifier would be sensitive to the β of the particular transistor that is used.
5. Both stages are CE amplifiers, therefore they each change the phase by 180°. The result is that there is no phase shift to the output.

Experiment 7 Power Amplifiers

Part 1: The Class-A Power Amplifier

Table 7-1

Resistor	Listed Value	Measured Value
R_1	10 kΩ	9.9 kΩ
R_2	22 kΩ	21.9 kΩ
R_E	22 Ω, 2 W	23 Ω

Table 7-2

CC Amp ($Q_{1,2}$)	Computed Value	Measured Value
V_B	8.25 V	8.05 V
V_E	6.85 V	6.75 V
I_E	311 mA	
V_{CE}	5.15 V	5.25 V
r_e	1 Ω (est.)	
$A_{v(NL)}$	0.99	0.98
$A_{v(FL)}$	0.98	0.96

Table 7-3

Quantity	Value
Load resistance, R_L	8 Ω
Input resistance, R_{in}	6.81 kΩ
Output rms voltage, V_{out}	0.848 V_{rms}
Input rms voltage, V_{in}	0.883 V_{rms}
Load power, P_L	90 mW
Input power, P_{in}	0.113 mW
Power gain, A_p	796

Table 7-4

Quantity	Value
Quiescent power, P_Q	3.73 W
Load power, P_L	90 mW
Efficiency (percentage)	2.4%

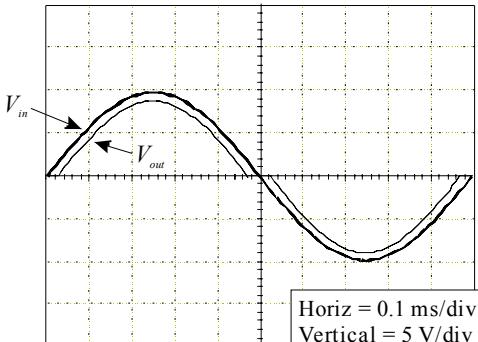
Questions: Part 1

- The efficiency will be higher because there is no wasted power in the emitter resistor. The disadvantage is that there is dc voltage across the speaker.
 - The efficiency will be higher because a larger fraction of the input power will become ac power to the load. Although both the dc and ac power will rise, the ac rises in greater proportion. (This can be tested with the Multisim simulation that goes with this experiment.)
- The Darlington arrangement isolates the load more and increases the input resistance of the amplifier.

Part 2: The Class-B Power Amplifier

Table 7-5

Resistor	Listed Value	Measured Value
R_L	330 Ω	351 Ω
R_1	10 k Ω	9.92 kΩ
R_2	10 k Ω	9.90 kΩ
R_3	68 k Ω	67.4 kΩ
R_4	2.7 k Ω	2.68 kΩ



Plot 7-1

Table 7-6

DC Parameter	Computed Value	Measured Value
V_E	0 V	0.015 V
V_{B1}	0.7 V	0.64 V
V_{B2}	-0.7 V	-0.60 V
$I_{R1} = I_{CQ}$	830 μA	

Table 7-7

AC Parameter	Computed Value	Measured Value
$V_{p(out)}$	7.5 V_p	7.2 V
$I_{p(out)}$	23.1 mA_p	
$P_{(out)}$	86.5 mW	

Table 7-8

DC Parameter	Computed Value	Measured Value
V_{B3}	-6.11 V	-6.15 V
V_{E3}	-6.81 V	-6.78 V
I_{CQ3}	811 μA	

Table 7-9

AC Parameter	Computed Value	Measured Value
A_v'	3.21	3.14

Questions: Part 2

1. Open D_2 , bad Q_2 , no -9 V voltage.
2. Half the signal will be missing.
3. Bypass R_4 .

Experiment 8 Field-Effect Transistors

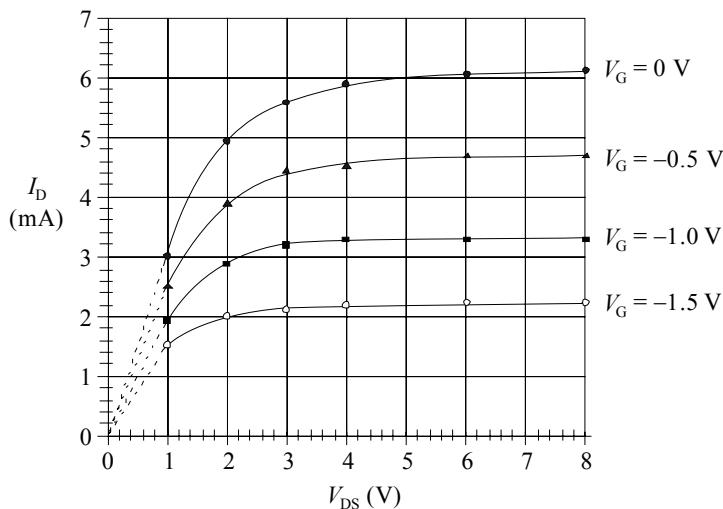
Part 1: JFET Characteristic Curve

Table 8-1

Resistor	Listed Value	Measured Value
R_1	10 kΩ	10.0 kΩ
R_2	100 Ω	100 Ω

Table 8-2

V_{DS}	$V_G = 0 \text{ V}$		$V_G = -0.5 \text{ V}$		$V_G = -1.0 \text{ V}$		$V_G = -1.5 \text{ V}$	
	V_{R2}	I_D	V_{R2}	I_D	V_{R2}	I_D	V_{R2}	I_D
1.0 V	0.304 V	3.04 mA	0.248 V	2.48 mA	0.197 V	1.97 mA	0.152 V	1.52 mA
2.0 V	0.487 V	4.87 mA	0.388 V	3.88 mA	0.291 V	2.91 mA	0.201 V	2.01 mA
3.0 V	0.560 V	5.60 mA	0.443 V	4.43 mA	0.320 V	3.20 mA	0.214 V	2.14 mA
4.0 V	0.588 V	5.88 mA	0.458 V	4.58 mA	0.328 V	3.28 mA	0.218 V	2.18 mA
6.0 V	0.605 V	6.05 mA	0.469 V	4.69 mA	0.333 V	3.33 mA	0.222 V	2.22 mA
8.0 V	0.616 V	6.16 mA	0.469 V	4.69 mA	0.333 V	3.33 mA	0.223 V	2.23 mA



Plot 8-1

Step 12: At $V_{DS} = 3.22 \text{ V}$, the current for the test transistor reached 5.46 mA , 90% of I_{DSS} .

Questions: Part 1

1. In the constant-current region, read I_D for each value of V_{GS} . Plot V_{GS} on the negative x -axis as a function of I_D .
2. (a) The transconductance is dependent on V_{GS} .
(b) Each characteristic curve was drawn with the same increase in V_{GS} , but the corresponding drain currents do not follow a linear pattern.

Table 8-3

Measured JFET Parameters
$V_{GS(\text{off})} = -3.22 \text{ V}$
$I_{DSS} = 6.1 \text{ mA}$

Part 2: JFET as a Voltage-Controlled Resistor

Table 8-4

Resistor	Listed Value	Measured Value
R_1	56 kΩ	56.3 kΩ
R_2	39 kΩ	38.7 kΩ
R_E	6.2 kΩ	6.24 kΩ
R_C	3.9 kΩ	3.88 kΩ
R_3	100 kΩ	100.4 kΩ

Table 8-5

DC Quantity	Computed Value	Measured Value
V_B	6.11 V	6.01 V
V_E	5.41 V	5.39 V
I_E	0.867 mA	
V_C	11.64 V	11.68 V
V_{CE}	6.23 V	6.29 V

Table 8-6

	Predicted Gain	Measured V_{out}	Measured Gain
Maximum Gain $V_{GG} = 0$ V	13.8	4.92 V_{pp}	12.3*
Gain with $V_{GG} = -0.5$ V		4.24 V_{pp}	10.6
Gain with $V_{GG} = -1.0$ V		3.56 V_{pp}	8.9
Gain with $V_{GG} = -1.5$ V		2.84 V_{pp}	7.1
Gain with $V_{GG} = -2.0$ V		2.00 V_{pp}	5.0
Gain with $V_{GG} = -2.5$ V		0.98 V_{pp}	2.45
Gain with $V_{GG} = -3.0$ V		0.26 V_{pp}	0.65
Gain with $V_{GG} = -5.0$ V		0.24 V_{pp}	0.60

* Three FETs were tested. The smallest observed gain for 0 bias was 9.8 but all fell to a minimum of 0.6.

Step 5: The output continues to drop as V_{GG} is increased until $V_{GS(off)}$ is reached; then it remains at a gain of about 0.60.

Table 8-7

	Measured V_{out}	Measured Gain
$V_{in} = 100$ mV _{pp}	1.06 V_{pp}	10.6
$V_{in} = 400$ mV _{pp}	3.40 V_{pp}	8.5
$V_{in} = 800$ mV _{pp}	3.56 V_{pp}	4.45
$V_{in} = 1.2$ V _{pp}	2.84 V_{pp}	2.37

Questions: Part 2

- The ac signal is coupled through C_3 and rectified by D_1 . Negative excursions charge capacitor C_4 , which biases the FET. A larger signal produces a larger dc voltage on the gate, thus increasing the emitter resistance of Q_1 and reducing the gain.
- R_4 and C_4 maintain a dc voltage on the gate and determine how fast the gate voltage can respond to an input signal change.

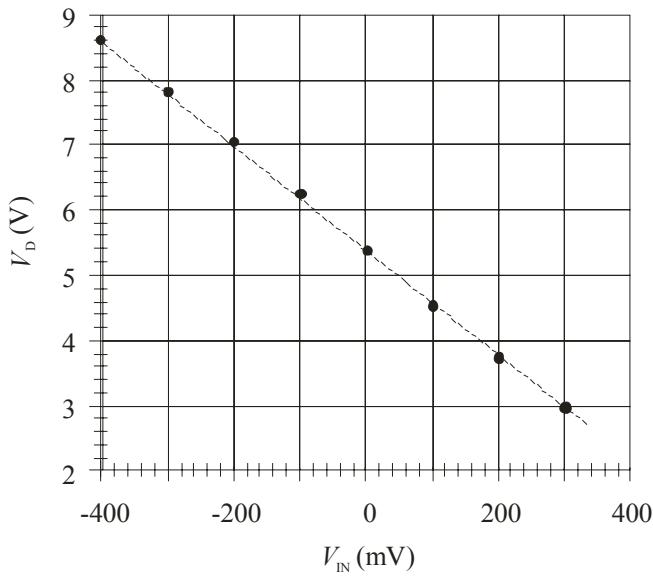
Part 3: JFET as a DC Amplifier

Table 8-8

Resistor	Listed Value	Measured Value
R_1	5.6 kΩ	5.63 kΩ
R_2	620 Ω	614 Ω
R_3	1.0 MΩ	998 kΩ
R_S	180 Ω	177 Ω
R_D	3.9 kΩ	3.91 kΩ

Table 8-9

V_{IN}	V_D (measured)
300 mV	2.99 V
200 mV	3.71 V
100 mV	4.53 V
0 V	5.36 V
-100 mV	6.21 V
-200 mV	7.03 V
-300 mV	7.81 V
-400 mV	8.80 V



Plot 8-2

Questions: Part 3

1. The transfer curve in Plot 8-2 indicates the output is a linear function of the input dc voltage.
2. The bias is self-bias, with the voltage developed across R_S making the source more positive than the gate.
3. An increase in the power supply voltage will increase the drain current, which is partially offset by the self-bias. The drain voltage will increase, but should still have a linear response.

Experiment 9 FET Amplifiers and Switching Circuits

Part 1: The Common-Source JFET Amplifier

Table 9-1

Resistor	Listed Value	Measured Value
R_S	1.0 kΩ	1.02 kΩ
R_D	3.3 kΩ	3.26 kΩ
R_G	1.0 MΩ	1.01 MΩ
R_L	10 kΩ	9.9 kΩ

Table 9-2 Parameters for CS Amplifier

Quantity	DC values	AC values
Gate voltage, V_G	0 V	
Source voltage, V_S	1.73 V	
Drain voltage, V_D	9.24 V	
Drain current, I_D	1.77 mA	
Input voltage, V_{in}		500 mV_{pp}
Output voltage, V_{out}		2.26 V_{pp}
Voltage gain, A_v		4.53
Phase difference		180°

4. The measured output voltage went from 2.26 V_{pp} to 2.44 V_{pp} when the 1.0 kΩ source resistor was replaced with 510 Ω. The transconductance, g_m , increases because the bias current increases. Gain is $A_v = g_m r_d$.
5. When the load resistor was changed from 10 kΩ to 100 kΩ, the output voltage went from 2.44 V_{pp} to 3.06 V_{pp} due to the increase in ac drain resistance, r_d . As before, gain is $A_v = g_m r_d$.

Table 9-3

Fault	Observation
C_2 is open	No change to dc; gain drops to 1.6.
Source and drain reversed	No difference; gain remains at 4.5.
V_{DD} drops to +12 V	Slight drop in gain (to 4.4).
R_G open	Gate has small variations in dc level; ac ok but can drop out completely.

Questions: Part 1

1. There is no effect because the input impedance is controlled only by gate resistor.
2. The BJT will significantly load a 100 kΩ source; the FET will not, so it is better suited for this application.

Part 2: The Common-Drain JFET Amplifier

Table 9-4 Parameters for CD Self-Biased Amplifier

Quantity	DC values	AC values
Gate voltage, V_G	0 V	
Source voltage, V_S	1.83 V	
Drain voltage, V_D	15.0 V	
Drain current, I_D	1.83 mA	
Input voltage, V_{in}		2.0 V_{pp}
Output voltage, V_{out}		1.27 V_{pp}
Voltage gain, A_v		0.64
Phase difference		0°

Table 9-5 Parameters for CD Current-Source Biased Amplifier

Quantity	DC values	AC values
Q_1 gate voltage, V_G	0 V	
Q_1 source voltage, V_S	1.72 V	
Q_1 drain voltage, V_D	15.0 V	
Q_2 gate voltage, V_G	-15.0 V	
Q_2 source voltage, V_S	-13.3	
Q_2 drain voltage, V_D	0 V	
Drain current, I_D	1.70 mA	
Input voltage, V_{in}		2.01 V_{pp}
Output voltage, V_{out}		2.00 V_{pp}
Voltage gain, A_v		0.996
Phase difference		0°

Step 4: With a 10 kΩ load, the signal level drops to 1.74 V_{pp} (measured). When the signal was increased, the output was observed to have a 20 V_{pp} signal with no clipping (the limit of the signal generator).

Step 5: The dc offset remained very close to 0 V. Student answers may differ as the offset will change if the transistors are not matched.

Questions: Part 2

1. The current source acts like a very high load impedance on the CD amplifier.
2. The input resistance is equal to $R_G = 1.0 \text{ M}\Omega$. The loading observed by the 10 kΩ load resistor indicates that the output impedance is 1.5 kΩ.

Part 3: A Cascode Amplifier

Table 9-6

Resistor	Listed Value	Measured Value
R_1	5.6 kΩ	5.63 kΩ
R_2	620 Ω	618 Ω
R_3	1.0 MΩ	0.96 MΩ
R_4	1.5 MΩ	1.56 MΩ
R_G	1.0 MΩ	1.02 MΩ
R_S	100 Ω	99.8 Ω

Table 9-7

Parameter	Measured Value
$V_{G(Q1)}$	8.63 V
$V_{S(Q1)}$	10.37 V
$V_{G(Q2)}$	0.001 V
$V_{S(Q2)}$	0.215 V

Table 9-8 (Data for 500 kHz)

Parameter	Measured Value
V_{in}	50 mV _{pp}
V_{out}	1.16 V_{pp}
$A_{v(Q1/Q2)}$	23.2

Table 9-9 (Data for 50 kHz)

Parameter	Measured Value
V_{in}	50 mV _{pp}
V_{out}	2.68 V_{pp}
$A_{v(Q1/Q2)}$	53.6

Step 6: The output drops. At 10 Vdc, the output at 50 kHz drops to 1.06 V_{pp}.

Questions: Part 3

1. The data shows that the source voltage is higher than the gate voltage for both FETs.
2. Because the higher frequencies have less gain, a parallel capacitance path to ground is suspected. This is likely caused by the capacitance of the protoboard.

Experiment 10 Amplifier Frequency Response

Part 1: Low-Frequency Response

Table 10-1

Resistor	Listed Value	Measured Value
R_A	1.0 kΩ	5.58 kΩ
R_B	47 Ω	617 Ω
R_1	68 kΩ	9.91 kΩ
R_2	10 kΩ	67.1 kΩ
R_{E1}	10 Ω	565 Ω
R_{E2}	560 Ω	10 Ω
R_C	3.9 kΩ	3.87 kΩ
R_L	10 kΩ	9.88 kΩ

Table 10-2

Parameter	Computed Value	Measured Value
V_B	13.1 V	13.2 V
V_E	13.8 V	13.8 V
I_E	2.1 mA	
V_C	8.21 V	8.15 V
V_{CE}	-5.59 V	-5.55 V
r_e	11.9 Ω	
A_v	127	100
V_{out}	1.27 V	1.00 V

Table 10-3

Capacitor	R_{eq}
C_1	3.5 kΩ*
C_2	24 Ω
C_3	13.9 kΩ

Table 10-4

Capacitor	$-- f_{critical} --$	
	Computed	Measured
C_1	45 Hz	41 Hz
C_2	66 Hz	70 Hz
C_3	52 Hz	52 Hz
Overall	163 Hz	122 Hz

Table 10-5

Computed value of C_2	Measured low frequency
25 μF	f = 330 Hz

Calculated capacitance to raise low frequency to 300 Hz is 25 μF as follows:

$$C = \frac{1}{2\pi f R_{eq}} = \frac{1}{2\pi f (R_{E2} \parallel (R_{E1} + r_e))} = \frac{1}{2\pi(300 \text{ Hz})(560 \Omega \parallel (10 \Omega + 11.9 \Omega))} = 25 \mu\text{F} \text{ (use } 22 \mu\text{F)}$$

Questions: Part 1

- C_2 has the greatest effect because the RC time constant is lower than the others.
- Because all three responses are similar, capacitors that are 5X larger are the simplest change to reduce the lower frequency cutoff by a factor of five.

Part 2: High-Frequency Response

Table 10-6

Parameter	Computed Value	Measured Value
V_B	1.91 V	1.80 V
V_E	1.22 V	1.13 V
I_E	2.12 mA	
V_C	6.67 V	7.35 V
V_{CE}	5.46 V	6.22 V
r_e	12.3 Ω	
A_v	124	111
V_{out}	2.48 V_{pp}	2.22 V_{pp}

Table 10-7

Step	Parameter	Computed Value	Measured Value
4	C_{in}	11.3 nF	
5	$R_{eq(in)}$	44.8 Ω	
6	$f_{c(in)}$	314 kHz	
7	C_{out}	201 pF	
8	R_c	2.81 kΩ	
9	$f_{c(out)}$	281 kHz	
10	f_{cu}	148 kHz	159 kHz

Questions: Part 2

1. The unbypassed emitter resistor reduces the gain of the amplifier and increases the upper frequency response. The Miller capacitance is directly proportional to the gain, so the reduced gain increases the upper frequency cutoff as a result.
2. (a) For a wide band amplifier, the upper critical frequency and the bandwidth are essentially identical. Rise time is measured by using a fast-rising pulse at the input and observing the (inverted) pulse on the output for an inverting amplifier. The time required for the output to change from 90% to 10% is measured and substituted into the equation.
 (b) The calculated rise time (based on a measured value of 159 kHz) is 2.2 μs. (Measured result was 2.12 μs).

Experiment 11 Thyristor

Part 1: The SCR

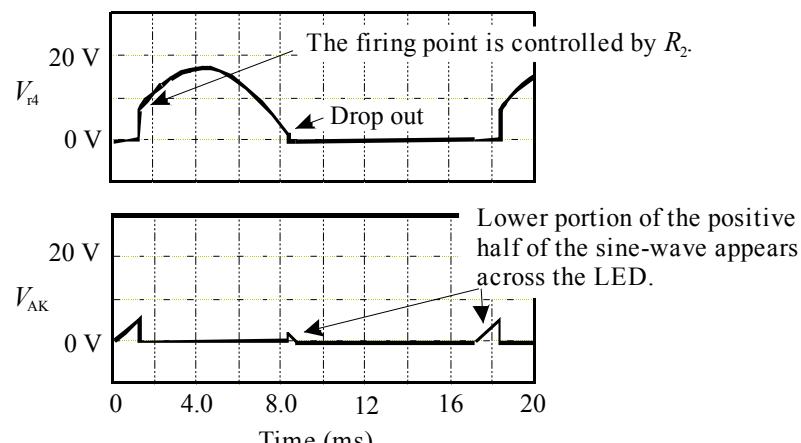
Table 11-1

Resistor	Listed Value	Measured Value
R_1	1.0 kΩ	993 Ω
R_3	160 Ω	161 Ω
R_4	1.0 kΩ	1.001 kΩ
R_5	10 kΩ	9.94 kΩ

Table 11-2

Parameter	Transistor Latch	SCR
$V_{AK(\text{off state})}$	13.5 V	13.5 V
$V_{AK(\text{on state})}$	0.803 V	0.769 V
$V_{\text{Gate trigger}}$	0.768 V	0.736 V
V_{R4}	3.42 V	3.83 V
$I_{H(\min)}$	3.42 mA	3.83 mA

Step 7: S_1 turns on the SCR. S_2 turns it off.



Plot 11-1

Questions: Part 1

1. The voltage across R_4 is proportional to the conduction current. The SCR is on for a shorter time and the back of the SCR waveform will drop earlier.
2. In the circuit in Figure 11-3, the capacitor is charged by the positive supply voltage so that the right side is positive. Connecting it to ground through SW2 causes the anode to be more negative than the cathode, dropping the SCR out of conduction.

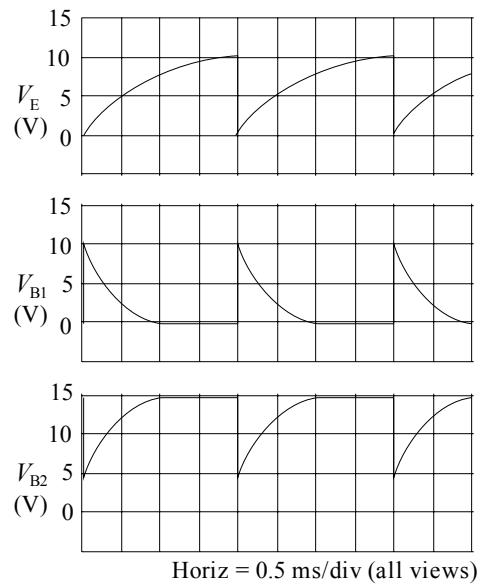
Part 2: The Unijunction Transistor

Table 11-3

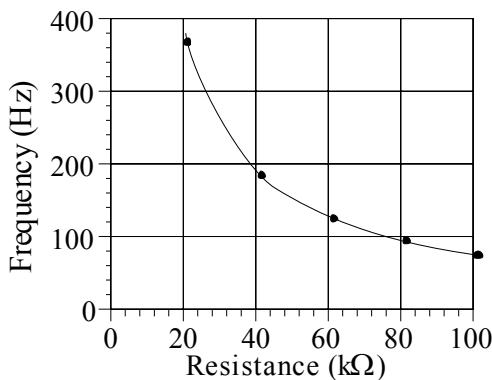
Resistor	Listed Value	Measured Value
R_1	47Ω	
R_2	220Ω	
R_3	$15 \text{ k}\Omega$	

Table 11-4

Resistance setting of R_4	Total Resistance	Measured Frequency
$5.0 \text{ k}\Omega$		
$25 \text{ k}\Omega$		
$45 \text{ k}\Omega$		
$65 \text{ k}\Omega$		
$85 \text{ k}\Omega$		



Plot 11-2



Plot 11-3

4. The frequency decreases in a nonlinear manner as the total resistance increases.
5. The period of the RC charging waveform decreases as the total resistance decreases. The amplitude is not changed.
6. The frequency is unaffected. The amplitude varies directly with the power supply.

Questions: Part 2

1. 6.7 V
2. The emitter voltage must be at least one diode drop (about 0.7 V) higher than V_K , the voltage established inside the device by the intrinsic standoff ratio.

Experiment 12-A Operational Amplifiers

Part 1: The Differential Amplifier

Table 12-1

Resistor	Listed Value	Measured Value
R_{B1}	100 kΩ	102 kΩ
R_{B2}	100 kΩ	102 kΩ
R_{E1}	100 Ω	99 Ω
R_{E2}	100 Ω	100 Ω
R_T	10 kΩ	10.2 kΩ
R_{C2}	10 kΩ	10.3 kΩ

Table 12-2

DC Parameter	Computed Value	Measured Value
V_A	-1 V	-1.1 V
I_T	1.4 mA	
$I_{E1} = I_{E2}$	0.7 mA	
$V_{C(Q1)}$	+15.0 V	+15.0 V
$V_{C(Q2)}$	+8.0 V	+8.35 V

Table 12-3

AC Parameter	Computed Value	Measured Value
$V_{b(Q1)}$	100 mV _{pp}	100 mV_{pp}
V_A	50 mV_{pp}	50 mV_{pp}
$r_{e(Q1)} = r_{e(Q2)}$	35.7 Ω	
$A_{v(d)}$	36.8	35.5
$V_{c(Q2)}$	3.68 V_{pp}	3.55 V_{pp}
$R_{in(tot)}$	35.1 kΩ	36.5 kΩ
$A_{v(cm)}$	0.5	0.44
CMRR'	37.3	38.1

Step 9: The CMRR' rises significantly due to a much smaller common mode gain. The observed common-mode output was approximately 5 mV_{pp} for a 7.7 V_{pp} input signal. This translates to a measured CMRR' of 95 dB. This result is better than expected based on previous tests with this circuit; student answers will likely be lower.

Questions: Part 1

1. It assures that the measurement is made when the amplifier is operating in its linear region.
2. 1.45 mA

Part 2: Op-Amp Specifications

Table 12-4

Step	Parameter	Specified Value			Measured Value
		Minimum	Typical	Maximum	
2d	Input offset voltage, V_{OS}		2.0 mV	6.0 mV	0.66 mV
3d	Input bias current, I_{BIAS}		80 nA	500 nA	98 nA
3e	Input offset current, I_{OS}		20 nA	200 nA	1 nA
4b	Differential gain, $A_{v(d)}$				1000
4c	Common-mode gain, A_{cm}				0.032
4d	CMRR	70 dB	90 dB		89.9 dB
5	Slew rate		0.5 V/ μ s		0.8 V/μs

Table 12-5

Resistor	Listed Value	Measured Value
R_f	1.0 M Ω	1.01 MΩ
R_i	10 k Ω	10.2 kΩ
R_C	10 k Ω	10.2 kΩ

Table 12-6

Resistor	Listed Value	Measured Value
R_1	100 k Ω	102 kΩ
R_2	100 k Ω	102 kΩ

Table 12-7

Resistor	Listed Value	Measured Value
R_A	100 Ω	102 Ω
R_B	100 Ω	101 Ω
R_C	100 k Ω	102 kΩ
R_D	100 k Ω	102 kΩ

Questions: Part 2

1. The input bias current is the average of the input currents; the input offset current is the difference between the input currents when the output voltage is 0 V.
2. The advantage is the rejection of common-mode signals; these are undesired and frequently represent cross-talk, or other form of interference.

Part 3: Basic Op-Amp Circuits

Table 12-8

Resistor	Listed Value	Measured Value
R_1	1.0 kΩ	1.02 kΩ
R_f	10 kΩ	10.2 kΩ

Table 12-9

Parameter	Computed Value	Measured Value
V_{in}	500 mV _{pp}	500 mV_{pp}
$A_{cl(I)}$	-10	
V_{out}	-5.0 V_{pp}	-4.95 V_{pp}
$V_{(-)}$		0 V_{pp}
R_{in}		1.0 kΩ

Table 12-10

Parameter	Computed Value	Measured Value
V_{in}	500 mV _{pp}	500 mV_{pp}
$A_{cl(NI)}$	11	
V_{out}	5.5 V_{pp}	5.5 V_{pp}
$V_{(-)}$		500 mV_{pp}
R_{in}		5 MΩ

Step 3: The observed gain at 1 kHz was 149.3. As the frequency is raised, the gain is observed to go down. At 10 kHz, the measured gain was 98.6.

Questions: Part 3

1. Amplifier 1 gain = $20 \log (11) = 20.8 \text{ dB}$
Amplifier 2 gain = $20 \log (10) = 20.0 \text{ dB}$
2. The voltage on the inverting terminal is not close to ground; it is nearly the same as the input voltage.
3. The RC low-pass filters within the op-amp cause the gain to roll-off as frequency increases.

Experiment 12B: Programmable Analog Design

Part 1: Introduction to AnadigmDesigner2

Instructor note:

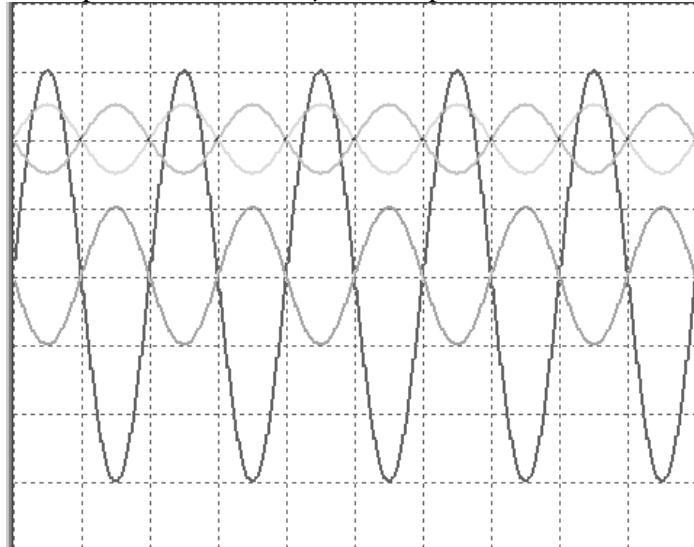
If lab time is critical and the students have laptops or other computer access to the web, Part 1 can be done outside of the lab time.

Steps 1-10: These steps are tutorial in nature and do not require a response from students.

Step 11: Observations: The traces are described in the procedure but are summarized as follows: The largest trace (violet) is the 6 V_{pp} signal from the oscillator. In the

center of the screen is an inverted and attenuated 2 V_{pp} signal (green) that represents the output of the amplifier. The output traces (yellow and blue) are at the top of the display. They are offset by 2 V and have opposite phases and represent the differential outputs from the Anadigm chip.

Time per division is 10 μ s, volts per division is 1V with no offset for all signals.



Plot 12-1 Waveforms for 3 V 50 kHz sine wave amplified by $-1/3$.

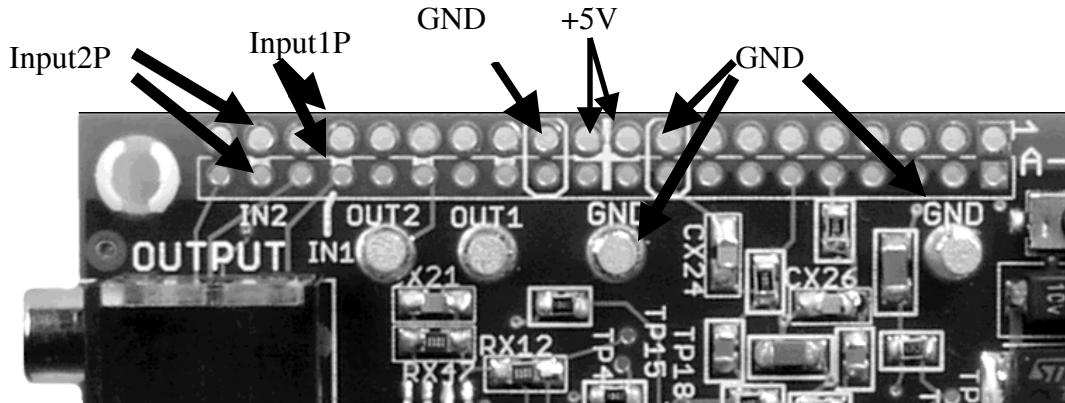
Step 12: The file extension is .ad2.

Questions: Part 1

1. (a) 0.25 V
(b) -0.333
2. A ground referenced sine wave is centered on 0 V, with each peak an equal amount away from 0 V.
3. The peaks of a 1 V peak sine are +1 V and -1 V from the reference. With a reference of +2 V, the peaks are at +3 V and +1 V.
4. (a) The differential signal is the difference between the two signals.
Mathematically, this can be expressed as OutputA – OutputB for the two outputs.
(b) The differential signal is the same.
5. .ad2

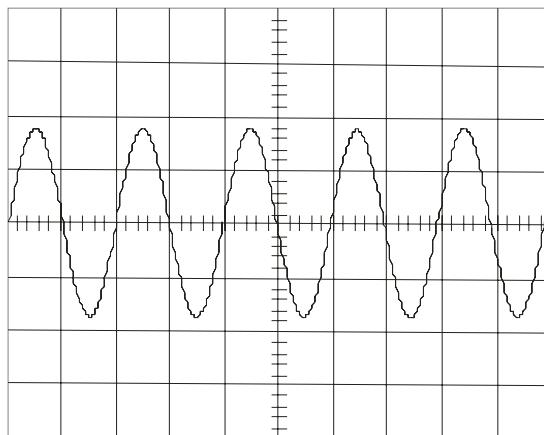
Part 2: Downloading the Configuration File

Instructor note: There are +5 V and ground points located on the PAM board edge that must not be shorted together. Explain to students to be careful when connecting a probe to the board and make sure that the probe's ground clip does not contact any point except a marked ground terminal. The additional points are shown here (but we chose not to show them in the student manual).



Signal, power, and ground points on the PAM board edge.

Step 3: The signal level is approximately 1 V_p , but depends on the setting of the gain on the PAM output buffer. For the several PAM units tested the amplitude was 0.85 V to 1.05 V. More recently produced PAMs will show an output close to 1 V indicating an input-to-output system gain close to +1. For the board tested the amplitude was 0.85 V. The output resembles the simulation waveform from the inverting amplifier.



Time per division is $10 \mu\text{s}$, volts per division is 500 mV

Plot 12-2 Measured waveform.

The output resembles the output of the gain stage shown on the internal simulation but with slightly lower amplitude (see the green waveform in the simulation).

Step 4: The simulated waveform is 2.0 V_pp at 50 kHz referenced to ground. The observed signal from the PAM is 1.67 V_pp at 50 kHz referenced to ground.

Instructor note: The Anadigm ASP and the PAM operate using a mixture of single-ended signals and differential-signals which can be confusing. The lab manual explains this through Experiments 12, 13 and 14 culminating in Figure 14-11 that shows the full details of the input signal path, connections to the Anadigm ASP and the output signal path. Here is a preview of the relevant facts (see Figure 14-11 as you read this):

- 1) The inputs and outputs of the PAM at the board edge (INPUT1, INPUT2, OUT1, OUT2) are referenced to ground.
- 2) The input buffer and output buffer devices provided on the PAM board operate using +5 V and -5 V power supplies to be able to deal with signals that are above and below ground.
- 3) The Anadigm ASP operates using only 0 V and +5 V power supplies so it can only handle signals that are above ground level.
- 4) The designers of the Anadigm ASP decided to do all signal processing level shifted to +2.0 V which they call the “mid-range reference level”.
- 5) The input buffers and output buffers on the PAM take care of level shifting between ground referenced signals in the outside world and the +2.0 V mid-range referenced signals of the Anadigm ASP. This is done so that the student will not need to worry about or even know much about the level shifted signal processing that the Anadigm ASP performs.
- 6) The Anadigm ASP does all of its internal signal processing differentially, even though the wires in the AD2 design space and the waveforms in the simulator are shown as if they are signal-ended ground referenced signals.
- 7) The signal outputs of the Anadigm ASP are differential. The PAM provides output buffers that do two things:
 - i) Convert the Anadigm ASP differential outputs to single-ended signals.
 - ii) Level shift the Anadigm ASP outputs from +2V to ground reference. This feature allows the student to observe signals on the simulator display and at the OUT1 and OUT2 terminals on the PAM without confusion regarding differential vs. single-ended and +2.0 V referenced vs. ground referenced.
- 8) There are test points provided on the top surface of the PAM to observe the signals out of the Anadigm ASP:

For the Anadigm ASP Output1, TP4 is the positive output and TP3 is the negative output.
For the Anadigm ASP Output2, TP2 is the positive output and TP1 is the negative output.
The positive differential signal observed at TP4 will have $\frac{1}{2}$ the amplitude of the total Output1 signal with the +2.0 V offset.
- 9) The signals into the Anadigm ASP are differential. The PAM provides input buffers that do two things:
 - i) Allow the input of either differential signals or single-ended signals according the Input Termination DIP switch settings.
 - ii) Level shift ground referenced input signals to the +2.0 V referenced signals for the Anadigm ASP to use.
- 10) The differential input buffers on the PAM have a gain of approximately +1 for differential input signals and a gain of approximately $\frac{1}{2}$ for single-ended input signals. This $\frac{1}{2}$ gain characteristic is typical for differential amplifiers where only one leg of the input is driven by a signal.

Step 5: Answers can vary depending on the particular PAM board. For the one tested, the required gain is:

$$A_v = \frac{2.0 \text{ V}_{\text{pp}}}{1.67 \text{ V}_{\text{pp}}} \times 0.33 = 0.395$$

Step 6: Measured output amplitude is 1.0 V_p (2.0 V_{pp}).

Step 7: Answers will vary, depending on the setting of the gain stage and the particular PAM version. With the gain stage set for a gain of 0.395, the simulated amplitude is 1.17 V_p (2.34 V_{pp}). The measured amplitude for the PAM tested drops to 0.79 V_p (1.58 V_{pp}).

Instructor note: The remaining steps in the experiment are observations only and require a set of computer speakers, so that students can hear the audio tone that is generated. If speakers are not available, these steps can be skipped.

Questions: Part 2

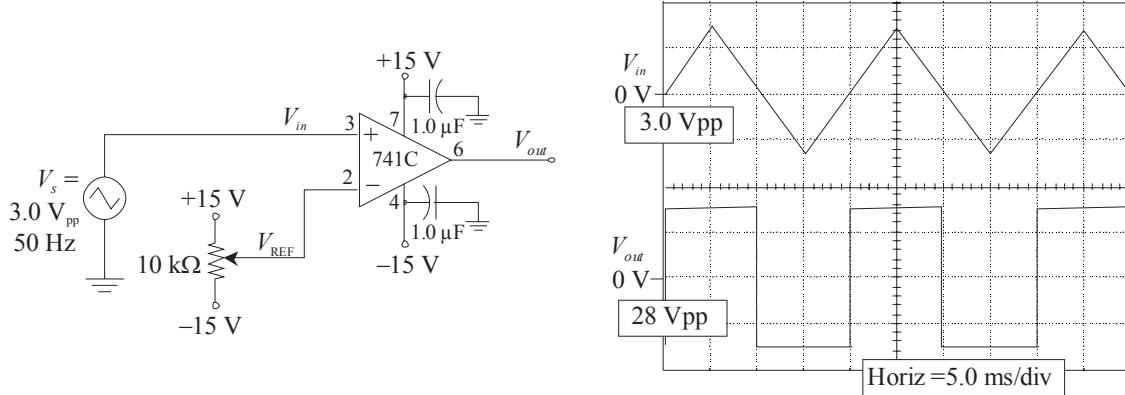
1. Steps to change gain are:
 - Double-click the gain's stage to open the CAM window
 - Change gain value in the CAM window
 - Click in another part of the window to update and verify the realized value
 - Close the CAM window
 - Download the new configuration
2. Signals internal to the Anadigm IC; and some signals at the pins of the Anadigm IC that are not sent to the output of the PAM board
3. Increase the gain of the gain stage by the ratio of the desired output signal to the observed output signal.

Instructor note: This procedure changes the gain at all frequencies. There are filter adjustments that can avoid this, but this answer is not expected from students.)

4. The Anadigm IC resets, losing the configuration information.

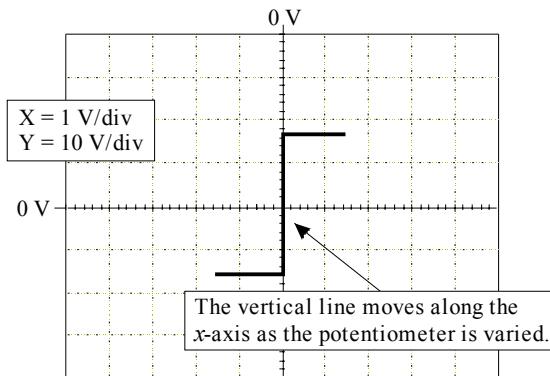
Experiment 13-A Basic Op-Amp Circuit

Part 1: The Comparator and Schmitt Trigger

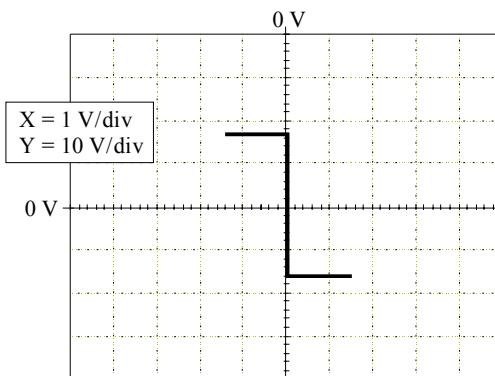


Plot 13-1 Comparator waveform

Step 2: Varying the potentiometer changes the duty cycle of the output from 0 to 100%. The sine wave shows the same response.



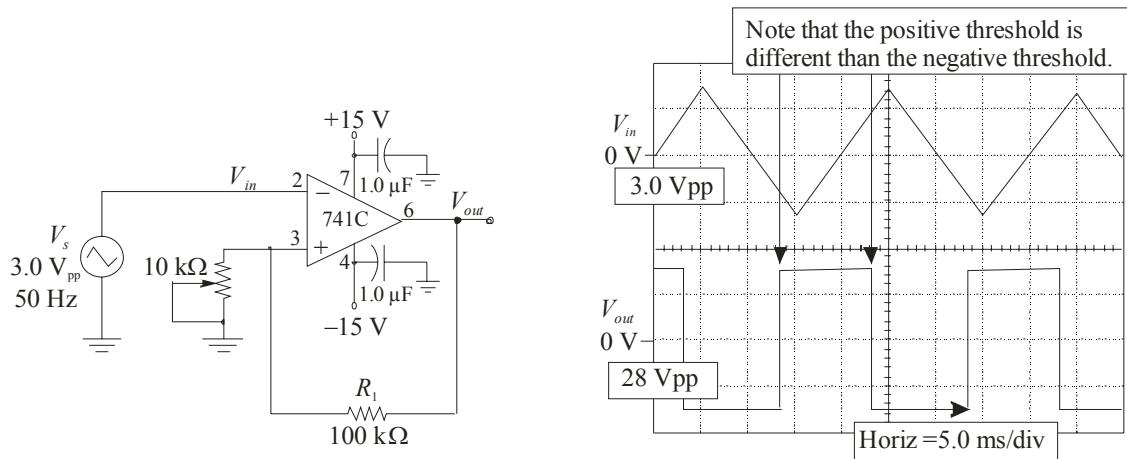
Plot 13-2 Comparator transfer curve



Plot 13-3 Comparator transfer curve
(inputs reversed)

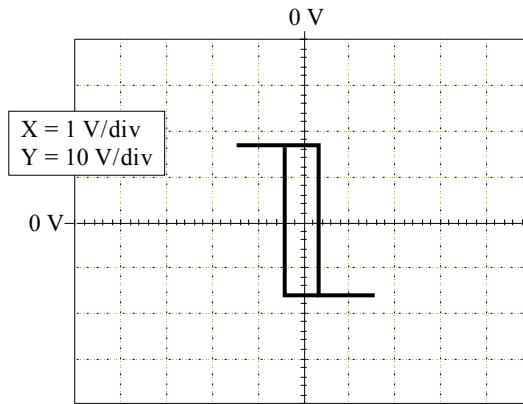
Step 4: Varying the potentiometer causes the vertical line along the x -axis.

Steps 6/7: When the potentiometer is set to maximum, the output is in positive saturation. As the potentiometer is varied (less resistance), the output waveform suddenly becomes a 50% duty cycle. Reducing the resistance more causes the output waveform to shift to the left.



Plot 13-4 Schmitt trigger waveform

Step 8: The potentiometer varies the hysteresis; the upper and lower thresholds move apart as resistance is increased.



Plot 13-5 Schmitt trigger transfer curve

Questions: Part 1

1. The threshold voltage is a dc quantity that adds to or subtracts from the input plotted along the x -axis of the transfer curve. Varying the threshold shifts the vertical line along the x -axis.
2. The offset control on the generator does *not* affect the threshold for the circuit but it adds a dc component to the input voltage. As a result, the duty cycle of the output waveform can be changed by the offset control. (Note: it is useful to show this with the transfer curve – it varies only the endpoints of the transfer curve, not the vertical line).
3. The transfer curve is a characteristic that is independent of the input. On an analog oscilloscope, the transfer curve will show various intensities that depend

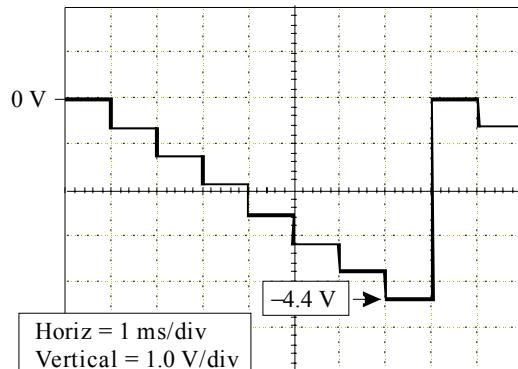
on the input because the waveform determines the time the beam spends in graphing any given point on the curve.

4. A comparator has the same threshold for rising or falling signals; a Schmitt trigger has a different threshold for each.

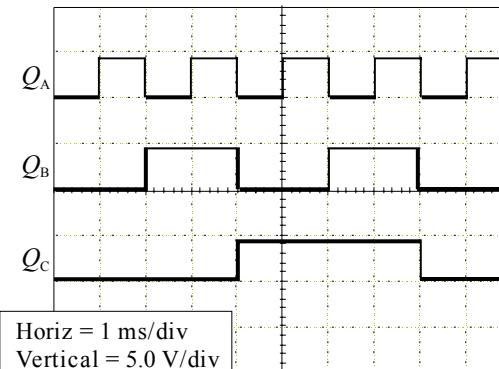
Part 2: The Summing Amplifier

Table 13-1

Resistor	Listed Value	Measured Value
R_A	20 kΩ	20.0 kΩ
R_B	10 kΩ	10.1 kΩ
R_C	5.1 kΩ	5.08 kΩ
R_f	3.9 kΩ	3.93 kΩ



Plot 13-6

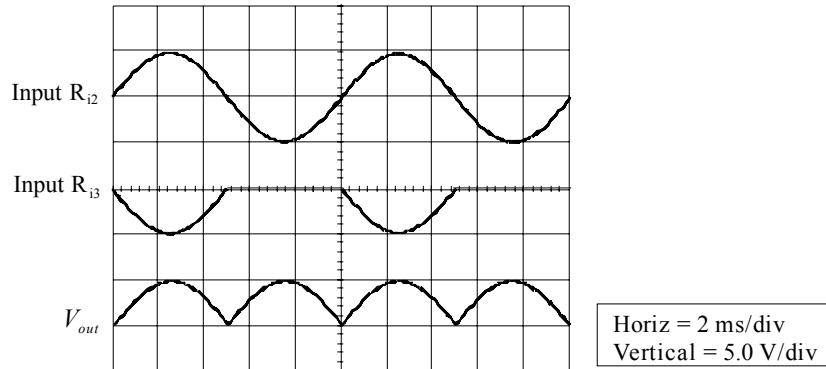


Plot 13-7

Step 4: The output waveform is the positive portion of the input waveform with no offset. The small jump on the output is due to slew rate limitation as the output moves from negative saturation.

Step 5: The output is a negative half-wave rectified signal. With D_1 removed, the output appears to be a full-wave rectified signal with overshoot on the back side of every other pulse. This overshoot is frequency dependent, and disappears at a few hundred hertz.

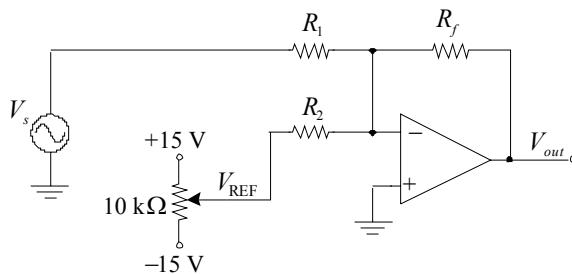
Step 6: The output is a positive full-wave rectified signal. The signals are shown in Plot 13-8.



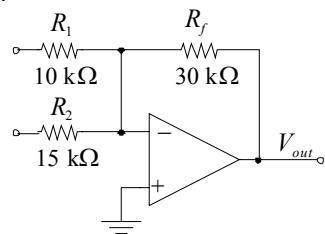
Plot 13-8

Questions: Part 2

1. (a) To approximate the column values in the binary system (1,2,4, etc.), the three inputs are amplified in proportion to the column values they represent. (This is in effect a three bit D/A converter).
 - (b) Add an inverting amplifier to the output.
2. Gains are -0.195 , -0.39 , and -0.76 . The output is $4.5 \text{ V} \times (-0.195 - 0.39 - 0.76) = -6.05 \text{ V}$
3. One of the inputs to the summing amplifier is a variable dc as shown:



4. The inverted half-wave rectified signal is amplified twice as much as the sine wave input in order to cancel the negative excursion of the sine wave and add a positive-going signal to it.
5. The resistors shown are representative and can have other values; the ratios are important.

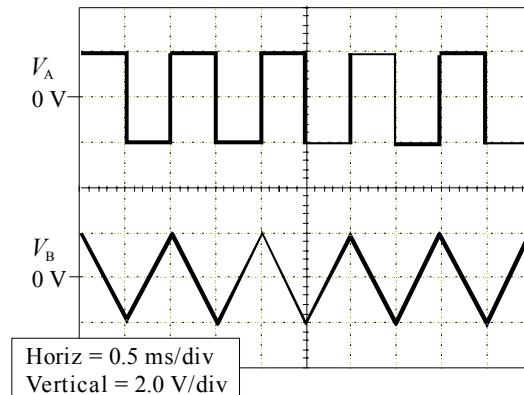


Part 3: The Integrator and Differentiator

Table 13-2

V_{OUT}	V_{REF}	
Red ON	Green ON	Threshold
+2.1 V	-2.0 V	0.001 V

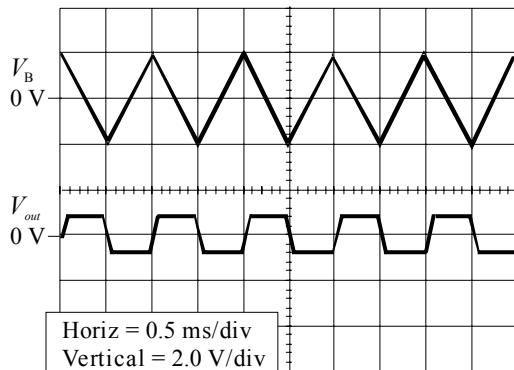
Step 3: Duty cycle changes as R_3 is varied; output B slope follows.



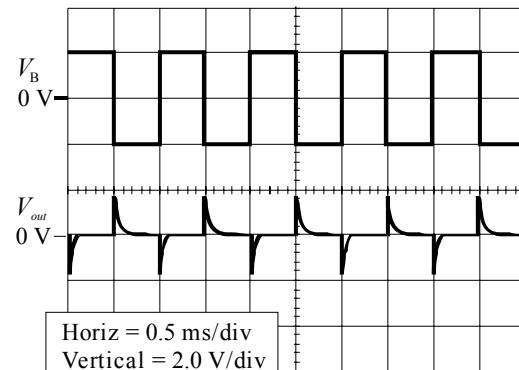
Plot 13-9

Table 13-3

Trouble	Symptoms
No Negative Power Supply	Red LED on; B goes to positive saturation
Red LED open	A = -2 V to + sat; B = - sat w/small deviation
C_1 open	B goes to a square wave (+ and - saturation)
R_5 open	No change in A; B goes toward - saturation.



Plot 13-10



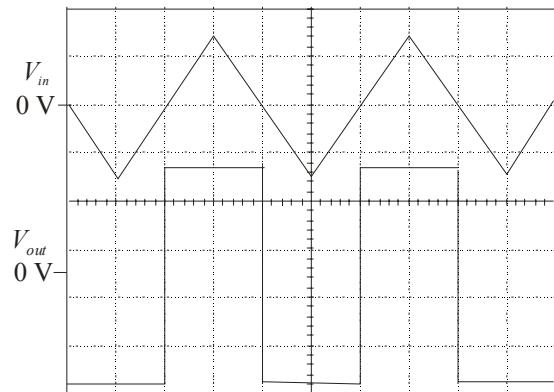
Plot 13-11

Questions: Part 3

1. $V_{REF(MIN)} = -714 \text{ mV}$ $V_{REF(MAX)} = +714 \text{ mV}$
2. The LEDs drop a maximum of about 2.0 V at the op-amp's current limit.
3. (a) R_4 establishes a virtual ground at the inverting input through negative feedback and stabilizes the operating point. Without it, the output will saturate.
(b) The output went to negative saturation.
4. Differentiator circuit

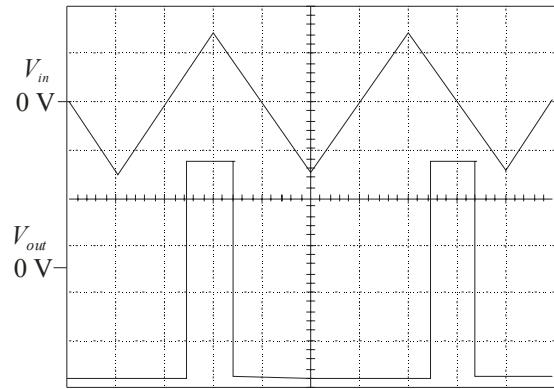
Experiment 13-B Programmable Analog Design

Part 1: The Comparator and Comparator with Hysteresis



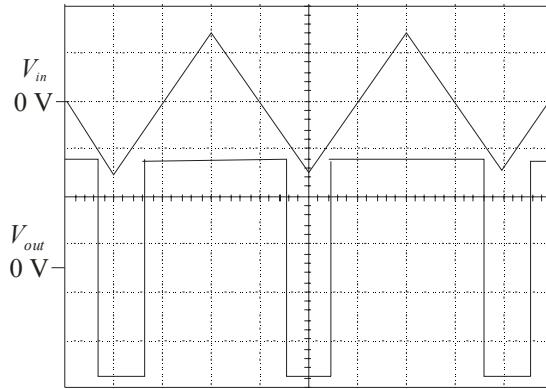
Vertical = 2.0 V/div (both channels)
Horizontal = 5.0 ms/div

Plot 13-12



Vertical = 2.0 V/div (both channels)
Horizontal = 5.0 ms/div

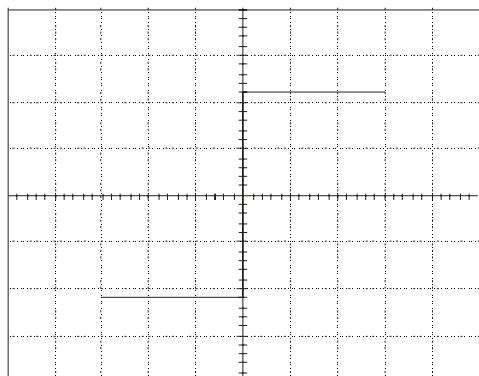
Plot 13-13



Vertical = 2.0 V/div (both channels)
Horizontal = 5.0 ms/div

Plot 13-14

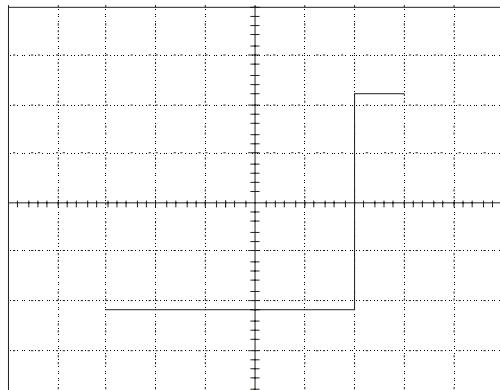
Step 8: As the offset voltage is increased, the output positive time increases and the negative time decreases; when the offset voltage is decreased, the opposite occurs.



x-axis = 1.0 V/div y-axis = 2.0 V/div

Plot 13-15 Comparator transfer curve.

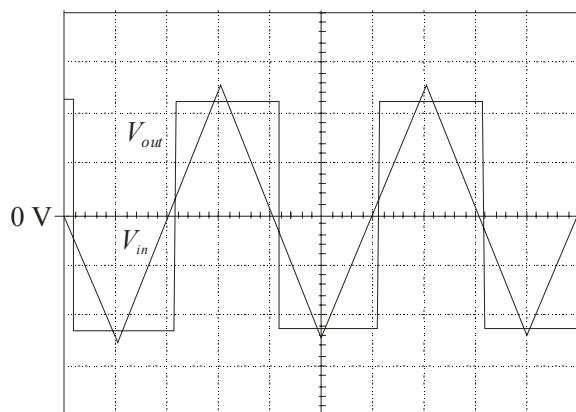
Step 10: The vertical transition on the transfer curve moves to the right to approximately 2.0 V on the x -axis. (For reference, the plot is shown here, but not required in the experiment. Note that the 2.0 V result is because the internal differential signal is $\frac{1}{2}$ the external single-ended signal.)



x -axis = 1.0 V/div y -axis = 2.0 V/div

Step 10 result

Step 11: The end points on the transfer curve move left or right, following the offset control.

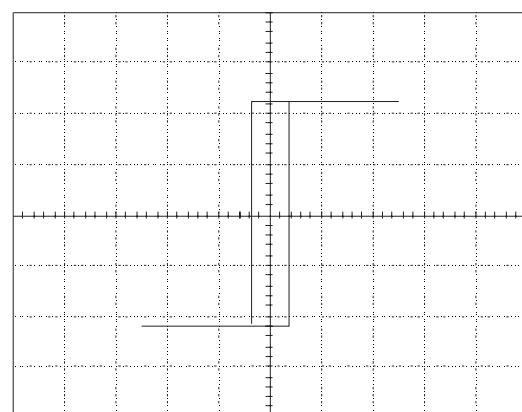


Channel 1 (V_{in}): Vertical = 200 mV/div

Channel 2 (V_{out}): Vertical = 2.0 V/div

Horizontal = 5.0 ms/div

Plot 13-16 Comparator with hysteresis.



x -axis = 200 mV/div y -axis = 2.0 V/div

persist ON

Plot 13-17 Schmitt trigger transfer curve.

Questions: Part 1

Instructor note: The questions in Part 1 are stand alone, i.e. they do not specifically apply to the experiments completed in the laboratory work for this section.

1. In a single-ended signal, the signal is referenced to a static value, which is typically ground. In a differential signal, the signal is referenced to another signal.
2. Hysteresis is a characteristic of a circuit in which the trigger level (or switching point) for a rising signal is different than that of a falling signal.
3. Hysteresis helps reduce the susceptibility to noise for a comparator.

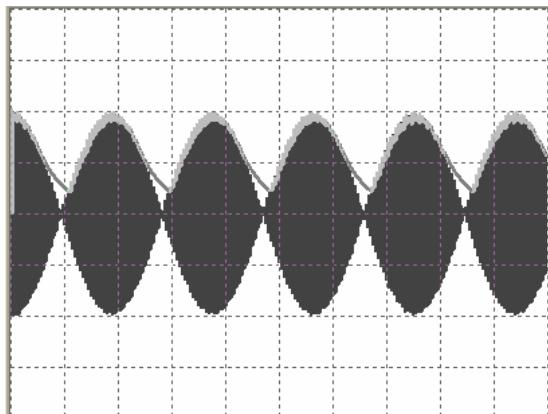
- In a triangle wave the change of voltage over time is linear; in a sine wave the change in voltage over time is not linear. The transfer curve would look similar, but with a sine wave, the ends of the transfer curve would be brighter and the center dimmer on an analog scope display.

Part 2: The Summing Amplifier and Peak Detector

Step 5: The simulation shows the sum of the two signals. The sum shows a pulsating appearance; the envelope represents the difference in the two frequencies.

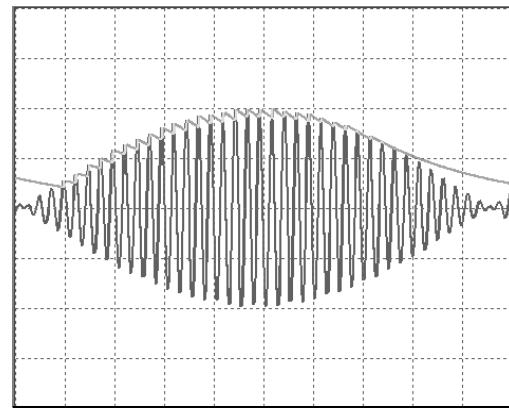
Step 7: An audio tone is heard in the speaker that represents the difference frequency between the two oscillators. The peak detector is necessary to hear the tone.

Instructor note: The simulated and measured waveforms are virtually identical. The simulated waveform is shown in Plot 13-18 for reference; the light gray signal on top is from the peak detector. A. A magnified view of the signals is shown in the unnumbered plot. (Note the decay time for the peak detector.)



Both channels: 1 V/div, 1 ms/div

Plot 13-18 Summing amplifier and peak detector outputs.



Both channels: 1 V/div, 200 µs/div

Magnified view of summing amplifier and peak detector outputs

Step 8: The sound heard will be the difference frequency between the oscillators.

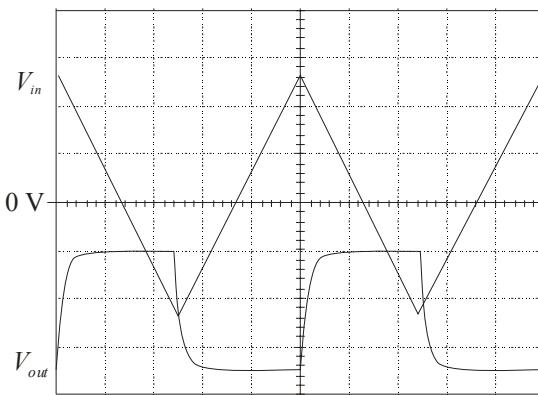
Step 9: There is no sound when the peak detector is removed.

Questions: Part 2

- The decay time constant controls how fast the peak detector responds to changes. A smaller time constant would allow the peak signal to show as a group of spikes that follow the wave instead of the smooth envelope that was observed.
- The peak detector converts the envelope to a frequency that can be heard. Without it, there is no audible frequency in the signal.
- The peak detector follows the envelope which represents a “beat” or difference frequency between the oscillators.

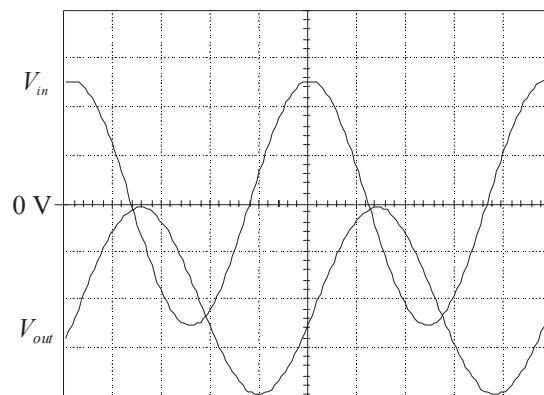
Part 3: The Differentiator

Instructor note: The ASP outputs are not precisely differential, meaning that there is a slight DC offset between the two parts of each output. The output buffer, a difference amplifier, exacerbates this by subtracting the two signals. The amount of dc offset varies with different PAM units. In an actual application a DC blocking capacitor to remove the offset is recommended; students can use AC coupling on the scope to see true differentiation.



Both channels = 1.0 V/div, ground at center
Horizontal: 10 μ s/div (see note about dc offset)

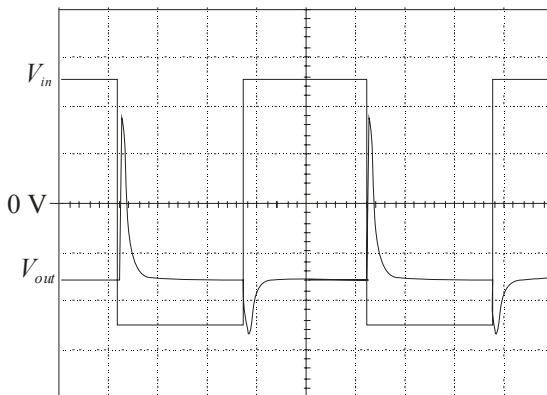
Plot 13-19 Differential output of a triangle wave.



Both channels = 1.0 V/div, ground at center
Horizontal: 10 μ s/div

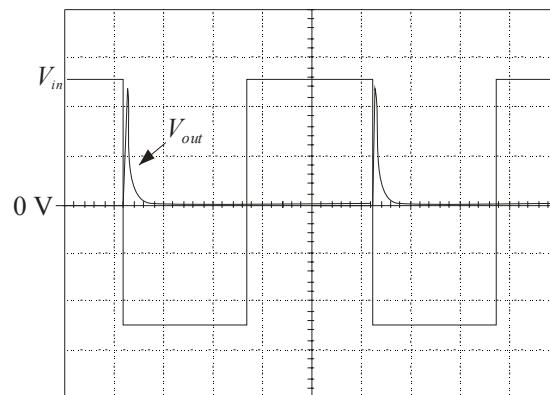
Plot 13-20 Differential output of a sine wave.

Step 4: The output waveform is not affected by small changes in the dc offset.



Input = 1.0 V/div, output = 2.0 V/div
Horizontal: 10 μ s/div

Plot 13-21 Differential output of a square wave.



Input = 1.0 V/div, output = 2.0 V/div
Horizontal: 10 μ s/div
Step 7 result with a rectifier filter.

Step 7: The output has only positive excursions from 0 to 4.3 V, as shown in the unnumbered plot above.

Questions: Part 3

1. The dc level had no effect because the rate of change of dc (a constant) is zero.
2. For a constant amplitude input, changing the frequency changes the slope. A higher frequency will have a larger slope and hence a larger amplitude derivative.
3. The derivative of a sine wave has the same shape but lags the input by 90°.

Experiment 14-A Special-Purpose Op-Amp Circuits

Part 1: The Instrumentation Amplifier

Table 14-1

Resistor	Listed Value	Measured Value
R_1	10 kΩ	9.87 kΩ
R_2	10 kΩ	9.87 kΩ
R_G	470 Ω	463 Ω
R_3	10 kΩ	9.91 kΩ
R_4	10 kΩ	9.87 kΩ
R_5	10 kΩ	9.88 kΩ
R_6	8.2 kΩ	8.10 kΩ
R_8	100 kΩ	101 kΩ
R_9	100 kΩ	100 kΩ

Table 14-3

Parameter	Measured Value
Oscillator frequency	682 Hz
$V_{out(pp)}$ from oscillator	7.6 V_{pp} [*]
$V_{out(pp)}$ from IA	170 mV_{pp} [*]

*Output amplitude depends on battery voltage

Table 14-2

Step	Parameter	Computed Value	Measured Value
3	Differential input voltage, $V_{in(d)}$	300 mV _{pp}	300 mV_{pp}
	Differential gain, $A_{v(d)}$	43.5	43.0
	Differential output Voltage, $V_{out(d)}$	13.1 V_{pp}	13.0 V_{pp}
4	Common-mode input voltage, $V_{in(cm)}$	10 V _{pp}	10.0 V_{pp}
	Common-mode gain, $A_{v(cm)}$		0.008
	Common-mode output voltage, $V_{out(cm)}$		80 mV_{pp}
5	CMRR'		74.6 dB

Step 8: The measured differential signal was a 170 mV, 682 Hz square wave (from the 555 timer). It was amplified by the IA but the 10 V_{pp} common-mode signal was almost completely eliminated from the output as viewed on an oscilloscope.

Questions: Part 1

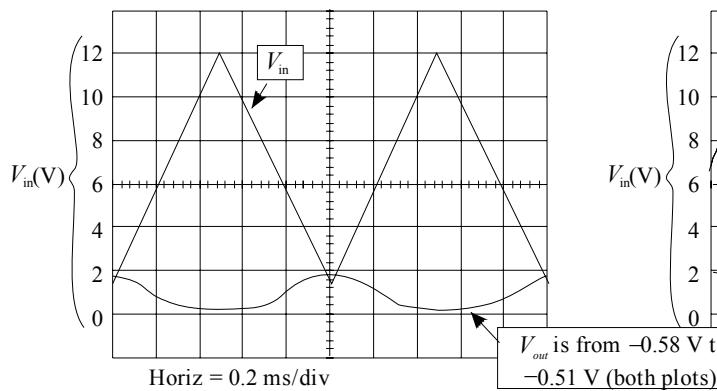
- For a CMRR of 130 dB, the ratio of $A_{v(d)}$ to $A_{v(cm)}$ is 3.16×10^6 . This implies that the common-mode gain for the experiment is $43/3.16 \times 10^6 = 13.6 \times 10^{-6}$. The expected output signal is $10 \text{ V}_{\text{pp}} \times 13.6 \times 10^{-6} = 136 \mu\text{V}_{\text{pp}}$.
- The oscillator signal was a differential-mode signal but the signal generator was a common-mode signal.
- The reference ground for the 555 timer needs to be isolated from the ground for the IA. The simplest way to do this is power it from an independent source.

4. The IA has CMRR, both inputs to the IA are balanced, and it has high input impedance. (The input impedance was $100 \text{ k}\Omega$, but it can be much higher).

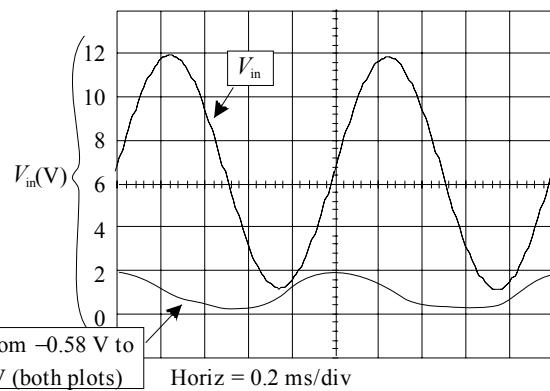
Part 2: The Log Amplifier and Antilog Amplifier

Table 14-4

Resistor	Listed Value	Measured Value
R_1	$100 \text{ k}\Omega$	$100 \text{ k}\Omega$
R_2	$100 \text{ k}\Omega$	$100 \text{ k}\Omega$



Plot 14-1



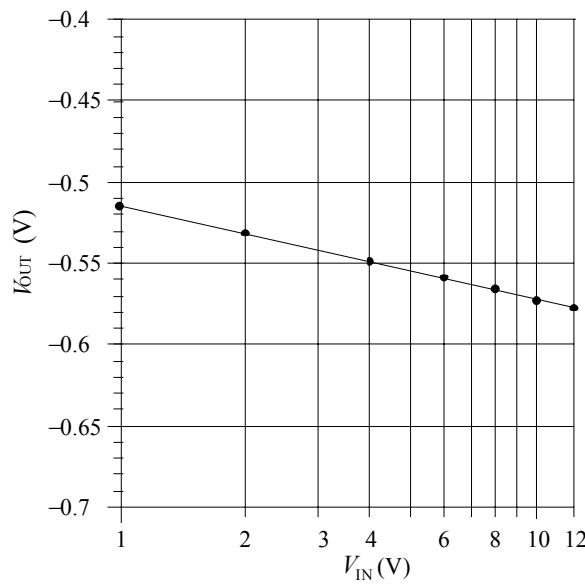
Plot 14-2

Step 5: The output from the antilog amp matches the input to the log amp, as it should.

Step 6: When the log amp is warmed (by touch), the output goes down; when the antilog amp is warmed (by touch), the output increases.

Table 14-5 Data for Log Amp

V_{IN}	V_{OUT}
+1.0 V	-0.513 V
+2.0 V	-0.532 V
+4.0 V	-0.548 V
+6.0 V	-0.559 V
+8.0 V	-0.566 V
+10.0 V	-0.572 V
+12.0 V	-0.577 V



Plot 14-3

Questions: Part 2

1. Advantages of integrated circuit IA's include
 - (a) less temperature sensitivity
 - (b) greater dynamic range (5 or 6 decades)
 - (c) gain control
 - (d) single package design
 - (e) high accuracy and linearity
 - (f) very low bias current (max of 5 pA in the LOG100)
2. The antilog amp transfer curve is also a straight line plotted on semilog paper; however, the input voltage should be plotted on the linear scale and the output voltage is plotted on the log scale.
3. With the same resistor in the log and antilog circuit, the original signal applied to the log amp is restored by the antilog amp. If the antilog amp has a larger resistor, its transfer curve is shifted up, resulting in more gain.
4. (a) Multiplication of the inputs (and multiplying by -1 because of the three inversions). (Note the summing amplifier added the logs; the antilog amplifier returns the product of the original numbers but with opposite sign).
(b) -6.0 V

Experiment 14-B Programmable Analog Design

Part 1: Single-Ended Signals into a Differential Signal Circuit

Step 3: (a) $1.00\text{ V}_{\text{pp}}$ (b) $0.50\text{ V}_{\text{pp}}$

Step 4: Typical values for $\text{OUT1} = 0.445\text{ V}_{\text{pp}}$ to $0.468\text{ V}_{\text{pp}}$. (Answers to these steps depend on the particular PAM.)

Step 5: Typical values for $\text{OUT2} = 0.455\text{ V}_{\text{pp}}$ to $0.494\text{ V}_{\text{pp}}$.

Step 6: Typical values for gain settings to equalize outputs = 0.970 to 978.

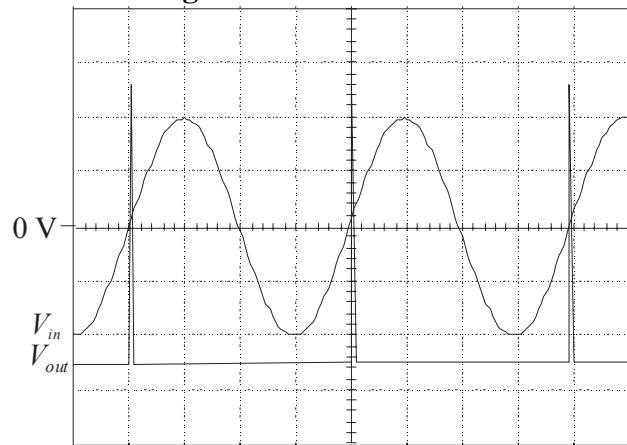
Step 7: Some trial and error may be required, because the ASP cannot set exact gains. The ASP outputs of $0.445\text{ V}_{\text{pp}}$ need to be multiplied by 2.25 to achieve 1.0 V_{pp} , but a small adjustment was needed for one of the PAMs tested; the final gain setting for this PAM was 2.16.

Questions: Part 1

1. This reduces any errors caused by differences in the equipment or problems with calibration.
2. Any unshielded wire will capture nearby signals.
3. Ground paths are sometimes called “returns”. If several signals use the aluminum structure for the return path, signals can combine, increasing the noise for any given signal. In short, this is a bad idea.
4. Small differences in the actual gain are generally due to component variations.

Part 2: Instrumentation CAMs

Zero-crossing Detector



Ch 1 (V_{in}): Vertical 500 mV/div

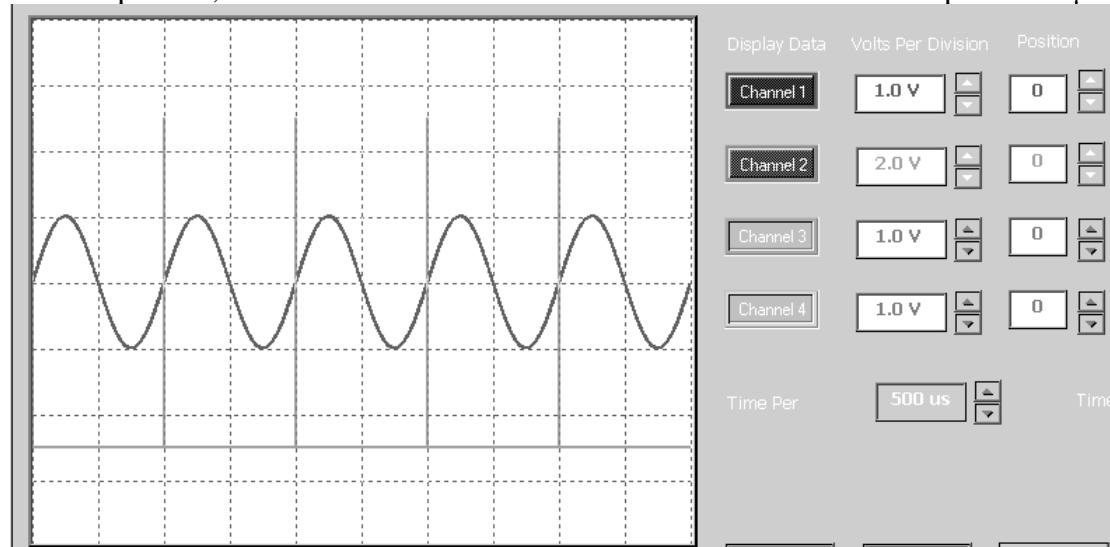
Ch 2 (V_{out}): Vertical 2.0 V/div

Horizontal: 250 μ s/div

Plot 14-4 Sine wave input and zero-crossing detector output.

The output is at a level of -5 V and pulses to $+5.0\text{ V}$ when the zero crossing occurs.

For comparison, the simulation data is shown. The simulation shows the pulse is 2 μ s wide.



Step 4: The delay is approximately 5 μ s when the output is positive, which is significant at 50 kHz, representing 25% of the period. It is positive for about 2 μ s, in good agreement with the simulation.

Step 5: The zero crossing pulse is closer to the actual zero crossing as the frequency is increased.

Peak Detector

Step 8: The signal at OUT1 is a half-wave signal that is $\frac{1}{2}$ of the input peak. The signal at OUT2 is a full-wave signal that is also $\frac{1}{2}$ of the input peak.

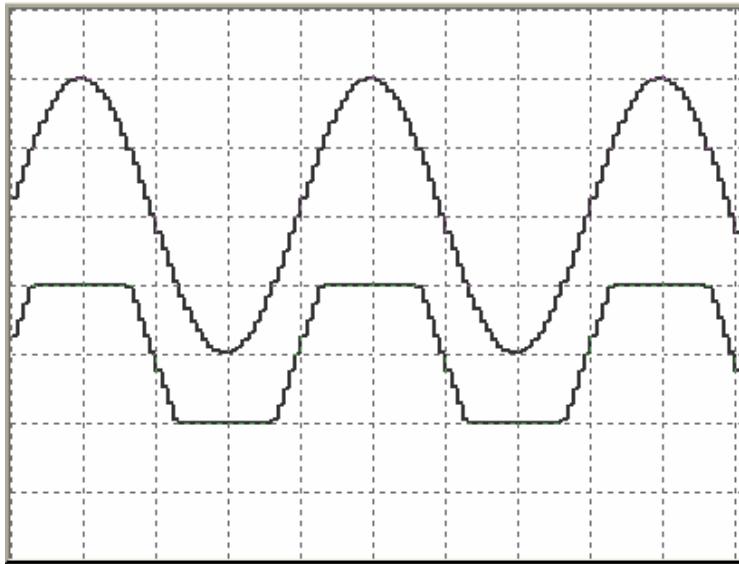
Step 9: The half-wave signal returns to the base line between peaks, but the full-wave signal does not.

Step 10: Neither the half-wave nor full-wave signal return to the baseline between peaks. The half-wave signal drops about 50%; the full-wave drops about 25%.

Step 11: The signals approach the dc level of the peak as the frequency is raised.

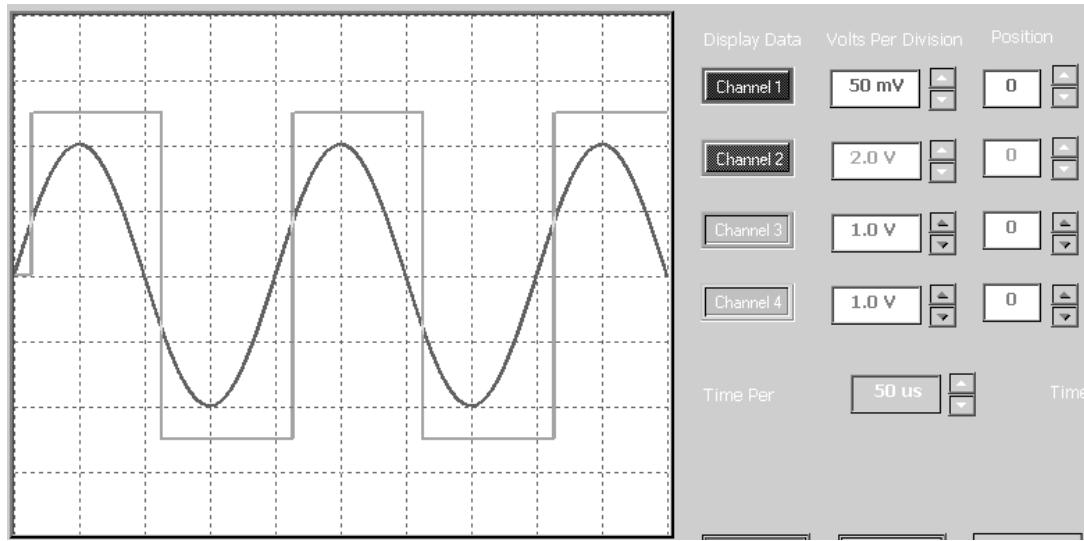
Gain-Limiter

Steps 13 and 14: The simulated waveform and the measured waveform are virtually identical. The waveforms shown below are from the simulation, with the top waveform offset by +10 (1 div) and the bottom waveform offset by -10.

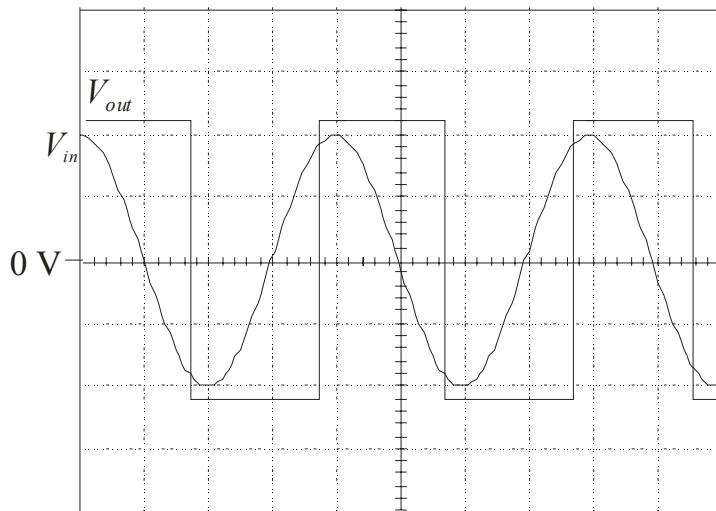


Plot 14-5 Simulated limiter waveform. (Plot 14-6 will be the same.)

Comparator Application – Tank Experiment



Plot 14-7 Simulated comparator waveform. The simulator waveform shows the trigger points at +40 mV and at -40 mV.



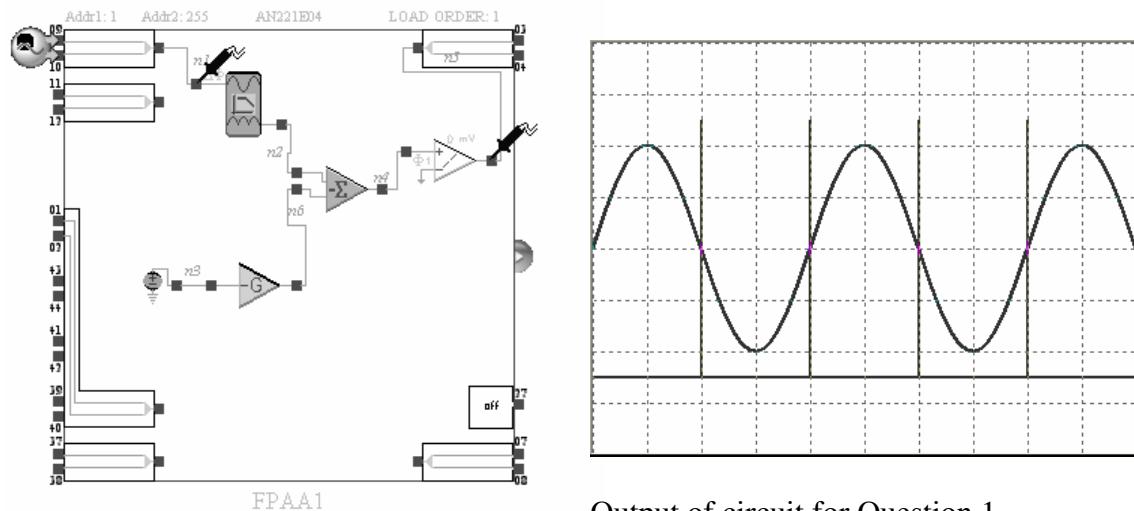
Plot 14-8 Actual comparator waveform.

Step 17: The trigger points on the actual waveform are at +80 mV and -80 mV.

Questions: Part 2

- (a) One method is to rectify the input signal and combine it with a small negative dc voltage to offset the output and force it to cross 0 V. The rectified signal is twice the frequency of the input, which is then passed on to a zero-crossing detector. The configuration for this solution is shown. Note that the small dc voltage is generated with the *Voltage CAM* set to +3 V and a *GainInv* stage with a gain set to 0.02.

Instructor note: You can also generate a small dc voltage using the *PeriodicWave* CAM by cycling through a constant voltage. This CAM is discussed in Experiment 16-B, part 3.



Circuit for Question 1

- (b) This circuit could be used to measure the time an arbitrary wave is above 0 V.
- When the time constant is short, the peak detector tends to follow the positive half-cycle if the input.
- (a) A long time constant causes the change from the peak value to decay slowly, acting as a low-pass filter.
(b) A higher frequency causes the output to reset to the peak value sooner than a low frequency and tends to smooth the output as a result.
- Using a high-gain amplifier causes the signal to rapidly reach the limiter cutoff values, so the output signal looks like a square wave.
- Without hysteresis, the decision point for turning the valve on or off could be crossed several times because of noise in the system. Thus, the valve would tend to chatter.

Experiment 15-A Active Filters

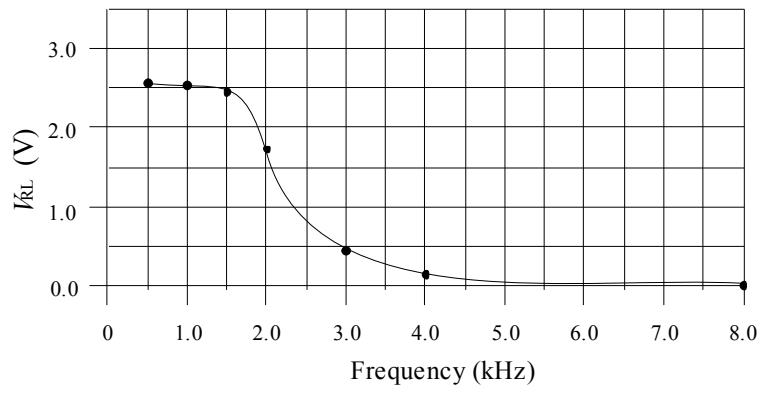
Part 1: Four-pole Low-Pass Filter

Table 15-2

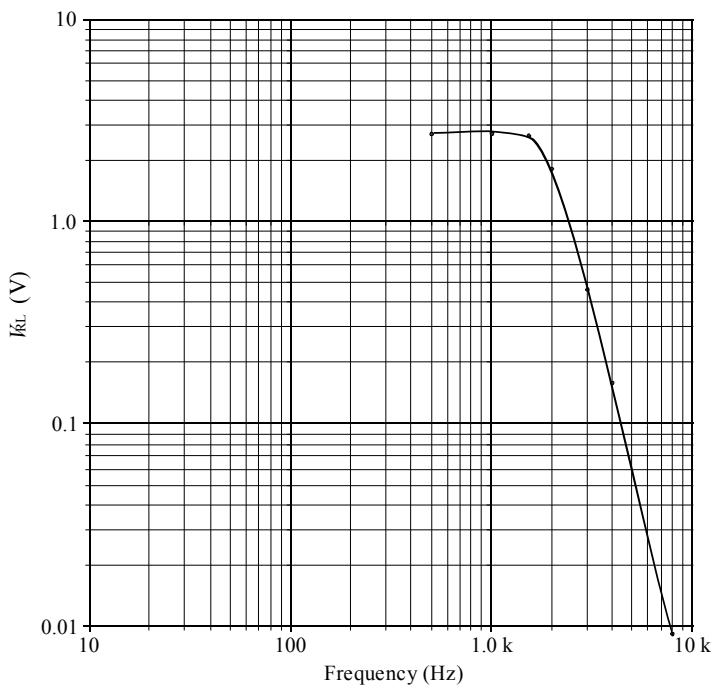
Component	Listed Value	Measured Values			
		A1	B1	A2	B2
$R_{A1}, R_{B1}, R_{A2}, R_{B2}$	8.2 k Ω	8.17 kΩ	8.37 kΩ	8.00 kΩ	8.22 kΩ
$C_{A1}, C_{B1}, C_{A2}, C_{B2}$	0.01 μF	0.01 μF	0.01 μF	0.01 μF	0.01 μF
R_{i1}	10 k Ω	10.1 kΩ			
R_{f1}	1.5 k Ω	1.5 kΩ			
R_{i2}	22 k Ω	21.9 kΩ			
R_{f2}	27 k Ω	26.8 kΩ			

Table 15-3

Frequency	V_{RL}
500 Hz	2.55 V
1000 Hz	2.52 V
1500 Hz	2.45 V
2000 Hz	1.72 V
3000 Hz	0.45 V
4000 Hz	0.14 V
8000 Hz	0.009 V



Plot 15-1



Plot 15-2

Questions: Part 1

1. (a) The cutoff frequency is approximately 2.0 kHz.
 (b) Answers vary; for the tested circuit, the average R is $8.19 \text{ k}\Omega$, the average C is $0.010 \mu\text{F}$. The computed cutoff frequency from these values is 1.94 kHz.
2. (a) The measured voltage gain in the band pass is **2.55**.
 (b) The desired value for a four-pole filter (from Table 15-1) is **2.574** (This is the product of the two gains: $1.152 \times 2.235 = 2.574$).
3. The output is reduced by a factor of 10^4 (-80 dB for this filter), which is approximately $250 \mu\text{V}$.
4. The constructed filter is very close to the theoretical roll-off.
5. (a) The gain computed from the actual resistors in the first stage is 1.149.
 (b) The gain computed from the actual resistors in the second stage is 2.227. The product of these gains results in an overall gain of **2.559** (compare to question 2).

Part 2: State-Variable Filter

Table 15-4

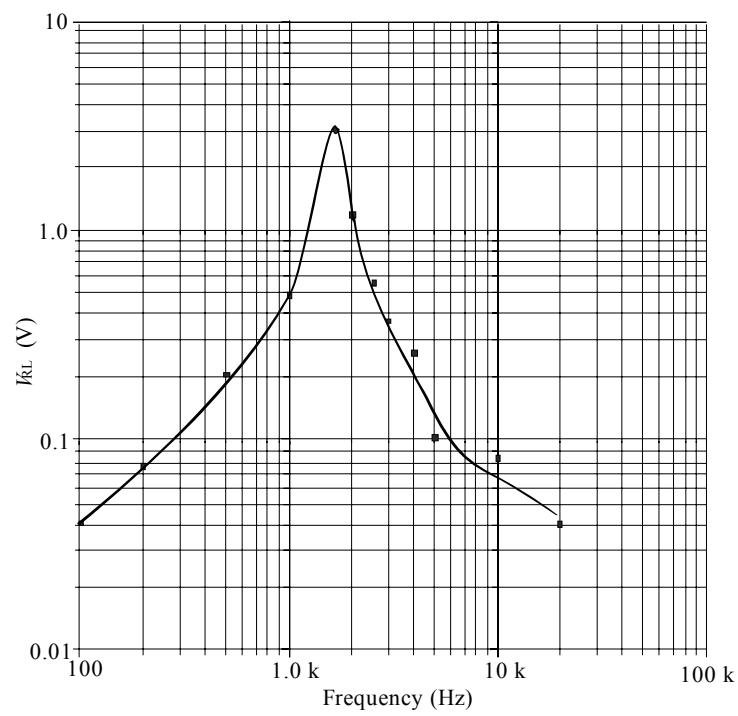
Component	Listed Value	Measured Value
R_1	$10 \text{ k}\Omega$	$10.0 \text{ k}\Omega$
R_2	$10 \text{ k}\Omega$	$10.1 \text{ k}\Omega$
R_3	$10 \text{ k}\Omega$	$9.91 \text{ k}\Omega$
R_4	$1.0 \text{ k}\Omega$	$1.01 \text{ k}\Omega$
R_5	$100 \text{ k}\Omega$	$101 \text{ k}\Omega$
R_6	$1.0 \text{ k}\Omega$	$1.00 \text{ k}\Omega$
R_7	$1.0 \text{ k}\Omega$	$1.02 \text{ k}\Omega$
C_1	$0.1 \mu\text{F}$	$0.0979 \mu\text{F}$
C_2	$0.1 \mu\text{F}$	$0.1006 \mu\text{F}$

Table 15-5

Quantity	Computed	Measured
Center frequency, $f_0 =$	1.59 kHz	1.62 kHz
$V_{pp(\text{center})} =$		13.3 V_{pp}
Upper cutoff, $f_{cu} =$		1.649 kHz
Lower cutoff, $f_{cl} =$		1.60 kHz
Bandwidth, $BW =$	0.047 kHz	0.049 kHz
$Q =$	33.7	32.4

Table 15-6

Frequency	Output voltage $V_{out(pp)}$
100 Hz	40 mV_{pp}
200 Hz	75 mV_{pp}
500 Hz	200 mV_{pp}
1.0 kHz	0.48 V_{pp}
1.5 kHz	3.0 V_{pp}
2.0 kHz	1.14 V_{pp}
2.5 kHz	0.54 V_{pp}
3.0 kHz	0.37 V_{pp}
4.0 kHz	0.24 V_{pp}
5.0 kHz	180 mV_{pp}
10 kHz	82 mV_{pp}
20 kHz	41 mV_{pp}

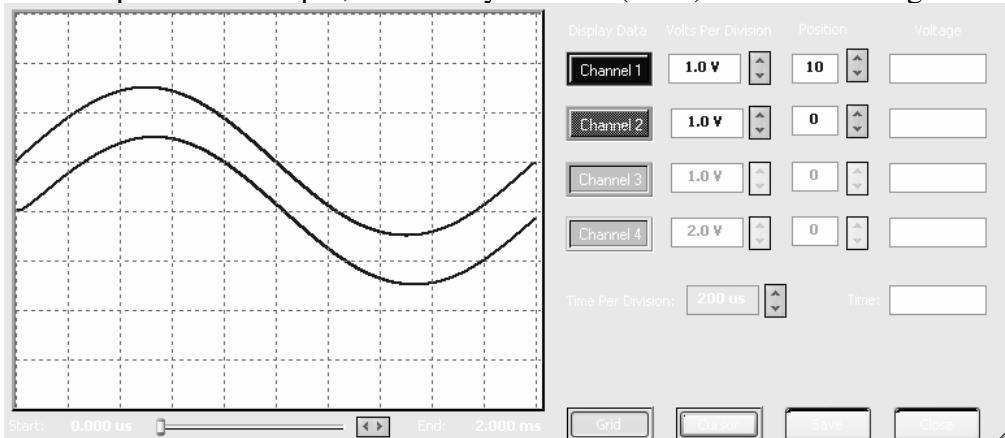
**Plot 15-3****Questions: Part 2**

1. If the Q of the circuit is made smaller, the output can be increased.
2. (a) Advantages: high Q , easily tuned, and both high- and low-pass outputs are available.
(b) The change of R_6 to 100 k Ω , as noted in step 6, will eliminate the peaking, but greatly decreases the Q of the circuit so it affects the response of the band-pass filter.
3. (a) To double the frequency, reduce R_4 and R_7 or reduce C_1 and C_2 by half.
(b) To lower the Q , increase the value of R_6 .
4. (a) A band reject or notch filter.
(b) Rejection of an interfering noise frequency.

Experiment 15-B Programmable Analog Design

Part 1: Single-Pole Low-Pass Filter using the Bilinear Filter CAM

The simulation scope is shown. The two signals are nearly identical, so Channel 1, which represents the input, is offset by 10 units (1 div) to show both signals.



Plot 15-4 Input and output waveforms from a single-pole low-pass filter.

Table 15-7 Simulated input and output voltage and time.

f	T	Δt	Phase shift	Input Peak Voltage, V_p	Output Peak Voltage, V_p
500 Hz	2000 μ s	32 μs	5.8°	1.50	1.49
2.5 kHz	400 μ s	29 μs	26.1°	1.50	1.34
5.0 kHz	200 μ s	25 μs	45.0°	1.50	1.06
10 kHz	100 μ s	18 μs	64.8°	1.50	0.67
50 kHz	20 μ s	5.0 μs	90.0°	1.50	0.15

Table 15-8 Measured input and output voltage and time.

f	T	Δt	Phase shift	Input Peak Voltage, V_p	Output Peak Voltage, V_p
500 Hz	2000 μ s	38.0 μs	6.8°	3.02	1.67
2.5 kHz	400 μ s	30.3 μs	27.3°	3.02	1.47
5.0 kHz	200 μ s	25.6 μs	46.1°	3.02	1.18
10 kHz	100 μ s	18.5 μs	66.4°	3.02	0.750
50 kHz	20 μ s	5.45 μs	98.1°	3.02	0.17

Step 9: The shape of the responses is nearly identical but the measured outputs are slightly larger than the simulation. The attenuation in the PAM input buffer required the larger specified input signal, and may account for the differences.

Questions: Part 1

- At the zero crossing, the signals are changing at the maximum rate, so it is easier to read time precisely. Also, the signals are not as sensitive to alignment on the scope.

2. Yes. In general, low-pass filters are constructed as RC networks with the output taken across C , causing a phase lag. With RL networks, the output is taken across R , also producing a phase lag.
3. The response of the simulation is nearly identical to theory for the points at $0.1f_c$, f_c , and $10f_c$. The measured responses are higher at all frequencies. This may be accounted for by the PAM input buffer amplifier.

Part 2: Single-Pole Low-Pass Filter Using AnadigmFilter

Step 9: Both filters have identical responses at all frequencies tested.

Table 15-9 Simulated input and output voltage for a five-pole low-pass filter.

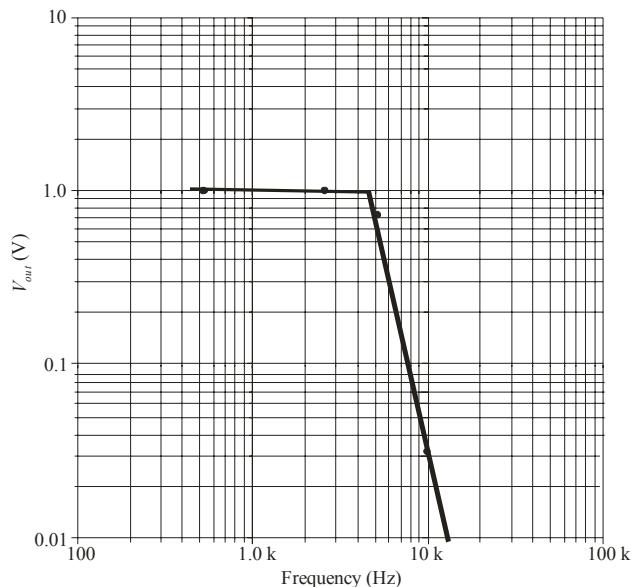
f	Input Peak Voltage, V_p	Output Peak Voltage, V_p
500 Hz	1.00	1.00
2.5 kHz	1.00	1.00
5.0 kHz	1.00	0.71
10 kHz	1.00	0.0316
50 kHz	1.00	0.00

Step 14: At the cutoff frequency of 5 kHz, the measured output is 0.73 V_p (1.46 V_{pp}).

Step 15: At 10 kHz, the measured output is 0.377 V_p (73.5 mV_{pp}).

Questions: Part 2

1. The filter has a very sharp roll-off. At one decade, the predicted output is too small to measure (it should be approximately 10 μ V).
2. (a) See Plot 15-5.
 (b) The frequency as read on the plot for $V_{out} = 10$ mV is approximately 13 kHz. This agrees with the calculated value for a 5 pole filter of 13.3 kHz.



Plot 15-5

Experiment 16-A Oscillators

Part 1: The Wien-Bridge Oscillator

Table 16-1

Component	Listed Value	Measured Value
R_1	10 kΩ	10 kΩ
R_2	10 kΩ	10 kΩ
C_1	0.01 μF	0.01 μF
C_2	0.01 μF	0.01 μF

Table 16-2

	Computed	Measured
f_r	1.59 kHz	1.46 kHz

Step 2: The output saturates on both positive and negative peaks. Freeze spray causes circuit to change and even stop oscillating. Circuit is temperature sensitive.

Table 16-3

$V_{out(pp)}$ (pin 6)	$V_{(+)(pp)}$ (pin 3)	$V_{(-)(pp)}$ (pin 2)	V_G
4.0 V_{pp}	1.5 V_{pp}	1.5 V_{pp}	-1.0 V_{dc}

Step 5: The phase shift is 0°.

Step 6: Very little effect with freeze spray. The output is much more stable.

Table 16-4

$V_{out(pp)}$ (pin 6)	$V_{(+)(pp)}$ (pin 3)	$V_{(-)(pp)}$ (pin 2)	V_G
4.6 V_{pp}	1.56 V_{pp}	1.56 V_{pp}	-1.29 V_{dc}

Questions: Part 1

1. (a) Feedback fraction is very close to 1/3.
 (b) The measured result agrees with theory.
2. The extra diode causes C_3 to charge for a smaller part of the cycle decreasing V_G . This causes the FET resistance to drop (temporarily). The op-amp's gain (and output voltage) increase until the charge on C_3 is returned to the proper level for a stable output.
3. The diode causes the negative half-cycle of the output to charge the capacitor and bias the FET with a negative bias voltage.
4. The frequency is halved to 790 Hz.

Part 2: The Hartley and Colpitts Oscillators

Table 16-5

Resistor	Listed Value	Measured Value
R_1	10 k Ω	9.98 kΩ
R_2	3.3 k Ω	3.31 kΩ
R_{E1}	50 Ω *	50 Ω
R_{E2}	1.0 k Ω	1.01 kΩ
R_C	2.7 k Ω	2.69 kΩ

* Set to the center position

Table 16-6

DC Parameter	Computed Value	Measured Value
V_B	3.01 V	2.97 V
V_E	2.31 V	2.32 V
I_E	2.18 mA	
V_C	6.11 V	6.07 V

Table 16-7

AC Parameter	Computed Value	Measured Value
V_b	100 mV_{pp}	100 mV_{pp}
r_e'	61.5 Ω	
A_v	43.9	39.0
V_c	4.39 V_{pp}	3.9 V_{pp}

Table 16-8

Hartley Oscillator	Computed Value	Measured Value
frequency	969 kHz	961 kHz
amplitude		5.5 V_{pp}

Table 16-9

Colpitts Oscillator	Computed Value	Measured Value
frequency	1.06 MHz	1.04 MHz
amplitude		7.4 V_{pp}

Step 6: Both the amplitude and the frequency of the oscillator decreased.

Questions: Part 2

1. The amount of feedback decreased.
2. The two conditions are positive feedback and a loop gain equal or greater than 1.
3. In the Hartley oscillator, an inductor is used to provide positive feedback from the tank circuit. In a Colpitts oscillator, a capacitor is used to supply positive feedback.

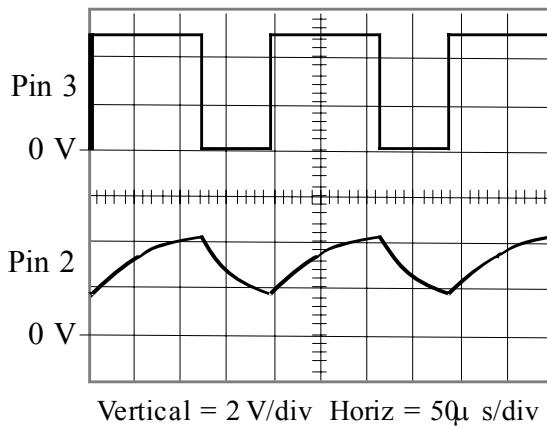
Part 3: The 555 Timer

Table 16-10

Component	Listed Value	Measured Value
R_1	8.2 kΩ	8.14 kΩ
R_2	10 kΩ	9.91 kΩ
C_{ext}	0.01 μF	10.3 nF

Table 16-11

Component	Computed Value	Measured Value
Frequency	4.96 kHz	5.15 kHz
Duty cycle	0.65	0.65



Step 5: The capacitor waveform shows the charge and very fast discharge. Frequency rises to 12.5 kHz, with only negative triggers on the output.

Steps 6 and 7: Student answers will vary. One possible circuit is to change both R_A and R_B to 4.7 kΩ (no change to C). This will give a calculated frequency of 10.1 kHz.

Questions: Part 3

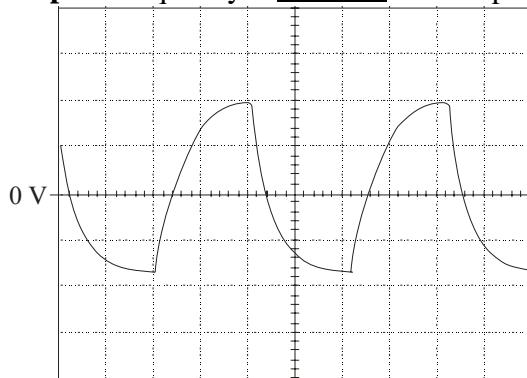
1. The value of R_1 needs to be larger and R_2 smaller. R_1 will need to be increased by twice the amount of reduction to R_2 . For example if R_2 is reduced to 5.1 kΩ, then R_1 should be a resistor that is near 2×4.9 kΩ larger than 8.2 kΩ, which is 18 kΩ.
2. The shape will remain the same, but the waveform will go between 5 V and 10 V (1/3 and 2/3 of V_{CC}).
3. For any real value of R_1 , the fraction $(R_1+R_2)/(R_1+2R_2) > 0.5$.
4. (a) The trigger points are 1/3 and 2/3 of V_{CC} . The capacitor charges and discharges between these two levels.
(b) It has no effect on the frequency because the frequency is determined solely by the time constants.
5. (a) The maximum output source or sink current is 200 mA but depends on the acceptable output voltage levels for high and low.
(b) The high output voltage drops and the low output voltage rises.

Experiment 16-B Programmable Analog Design

Part 1: Ring Oscillators

Instructor Note: Values for frequency and amplitude will vary for different PAMs.

Step 3: Frequency = 470 kHz Amplitude = 3.68 V_p (7.36 V_{pp})

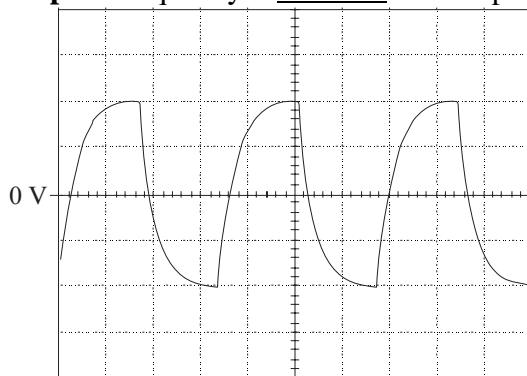


Vertical: 2.00 V/div

Horizontal 500 ns/div

Plot 16-2 Three-stage ring oscillator.

Step 4: Frequency = 285 kHz Amplitude = 4.04 V_p (8.08 V_{pp})

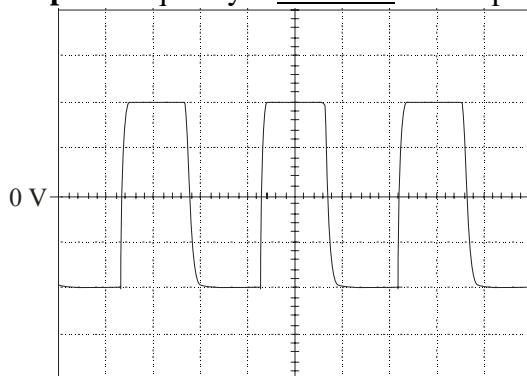


Vertical: 2.00 V/div

Horizontal 1.0 μs/div

Plot 16-3 Seven-stage ring oscillator.

Step 6: Frequency = 6.50 kHz Amplitude = 1.05 V_p (2.10 V_{pp})



Vertical: 500 mV/div

Horizontal 50 μs/div

Plot 16-4 Waveform from the special ring oscillator.

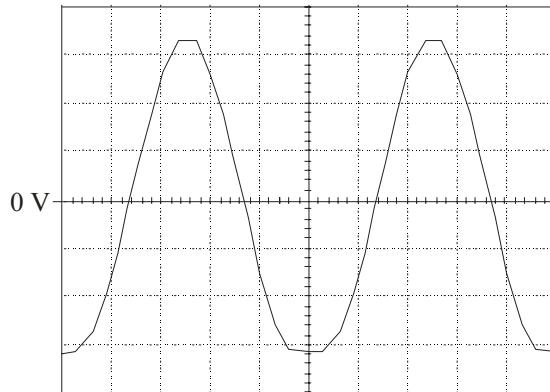
Step 7: As the integration time constant is increased, the frequency increases. An integration time constant of 4.0 produces a 12 kHz square wave.

Step 8: The last circuit used most of the available resources. The LUT and counter are shown as available but only 2 capacitors (in CAB2) are available.

Questions: Part 1

1. Each time a signal goes through the loop it represents either a logical LOW or logical HIGH. Thus each pass represents $\frac{1}{2}$ the period of the wave.
2. The measured frequency in step 4 is 285 kHz with a period of 3.50 μ s. This time represents fourteen total delays (two passes through seven stages). Thus the delay for one stage is approximately $3.50 \mu\text{s}/14 = \underline{250 \text{ ns}}$.
Note that this is an average for all stages and ignores other delays in the system such as the input and output buffers on the PAM unit.
3. Make one inverting stage and the rest non-inverting stages. (This can be implemented as one instance of a *GainInv* CAM and three instances of a *GainLimiter* CAM.)
4. In addition to showing how much of the available resources are used, it also indicates the power consumption.

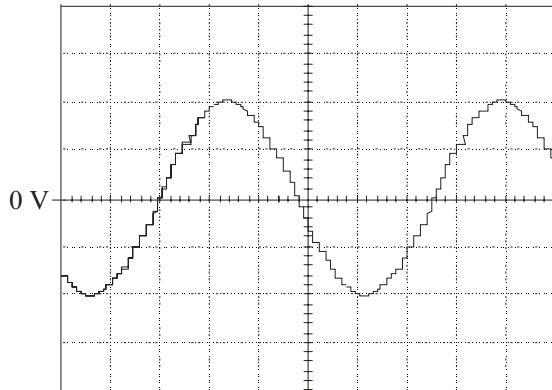
Part 2: The Sine Wave Oscillator



Vertical: 500 mV/div

Horizontal: 500 ns/div

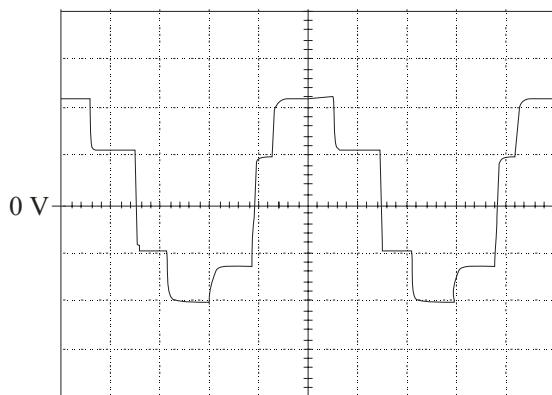
Plot 16-5 Oscillator signal at OUT1 of PAM.



Vertical: 1.0 V/div

Horizontal: 25 μ s/div

Plot 16-6 A 7 kHz sine wave using the internal 250 kHz clock.



Vertical: 1.0 V/div

Horizontal: 5.0 μ s/div

Plot 16-7 A 41 kHz sine wave using the internal 250 kHz clock (from a single-shot display.)

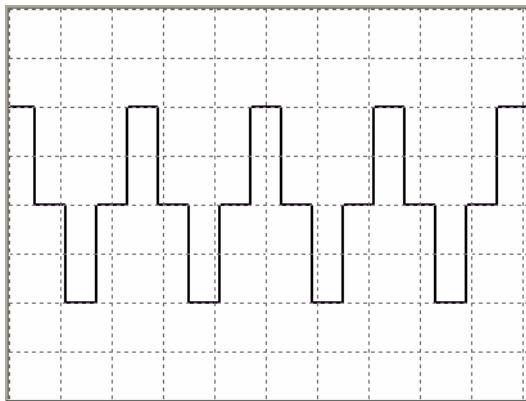
Questions: Part 2

1.
 - (a) At 5 samples per cycle of a sine wave, the reconstructed wave is recognizable but the steps are clearly visible between sample points. A smoothing filter gives a better result. (Note: Typical simulator software tools such as PSPICE, Multisim, or Saber) use at least 20 samples per cycle.)
 - (b) The Nyquist criteria requires more than two samples per cycle as the minimum sampling rate to reconstruct the frequency of the sine wave.
2. The intent of the output stage smoothing filter is to make the steps in the output look more like a sine wave. Because the filter frequency on the PAM5002 is set to approximately 432 kHz, it is not effective for the 41 kHz signal used in the experiment (the signal is more than a factor of 10 below the filter f_c).
3. The signal is 800 MHz but looks more like a triangle wave than a sine wave, even after the 432 MHz smoothing filter.

Part 3: The Arbitrary Waveform Generator

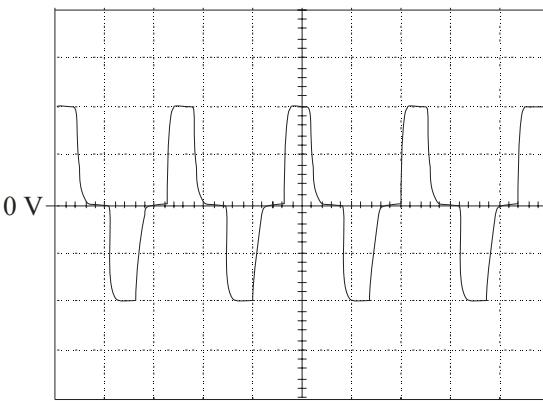
Instructor note: ClockA = 2000 kHz (500 ns period). With 24 samples, the period is $T = (500\text{ns})(24 \text{ samples}) = 12,000 \text{ ns} = 12 \mu\text{s}$. This implies $f = 83.3 \text{ kHz}$.

If a student reports an incorrect value, check that he or she has set the counter reset value to = 23, not 24 or some other value.



Vertical: 500 mV/div
Horizontal: 5.0 $\mu\text{s}/\text{div}$

Plot 16-8 Simulated waveform.
Frequency: Simulated 83.3 kHz



Vertical: 500 mV/div
Horizontal: 5.0 $\mu\text{s}/\text{div}$

Plot 16-9 Measured waveform
Measured 83.3 kHz

Step 6: The output filter on the PAM has a cutoff frequency at 432 kHz that affects the higher harmonics in the signal. This causes rounding of the edges as shown in Plot 16-9.

Step 7: The frequency drops to 10.4 kHz, so the measured waveform has steeper changes and approaches the ideal wave. (The simulator shows the ideal wave.)

Step 11: The frequency measured on the simulator is 1.64 kHz. The period is 0.61 ms.

Step 12: The frequency measured from the PAM is 1.64 kHz. The period is 0.61 ms.

Step 13: The frequency goes to 13.2 kHz. This is 8 times faster, which is expected because the sample clock was increased by 8 times.

Step 14: The dc voltage on the simulator is -3.46 V. The measured voltage on the PAM (using a DMM) is -3.55 V.

The measured voltage in the PAM is after the output buffer. Small variations in component values can affect the gain of the buffer.

Questions: Part 3

1. There are 152 steps read at 250 kHz. This implies 4 μs per step.
 $T = (152 \text{ steps})(4 \mu\text{s per step}) = 608 \mu\text{s}$, which is a frequency of 1.64 kHz.
2. Examples are CD and MP3 players.
3. The clock determines how fast the lookup table is sampled, which determines how fast values are presented to the DAC.

Experiment 17 Voltage Regulators

Part 1: The Series Regulator

Table 17-1

Resistor	Listed Value	Measured Value
R_1	2.7 kΩ	2.69 kΩ
R_2	330 Ω	329 Ω
R_3	1.0 kΩ	1.00 kΩ
R_4^*	1 kΩ	1.00 kΩ
R_5	1.2 kΩ	1.19 kΩ
R_L	330 Ω	328 Ω

*potentiometer; record maximum resistance

Table 17-3

V_{IN}	V_{OUT} (measured)
+18.0 V	+10.0 V
+17.0 V	9.94 V
+16.0 V	9.88 V
+15.0 V	9.82 V
+14.0 V	9.75 V

Table 17-2

Parameter	Computed Value	Measured Value
$V_{OUT(\min)}$	8.30 V	8.54 V
$V_{OUT(\max)}$	15.3 V	15.09 V

Table 17-4

Step	Quantity	Measured Value
6	Line regulation	0.63%
7	V_{NL}	+10.0 V
	V_{FL}	9.96 V
	Load regulation	0.4%
8	$V_{\text{ripple(in)}}$	700 mV_{pp}
	$V_{\text{ripple(out)}}$	45 mV_{pp}

Questions: Part 1

1. Increase the size of C_1 . (A second 1000 μF capacitor in parallel with C_1 halved the ripple).
2. The power delivered to the load is 0.91 W. The efficiency is 45%.

Part 2: IC Regulators

Step 1: The regulated output had approximately 1 mV of ripple. The ripple waveform showed only the tip of the positive waveform. Noise level was less than 1 mV. Although a larger filter capacitor was specified here, the ripple is significantly smaller than the unregulated supply in Step 9 of Experiment 2.

Step 2: The LED brightness was the same for all input voltages because of the current source as indicated by the data in Table 17-5.

Step 3: The current was nearly identical to the current in the single LED as indicated by the data in Table 17-6.

Table 17-5 Data for one LED

Voltage	Current
10 V	18.61 mA
12 V	18.65 mA
14 V	18.67 mA
16 V	18.69 mA

Table 17-6 Data for two LEDs

Voltage	Current
10 V	18.61 mA
12 V	18.61 mA
14 V	18.61 mA
16 V	18.61 mA

Questions: Part 2

- There is a small additional current from the common (“ground”) lead on the regulator that adds to the current sourced by R_1 .
- Change R_1 to 680 Ω (nearest standard value to 666 Ω).

Experiment 18 Communications Circuits**Part 1: The IF Amplifier****Table 18-1**

Resistor	Listed Value	Measured Value
R_1	56 k Ω	56.1 kΩ
R_2	4.7 k Ω	4.62 kΩ
R_3	10 k Ω	10.1 kΩ
R_{E1}	220 Ω	222 Ω
R_{E2}	470 Ω	467 Ω
R_L	10 k Ω	10.1 kΩ

Table 18-2

DC Parameter	Computed Value	Measured Value
V_B	0.697 V	0.697 V
V_E	0.0 V*	0.0999 V
I_E	0 mA	
V_C	9.00 V	8.99 V
V_{CE}	9.00 V	8.99 V

*assuming V_E cannot be negative**Table 18-3**

AC Parameter	Measured Value
V_b	300 mV_{pp}*
V_c	8.0 mV_{pp}**
A_v	26.7
$V_{out(tot)}$	1.2 mV_{pp}

* Signal gen set to approx 500 mV_{pp}

** Different transformers were tested. Results varied more than usual. Typical results shown.

Table 18-4

AC Parameter	Measured Value*
f_c	455.8 kHz
f_{cu}	461.4 kHz
f_{cl}	444.6 kHz
BW	16.8 kHz
Q	27.1

*frequency counter suggested for frequency measurements

Questions: Part 1

- Adding a second probe doubles the loading effect. If probe loading is not a problem, no effect will be observed when the second probe is connected to the circuit.
- The resonant circuit has highest reactance at resonance; thus, amplifier gain is also highest here.

4. The voltage across R_{in} is 3X larger than that dropped across R_3 , hence
 $R_{in} = 3 \times 10 \text{ k}\Omega = 30 \text{ k}\Omega$.
5. Answers (a) and (e) could account for 0 V on the collector.

Part 2: The Phase-Locked Loop

Table 18-5

Component	Listed Value	Measured Value
R_1^*	2.0 k Ω	1.99 kΩ
R_2	1.0 k Ω	1.00 kΩ
R_3	1.0 k Ω	1.01 kΩ
C_1	2200 pF	2200 pF
C_2	0.1 μF	0.1 μF
C_3	1000 pF	1000 pF

* plus 10 k Ω potentiometer in circuit

Table 18-6

Step	Quantity	Computed Value	Measured Value
2 and 3	free-running frequency, $f_{0(\min)}$	11.54 kHz	11.65 kHz
	free-running frequency, $f_{0(\max)}$	68.5 kHz	68.3 kHz
4	lower capture frequency	Range =	23.8 kHz
5	upper capture frequency	$\pm 1.9 \text{ kHz}$	28.1 kHz
6	lower lock frequency	Range =	17.5 kHz
	upper lock frequency	$\pm 8.3 \text{ kHz}$	34.6 kHz
8	frequency in (multiplier)	2.5 kHz	2.5 kHz
	frequency out (multiplier)	25.0 kHz	25.0 kHz

Step 7: Pin 7 shows a capacitor charge and discharge waveform that goes between 8 and 10 V. The frequency is twice the input frequency.

Questions: Part 2

1. A decrease in either R_1 or C_1 by a factor of ten will multiply the free-running frequency by ten.
2. The transistor limits the input signal to the logic circuit between 0 and 5 V.
3. The capture range is the range of frequencies over which the VCO can establish synchronization. After a signal is captured, the VCO can track it over the lock range.
4. It must be multiplied by two.
5. (a) $\pm 12 \text{ V}$
(b) The power supply voltage is inversely proportional to the lock range.

Test Item File

Electronic Devices

Eighth Edition

Thomas L. Floyd

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Chapter 1 Introduction to Semiconductors

- 1) A molecule is the smallest particle of an element that retains the characteristics of that element.

Diff: 2

- 2) A conducting germanium diode has a potential of about 0.7 V across it.

Diff: 2

- 3) Silicon doped with impurities is used in the manufacture of semiconductor devices.

Diff: 2

- 4) Reverse bias permits full current through a pn junction.

Diff: 2

- 5) Semiconductor material of the p-type has few free electrons.

Diff: 2

- 6) The application of a dc voltage to control diode conduction is called

A) oscillation. B) amplification. C) bias. D) a pn junction.

Diff: 2

- 7) Holes are the majority carriers in

A) an n-type semiconductor. B) a p-type semiconductor.

C) a pn junction semiconductor. D) None of the above.

Diff: 2

- 8) Semiconductor materials are those with

A) conductive properties that are in between those of a conductor or an insulator.

B) conductive properties that are very good.

C) no conductive properties.

D) Either A or B.

Diff: 2

- 9) There is current through the junction of a forward-biased diode. This current is called

A) forward current.

B) reverse breakdown current.

C) avalanche current.

D) reverse leakage current.

Diff: 2

- 10) A typical value of reverse breakdown voltage in a diode is

 - A) 0 V.
 - B) 0.3 V.
 - C) 0.7 V.
 - D) 50 V or larger.

Diff: 2

- 11) The small current when a diode is reverse-biased is called

 - A) forward-bias current.
 - B) reverse breakdown current.
 - C) conventional current.
 - D) reverse-leakage current.

Diff: 2

- 12) As the forward current through a forward-biased diode decreases, the voltage across the diode

 - A) increases.
 - B) immediately drops to 0 V.
 - C) is relatively constant.
 - D) increases and then decreases.

Diff: 2

- 13) Which statement best describes a p-type semiconductor?

 - A) Silicon with pentavalent impurity.
 - B) Silicon with trivalent impurity atoms added.
 - C) A material where holes are the minority carriers.
 - D) Pure intrinsic silicon.

Diff: 3

- 14) The resistance of a forward-biased diode is

 - A) perfectly linear.
 - B) infinite.
 - C) minimal below the knee of the curve.
 - D) minimal above the knee of the curve.

Diff: 2

- 15) A silicon diode measures a high value of resistance with the meter leads in both positions. The trouble, if any, is

 - A) the diode is open.
 - B) the diode is shorted to ground.
 - C) the diode is internally shorted.
 - D) nothing; the diode is good.

Diff: 2

- 16) The forward voltage across a conducting silicon diode is about
A) 1.3 V. B) 0.3 V. C) 0.7 V. D) -0.3 V.

Diff: 2

17) An unknown type of diode is in a circuit. The forward voltage measured across it is found to be 0.3 V. The diode is

- A) a silicon diode.
- B) a germanium diode.
- C) a transistor.
- D) shorted.

Diff: 2

18) A reverse-biased diode has the _____ connected to the positive side of the source, and the _____ connected towards the negative side of the source.

- A) cathode, anode
- B) cathode, base
- C) base, anode
- D) anode, cathode

Diff: 3

19) The boundary between p-type material and n-type material in a diode is called

- A) the cathode.
- B) the control grid.
- C) the pn junction.
- D) the anode.

Diff: 2

20) The atomic number of an atom refers to the

- A) number of protons in the nucleus.
- B) number of electrons in a charged atom.
- C) net electrical charge of the atom.
- D) number of neutrons in the nucleus.

Diff: 1

21) Electrons orbiting the nucleus of an atom are grouped into energy bands known as

- A) slots.
- B) tracks.
- C) shells.
- D) tunnels.

Diff: 2

22) Valence electrons have _____ energy level of all the electrons in orbit around the nucleus of a given atom.

- A) the lowest
- B) the highest
- C) the same
- D) None of the above.

Diff: 2

23) The difference in energy levels that exists between the valence band and the conduction band is called

- A) covalent gap.
- B) semiconductor region.
- C) spark gap.
- D) energy gap.

Diff: 3

- 24) The valence electron of a copper atom experiences what kind of attraction toward the nucleus?
- A) None
 - B) Weak
 - C) Strong
 - D) Impossible to say

Diff: 2

- 25) What must be used in series with a forward-biased diode to prevent damage due to excessive current?
- A) Ammeter
 - B) Resistor
 - C) NC switch
 - D) Nothing is required

Diff: 2

- 26) Reverse bias is a condition that essentially _____ current through the diode.
- A) prevents
 - B) allows
 - C) increases
 - D) amplifies

Diff: 2

- 27) The knee voltage of a diode is approximately equal to the
- A) applied voltage.
 - B) barrier potential.
 - C) breakdown voltage.
 - D) reverse voltage.

Diff: 2

- 28) A nonconducting diode is _____ biased.
- A) forward
 - B) inverse
 - C) poorly
 - D) reverse

Diff: 2

- 29) On diode check, a shorted diode will measure
- A) 0 V.
 - B) 0.3 V.
 - C) 0.7 V.
 - D) 0.79 V.

Diff: 2

- 30) How much forward diode voltage is there with the ideal-diode approximation?
- A) 0 V
 - B) 0.7 V
 - C) More than 0.7 V
 - D) 1 V

Diff: 1

- 31) A DMM measures $0.13\ \Omega$ in both directions when testing a diode. The diode is
- A) constructed of Si and is good.
 - B) open.
 - C) operating normally.
 - D) shorted.

Diff: 3

32) If the positive lead of an ohmmeter is placed on the cathode and the negative lead is placed on the anode, which of the following readings would indicate a defective diode?

- A) 0Ω B) $\infty \Omega$ C) $1 M\Omega$ D) $400 k\Omega$

Diff: 3

33) What is the maximum number of electrons that can exist in the shell closest to the nucleus of an atom?

- A) 1 B) 2 C) 4 D) 8

Diff: 2

34) All of the following are semiconductors except

- A) carbon. B) germanium. C) silicon. D) copper.

Diff: 2

35) A reverse-biased silicon diode is connected in series with a 12 V source and a resistor. The voltage across the diode is

- A) 0 V. B) 0.3 V. C) 0.7 V. D) 12 V.

Diff: 2

36) A reverse-biased silicon diode is connected in series with a 12 V source and a resistor. The voltage across the resistor is

- A) 0 V. B) 0.3 V. C) 0.7 V. D) 12 V.

Diff: 2

37) Silicon and germanium contain _____ valence electrons.

- A) one B) two C) four D) eight

Diff: 1

38) Germanium has limited use in modern electronics due to

- A) shortages of raw materials.
B) higher forward voltage drop when compared to Si.
C) high temperature instability.
D) filament warm-up time.

Diff: 2

39) A diode is operated in reverse bias. As the reverse voltage is decreased, the depletion region

- A) narrows. B) has a constant width.
C) widens. D) is not related to reverse voltage.

Diff: 2

Chapter 2 Diode Applications

- 1) A diode conducts current when forward-biased and blocks current when reverse-biased.

Diff: 2

- 2) The larger the ripple voltage, the better the filter.

Diff: 2

- 3) Clamping circuits use capacitors and diodes to add a dc level to a waveform.

Diff: 2

- 4) One of the advantages of using transformer coupling in a half-wave rectifier is that it allows the ac source to be directly connected to the load.

Diff: 2

- 5) The PIV rating of a diode in a full-wave bridge rectifier is more than that required for a full-wave center-tapped configuration.

Diff: 2

- 6) The diode in a half-wave rectifier conducts for _____ of the input cycle.

A) 0° B) 45° C) 90° D) 180°

Diff: 2

- 7) A full-wave bridge rectifier uses _____ diode(s) in a bridge circuit.

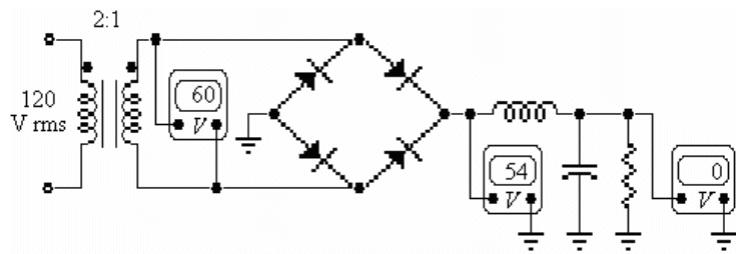
A) 1 B) 2 C) 3 D) 4

Diff: 2

- 8) A silicon diode is connected in series with a $10\text{ k}\Omega$ resistor and a 12 V battery. If the cathode of the diode is connected to the positive terminal of the battery, the voltage from the anode to the negative terminal of the battery is

A) 0 V. B) 0.7 V. C) 11.3 V. D) 12 V.

Diff: 3



- 9) Refer to the figure above. If the voltmeter across the transformer secondary reads 0 V, the probable trouble is that

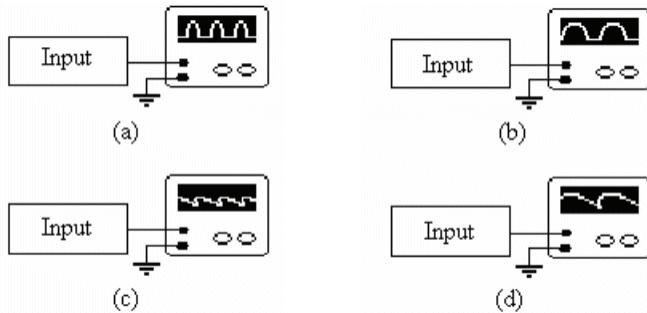
- A) one of the diodes is open.
- B) the filter capacitor is open.
- C) the transformer secondary is open.
- D) the inductor is open.
- E) No trouble exists; everything is normal.

Diff: 3

- 10) Refer to the figure above. In servicing this power supply, you notice that the ripple voltage is higher than normal and that the ripple frequency has changed to 60 Hz. The probable trouble is that

- | | |
|-------------------------------------|-----------------------------|
| A) the filter capacitor has opened. | B) the inductor has opened. |
| C) a diode has shorted. | D) a diode has opened. |

Diff: 3



- 11) Refer to the figure above. This oscilloscope trace indicates the output from

- A) a half-wave filtered rectifier.
- B) a full-wave rectifier with no filter and an open diode.
- C) a full-wave filtered rectifier.
- D) a full-wave filtered rectifier with an open diode.

Diff: 3

12) Refer to the figure above. The trace on this oscilloscope indicates the output from

- A) a half-wave rectifier with no filter.
- B) a full-wave rectifier with no filter.
- C) a full-wave filtered rectifier.
- D) a full-wave filtered rectifier with an open diode.

Diff: 3

13) Refer to the figure above. This is the output from

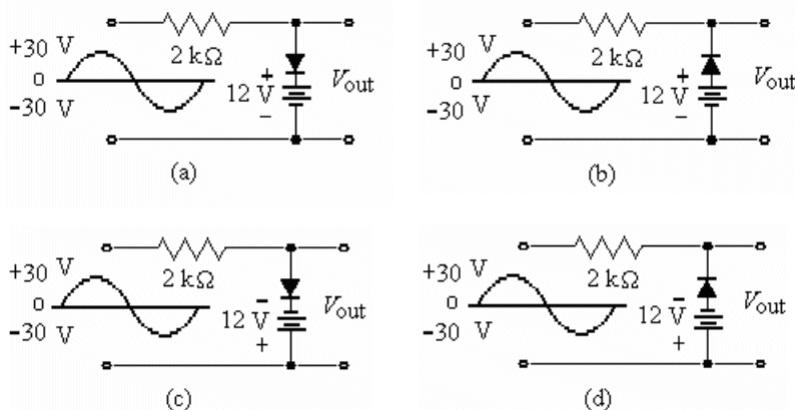
- A) a half-wave rectifier with no filter.
- B) a full-wave rectifier with no filter and an open diode.
- C) a full-wave filtered rectifier.
- D) a full-wave filtered rectifier with an open diode.

Diff: 3

14) Refer to the figure above. This trace shows the output from

- A) a half-wave rectifier with no filter.
- B) a full-wave rectifier with no filter and an open diode.
- C) a half-wave rectifier with an open diode.
- D) a full-wave filtered rectifier with an open diode.

Diff: 2



15) Refer to the figure above. These circuits are known as

- A) amplifiers.
- B) clippers.
- C) clampers.
- D) rectifiers.

Diff: 2

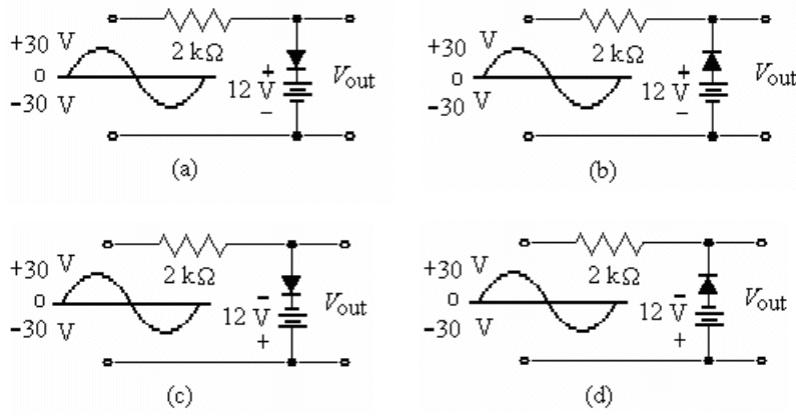


Figure I

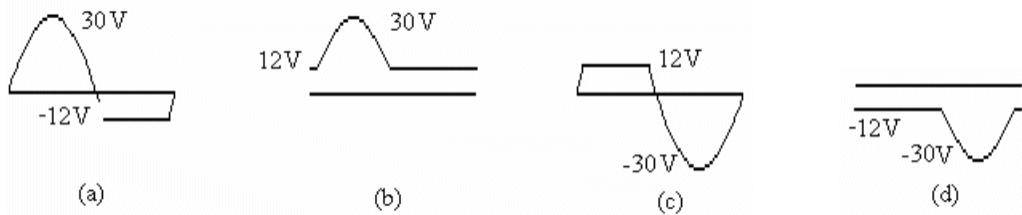


Figure II

16) Which of the circuits in Figure I will produce the signal in Figure II (a)?

- A) (a) B) (b) C) (c) D) (d)

Diff: 2

17) Which of the circuits in Figure I will produce the signal in Figure II (b)?

- A) (a) B) (b) C) (c) D) (d)

Diff: 2

18) Which of the circuits in Figure I will produce the signal in Figure II (c)?

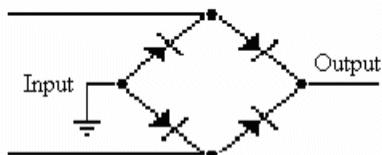
- A) (a) B) (b) C) (c) D) (d)

Diff: 2

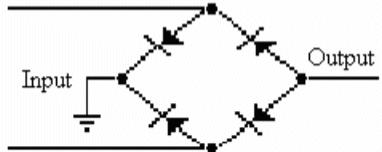
19) Which of the circuits in Figure I will produce the signal in Figure II (d)?

- A) (a) B) (b) C) (c) D) (d)

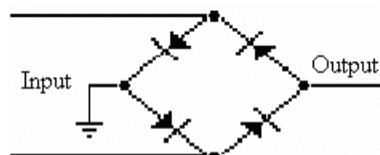
Diff: 2



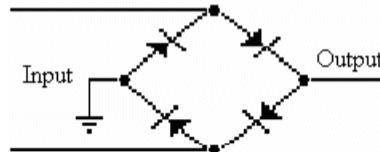
(a)



(c)



(b)



(d)

20) Refer to (c) in the figure above. This rectifier arrangement

- A) will produce a positive output voltage.
- B) will produce a negative output voltage.
- C) is incorrectly connected.
- D) A or C above.

Diff: 2

21) Refer to (d) in the figure above. This rectifier arrangement

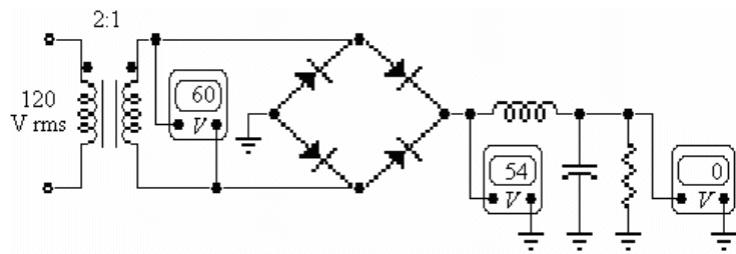
- A) will produce a positive output voltage.
- B) will produce a negative output voltage.
- C) is incorrectly connected.
- D) None of the above.

Diff: 2

22) A silicon diode has a voltage to ground of 117 V from the anode. The voltage to ground from the cathode is 117.7 V. The diode is

- A) conducting.
- B) shorted.
- C) forward-biased.
- D) reverse-biased.

Diff: 2



23) Refer to the figure above. The probable trouble, if any, indicated by these voltages is

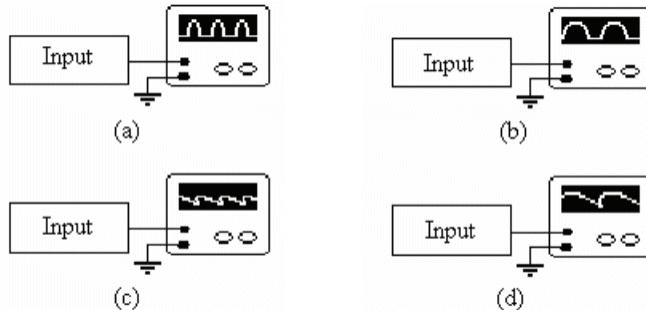
- A) one of the diodes is open.
- B) an open transformer primary.
- C) an open transformer secondary.
- D) the filter capacitor is open.
- E) the inductor is open.

Diff: 3

24) Refer to the figure above. If the voltmeter across the transformer secondary reads 0 V, the probable trouble, if any, would be

- | | |
|-------------------------------|---------------------------------|
| A) one of the diodes is open. | B) an open transformer primary. |
| C) the inductor is open. | D) the inductor is shorted. |

Diff: 3



25) Refer to the figure above. Which oscilloscope trace indicates the output from a filtered full-wave rectifier with an open diode?

- A) (a)
- B) (b)
- C) (c)
- D) (d)

Diff: 3

26) The ripple frequency of a bridge rectifier is

- A) the same as the input frequency.
- B) double the input frequency.
- C) four times the input frequency.
- D) one-half the input frequency.

Diff: 2

- 33) To reduce surge current, _____ should be added to a power supply circuit.
- A) additional filter capacitance
 - B) a larger fuse
 - C) a varactor tuning circuit
 - D) a surge-limiting resistor

Diff: 3

- 34) The dc current through each diode in a bridge rectifier equals
- A) twice the dc load current.
 - B) half the dc load current.
 - C) the load current.
 - D) one-fourth the dc load current.

Diff: 3

- 35) The peak inverse voltage across a nonconducting diode in an unfiltered bridge rectifier equals approximately
- A) half the peak secondary voltage.
 - B) twice the peak secondary voltage.
 - C) the peak value of the secondary voltage.
 - D) four times the peak value of the secondary voltage.

Diff: 3

- 36) The ideal dc output voltage of a capacitor-input filter equals the
- A) rms value of the rectified voltage.
 - B) peak value of the rectified voltage.
 - C) average value of the rectified voltage.
 - D) peak-to-peak value of the secondary voltage.

Diff: 3

- 37) A filtered full-wave rectifier voltage has a smaller ripple than does a half-wave rectifier voltage for the same load resistance and capacitor values because
- A) of the shorter time between peaks.
 - B) of the longer time between peaks.
 - C) the larger the ripple, the better the filtering action.
 - D) None of the above.

Diff: 3

- 38) As the load resistance in a filtered power supply varies, the output voltage
- A) remains constant.
 - B) is unaffected.
 - C) varies.
 - D) does not change.

Diff: 1

39) The voltage regulation stage in a power supply

- A) is located preceding the transformer's primary.
- B) follows the filter stage.
- C) is connected to the input of the rectifier(s).
- D) is inside the transformer.

Diff: 2

40) A voltage regulator compensates for changes in

- A) the input voltage.
- B) temperature.
- C) the load conditions.
- D) All of the above.

Diff: 2

41) Another name for a diode limiter is

- A) bridger.
- B) clipper.
- C) clamper.
- D) dc restorer.

Diff: 1

42) A diode clamper will

- A) clip off a portion of the input signal.
- B) eliminate the positive or negative alternation of a signal.
- C) add an ac voltage to a signal.
- D) add a dc voltage to a signal.

Diff: 3

43) Voltage multipliers use _____ action to increase peak rectified voltages without increasing the input transformer voltage rating.

- A) clipping
- B) clamping
- C) charging
- D) cropping

Diff: 3

44) All of the following diode information is provided by a manufacturer's data sheet except

- A) frequency response.
- B) PIV ratings.
- C) mechanical data.
- D) temperature parameters.

Diff: 4

Chapter 3 Special-Purpose Diodes

- 1) The regulating ability of a zener diode depends upon its ability to operate in a breakdown condition.

Diff: 2

- 2) Dark current is the amount of thermally generated forward current in a photodiode in the absence of light.

Diff: 2

- 3) A _____ diode maintains a constant voltage across it when operating in the breakdown condition.

- A) silicon
 - B) germanium
 - C) zener
 - D) None of the above.

Diff: 2

- 4) A tunnel diode has _____ characteristic(s).

- A) an extremely wide depletion region
 - B) a negative resistance
 - C) a linear
 - D) extremely light doping

Diff: 2

- 5) Typically, the maximum VF for an LED is between

- A) 0 V and 0.7 V.
 - B) 1 V and 1.4 V.
 - C) 1.2 V and 3.2 V.
 - D) 3.2 V and 10 V.

Diff: 2

- 6) An OLED produces light by a process called _____.

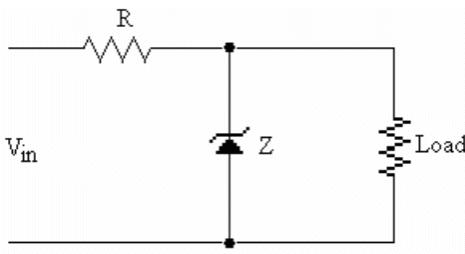
- A) Electrophosphorescence.
 - B) Organic light emission.
 - C) Avalanche light emission.
 - D) Photonic light emission.

Diff: 2

- 7) When a zener diode is forward-biased, it

- A) operates like a rectifier diode.
 - B) exhibits a voltage drop of $V_Z + 0.7\text{ V}$.
 - C) conducts no current.
 - D) emits visible light.

Diff: 2



8) Refer to the figure above. If V_{in} increases, V_R will

- A) increase.
- B) decrease.
- C) remain the same.
- D) Unable to determine.

Diff: 3

9) Refer to the figure above. If the zener shorts

- A) V_{in} will be equal to V_R .
- B) V_{RL} will be equal to zero.
- C) there is no current through R_L .
- D) All of the above.

Diff: 3

10) Refer to the figure above. Measurements show that V_{RL} has increased. Which of the following faults, if any, could have caused this problem?

- A) R opens.
- B) The zener shorts.
- C) V_{in} has decreased.
- D) The zener opens.

Diff: 3

11) Refer to the figure above. As long as the zener is in regulation

- A) there is no current through R_L .
- B) there is no current through the zener.
- C) V_{RL} will be equal to 0.7 V.
- D) the current (I_{RL}) remains constant.

Diff: 3

12) Refer to the figure above. If the load current increases, I_R will _____ and I_Z will _____.

- A) remain the same, increase
- B) decrease, remain the same
- C) increase, remain the same
- D) remain the same, decrease

Diff: 3

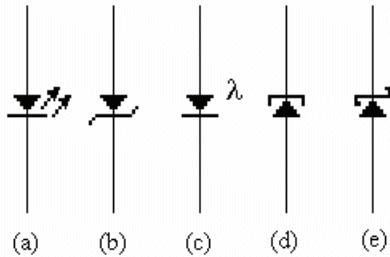
13) Refer to the figure above. If V_{in} decreases, I_R will

- A) increase.
- B) decrease.
- C) remain the same.
- D) Unable to determine.

Diff: 2

- 14) Refer to the figure above. If the load current increases in the zener regulator
- A) the series current increases.
 - B) the series current remains the same.
 - C) the zener current increases.
 - D) Both B and C above.

Diff: 3



- 15) Refer to (a) in the figure above. The symbol is for
- A) a zener diode.
 - B) an LED.
 - C) a Schottky diode.
 - D) a photodiode.
 - E) a tunnel diode.

Diff: 2

- 16) Refer to (b) in the figure above. The symbol is for
- A) a zener diode.
 - B) an LED.
 - C) a Schottky diode.
 - D) a photodiode.
 - E) a tunnel diode.

Diff: 2

- 17) Refer to (c) in the figure above. The symbol is for
- A) a zener diode.
 - B) an LED.
 - C) a Schottky diode.
 - D) a photodiode.
 - E) a tunnel diode.

Diff: 2

18) Refer to (d) in the figure above. The symbol is for

- A) a zener diode.
- B) an LED.
- C) a Schottky diode.
- D) a photodiode.
- E) a tunnel diode.

Diff: 2

19) Refer to (e) in the figure above. The symbol is for

- A) a zener diode.
- B) an LED.
- C) a Schottky diode.
- D) a photodiode.
- E) a tunnel diode.

Diff: 2

20) A varactor is a diode that

- A) varies its resistance with temperature.
- B) changes its capacitance with voltage.
- C) emits light when forward-biased.
- D) switches very fast.
- E) exhibits an increase in reverse current with light intensity.

Diff: 2

21) A Schottky diode is a diode that

- A) varies its resistance with temperature.
- B) changes its capacitance with voltage.
- C) emits light when forward-biased.
- D) switches very fast.
- E) exhibits an increase in reverse current with light intensity.

Diff: 2

22) A photodiode is a diode that

- A) varies its resistance with temperature.
- B) changes its capacitance with light intensity.
- C) emits light when forward-biased.
- D) switches very fast.
- E) exhibits an increase in reverse current with light intensity.

Diff: 2

23) The correct way to illuminate an LED is to

- A) place the LED in reverse bias directly across a 5 V dc supply.
- B) place the LED in forward bias directly across a 5 V dc supply.
- C) place the LED in series with a resistor and a 5 V dc supply with the anode toward the positive side of the supply.
- D) place the LED in series with a resistor and a 5 V dc supply with the cathode toward the positive side of the supply.

Diff: 3

24) A diode with a negative-resistance characteristic is needed. The correct selection would be a

- | | |
|--------------------|--------------------|
| A) tunnel diode. | B) Gunn diode. |
| C) varactor diode. | D) Schottky diode. |

Diff: 2

25) A 6.2 V zener is rated at 1 watt. The maximum safe current the zener can carry is approximately

- | | | | |
|------------|------------|-------------|-------------|
| A) 1.61 A. | B) 161 mA. | C) 16.1 mA. | D) 1.61 mA. |
|------------|------------|-------------|-------------|

Diff: 2

26) An LED is forward-biased. The diode should be on, but no light is showing. A possible problem might be

- A) that the diode is open.
- B) that the series resistor is too small.
- C) none; the diode should be off if forward-biased.
- D) that the power supply voltage is too high.

Diff: 3

27) The best type of diode to use in a tuning circuit is

- | | |
|------------------|----------------------|
| A) an LED. | B) a Schottky diode. |
| C) a Gunn diode. | D) a varactor. |

Diff: 2

- 28) What is true about the breakdown voltage in a zener diode?
- A) It decreases when current increases. B) It destroys the diode.
C) It occurs only in the forward region. D) It is approximately constant.
- Diff:* 2
- 29) Two types of reverse breakdown in a zener diode are
- A) avalanche and zener. B) avalanche and reverse.
C) avalanche and forward. D) charge and discharge.
- Diff:* 2
- 30) For zener diodes, the temperature coefficient is
- A) always positive.
B) always negative.
C) negative for breakdown voltages less than 5 V and positive for breakdown voltages greater than 6 V.
D) always zero.
- Diff:* 2
- 31) Data sheets for zener diodes usually specify the zener voltage at a particular test current designated
- A) I_S . B) I_{ZK} . C) I_{ZM} . D) I_{ZT} .
- Diff:* 1
- 32) When the source voltage increases in a zener regulator, the current that remains approximately constant is the
- A) series current. B) zener current. C) load current. D) total current.
- Diff:* 3
- 33) If the load resistance decreases in a zener regulator, the zener current
- A) decreases.
B) stays the same.
C) increases.
D) equals the source voltage divided by the series resistance.
- Diff:* 2

34) If the load resistance decreases in a zener regulator, the series current

- A) decreases.
- B) stays the same.
- C) increases.
- D) equals the source voltage divided by the series resistance.

Diff: 2

35) The varactor is usually

- A) forward-biased.
- B) reverse-biased.
- C) unbiased.
- D) operated in the breakdown region.

Diff: 2

36) The capacitance of a varactor diode

- A) remains constant as the bias voltage varies.
- B) decreases as the reverse bias voltage increases.
- C) increases as the reverse bias voltage increases.
- D) is usually 1000 μF or more.

Diff: 3

37) A photodiode is normally

- A) reverse-biased.
- B) forward-biased.
- C) not biased.
- D) used to regulate voltage.

Diff: 2

38) When the light increases, the reverse minority carrier current in a photodiode

- A) decreases.
- B) increases.
- C) is unaffected.
- D) reverses direction.

Diff: 1

39) LED color is determined by

- A) the applied LED voltage.
- B) the impurities added during doping to control wavelength.
- C) the LED current.
- D) the material used for the incandescent filament.

Diff: 2

- 40) To display the digit 8 in a seven-segment indicator
- A) only C must be lighted.
 - B) G must be off.
 - C) only F must be on.
 - D) all segments must be on.

Diff: 2

- 41) Modern traffic signals and large video screens are implemented with
- A) PIN diodes.
 - B) infrared photodiodes.
 - C) high intensity LED arrays.
 - D) hot filament bulbs.

Diff: 2

- 42) A Schottky diode
- A) has a forward voltage drop of about 2 V.
 - B) has no limit on maximum current.
 - C) has a metal-to-semiconductor junction.
 - D) cannot operate properly at high frequencies.

Diff: 2

- 43) The PIN diode, when reverse-biased, acts like a nearly constant
- A) resistance.
 - B) capacitance.
 - C) voltage source.
 - D) current source.

Diff: 3

- 44) Which of the following has a negative-resistance region?
- A) Tunnel diode
 - B) Rectifier diode
 - C) Schottky diode
 - D) LED

Diff: 2

- 45) The radiation pattern for an LED
- A) shows how directional the light is.
 - B) shows the current vs. voltage curve of the LED.
 - C) visually shows the color of the light.
 - D) shows the wavelength of the light.

Diff: 3

- 46) All of the following are characteristics of a laser diode except
- A) emits monochromatic light.
 - B) emits incoherent light.
 - C) emits light of a single color.
 - D) contains a pn junction.

Diff: 3

Chapter 4 Bipolar Junction Transistors

- 1) BJT transistors have two pn junctions.

Diff: 2

- 2) A BJT transistor has the base-emitter junction reverse-biased for proper operation.

Diff: 2

- 3) The ratio I_E/I_C is β_{dc} .

Diff: 2

- 4) Proper operation of a BJT requires that the base-collector junction should be reverse-biased.

Diff: 2

- 5) The formula for I_C is $I_C = I_E - I_B$.

Diff: 2

- 6) When a transistor is checked out-of-circuit, a very low resistance reading should be obtained between the C and E leads of a good transistor.

Diff: 2

- 7) Phototransistors come in both two and three terminal configurations.

Diff: 3

- 8) A BJT has an I_B of 75 μ A and a β_{dc} of 100. The value of I_C is

A) 175 μ A. B) 75 mA. C) 10 mA. D) 7.5 mA.

Diff: 2

- 9) A certain transistor has an $I_C = 12$ mA and an $I_B = 125$ μ A. β_{dc} is

A) 150. B) 15. C) 96. D) 12.

Diff: 2

- 10) Normal operation of an NPN BJT requires the base to be _____ with respect to the emitter, and _____ with respect to the collector.

A) positive, negative B) positive, positive
C) negative, positive D) negative, negative

Diff: 2

- 11) A transistor amplifier has an input voltage of 67 mV and an output voltage of 2.48 V. The voltage gain is

A) 67.

B) 37.

C) 27.

D) 17.

Diff: 2

- 12) A 22 mV signal is applied to the base of a properly biased transistor that has an $r'_e = 7 \Omega$ and an $R_C = 1.2 \text{ k}\Omega$. The output voltage at the collector is

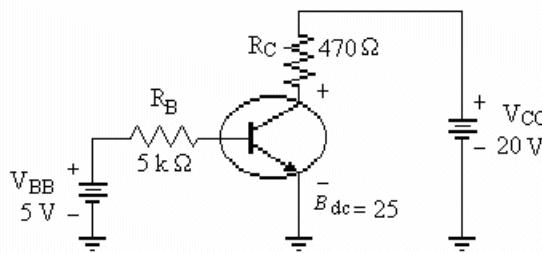
A) 22 mV.

B) 17.1 V.

C) 7 V.

D) 3.77 V.

Diff: 2



- 13) Refer to the figure above. This circuit is operating

A) in cutoff.

B) in saturation.

C) in the active region.

D) incorrectly because the bias voltages are wrong.

Diff: 3

- 14) Refer to the figure above. The value of I_B is

A) 8.6 mA.

B) 860 μ A.

C) 1 mA.

D) 0.7 μ A.

Diff: 2

- 15) Refer to the figure above. If the value of V_{BB} were increased to 10 V, the transistor would be operating in

A) cutoff.

B) saturation.

C) the active region.

D) Cannot be determined.

Diff: 3

- 16) Refer to the figure above. If this transistor is operating in saturation, the value of $I_C(\text{sat})$ is

A) 9.4 mA.

B) 4.26 mA.

C) 28.6 mA.

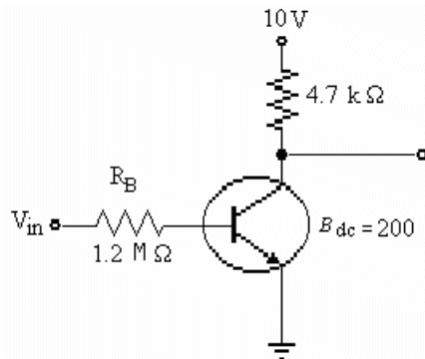
D) 42.6 mA.

Diff: 3

17) Refer to the figure above. Assume that this circuit is operating in cutoff. The measurement, if any, that would confirm this assumption is

- A) $V_{BE} = 0.7 \text{ V}$.
- B) $V_{CE} = 8 \text{ V}$.
- C) $V_{CE} = 20 \text{ V}$.
- D) $V_{CC} = 20 \text{ V}$.
- E) None of the above.

Diff: 3



18) Refer to the figure above. The value of I_C at cutoff is

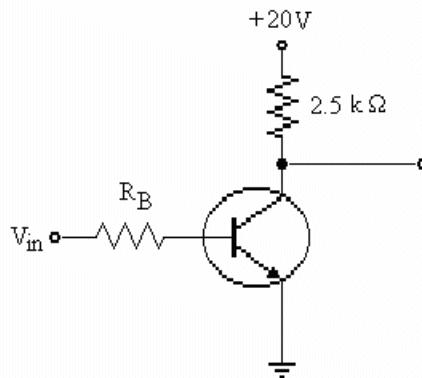
- A) 0 mA.
- B) 2.13 mA.
- C) 10.65 μA .
- D) 10 mA.

Diff: 2

19) Refer to the figure above. If the value of the collector resistor is increased to 6.8 kΩ, the new value of $I_{C(\text{sat})}$ is

- A) 2.13 mA.
- B) 0.68 mA.
- C) 1.47 mA.
- D) 0 mA.

Diff: 2



- 20) Refer to the figure above. If the collector resistor value is changed to $4.7\text{ k}\Omega$ and $\beta_{dc} = 200$, $I_{C(sat)}$ would be

A) 4.26 mA. B) 8 mA. C) 4.26 μA . D) 8.426 mA.

Diff: 2

- 21) Refer to the figure above. If the measured voltage from the collector to ground were 0 V, the transistor is operating in

A) saturation. B) cutoff.
C) the active region. D) Not enough data to determine.

Diff: 2

- 22) Refer to the figure above. This circuit is saturated. To get the circuit to operate close to its linear range

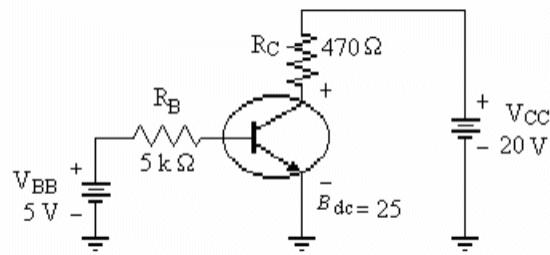
A) R_B should be decreased. B) R_C should be decreased.
C) V_{in} should be increased. D) R_B should be increased.

Diff: 3

- 23) A 35 mV signal is applied to the base of a properly biased transistor with an $r'_e = 8\text{ }\Omega$ and $R_C = 1\text{ k}\Omega$. The output signal voltage at the collector is

A) 3.5 V. B) 28.57 V. C) 4.375 V. D) 4.375 mV.

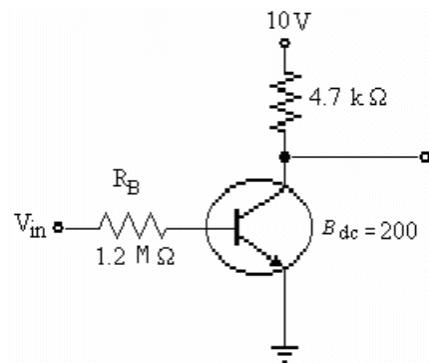
Diff: 2



24) Refer to the figure above. The value of V_{CE} is

- A) 9.9 V. B) 9.2 V. C) 0.7 V. D) 19.3 V.

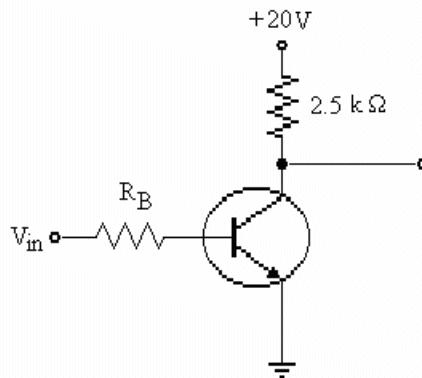
Diff: 2



25) Refer to the figure above. The minimum value of I_B that will produce saturation is

- A) 0.25 mA. B) 5.325 μA. C) 1.064 μA. D) 10.64 μA

Diff: 2



26) Refer to the figure above. The voltage V_{CE} was measured and found to be 20 V. The transistor is operating in

- A) saturation.
- B) cutoff.
- C) the active region.
- D) Not enough data to determine.

Diff: 2

27) Refer to the figure above. If V_{CE} is measured and is equal to nearly zero, the transistor is operating in

- A) cutoff.
- B) the active region.
- C) saturation.
- D) Cannot be determined.

Diff: 3

28) In an NPN transistor, the majority carriers in the base are

- A) free electrons.
- B) holes.
- C) neither.
- D) both.

Diff: 1

29) The base of an NPN transistor is thin and

- A) heavily doped.
- B) lightly doped.
- C) metallic.
- D) doped by a pentavalent material.

Diff: 2

30) In a transistor, the relation of the three transistor currents is

- A) $I_C = I_E + V_C/R_C$.
- B) $I_C = I_B - 2I_E$.
- C) $I_E = I_C + I_B$.
- D) $I_C = I_E + I_B$.

Diff: 2

31) A transistor has a β_{DC} of 250 and a base current, I_B , of 20 μ A. The collector current, I_C , equals

- A) 500 μ A. B) 5 mA. C) 50 mA. D) 5 A.

Diff: 2

32) In a bipolar junction transistor, collector current is controlled by

- A) collector voltage. B) base current.
C) collector resistance. D) All of the above.

Diff: 2

33) Most of the electrons in the base of an NPN transistor flow

- A) out of the base lead. B) into the collector.
C) into the emitter. D) into the base supply.

Diff: 2

34) When a transistor is operated in the active region, changes in the collector supply voltage V_{CC}

- A) produce changes in collector current.
B) produce changes in base voltage.
C) have little or no effect on collector current.
D) produce changes in emitter voltage.

Diff: 2

35) A bipolar junction transistor has _____ regions of operation.

- A) 1 B) 2 C) 3 D) 4

Diff: 2

36) The region in a transistor that has to dissipate the most heat is the

- A) emitter. B) base. C) collector. D) anode.

Diff: 2

37) The symbol h_{FE} is the same as

- A) β_{DC} . B) α_{DC} . C) h_{j-f} . D) β_{ac} .

Diff: 2

38) V_{CE} approximately equals _____ when a transistor switch is in saturation.

- A) V_C . B) V_B . C) 0.2 V D) 0.7 V

Diff: 2

- 39) When a transistor switch is on, the collector current is limited by
- A) the base current.
 - B) the collector resistance.
 - C) the base voltage.
 - D) the base resistance.

Diff: 2

- 40) The signal output voltage (V_{out}) is a function of the
- A) current from base to collector.
 - B) voltage drop from base to collector.
 - C) power being dissipated by the base supply voltage.
 - D) changing collector current (I_C) through the collector resistor R_C .

Diff: 2

- 41) The signal voltage gain of an amplifier, A_V , is defined as

A) $A_V = \frac{V_{out}}{V_{in}}$.

B) $A_V = I_B \times R_B$.

C) $A_V = \frac{r'_e}{R_C}$.

D) $A_V = \frac{R_C}{R_L}$.

Diff: 2

- 42) When transistors are used in digital circuits they usually operate in the
- A) active region.
 - B) breakdown region.
 - C) saturation and cutoff regions.
 - D) linear region.

Diff: 1

- 43) Besides operating as an amplifier, the BJT is often applied as a
- A) variable inductor.
 - B) switch.
 - C) voltage controlled capacitance.
 - D) varactor.

Diff: 2

44) An open base resistor (R_B) in a transistor switch will result in the

- A) transistor always being ON.
- B) transistor always being OFF.
- C) transistor operating in the active region.
- D) transistor being instantly destroyed.

Diff: 3

45) A transistor collector characteristic curve is a graph showing

- A) emitter current (I_E) versus collector-emitter voltage (V_{CE}) for specified values of base current (I_B).
- B) collector current (I_C) versus collector-emitter voltage (V_{CE}) for specified values of base current (I_B).
- C) collector current (I_C) versus collector-emitter voltage (V_C) for specified values of base current (I_B).
- D) collector current (I_C) versus collector-emitter voltage (V_{CC}) for specified values of base current (I_B).

Diff: 3

46) The base-to-emitter junction of a certain transistor is checked with a DMM on diode check in the forward bias direction. If the DMM indicates 0.700, the transistor is

- | | |
|------------------------------------|---------------------------------------|
| A) definitely defective. | B) silicon and measuring normal. |
| C) germanium and measuring normal. | D) open between the base and emitter. |

Diff: 2

47) If the collector resistance in a transistor amplifier is open, the dc voltage at the collector will be closest to

- | | | | |
|---------------|---------------|-----------------|---------|
| A) V_{BB} . | B) V_{CC} . | C) $V_{CC}/2$. | D) 0 V. |
|---------------|---------------|-----------------|---------|

Diff: 2

Chapter 5 Transistor Bias Circuits

- 1) Biasing a BJT amplifier means establishing dc operating voltages for proper operation.

Diff: 2

- 2) A transistor operating in saturation has very little collector current.

Diff: 2

- 3) Voltage-divider biasing is rarely used due to instability.

Diff: 2

- 4) Negative feedback in the collector-feedback circuit provides more stable operation.

Diff: 2

- 5) The correct formula for finding the dc current gain is $\beta_{DC} = I_C/I_B$.

Diff: 2

- 6) A certain transistor in a fixed-bias circuit has the following values: $I_B = 50 \mu\text{A}$, $\beta_{DC} = 125$, $V_{CC} = 18 \text{ V}$, and $R_C = 1.2 \text{ k}\Omega$. V_C is

A) 0 V. B) 7.5 V. C) 10.5 V. D) 18 V.

- Diff: 2

Adding an emitter resistor to a base-bias circuit produces a bias circuit called

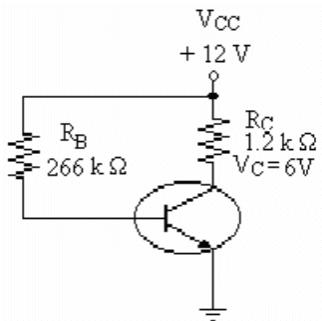
 - A) emitter bias.
 - B) base-emitter bias.
 - C) emitter-feedback bias.
 - D) None of the above.

Diff. 2

- 8) An indication of cutoff is that

A) $I_C = I_{C(sat)}$ B) $V_{CE} = 0$ V. C) $V_{BE} = 0.7$ V. D) $V_{CE} = V_{CC}$

Diff: 2



9) Refer to the figure above. This transistor is biased for _____ operation.

- A) saturation
- B) linear
- C) cutoff
- D) Either A or C above.

Diff: 2

10) Refer to the figure above. The voltage at the base of this silicon transistor is

- A) 0.3 V.
- B) 0 V.
- C) 12 V.
- D) 11.3 V.
- E) 0.7 V.

Diff: 2

11) Refer to the figure above. If $\beta_{DC} = 100$, the minimum value of I_B that would cause this transistor to saturate is

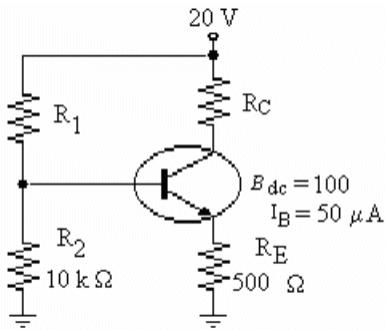
- A) 100 μA.
- B) 50 μA.
- C) 1 mA.
- D) 0.1 mA.

Diff: 3

12) Refer to the figure above. If V_C increases to 9 V, which of the following would make the dc collector voltage return to 6 V?

- A) Increase the value of R_B
- B) Replace the transistor with one with a lower β_{dc}
- C) Decrease the value of R_B
- D) Increase V_{CC}

Diff: 3



13) Refer to the figure above. The value of R_C that will produce a value of $V_C = 10$ V is

- A) 2.2 kΩ. B) 2 kΩ. C) 1 kΩ. D) 500 Ω.

Diff: 3

14) Refer to the figure above. If the transistor were replaced with a transistor whose $\beta_{DC} = 200$, the change that might occur is

- A) V_C would increase to near 20 V. B) V_C would decrease to near 0 V.
 C) I_B would increase significantly. D) V_C would change a small amount.

Diff: 3

15) Refer to the figure above. If $R_1 = 10$ kΩ, the dc voltage present at the base of this silicon transistor is

- A) 0.7 V. B) 9.1 V. C) 10 V. D) 20 V.

Diff: 3

16) Refer to the figure above. The purpose for R_1 and R_2 is to

- A) establish a dc base voltage.
 B) stabilize the operating point with negative feedback.
 C) develop the output voltage.
 D) maintain V_{BE} at 0.7 V.

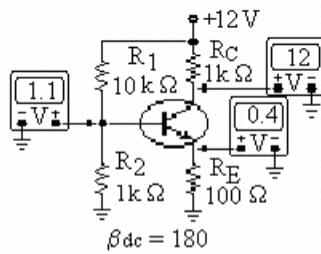
Diff: 3

17) Refer to the figure above. The purpose of R_C is to

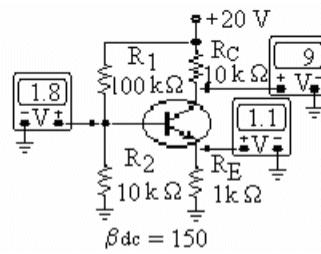
- A) establish a dc base voltage.
 B) stabilize the operating point with negative feedback.
 C) develop the output voltage.
 D) maintain V_{BE} at 0.7 V.

Diff: 2

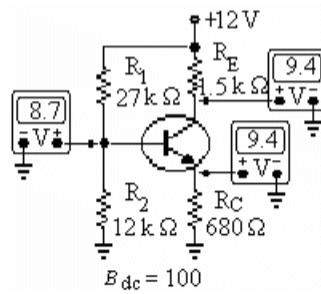
- 18) Refer to the figure above. The purpose of R_E is to
- A) establish a dc base voltage.
 - B) stabilize the operating point with negative feedback.
 - C) develop the output voltage.
 - D) maintain V_{BE} at 0.7 V.
- Diff:* 2
- 19) Two important yet easily measured quantities that can help determine if a transistor amplifier is operating correctly are
- A) β_{dc} and I_B .
 - B) I_C and V_C .
 - C) V_C and V_{BE} .
 - D) V_{BE} and I_E .
- Diff:* 2
- 20) Saturation and cutoff are operating conditions that are very useful when operating the transistor as
- A) a linear amplifier.
 - B) a switch.
 - C) a current amplifier.
 - D) None of the above.
- Diff:* 2
- 21) For linear operation, it is usual to set the Q-point so that
- A) $V_{CE} = V_{CC}$.
 - B) $V_{CE} = V_E$.
 - C) $V_{CE} = V_{CC}/4$.
 - D) $V_{CE} = V_{CC}/2$.



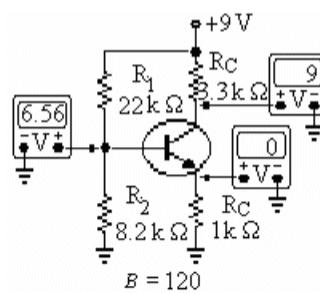
(a)



(b)



(c)



(d)

- 22) Refer to (a) in the figure above. The most probable cause of trouble, if any, from these voltage measurements would be

- A) the base-emitter junction is open.
- B) RE is open.
- C) a short from collector to emitter.
- D) There are no problems.

Diff: 3

- 23) Refer to (b) in the figure above. The most probable cause of trouble, if any, from these voltage measurements is

- A) the base-emitter junction is open.
- B) RE is open.
- C) a short from collector to emitter.
- D) There are no problems.

Diff: 3

- 24) Refer to (c) in the figure above. The most probable cause of trouble, if any, from these voltage measurements is

- A) the base-emitter junction is open.
- B) RE is open.
- C) a short from collector to emitter.
- D) There are no problems.

Diff: 3

- 25) Refer to (d) in the figure above. The most probable cause of trouble, if any, from these voltage measurements is

- A) the base-emitter junction is open.
- B) RE is open.
- C) a short from collector to emitter.
- D) There are no problems.

Diff: 3

26) The most suitable biasing technique used is the

- A) base-bias.
- B) emitter-bias.
- C) voltage-divider bias.
- D) collector-bias.

Diff: 2

27) Improper biasing can cause distortion in an amplifier's

- A) input signal.
- B) output signal.
- C) power dissipation.
- D) frequency response.

Diff: 2

28) On a dc load line, the area between saturation and cutoff is called the

- A) saturation zone.
- B) depletion region.
- C) linear region.
- D) breakdown region.

Diff: 3

29) Three different Q-points are shown on a dc load line. The upper Q-point represents the

- A) minimum current gain.
- B) intermediate current gain.
- C) maximum current gain.
- D) cutoff point.

Diff: 2

30) If a transistor operates at the middle of the dc load line, a decrease in the current gain will move the Q-point

- A) off the load line.
- B) nowhere.
- C) up.
- D) down.

Diff: 2

31) The input resistance, R_{IN} , of a voltage-divider biased NPN transistor is _____ by a factor of Beta.

- A) stepped-up
- B) stepped-down
- C) not affected
- D) None of the above.

Diff: 3

32) Voltage-divider bias provides

- A) an unstable Q-point.
- B) a stable Q-point.
- C) a Q-point that easily varies with changes in the transistor's current gain.
- D) Both A and C above.

Diff: 1

33) For transistors using voltage-divider bias, the base current should be

- A) much larger than the current through the voltage divider.
- B) about one-half the collector current.
- C) much smaller than the current through the voltage divider.
- D) Beta times larger than the collector current.

Diff: 3

34) Base bias provides

- A) a very stable Q-point.
- B) a very unstable Q-point.
- C) no current gain.
- D) zero current in the base and collector circuits.

Diff: 2

35) A circuit with a fixed emitter current is called

- | | |
|---------------|---------------------|
| A) base-bias. | B) emitter-bias. |
| C) grid-bias. | D) one-supply bias. |

Diff: 2

36) For a properly designed emitter-bias circuit, changes in current gain

- | | |
|------------------------------------|----------------------------------|
| A) do not affect the Q-point. | B) severely affect the Q-point. |
| C) do not occur in the transistor. | D) affect the collector voltage. |

Diff: 3

37) A linear amplifier should have the Q-point located

- A) close to saturation.
- B) close to cutoff.
- C) in the distortion region.
- D) approximately half-way between saturation and cutoff.

Diff: 2

38) The Q-point of a two supply emitter-bias circuit is not affected by

- | | |
|------------------------|--------------------------|
| A) V _{CC} . | B) collector resistance. |
| C) emitter resistance. | D) current gain. |

Diff: 3

39) The emitter resistor in a voltage-divider bias circuit is open. The collector voltage will equal approximately

- A) V_{CC}.
- B) 0 V.
- C) one-half V_{CC}.
- D) None of the above.

Diff: 2

40) If the base-emitter junction opens in a voltage-divider biased circuit, the emitter voltage will measure

- A) 0 V.
- B) 0.7 V less than the base.
- C) 0.7 V more than the base.
- D) a voltage nearly equal to V_{CC}.

Diff: 2

41) If the collector resistor decreases to zero in a base-biased circuit, the load line will become

- A) horizontal.
- B) vertical.
- C) useless.
- D) flat.

Diff: 3

42) The first step in analyzing emitter-biased circuits is to find the

- A) base current.
- B) emitter voltage.
- C) transistor power.
- D) collector current.

Diff: 2

43) The main difference between an NPN and PNP transistor amplifier is that

- A) PNP transistors need more heat sinking.
- B) NPN transistors are linear amplifiers, while PNP amplifiers are nonlinear.
- C) PNP transistors cannot amplify sine waves.
- D) PNP transistors require opposite bias polarities as compared to NPN.

Diff: 2

Chapter 6 BJT Amplifiers

- 1) A common-emitter amplifier has very high input impedance, high voltage gain, and high current gain.

Diff: 2

- 2) A high input impedance amplifier could be implemented with a Darlington pair.

Diff: 2

- 3) A common-collector amplifier is also known as an emitter follower.

Diff: 2

- 4) A common-base amplifier has a high current gain.

Diff: 2

- 5) The Sziklai pair uses to *pnp* transistors.

Diff: 2

- 6) A certain transistor has a dc emitter current of 25 mA. The value of r'_e is

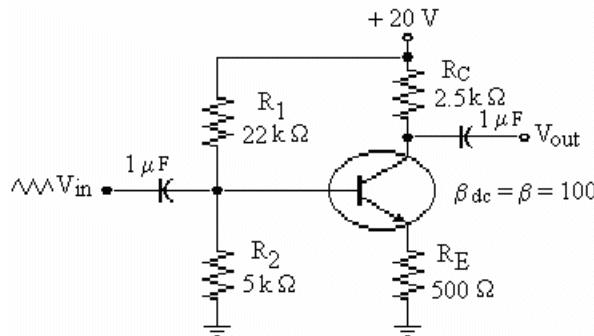
A) 25 Ω .

B) 2.5 Ω .

C) 1.2 Ω .

D) 1 Ω .

Diff: 2



- 7) Refer to the figure above. The value of V_C is

A) 20 V.

B) 10 V.

C) 5 V.

D) 0 V.

Diff: 2

- 8) Refer to the figure above. If an emitter-bypass capacitor were added, the voltage gain

A) would not change.

B) would decrease.

C) would increase.

D) would decrease to zero.

Diff: 2

9) Refer to the figure above. If R_2 opened, V_{CE} would be

- A) 0 V. B) 20 V. C) 10 V. D) 4.8 V.

Diff: 3

10) Refer to the figure above. If R_2 opened, the value of I_C would be

- A) 6 mA. B) 6.67 mA. C) 8 mA. D) 10 mA.

Diff: 3

11) Refer to the figure above. If R_C opened, V_E would

- A) increase. B) decrease.
C) remain the same. D) be undetermined.

Diff: 2

12) Refer to the figure above. If the emitter collector shorted, the voltage V_C would be

- A) 0 V. B) 20 V. C) 16.67 V. D) 3.33 V.

Diff: 2

13) Refer to the figure above. If the collector opened internally, the voltage on the collector would

- A) increase. B) decrease.
C) remain the same. D) be undetermined.

Diff: 3

14) Refer to the figure above. If $V_E = 0$, the trouble might be that

- A) R_E is open. B) R_C is open. C) R_2 is open. D) R_1 is open.

Diff: 2

15) Refer to the figure above. If an emitter-bypass capacitor were installed, the value of R_{in} would be

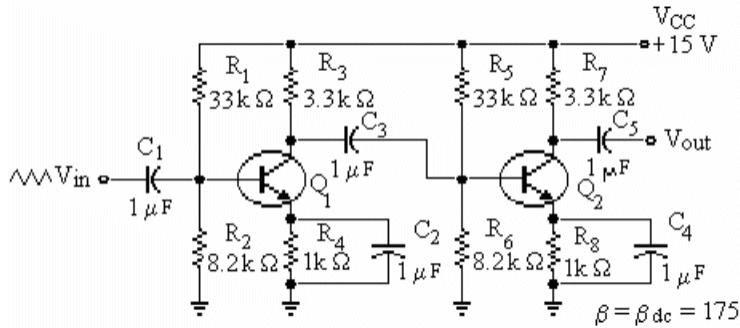
- A) 50Ω . B) 175Ω . C) 378Ω . D) 500Ω .

Diff: 2

16) Refer to the figure above. If an emitter-bypass capacitor were installed, the new A_V would be

- A) 4.96. B) 125. C) 398. D) 600.

Diff: 2



17) Refer to the figure above. If $A_{V1} = 75$ and $A_{V2} = 95$, AVT would be

- A) 75. B) 95. C) 1275. D) 7125.

Diff: 2

18) Refer to the figure above. Which of the following faults would account for the output voltage being lower than normal, but not a complete loss of output voltage?

- A) An open C1 B) An open C3 C) An open C4 D) An open C5

Diff: 3

19) Refer to the figure above. If V_{B2} were higher than normal, the problem, if any, could be that

- A) C3 is shorted. B) R3 is open. C) C1 is open. D) C2 is open.

Diff: 3

20) Refer to the figure above. In servicing this amplifier V_{out} has a dc component in addition to the normal ac output voltage. This would be caused by a(n)

- A) open C3. B) open C2.
C) open base-emitter of C2. D) shorted C5.

Diff: 3

21) Refer to the figure above. The output signal at the collector of Q1 is higher than normal. This could be caused by a(n)

- A) open C1. B) open C3.
C) open base-emitter of Q1. D) open C2.

Diff: 3

22) The best selection for a high input impedance amplifier is a

- A) low gain common-emitter. B) common-base.
C) common-collector. D) high gain common-emitter.

Diff: 2

- 23) Which of the following is not a characteristic of the common-base amplifier?
- A) High input impedance
 - B) Current gain of 1
 - C) High voltage gain
 - D) High output impedance

Diff: 2

- 24) Which of the following is not a characteristic of the emitter-follower?
- A) Voltage gain of 1
 - B) Low input impedance
 - C) Low output impedance
 - D) High current gain

Diff: 2

- 25) The best choice for a very high power amplifier is a(n)
- A) common-collector.
 - B) common-base.
 - C) common-emitter.
 - D) emitter-follower.

Diff: 2

- 26) For transistors
- A) the dc and ac current gains are the same.
 - B) the dc current gain is zero.
 - C) the dc and ac current gains are usually different.
 - D) amplification of signal voltage is not possible.

Diff: 2

- 27) The ac resistance of the emitter diode r'_e equals

$$\text{A) } \frac{25 \text{ mV}}{I_E} \quad \text{B) } 25 \text{ mV} \times I_C \quad \text{C) } \frac{25 \text{ mV}}{I_B} \quad \text{D) } \frac{25 \text{ mV}}{I_C}$$

Diff: 2

- 28) In general, coupling capacitors can be considered
- A) open for signal voltage and a short for dc.
 - B) short for signal voltage and an open for dc.
 - C) lossy.
 - D) short for signal voltage and a short for dc.

Diff: 2

- 29) The primary reason an ac load line differs from a dc load line is
- the effective ac collector resistance is greater than the dc collector resistance.
 - the effective ac collector resistance is less than the dc collector resistance.
 - changes in current are nonlinear for small-signal amplifier operation.
 - the ac load line is not as steep as the dc load line.
- Diff: 3*
- 30) The h-parameter, h_{fe} , is the same as _____ of the transistor.
- | | |
|------------------------------|-------------------------|
| A) dc Beta | B) ac Beta |
| C) maximum collector current | D) minimum hold current |
- Diff: 2*
- 31) The capacitor that produces an ac ground at a point in a circuit is called a(n)
- | | |
|----------------------|------------------------|
| A) bypass capacitor. | B) coupling capacitor. |
| C) dc short. | D) ac open. |
- Diff: 2*
- 32) Reducing all dc sources to zero is done to help obtain the
- | | |
|--------------------------------|------------------------------------|
| A) dc equivalent circuit. | B) ac equivalent circuit. |
| C) complete amplifier circuit. | D) voltage-divider biased circuit. |
- Diff: 2*
- 33) The input resistance, $R_{in(base)}$, of a common-emitter amplifier, consists of
- | | | | |
|--------------------------------|--------------------------|---------------------------------|---|
| A) $r_b \parallel \beta r_e$. | B) $\beta r_{ac} r'_e$. | C) $r_e \parallel \beta r'_e$. | D) $R_G \parallel r_c \parallel \beta r'_e$. |
|--------------------------------|--------------------------|---------------------------------|---|
- Diff: 3*
- 34) The three factors that must be taken into account when determining the actual signal voltage at the base of a small signal bipolar amplifier are
- source resistance, emitter resistance, and input resistance.
 - source resistance, bias resistance, and input resistance.
 - source resistance, collector resistance, internal resistance.
 - source resistance, bias resistance, and load resistance.
- Diff: 2*
- 35) The value of output resistance in a common-emitter amplifier, R_{out} , consists of
- | | | | |
|------------|------------------|----------------------------|--------------------------|
| A) R_C . | B) $R_L + R_C$. | C) $\beta \parallel R_C$. | D) $R_L \parallel R_C$. |
|------------|------------------|----------------------------|--------------------------|
- Diff: 2*

- 36) The voltage gain of an amplifier is defined as the
- ac input voltage divided by the ac output voltage.
 - ac collector current divided by the ac base current.
 - ac output voltage divided by the ac input voltage.
 - ac collector current divided by the ac emitter current.

Diff: 2

- 37) Removing a bypass capacitor from a fully bypassed, common-emitter amplifier circuit will _____ voltage gain and _____ ac input resistance.
- increase, decrease
 - decrease, increase
 - decrease, decrease
 - increase, increase

Diff: 3

- 38) The voltage gain of a common-emitter amplifier, A_V , can be defined as
- $A_V = \frac{V_b}{V_c}$.
 - $A_V = I_C \times R_C$.
 - $A_V = \frac{I_e R_C}{I_e r_e}$.
 - $A_V = \frac{R_C}{R_C + 1}$.

Diff: 3

- 39) For a bypass capacitor to work properly, the
- X_C should be ten times smaller than R_E at the minimum operating frequency.
 - X_C should equal R_E .
 - X_C should be ten times greater than R_E at the minimum operating frequency.
 - X_C should be twice the value of the R_E .

Diff: 2

- 40) A bypass capacitor is placed across the emitter resistor in a voltage-divider biased common-emitter amplifier circuit. This will
- place the emitter at ac ground.
 - shift the Q-point on the dc load line.
 - reduce the emitter's dc voltage to zero.
 - All of the above.

Diff: 2

- 41) Removing the emitter bypass capacitor from a common-emitter amplifier
- increases R_{in} and decreases voltage gain.
 - decreases R_{in} and increases voltage gain.
 - does not affect R_{in} .
 - increases the distortion.

Diff: 3

42) Increasing the resistance of the load resistor in an RC coupled common-emitter amplifier will have what effect on voltage gain?

- A) Does not affect the voltage gain
- B) Decreases the voltage gain
- C) Increases the voltage gain
- D) None of the above.

Diff: 3

43) Leaving some of the emitter resistance unbypassed in a common-emitter amplifier will

- A) reduce distortion.
- B) stabilize the voltage gain.
- C) increase the input impedance.
- D) All of the above.

Diff: 2

44) In a swamped amplifier, the effects of the emitter diode (r'_e) become

- A) important to voltage gain.
- B) critical to input impedance.
- C) significant to the analysis.
- D) insignificant.

Diff: 2

45) To reduce the distortion of an amplified signal, you can increase the

- A) collector resistance.
- B) emitter feedback resistance.
- C) generator resistance.
- D) load resistance.

Diff: 3

46) An emitter follower has a voltage gain that is

- A) much less than one.
- B) approximately equal to one.
- C) greater than one.
- D) zero.

Diff: 1

47) Where is the output coupling capacitor connected on a common-collector amplifier?

- A) Base
- B) Emitter
- C) Collector
- D) dc power supply

Diff: 2

48) The input resistance of the base of an emitter follower is usually

- A) low.
- B) high.
- C) shorted to ground.
- D) open.

Diff: 2

49) Often a common-collector will be the last stage before the load; the main function(s) of this stage is to

- A) provide a large voltage gain.
- B) buffer the voltage amplifiers from the low resistance load and provide impedance matching for maximum power transfer.
- C) provide phase inversion.
- D) provide a high frequency path to improve the frequency response.

Diff: 2

50) Output resistance in a common-collector amplifier circuit is stepped down by a factor of

- A) alpha α .
- B) Beta β .
- C) $R_E \parallel R_L$.
- D) $r'_e + r_e$.

Diff: 3

51) If two transistors are connected as a Darlington pair and each transistor has a Beta of 175, the overall current gain of the pair equals

- A) 30,625.
- B) 3,625.
- C) 10,000.
- D) 5,000.

Diff: 1

52) A three-stage amplifier has a gain of 20 for each stage. The overall decibel voltage gain is

- A) 60 dB.
- B) 400 dB.
- C) 78 dB.
- D) 8,000 dB.

Diff: 2

53) In a two-stage amplifier, the input resistance of the second stage

- A) does not affect the voltage gain of the first stage.
- B) affects the voltage gain of the first stage.
- C) is in parallel with the collector resistor of the first stage.
- D) Both B and C above.

Diff: 2

54) In a two-stage amplifier, the voltage gain of the first stage is 80 and the voltage gain of the second stage is 50. How much is the overall voltage gain?

- A) 72
- B) 130
- C) 4,000
- D) 400

Diff: 1

55) If a CE stage is direct coupled to an emitter-follower, how many coupling capacitors are there between the two stages?

- A) 0
- B) 1
- C) 2
- D) 3

Diff: 2

56) The quantity r'_e

- A) is external to the transistor.
- B) is temperature dependent.
- C) has no effect on gain in transistors.
- D) is a dc value.

Diff: 2

57) A differential amplifier provides an output that is the _____ of the two input quantities.

- A) square
- B) difference
- C) multiplication
- D) sine

Diff: 1

58) A differential amplifier should exhibit a _____ differential gain and a _____ common mode gain.

- A) high, low
- B) low, high
- C) high, high
- D) low, low

Diff: 2

59) Assume that a certain differential amplifier has a differential gain of 3,000 and a common mode gain of 0.25. What is the CMRR?

- A) 66.89
- B) 750
- C) 3,025
- D) 12,000

Diff: 2

60) Assume that a certain differential amplifier has a differential gain of 5,000 and a common mode gain of 0.3. What is the CMRR in dB?

- A) 0.3 dB
- B) 62.12 dB
- C) 84.44 dB
- D) 1,500 dB

Diff: 2

Chapter 7 Power Amplifiers

- 1) The class A amplifier is usually biased below cutoff.

Diff: 2

- 2) Darlington pair transistors are often used in power amplifiers because the input impedance is very low.

Diff: 2

- 3) For certain applications with low-resistance loads, a push-pull amplifier using Darlington transistors can be used to decrease the input resistance presented to the driving amplifier and avoid greatly reducing voltage gain.

Diff: 2

- 4) A class B amplifier conducts for _____ of the cycle.

A) 45° B) 90° C) 180° D) 360°

Diff: 2

- 5) The class of amplifiers that is the most efficient and has the most distortion is class _____ amplifiers.

A) A B) B C) C D) AB

Diff: 2

- 6) Push-pull amplifiers often use class _____ amplifiers.

A) A B) B or AB C) C

Diff: 2

- 7) If a class A amplifier has a voltage gain of 50 and a current gain of 75, the power gain is

A) 50. B) 75. C) 1500. D) 3750.

Diff: 2

- 8) If a class A amplifier has $R_C = 4.7 \text{ k}\Omega$ and $R_E = 1.5 \text{ k}\Omega$ and $V_{CC} = 24 \text{ V}$, $I_{C(\text{sat})}$ is

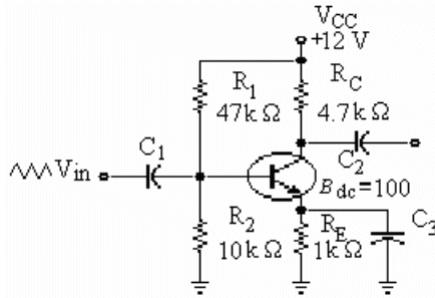
A) 5.1 mA. B) 16 mA. C) 3.87 mA. D) 0 mA.

Diff: 2

- 9) If an application for an amplifier requires operation in a linear mode, the most likely choice would be a

A) class A. B) class B. C) class C. D) class AB.

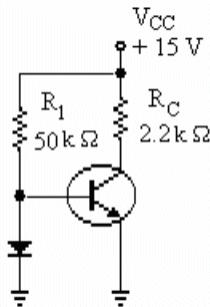
Diff: 2



- 10) Refer to the figure above. If R_1 opened, and V_{in} at the base was large, V_{out} at the collector would

- A) increase.
- B) decrease.
- C) remain the same.
- D) distort.

Diff: 3



- 11) Refer to the figure above. If the diode opened, this amplifier would be operating as

- A) class A.
- B) class B.
- C) class C.
- D) class AB.

Diff: 3

- 12) Refer to the figure above. The purpose of the diode is to bias the amplifier as

- A) class A.
- B) class B.
- C) class C.
- D) class AB.

Diff: 2

- 13) The maximum efficiency for a class A amplifier is about

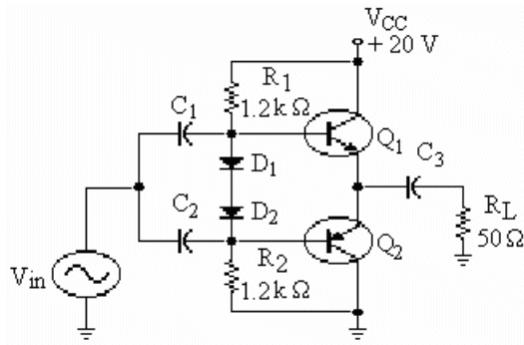
- A) 25%.
- B) 50%.
- C) 75%.
- D) 100%.

Diff: 2

- 14) The amplifier with the most distortion would be a _____ amplifier.

- A) class A
- B) class B
- C) class C
- D) class AB

Diff: 2



15) Refer to the figure above. With no signal input, the dc emitter voltage with respect to ground is

- A) 10.7 V. B) 9.3 V. C) 0 V. D) 10 V.

Diff: 2

16) Refer to the figure above. This amplifier only shows a positive alternation at the output. The possible trouble might be that

- A) C3 is shorted. B) BE1 is open. C) BE2 is open. D) R1 is open.

Diff: 3

17) Refer to the figure above. The dc voltage across R_L was measured at 10 V. A possible problem, if any, might be that

- A) C1 is open. B) C3 is shorted. C) R1 is open. D) C3 is open.

Diff: 3

18) Refer to the figure above. During the positive input alternation, Q1 is _____ and Q2 is _____.

- A) on, on B) on, off C) off, off D) off, on

Diff: 2

19) Refer to the figure above. The purpose for the diodes D1 and D2 is

- A) to apply equal signals to each transistor.
- B) to allow the correct bias voltages on the two bases.
- C) to maintain constant bias with temperature changes.
- D) All of the above.

Diff: 3

20) Refer to the figure above. The combination of the two transistors is called

- A) same.
- B) complementary.
- C) NPN.
- D) PNP.

Diff: 2

21) Refer to the figure above. This circuit is operating as a

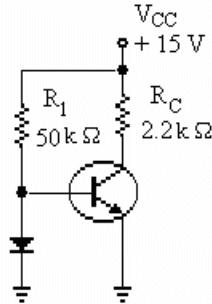
- A) class A push-pull.
- B) class AB push-pull.
- C) class C push-pull.
- D) class B push-pull.

Diff: 2

22) An application for a power amplifier to operate at radio frequencies is needed. The most likely choice would be a _____ amplifier.

- A) class A
- B) class B
- C) class C
- D) class AB

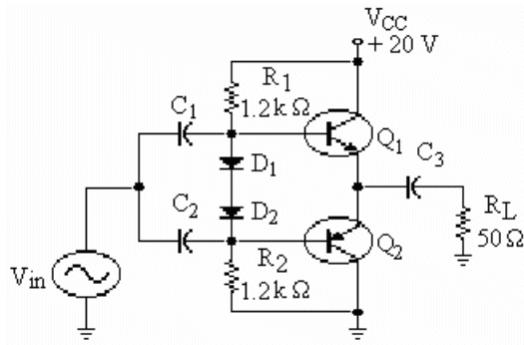
Diff: 2



23) Refer to the figure above. The approximate voltages on the base, collector, and emitter, respectively, are

- A) 0.7 V, 6.8 V, 0 V
- B) 0 V, 0 V, 0 V
- C) 0.7 V, 15 V, 0 V
- D) 0.7 V, 0 V, 15 V

Diff: 2



24) Refer to the figure above. If R_L shows a zero signal voltage on an oscilloscope, the problem might be that

- A) C_3 is open.
- B) BE1 is open.
- C) BE2 is open.
- D) R_1 is open.

Diff: 3

25) Refer to the figure above. If there were no output signal, and the measured dc voltage of Q_1 emitter were 0 V, the trouble might be that

- A) D_1 is shorted.
- B) D_2 is shorted.
- C) R_1 is open.
- D) No trouble; everything is normal.

Diff: 3

26) A class AB amplifier is biased

- A) at cutoff.
- B) slightly above the center of the load line.
- C) slightly above cutoff.
- D) at the center of the load line.

Diff: 3

27) Heat sinks reduce the

- A) transistor power.
- B) ambient temperature.
- C) junction temperature.
- D) collector current.

Diff: 1

28) An amplifier has two load lines because

- A) it has ac and dc collector resistances.
- B) it has two equivalent circuits.
- C) the dc and ac circuits are different.
- D) All of the above.

Diff: 3

29) When the Q-point is at the center of the ac load line, a maximum _____ signal can be obtained.

- A) class A
- B) class B
- C) class C
- D) None of the above.

Diff: 3

30) For maximum peak-to-peak output voltage, the Q-point should be

- A) near saturation.
- B) near cutoff.
- C) at the center of the dc load line.
- D) at the center of the ac load line.

Diff: 3

31) The ac load line is the same as the dc load line when the ac collector resistance equals the

- A) dc emitter resistance.
- B) ac emitter resistance.
- C) dc collector resistance.
- D) supply voltage divided by collector current.

Diff: 3

32) For a Q-point near the center of the dc load line, clipping is more likely to occur on the

- A) positive peak of input voltage.
- B) negative peak of output voltage.
- C) positive peak of output voltage.
- D) negative peak of emitter voltage.

Diff: 3

33) The ac load line usually

- A) equals the dc load line.
- B) has less slope than the dc load line.
- C) is steeper than the dc load line.
- D) is horizontal.

Diff: 2

34) For a class A CE amplifier, the power dissipation, PDQ

- A) is maximum when there is no input signal.
- B) increases when the peak-to-peak load voltage increases.
- C) is zero with no input signal.
- D) is maximum when the transistor is driven to cutoff.

Diff: 2

35) A CE amplifier has a load power of 10 mW and the dc power is 215 mW. The efficiency is

- A) 46.5%.
- B) 4.65%.
- C) 25%.
- D) 0%.

Diff: 2

- 36) To improve the efficiency of an amplifier, you have to
- A) reduce load power.
 - B) decrease unwanted power losses.
 - C) reduce the supply voltage.
 - D) increase the dc current.

Diff: 2

- 37) The quiescent collector current is the same as
- A) ac collector current.
 - B) ac load resistor current.
 - C) dc collector current.
 - D) None of the above.

Diff: 2

- 38) For each transistor in a class B amplifier, there is collector current for
- A) 270° of the input cycle.
 - B) 180° of the input cycle.
 - C) 360° of the input cycle.
 - D) 90° of the input cycle.

Diff: 2

- 39) In a class AB push-pull amplifier, the transistors are biased slightly above cutoff to avoid
- A) unusually high efficiency.
 - B) negative feedback.
 - C) crossover distortion.
 - D) a low input impedance.

Diff: 2

- 40) For a class AB push-pull amplifier to work properly, the emitter diodes must
- A) match the compensating diodes.
 - B) be germanium and the compensating diodes must be silicon.
 - C) be silicon and the compensating diodes must be germanium.
 - D) not match the compensating diodes.

Diff: 2

- 41) For a class AB push-pull amplifier, diode bias is used to
- A) allow the transistors to conduct for 360° .
 - B) ensure thermal runaway.
 - C) avoid thermal runaway.
 - D) saturate the output transistors.

Diff: 2

- 42) The maximum efficiency of a class B push-pull amplifier is
- A) 25 percent.
 - B) 50 percent.
 - C) 79 percent.
 - D) 100 percent.

Diff: 1

- 43) Under no-signal or quiescent conditions, the transistors of a class B push-pull amplifier
- A) have excessively high power dissipation.
 - B) get quite hot.
 - C) are in saturation.
 - D) dissipate very little power.

Diff: 2

- 44) Power MOSFETs have several advantages over bipolar power transistors. Which of the following statements is **not** correct?
- A) Less prone to ESD damage when compared to BJTs
 - B) Have simpler biasing circuits
 - C) Can be connected in parallel to increase current capacity
 - D) Have a low voltage drop across the device under high voltage and current conditions

Diff: 3

- 45) For a class C amplifier, there is collector current for
- A) 0° of the input cycle.
 - B) less than 180° of the input cycle.
 - C) 210° of the input cycle.
 - D) 360° of the input cycle.

Diff: 2

- 46) Class C amplifiers are almost always
- A) transformer-coupled between stages.
 - B) operated at audio frequencies.
 - C) tuned RF amplifiers.
 - D) wideband.

Diff: 2

- 47) The input signal of a class C amplifier
- A) is negatively clamped at the base.
 - B) is amplified and inverted.
 - C) produces brief pulses of collector current.
 - D) All of the above.

Diff: 2

- 48) The collector current of a class C amplifier
- A) is an amplified version of the input voltage.
 - B) has harmonics.
 - C) is negatively clamped.
 - D) flows for half a cycle.

Diff: 2

Chapter 8 Field-Effect Transistors (FETs)

- 1) A FET has three terminals named the source, drain, and gate.

Diff: 2

- 2) The JFET operates with a forward-biased gate-source pn junction.

Diff: 2

- 3) An E-MOSFET can be used as a switch.

Diff: 2

- 4) A D-MOSFET can operate with both positive and negative values of V_{GS} .

Diff: 2

- 5) The slope of the characteristic curve in the ohmic region of a JFET is defined by the equation:

$$R_{DS} = \frac{V_{DS}}{I_D}$$

Diff: 2

- 6) Special care is required in handling a MOSFET.

Diff: 2

- 7) JFET data sheets specify input resistance by giving the values for V_{GS} and I_{DSS} .

Diff: 2

- 8) The ohmic region of a JFET characteristic curve is roughly parabolic in shape.

Diff: 2

- 9) Under no signal conditions, midpoint bias allows the maximum amount of drain current swing between I_{DSS} and zero.

Diff: 2

- 10) A self-biased n-channel JFET has a $V_D = 8$ V, $V_{GS} = -5$ V. The value of V_{DS} is

A) 3 V.

B) 8 V.

C) -5 V.

D) -3 V.

Diff: 2

11) Field effect transistors are also known as

- A) unipolar devices.
- B) bipolar devices.
- C) three-charge carrier devices.
- D) None of the above.

Diff: 2

12) The FET that has no physical channel is

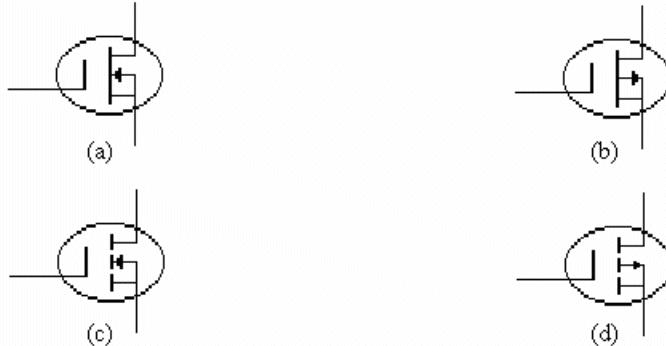
- A) the D MOSFET.
- B) the E MOSFET.
- C) the JFET.
- D) None of the above.

Diff: 2

13) A FET that has no IDSS parameter is the

- A) JFET.
- B) DE MOSFET.
- C) V MOSFET.
- D) E MOSFET.

Diff: 2



14) Refer to (a) in the figure above. This symbol identifies

- A) a p-channel E MOSFET.
- B) an n-channel D MOSFET.
- C) a p-channel D MOSFET.
- D) an n-channel E MOSFET.

Diff: 2

15) Refer to (b) in the figure above. This symbol identifies

- A) a p-channel E MOSFET.
- B) an n-channel D MOSFET.
- C) a p-channel D MOSFET.
- D) an n-channel E MOSFET.

Diff: 2

16) Refer to (c) in the figure above. This symbol identifies

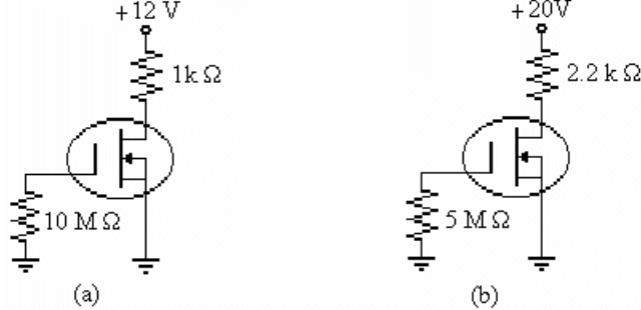
- A) a p-channel E MOSFET.
- B) an n-channel D MOSFET.
- C) a p-channel D MOSFET.
- D) an n-channel E MOSFET.

Diff: 2

17) Refer to (d) in the figure above. This symbol identifies

- A) a p-channel E MOSFET.
B) an n-channel D MOSFET.
C) a p-channel D MOSFET.
D) an n-channel E MOSFET.

Diff: 2



18) Refer to (a) in the figure above. If $I_D = 4 \text{ mA}$, the value of V_{DS} is

- A) 12 V.
B) 8 V.
C) 4 V.
D) 0 V.

Diff: 2

19) Refer to (b) in the figure above. If $I_D = 4 \text{ mA}$, the value of V_{GS} is

- A) 20 V.
B) 11.2 V.
C) 8.8 V.
D) 0 V.

Diff: 2

20) Refer to (b) in the figure above. If $I_D = 2 \text{ mA}$, the value of V_{DS} is

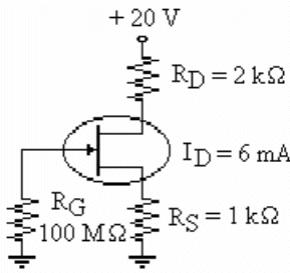
- A) 4.4 V.
B) 10 V.
C) 15.6 V.
D) 20 V.

Diff: 2

21) A JFET manufacturer's data sheet specifies $V_{GS(\text{off})} = -8 \text{ V}$ and $I_{DSS} = 6 \text{ mA}$. When $V_{GS} = -4 \text{ V}$, the value of I_D would be

- A) 6 mA.
B) 1.25 mA.
C) 1.5 mA.
D) 4 mA.

Diff: 3



22) Refer to the figure above. The value of the voltage drop across R_D is

- A) 20 V. B) 12 V. C) 6 V. D) 3 V.

Diff: 2

23) Refer to the figure above. This amplifier is biased for

- | | |
|----------------------|---------------------------|
| A) linear operation. | B) pinch-off operation. |
| C) saturation. | D) operation as a switch. |

Diff: 2

24) Refer to the figure above. In this circuit, V_{GS} is biased correctly for proper operation. This means that

V_{GS} is

- | | |
|---------------------------------|--------------|
| A) positive. | B) negative. |
| C) either negative or positive. | D) 0 V. |

Diff: 3

25) Refer to the figure above. Calculate the value of V_D .

- A) 20 V B) 8 V C) 6 V D) 2 V

Diff: 2

26) Refer to the figure above. Calculate the value of V_{DS} .

- A) 0 V B) 2 V C) 4 V D) -2 V

Diff: 2

27) For proper operation, an n-channel E-MOSFET should be biased so that V_{GS} is

- | | |
|---------------------------------|--------------|
| A) either positive or negative. | B) negative. |
| C) positive. | D) -4 V. |

Diff: 2

- 28) A good application for a VMOSFET would be as a
- A) power amplifier.
 - B) low power amplifier.
 - C) low input impedance device.
 - D) substitute for a diode.

Diff: 2

- 29) A VMOSFET device operates in
- A) the depletion mode.
 - B) the enhancement mode.
 - C) a JFET mode.
 - D) in either enhancement or depletion mode.

Diff: 2

- 30) The gate-source junction of a JFET is
- A) normally not biased.
 - B) normally forward-biased.
 - C) normally reverse-biased.
 - D) a low resistance path for dc current when reverse-biased.

Diff: 2

- 31) The channel width in a JFET is controlled by
- A) varying gate voltage.
 - B) varying drain voltage.
 - C) increasing forward bias on the gate-source junction.
 - D) increasing reverse bias on the drain-source junction.

Diff: 2

- 32) When operated in the ohmic area, a JFET acts like a(n)
- A) small resistor.
 - B) voltage source.
 - C) current source.
 - D) insulator.

Diff: 2

- 33) V_{DS} equals pinch-off voltage divided by the
- A) base current.
 - B) gate current.
 - C) ideal drain current.
 - D) drain current for zero gate voltage.

Diff: 3

34) I_{DSS} can be defined as the

- A) minimum possible drain current.
- B) maximum possible current with the drain shorted to the source.
- C) maximum current drain-to-source with a shorted gate.
- D) maximum drain current with the source shorted.

Diff: 2

35) The pinch-off voltage has the same magnitude as the

- A) gate voltage.
- B) drain-source voltage.
- C) gate-source voltage.
- D) gate-source cutoff voltage.

Diff: 3

36) JFETs are often called

- A) one-way switches.
- B) two-way switches.
- C) bipolar devices.
- D) unipolar devices.

Diff: 2

37) The transconductance curve of a JFET is a graph of

- A) I_S versus V_{DS} .
- B) I_C versus V_{CE} .
- C) I_D versus V_{GS} .
- D) $I_D \propto R_{DS}$.

Diff: 2

38) For a JFET, there is maximum drain current when

- A) V_{GS} equals $V_{GS(\text{off})}$.
- B) V_{DS} is zero.
- C) the drain and source are interchanged.
- D) V_{GS} is zero.

Diff: 2

39) The transconductance curve of a JFET is

- A) hyperbolic.
- B) linear.
- C) nonlinear.
- D) symmetrical.

Diff: 2

40) A _____ change in V_{DS} will produce a _____ change in I_D .

- A) small, large
- B) large, small
- C) large, large
- D) small, small

Diff: 3

- 41) To get a negative gate-source voltage in a self-biased JFET circuit, you must use a
- A) voltage divider.
 - B) source resistor.
 - C) ground.
 - D) negative gate supply voltage.

Diff: 3

- 42) The easiest way to bias a JFET in the ohmic region is with
- A) voltage-divider bias.
 - B) self-bias.
 - C) gate bias.
 - D) source bias.

Diff: 3

- 43) One advantage of voltage-divider bias is that the dependency of drain current I_D , on the range of Q-points is
- A) increased.
 - B) reduced.
 - C) not affected.
 - D) None of the above.

Diff: 2

- 44) The depletion-mode MOSFET can
- A) operate with only positive gate voltages.
 - B) operate with only negative gate voltages.
 - C) not operate in the ohmic region.
 - D) operate with positive as well as negative gate voltages.

Diff: 2

- 45) An n-channel E-MOSFET conducts when it has
- A) $V_{GS} > V_P$.
 - B) a thin layer of positive charges in the substrate region near the SiO_2 layer.
 - C) $V_{DS} > 0$.
 - D) a thin layer of negative charges in the substrate region near the SiO_2 layer.

Diff: 3

- 46) For an enhancement-mode MOSFET, the minimum V_{GS} required to produce drain current is called the
- A) threshold voltage, designated $V_{GS(\text{th})}$.
 - B) blocking voltage, designated V_B .
 - C) breakdown voltage.
 - D) I_{Dss} .

Diff: 2

- 47) Special handling precautions should be taken when working with MOSFETs. Which of the following is **not** one of these precautions?
- A) All test equipment should be grounded.
 - B) MOSFET devices should have their leads shorted together for shipment and storage.
 - C) Never remove or insert MOSFET devices with the power on.
 - D) Workers handling MOSFET devices should not have grounding straps attached to their wrists.

Diff: 2

- 48) The simplest method to bias a D-MOSFET is to

- A) set $V_{GS} = +4$.
- B) set $V_{GS} = -4$.
- C) set $V_{GS} = 0$.
- D) select the correct value R_D .

Diff: 3

- 49) The type(s) of bias most often used with E-MOSFET circuits is

- A) drain-feedback.
- B) constant current.
- C) voltage-divider.
- D) Both A and C above.

Diff: 2

Chapter 9 FET Amplifiers and Switching Circuits

- 1) The formula for the voltage gain of a common-source amplifier is R_D/g_m .

Diff: 2

- 2) Load resistance added to the output of an amplifier increases the voltage gain.

Diff: 2

- 3) The addition of a source bypass capacitor will increase the voltage gain.

Diff: 2

- 4) FETs are superior to BJTs in almost all switching applications.

Diff: 2

- 5) FET amplifiers generally have lower distortion than BJT amplifiers.

Diff: 2

- 6) Cascode amplifiers are used primarily in radio frequency applications.

Diff: 2

- 7) Most of the gain in a JFET-based cascode amplifier is provided by the CS amplifier.

Diff: 3

- 8) Class D amplifiers usually employ JFETs.

Diff: 2

- 9) The 3 stages in a class D amplifier are the pulse-width-modulator, the switching amplifier, and the low-pass filter.

Diff: 3

- 10) A pulse-width-modulator employs a square-wave generator and a comparator.

Diff: 3

- 11) A MOSFET switch is turned on and off by changing the source voltage.

Diff: 2

- 12) An analog MOSFET switch is turned on when the gate receives a positive voltage pulse.

Diff: 2

13) CMOS combines n-channel and p-channel D-MOSFETS.

Diff: 3

14) Power MOSFETs have a negative temperature coefficient and therefore are less prone to thermal runaway.

Diff: 3

15) In an amplifier using a JFET, the gate current is approximately 0.

Diff: 2

16) A common-source amplifier has a _____ phase shift between the input and the output.

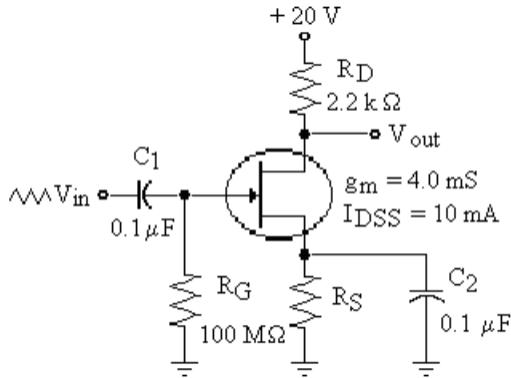
A) 45°

B) 90°

C) 180°

D) 360°

Diff: 2



17) Refer to the figure above. Assuming midpoint biasing, if V_{GS} = -4 V, the value of R_S that will provide this value is

A) 600 Ω.

B) 1.2 kΩ.

C) 80 Ω.

D) 800 Ω.

Diff: 2

18) Refer to the figure above. If V_{in} = 50 mVp-p, the output voltage is

A) 50 mVp-p.

B) 4.4 Vp-p.

C) 0.044 Vp-p.

D) 440 mVp-p.

Diff: 3

19) Refer to the figure above. If the measured value of V_{out} were below normal, the problem might be that

A) R_D is open.

B) C₂ is shorted.

C) C₂ is open.

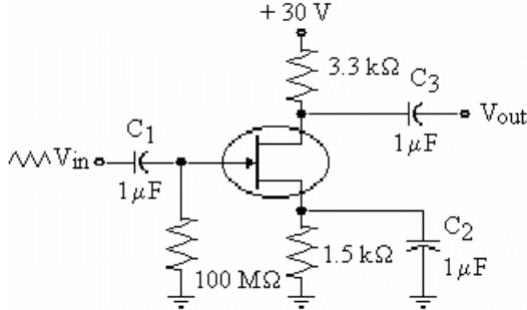
D) V_{in} has increased.

Diff: 3

20) Refer to the figure above. If $V_{in} = 1 \text{ V}_{\text{p-p}}$, the output voltage V_{out} would be

- A) undistorted.
 - B) clipped on the negative peaks.
 - C) clipped on the positive peaks.
 - D) 0 V.

Diff: 2



21) Refer to the figure above. If $I_D = 6 \text{ mA}$, the value of V_{GS} is

- A) 9 V. B) -9 V. C) -19.8 V. D) -10.2 V.

Diff: 2

22) Refer to the figure above. If $g_m = 6500 \mu\text{S}$ and an input signal of $125 \text{ mV}_{\text{p-p}}$ is applied to the gate, the output voltage V_{out} is

- A) 2.68 V_{P-P}. B) 0.8125 V_{P-P}. C) 1.625 V_{P-P}. D) 6.25 V_{P-P}.

Diff: 2

23) Refer to the figure above. If C₂ opened, the output signal would

- A) increase in value.
 - B) decrease in value.
 - C) not change.
 - D) decrease and then increase.

Diff: 2

24) Refer to the figure above. If $ID = 4 \text{ mA}$, $IDSS = 16 \text{ mA}$, and $V_{GS(\text{off})} = -8 \text{ V}$, V_{DS} would be

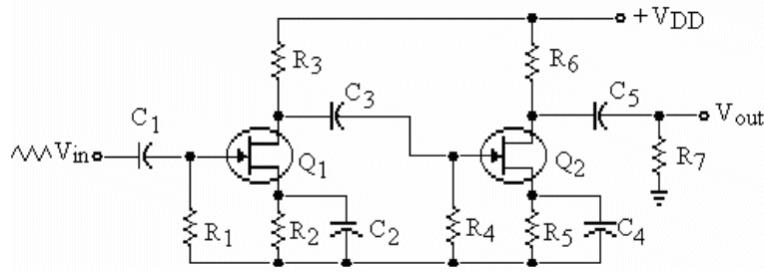
- A) 19.2 V. B) -6 V. C) 10.8 V. D) 30 V.

Diff: 2

25) Refer to the figure above. If $g_m = 4000 \mu\text{S}$ and a signal of 75 mV rms is applied to the gate, the p-p output voltage is

- A) 990 mV. B) 1.13 V_{p-p}. C) 2.8 V_{p-p}. D) 990 V_{p-p}.

Diff: 3



26) Refer to the figure above. If R_7 were to increase in value, V_{out} would

- A) increase.
- B) decrease.
- C) remain the same.
- D) distort.

Diff: 3

27) Refer to the figure above. If C_2 opened, V_{out} would

- A) increase.
- B) decrease.
- C) remain the same.
- D) distort.

Diff: 2

28) Refer to the figure above. If R_1 opened, V_{out} would

- A) increase.
- B) decrease.
- C) remain the same.
- D) distort.

Diff: 3

29) Refer to the figure above. If C_3 opened, V_{out} would

- A) increase.
- B) decrease.
- C) remain the same.
- D) distort.

Diff: 2

30) Refer to the figure above. If R_3 opened, V_{out} would

- A) increase.
- B) decrease.
- C) remain the same.
- D) distort.

Diff: 2

31) Refer to the figure above. If R_5 opened, V_{out} would

- A) increase.
- B) decrease.
- C) remain the same.
- D) distort.

Diff: 2

32) Refer to the figure above. If the source-drain of Q2 shorted, the output signal from Q1 would

- A) increase.
- B) decrease.
- C) remain the same.
- D) distort.

Diff: 3

33) Refer to the figure above. If $AV_1 = 18$ and $AV_t = 288$, the value of AV_2 would be

- A) 5184.
- B) 18.
- C) 49.18.
- D) 16.

Diff: 2

34) Refer to the figure above. If C_4 opened, the signal voltage at the drain of Q1 would

- A) increase.
- B) decrease.
- C) remain the same.
- D) distort.

Diff: 3

35) Refer to the figure above. If C_5 opened, the signal voltage across R_7 would

- A) increase.
- B) be zero.
- C) remain the same.
- D) distort.

Diff: 3

36) What component of an FET amplifier needs to be at least ten times greater than R_D to ensure maximum voltage gain?

- A) $r'_d s$
- B) R_S
- C) R_S
- D) g_m

Diff: 2

37) In a self-biased common-source amplifier, what purpose does resistor R_G serve?

- A) Keeps the gate at approximately zero volts
- B) Develops the gate-source bias current
- C) Prevents loading of the ac signal source
- D) Both A and C above.

Diff: 3

38) A CS amplifier has a voltage gain of

- A) $g_m R_d$.
- B) $g_m R_s$.
- C) $\frac{g_m R_s}{(1 + g_m R_d)}$.
- D) $\frac{g_m R_d}{(1 + g_m R_d)}$.

Diff: 3

39) The capacitor connected to the source of a common source amplifier

- A) is used for input coupling.
- B) is used for output coupling.
- C) makes the source an ac ground point.
- D) is needed for extra power supply filtering.

Diff: 2

40) Approximately how much signal voltage should be measured at the bypassed source of a common source amplifier?

- A) V_{in}
- B) $\frac{V_{in}}{2}$
- C) the same amount as the drain
- D) 0 V

Diff: 2

41) A source follower has a voltage gain of

- A) gmR_d .
- B) $\frac{gm}{R_S}$.
- C) $\frac{gmR_s}{(1 + gmR_S)}$.
- D) $\frac{gmR_d}{(1 + gmR_d)}$.

Diff: 2

42) When the input signal is large, a source follower has

- A) a voltage gain of less than one.
- B) a small distortion.
- C) a high input resistance.
- D) All of the above.

Diff: 2

43) Changing _____ can control the voltage gain of a common-source amplifier.

- A) the input voltage
- B) gm
- C) V_{DD}
- D) R_S

Diff: 2

44) Where is the input signal applied in a common-gate amplifier?

- A) Source
- B) Gate
- C) Drain
- D) Base

Diff: 1

45) If the interstage coupling capacitor opens in a two stage FET amplifier, the output signal will

- A) double in amplitude.
- B) be slightly decreased.
- C) be slightly increased.
- D) be zero.

Diff: 2

52) Which of the following is not a FET amplifier?

- A) Source-follower
- B) Common-gate
- C) Emitter-follower
- D) Common-drain

Diff: 1

53) If R_S is not bypassed

- A) the dc power supply will have excessive ripple.
- B) the gain will be extremely high.
- C) the gain will be reduced.
- D) no signal will be coupled to the output.

Diff: 2

54) Two common-source amplifiers are cascaded. The overall phase shift from the input of the first amplifier to the output of the second amplifier is

- A) 0° .
- B) 45° .
- C) 90° .
- D) 180° .

Diff: 2

55) Which of the following is not part of a class D amplifier?

- A) oscillator
- B) pulse-width modulator
- C) low-pass filter
- D) switching amplifier

Diff: 3

56) Which of the following is not a characteristic of a JFET-based cascode amplifier?

- A) high input resistance
- B) high input capacitance
- C) high frequency response
- D) high gain

Diff: 3

57) What is the role of the low-pass filter in a class D amplifier?

- A) limit amplifier frequency response
- B) remove hum
- C) prevent oscillation
- D) remove the modulating frequency and harmonics

Diff: 3

58) Which of the following is not an application of an analog MOSFET switch

- A) sample-and-hold circuit
- B) analog multiplexer
- C) inverter
- D) switched capacitor circuit

Diff: 2

Chapter 10 Amplifier Frequency Response

- 1) Coupling and bypass capacitors limit the low-frequency response of an amplifier.

Diff: 2

- 2) High-frequency response is limited by the internal capacitances of a transistor.

Diff: 2

- 3) At the cutoff frequency, the output is down by 3 dB.

Diff: 2

- 4) An octave of frequency is a ten-times change.

Diff: 2

- 5) The bandwidth is the sum of the two cutoff frequencies.

Diff: 2

- 6) To effectively analyze an RC coupled amplifier's high frequency response, you only need to consider the coupling and bypass capacitances. The internal capacitance can be ignored.

Diff: 2

- 7) If an amplifier has an output voltage of 12.7 V_{p-p} at the midpoint of the frequency range, the output voltage at the cutoff frequency would be

A) 12.7 V_{p-p}. B) 4.49 V_{p-p}. C) 5.89 V_{p-p}. D) 8.98 V_{p-p}.

Diff: 2

- 8) If an amplifier has an input signal voltage of 0.37 mV and an output voltage of 16.8 V, the voltage gain in dB would be

A) 45.4 dB. B) 33.1 dB. C) 93.1 dB. D) 46.6 dB.

Diff: 2

- 9) If an amplifier has a voltage gain of 54 dB, and an input signal of 22 mV, the output signal voltage would be

A) 11 V. B) 55.3 V. C) 2.45 V. D) 24.5 V.

Diff: 3

- 10) If an amplifier has a bandwidth of 47 kHz and a higher cutoff frequency of 104 kHz, the lower cutoff frequency would be

A) 151 kHz. B) 57 kHz. C) 47 kHz. D) 104 kHz.

Diff: 2

- 11) If an amplifier has an $R_{in} = 950 \Omega$, and a coupling capacitor of value $3.3 \mu F$, the approximate cutoff frequency would be

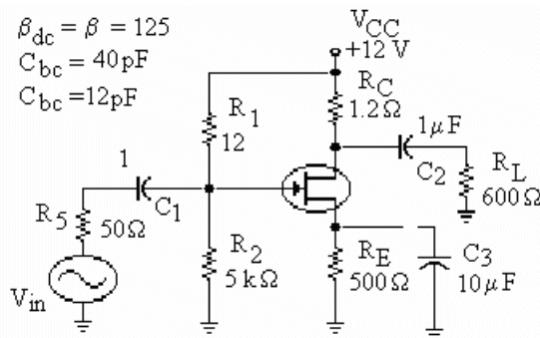
A) 508 Hz. B) 50.8 kHz. C) 50.8 Hz. D) 5.08 Hz.

Diff: 2

- 12) The f_C of a certain RC network that has values of $R = 470 \Omega$ and $C = 0.005 \mu F$ is

A) 67.7 kHz. B) 425 kHz. C) 213 kHz. D) 12 kHz.

Diff: 2



- 13) Refer to the figure above. Low frequency response is affected by

A) R_C . B) C_{BE} .
C) C_3 . D) All of the above.

Diff: 2

- 14) Refer to the figure above. High frequency response is affected by

A) R_C . B) C_{BE} .
C) C_3 . D) All of the above.

Diff: 2

- 15) Refer to the figure above. If the output voltage at the upper cutoff frequency was 7.19 Vp-p , the output voltage that would be expected at the lower cutoff frequency is

A) 5.08 Vp-p . B) 7.19 Vp-p . C) 10.17 Vp-p . D) 2.11 Vp-p .

Diff: 3

16) Refer to the figure above. The output voltage at f_{cl} is 22 mV. Ideally, V_{out} at the midpoint frequency would be

- A) 22 mV.
B) 17 mV.
C) 31.1 mV.
D) Not enough information to determine.

Diff: 3

17) Refer to the figure above. The bandwidth of this amplifier is

- A) the sum of the upper and lower frequencies.
B) the upper frequency divided by 0.707.
C) the difference between the upper and lower frequencies.
D) the lower frequency times 0.707.

Diff: 3

18) Refer to the figure above. The capacitance C_{bc} affects

- A) high-frequency response.
B) low-frequency response.
C) mid-range response.
D) nothing.

Diff: 2

19) Refer to the figure above. A definite reduction in the output voltage is noticed. The trouble is that

- A) C_3 has shorted.
B) C_1 has opened.
C) C_2 has opened.
D) C_3 has opened.

Diff: 3

20) Refer to the figure above. The reduction in the output at very high frequencies is due to

- A) the negative feedback effect of R_E .
B) the negative feedback effect of C_{bc} .
C) the positive feedback effect of V_{BE} .
D) R_L decreasing in value.

Diff: 2

21) Refer to the figure above. If the output voltage at f_{cl} is 12 mV, the actual output voltage at the midpoint frequency would be

- A) 12 mV.
B) 12 mVp-p.
C) 16.97 mV.
D) 8.48 mV.

Diff: 2

22) Refer to the figure above. If R_L increases in value, the output voltage would

- A) increase.
B) decrease.
C) remain the same.
D) Cannot be determined.

Diff: 2

23) A Bode plot

- A) is a testing method used for dc amplifiers.
- B) provides a visual presentation of decibel voltage gain vs. frequency.
- C) indicates voltage gain with no reference to frequency.
- D) indicates voltage gain only at 0 Hz.

Diff: 2

24) The cutoff frequency of a low pass filter occurs at

- A) -5 dB.
- B) -3 dB.
- C) +3 dB.
- D) -20 dB.

Diff: 2

25) A high pass filter may be used to

- A) pass low frequencies.
- B) pass high frequencies.
- C) pass frequencies between low and high.
- D) Both A and B above.

Diff: 2

26) A roll-off of 20 dB per decade is equivalent to a roll-off of _____ per octave.

- A) 3 dB
- B) 13 dB
- C) 12 dB
- D) 6 dB

Diff: 2

27) Which of the following capacitances affects the high frequency response of an amplifier?

- A) Stray wiring capacitance
- B) Internal pn junction capacitance
- C) Coupling and bypass capacitors
- D) Both A and B above.

Diff: 1

28) At low frequencies, the coupling capacitors produce a decrease in

- A) input resistance.
- B) voltage gain.
- C) generator resistance.
- D) generator voltage.

Diff: 2

29) If the value of a feedback capacitor is 50 pF, what is the input Miller capacitance when $A_V = 200$?

- A) 1 μ F
- B) 10 μ F
- C) 100 μ F
- D) 10 nF

Diff: 2

- 30) The critical frequencies of an amplifier are the frequencies where the output voltage is
A) half of V_{mid} . B) 0.707 of V_{mid} . C) zero. D) 0.25 of V_{mid} .

Diff: 2

- 31) The voltage gain of an amplifier is 200. The decibel voltage gain is
A) 23 dB. B) 46 dB. C) 200 dB. D) 106 dB.

Diff: 2

- 32) If the voltage gain doubles, the decibel voltage gain increases by
A) a factor of 2. B) 3 dB. C) 6 dB. D) 10 dB.

Diff: 2

- 33) In the midband of a CE amplifier
A) the emitter is not at ac ground.
B) the Miller effect has maximum influence.
C) the voltage gain is maximum.
D) the coupling and bypass capacitors appear open.

Diff: 2

- 34) If the power gain doubles, the decibel power gain increases by
A) a factor of 2. B) 3 dB. C) 6 dB. D) 10 dB.

Diff: 2

- 35) At low frequencies, the emitter-bypass capacitor
A) is no longer an ac short. B) has minimum X_C .
C) increases the output voltage. D) increases the voltage gain.

Diff: 2

- 36) Raising the frequency of 1 kHz by 2 octaves results in a frequency of
A) 4 kHz. B) 500 Hz. C) 250 Hz. D) 2 MHz.

Diff: 2

- 37) The frequency response of an amplifier is a graph of
A) voltage versus current. B) voltage versus time.
C) output voltage versus frequency. D) input voltage versus frequency.

Diff: 1

- 38) The voltage gain of an amplifier is 150. If the output voltage doubles (for the same amount of input voltage), the voltage gain equals

A) 21.7 db. B) 43.5 db. C) 49.5 db. D) 114 db.

Diff: 2

- 39) At the lower or upper cutoff frequency, the voltage gain is

A) 0.35 Av_{mid}. B) 0.5 Av_{mid}.
C) 0.707 Av_{mid}. D) 0.995 Av_{mid}.

Diff: 1

- 40) Phase shift in the input of an RC circuit will approach 90° when frequency approaches

A) zero. B) maximum. C) mid-range. D) cutoff.

Diff: 2

- 41) What effect does low frequency have on the emitter bypass RC circuit?

A) Decreases impedance and increases voltage gain
B) Increases impedance and decreases voltage gain
C) Increases impedance and increases voltage gain
D) Decreases impedance and decreases voltage gain

Diff: 2

- 42) For a lag network above the cutoff frequency, the voltage gain

A) decreases at the rate of 20 db per decade.
B) increases at the rate of 6 db per octave.
C) decreases at the rate of 6 db per octave.
D) A and C above.

Diff: 3

- 43) Semilog graph paper has

A) two (2) linear axis.
B) one vertical linear axis and one logarithmic horizontal axis.
C) one horizontal linear axis and one vertical logarithmic axis.
D) two (2) logarithmic axis.

Diff: 1

44) The unity-gain frequency (f_T) equals the product of mid-range voltage gain ($A_V(\text{mid})$) and the

- A) compensating capacitance.
- B) f_{cu} .
- C) BW.
- D) load resistance.

Diff: 2

45) At the unity-gain frequency, the open-loop voltage gain is

- A) 1.
- B) A_{mid} .
- C) zero.
- D) very large.

Diff: 2

Chapter 11 Thyristors

- 1) The SCR is a device that can be triggered on by a pulse applied to the gate.

Diff: 2

- 2) A device that conducts current in only one direction is called a diac.

Diff: 2

- 3) A device that can be turned on or off by a gate pulse is called an SCS.

Diff: 2

- 4) A triac can be turned on by a pulse applied to the gate.

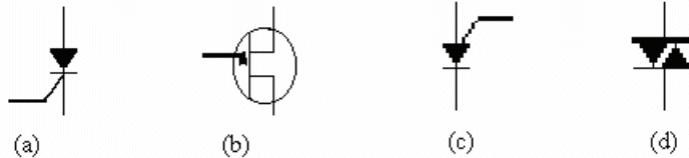
Diff: 2

- 5) A UJT is turned on by a negative pulse at the base.

Diff: 2

- 6) The forced commutation method requires momentarily forcing current in the direction opposite to the reverse conduction so that the net reverse current is reduced below the holding value.

Diff: 3



- 7) Refer to (a) in the figure above. The symbol is for

A) a triac. B) a UJT. C) a diac. D) a PUT. E) an SCR.

Diff: 2

- 8) Refer to (b) in the figure above. The symbol is for

A) a triac. B) a UJT. C) a diac. D) a PUT. E) an SCR.

Diff: 2

- 9) Refer to (c) in the figure above. The symbol is for

A) a triac. B) a UJT. C) a diac. D) a PUT. E) an SCR.

Diff: 2

- 10) Refer to (d) in the figure above. The symbol is for
A) a triac. B) a UJT. C) a diac. D) a PUT. E) an SCR.

Diff: 2

- 11) To avoid confusing the schematic symbols for a JFET and a UJT, keep in mind that the UJT symbol
A) has two circles.
B) has no arrow.
C) uses a dot.
D) has four terminals.
E) has an arrow at an angle.

Diff: 2

- 12) A good choice to trigger a triac would be a(n)
A) 4-layer diode. B) SCR.
C) diac. D) Schockley diode.

Diff: 2

- 13) The best choice to control a small variable speed ac motor is a(n)
A) triac. B) diac. C) SCR. D) UJT. E) PUT.

Diff: 2

- 14) The best choice to shut down a dc power supply in case of an abnormally high voltage condition is a(n)
A) triac. B) diac. C) SCR. D) UJT. E) PUT.

Diff: 2

- 15) Each of the following has a gate except the
A) triac. B) diac. C) SCR. D) PUT.

Diff: 2

- 16) The most likely device to be used in an oscillator is a(n)
A) triac. B) diac. C) SCR. D) UJT. E) PUT.

Diff: 2

- 17) An SCS has a unique ability to
A) be turned on or off with a pulse. B) be turned off only with a pulse.
C) control a PUT. D) All of the above.

Diff: 2

18) If an SCR starts to conduct when a gate current is established, when the gate circuit is interrupted the SCR

- A) will turn off.
- B) current will increase.
- C) will continue to conduct.
- D) gate current will increase.

Diff: 3

19) An SCR will turn off when the voltage across it is

- A) increased to the supply voltage.
- B) decreased to near 0 V.
- C) timed out.
- D) decreased by the value of the gate voltage.

Diff: 2

20) A triac is used for ac because

- A) it conducts on both alternations.
- B) it is turned off when the ac voltage reaches zero.
- C) it can deliver more power to the load in a cycle.
- D) All of the above.

Diff: 2

21) A device is needed to trigger an SCR. One possible device to use might be a(n)

- A) SCR.
- B) UJT.
- C) Schockley diode.
- D) PUT.

Diff: 2

22) The best device to be used to control a dc motor is the

- A) triac.
- B) PUT.
- C) SCR.
- D) diac.

Diff: 2

23) An SCR is used to control the speed of a dc motor by _____ the _____ of the pulse delivered to the motor.

- A) varying, width
- B) increasing, amplitude
- C) decreasing, gate width
- D) None of the above.

Diff: 3

- 24) Of the following applications, the likely one to use a diac is a(n)
- A) battery charger.
 - B) oscillator.
 - C) high frequency amplifier.
 - D) lamp dimmer.

Diff: 2

- 25) If the gate circuit is open on a triac used for ac motor control, the motor
- A) can never turn on.
 - B) will constantly run at half speed.
 - C) will constantly run at full speed.
 - D) will run at 60 RPM.

Diff: 3

- 26) A thyristor can be used as
- A) a resistor.
 - B) an amplifier.
 - C) a switch.
 - D) a power source.

Diff: 2

- 27) The minimum input current that can turn on a thyristor is called the
- A) holding current.
 - B) switching current.
 - C) breakdown current.
 - D) low-current dropout current.

Diff: 2

- 28) The minimum current that keeps a latch closed is called the
- A) pick-up current.
 - B) critical rate of current rise.
 - C) trigger current.
 - D) holding current.

Diff: 2

- 29) The only way to make a four-layer diode conduct is with
- A) a trigger input applied to the gate.
 - B) forward breakdown voltage.
 - C) low-current dropout.
 - D) None of the above.

Diff: 3

- 30) The only way to stop an SCR that is conducting is by
- A) a positive trigger.
 - B) low-current drop out.
 - C) breakdown.
 - D) reverse-bias triggering.

Diff: 2

31) A silicon controlled rectifier has

- A) two external leads.
- B) three external leads.
- C) four external leads.
- D) three doped regions.

Diff: 1

32) An SCR is usually turned on by

- A) breakdown.
- B) a gate trigger.
- C) breakdown.
- D) holding current.

Diff: 2

33) SCRs are

- A) low-power devices.
- B) four-layer diodes.
- C) high-current devices.
- D) bidirectional.

Diff: 2

34) The trigger voltage of an SCR is closest to

- A) 0 V.
- B) 0.7 V.
- C) 4 V.
- D) breakdown voltage.

Diff: 2

35) The voltage across a conducting SCR

- A) equals the breakdown voltage.
- B) is approximately zero.
- C) decreases with more anode current.
- D) equals the source voltage.

Diff: 2

36) Disconnecting the gate lead on an SCR

- A) will result in maximum gate current.
- B) results in the SCR staying on all the time.
- C) destroys the device.
- D) means that the SCR cannot be triggered on.

Diff: 3

37) A conducting SCR can be turned off by

- A) reducing the source voltage to zero.
- B) opening the anode circuit.
- C) temporarily shorting across the SCR's anode to cathode.
- D) All of the above.

Diff: 2

38) An SCR crowbar circuit is used to

- A) protect against undervoltage conditions.
- B) detect when a circuit is overheating.
- C) protect against overvoltage conditions.
- D) control three phase ac motors.

Diff: 2

39) Once a diac is conducting, the only way to turn it off is with

- A) low-current dropout.
- B) breakdown.
- C) a negative gate voltage.
- D) a positive gate voltage.

Diff: 2

40) The diac is equivalent to

- A) two four-layered diodes in parallel.
- B) two SCRs in parallel.
- C) two four-layer diodes in series.
- D) two triacs in parallel.

Diff: 3

41) The diac is a

- A) transistor.
- B) unidirectional device.
- C) three-layer device.
- D) bidirectional device.

Diff: 2

42) A triac acts like

- A) two SCRs in parallel.
- B) two SCRs in series.
- C) two diacs in parallel.
- D) a normal transistor.

Diff: 1

43) A triac

- A) can trigger only on positive gate voltages.
- B) can trigger only on negative gate voltages.
- C) can be triggered by either a positive or a negative gate voltage.
- D) cannot be triggered with gate voltages.

Diff: 2

44) A silicon-controlled switch

- A) has only 1 gate lead.
- B) has two gate leads.
- C) can only be turned off with low-current dropout.
- D) is bidirectional.

Diff: 2

45) A UJT has

- A) two base leads.
- B) one emitter lead.
- C) two emitter and one base leads.
- D) both A and B above.

Diff: 2

46) For a UJT, the intrinsic standoff ratio is

- A) equal to 1.
- B) always greater than 1.
- C) always less than 1.
- D) usually around 1 k Ω or so.

Diff: 2

47) The PUT (Programmable Unijunction Transistor) is actually a type of

- A) thyristor.
- B) FET device.
- C) triac.
- D) SCR.

Diff: 2

Chapter 12 The Operational Amplifier

- 1) A good op-amp has high voltage gain, low output impedance, and high input impedance.

Diff: 2

- 2) An inverting amplifier has an input resistance equal to the input resistor.

Diff: 2

- 3) CMRR is the measure of an op-amp's voltage gain for an inverting amplifier.

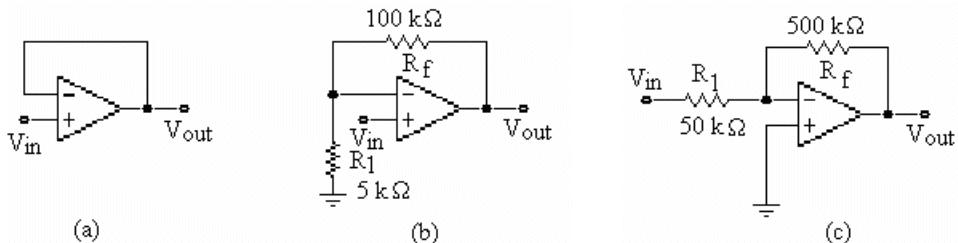
Diff: 2

- 4) The differential amplifier is used as the input stage of an operational amplifier.

Diff: 2

- 5) A voltage follower has a very high input impedance, and is often used as a high voltage gain amplifier.

Diff: 2



- 6) Refer to the figure above. Which circuit is the inverting amplifier?

A) (a)

B) (b)

C) (c)

D) None of the above.

Diff: 2

- 7) Refer to the figure above. Which circuit is a voltage follower?

A) (a)

B) (b)

C) (c)

D) None of the above.

Diff: 2

- 8) Refer to the figure above. Which circuit is the noninverting amplifier?

A) (a)

B) (b)

C) (c)

D) None of the above.

Diff: 2

9) Refer to the figure above. Which circuit has a voltage gain of 1?

- A) (a) B) (b)
C) (c) D) None of the above.

Diff: 2

10) See the figure above. Which circuit has an input impedance of about $5\text{ k}\Omega$?

- A) (a) B) (b)
C) (c) D) None of the above.

Diff: 3

11) Refer to the figure above. Which circuit has a voltage gain of 10?

- A) (a) B) (b)
C) (c) D) None of the above.

Diff: 2

12) Refer to the figure above. Which circuit has a voltage gain of 20?

-3

13) Refer to (a) in the figure above. If this circuit has a $V_{in} = 12$ V_{p-p}, the value of V_{out} would be

- A) 20 V B) -20 V C) 8.48 V_{p-p} D) 12 V_{p-p}

Diff: 2

14) Refer to (b) in the figure above. If this circuit has a $V_{in} = 0.7$ V, V_{out} would be

- A) 14.7 V B) -14.7 V C) 14 V D) 0 V

Diff. 2

15) Refer to (c) in the figure above. $V_{in} = -60$ mV. The value of V_{out} is

- A) 600 mV B) -600 mV C) 660 mV D) about 16 V

Diff. 2

16) See the figure above. If these three circuits were connected as a multiple-stage amplifier, the total voltage gain would be

- A) 1 B) 10 C) 21 D) 210

Diff. 2

17) Refer to (c) in the figure above. If R_f is changed to $1 \text{ M}\Omega$, the new A_{cl} would be

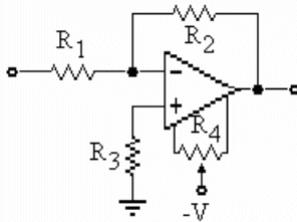
- A) 20. B) -20. C) 21. D) -21.

Diff: 2

18) Refer to (c) in the figure above. If an amplifier with an input impedance of $12 \text{ k}\Omega$ and the same voltage gain is needed, the new value of R_1 would be _____ and the new value of R_f would be _____.

- A) $10 \text{ k}\Omega, 100 \text{ k}\Omega$ B) $13.3 \text{ k}\Omega, 120 \text{ k}\Omega$
C) $12 \text{ k}\Omega, 108 \text{ k}\Omega$ D) $12 \text{ k}\Omega, 120 \text{ k}\Omega$

Diff: 2



19) Refer to the figure above. This op-amp has a slew rate of $1.33 \text{ V}/\mu\text{s}$. How long would it take the output voltage to change from -12 V to $+12 \text{ V}$?

- A) $18 \mu\text{s}$ B) $16 \mu\text{s}$ C) $36 \mu\text{s}$ D) $48 \mu\text{s}$

Diff: 2

20) Refer to the figure above. Which components are used to set input impedance and voltage gain?

- A) R_4 B) R_3 C) R_1 and R_2 D) R_3 and R_4

Diff: 2

21) Refer to the figure above. Which components are used for offset voltage compensation?

- A) R_4 B) R_3 C) R_1 and R_2 D) R_2

Diff: 3

22) Refer to the figure above. Which components are used for bias current compensation?

- A) R_4 B) R_3 C) R_1 and R_2 D) R_2

Diff: 2

23) Refer to the figure above. The purpose of R₁ and R₂ is

- A) for bias current compensation.
- B) for input offset voltage compensation.
- C) to set input impedance only.
- D) to set input impedance and voltage gain.

Diff: 2

24) It takes an op-amp 22 μ s to change its output from -15 V to +15 V. The slew rate for this amplifier is

- A) 1.36 V/ μ s.
- B) 0.68 V/ μ s.
- C) 0.73 V/ μ s.
- D) 660 V/ μ s.

Diff: 2

25) A voltage follower amplifier comes to you for service. With a sine wave input of 1 V, the output is squared off at approximately 30 V peak-to-peak. The most likely problem is

- A) no dc supply voltage.
- B) the input is shorted to ground.
- C) open feedback loop.
- D) the output is shorted to ground.

Diff: 3

26) The op-amp can amplify

- A) ac signals only.
- B) dc signals only.
- C) both ac and dc signals.
- D) neither ac nor dc signals.

Diff: 1

27) The typical input stage of an op-amp has a(n)

- A) emitter follower.
- B) single-ended input and differential output.
- C) push-pull circuit.
- D) two-input differential amplifier.

Diff: 2

28) The common-mode signal is applied to

- A) the noninverting input.
- B) the inverting input.
- C) both inputs.
- D) None of the above.

Diff: 2

- 29) If an op-amp were perfect, the CMRR would
- A) be zero.
 - B) approach infinity.
 - C) be very small.
 - D) be less than one.

Diff: 2

- 30) In an op-amp, the CMRR is limited mostly by the
- A) the common-mode gain of the op-amp.
 - B) gain-bandwidth product.
 - C) supply voltages.
 - D) tolerance of the resistors.

Diff: 2

- 31) The open-loop voltage gain (A_{OL}) of an op-amp is the
- A) external voltage gain the device is capable of.
 - B) internal voltage gain the device is capable of.
 - C) most controlled parameter.
 - D) same as A_{CM} .

Diff: 2

- 32) The input offset current is
- A) the difference between the input bias currents.
 - B) not related to the input bias currents.
 - C) less than the input offset voltage.
 - D) unimportant when a base resistor is used.

Diff: 2

- 33) With both inputs grounded, the only offset that produces an error is the
- A) input offset current.
 - B) input bias current.
 - C) input offset voltage.
 - D) input short circuit current.

Diff: 2

- 34) The input offset current equals the
- A) difference between two base currents.
 - B) average of two base currents.
 - C) collector current divided by current gain.
 - D) difference between two base-emitter voltages.

Diff: 2

35) The ideal op-amp has

- A) infinite input impedance and zero output impedance.
- B) infinite output impedance and zero input impedance.
- C) infinite voltage gain and infinite bandwidth.
- D) Both A and C.

Diff: 2

36) The two basic ways of specifying input impedance of an op-amp are

- A) differential and extremely high.
- B) differential and common-loop.
- C) differential and common-mode.
- D) closed-loop and common-mode.

Diff: 2

37) What type of input is provided to an op-amp for slew-rate measurement?

- A) Constant dc voltage
- B) Sinusoidal voltage
- C) Step input voltage
- D) Triangle waveform

Diff: 2

38) When the initial slope of a sine wave is greater than the slew rate

- A) distortion occurs.
- B) the output looks exactly like the input.
- C) voltage gain is maximum.
- D) the op-amp works best.

Diff: 2

39) Which op-amp parameter is dependent upon the high frequency response of the amplifier stages inside the op-amp?

- A) Input bias current
- B) Short-circuit output current
- C) Slew rate
- D) Input offset voltage

Diff: 2

40) With negative feedback, the returning signal

- A) aids the input signal.
- B) opposes the input signal.
- C) is proportional to output current.
- D) is proportional to differential voltage gain.

Diff: 2

- 41) The closed-loop voltage gain of an inverting amplifier equals
- A) the ratio of the input resistance to the feedback resistance.
 - B) the open-loop voltage gain.
 - C) the feedback resistance divided by the input resistance.
 - D) the input resistance.

Diff: 2

- 42) An inverting amplifier with a gain of -8 means that
- A) the signal is attenuated by a factor of 8.
 - B) ac and dc signals are increased by a factor of 8 with no phase shift.
 - C) the signal amplitude is increased by a factor of 8 with a 180° phase shift.
 - D) the stage reduces the signal by a factor of 8 from input to output.

Diff: 2

- 43) The voltage follower has a
- A) closed-loop voltage gain of unity.
 - B) small open-loop voltage gain.
 - C) closed-loop bandwidth of zero.
 - D) large closed-loop output impedance.

Diff: 2

- 44) The feedback fraction " B "
- A) is always less than 1.
 - B) is usually greater than 1.
 - C) may equal 1.
 - D) may not equal 1.

Diff: 2

- 45) The loop gain $AOLB$
- A) is usually much smaller than 1.
 - B) is usually much greater than 1.
 - C) may not equal 1.
 - D) is between 0 and 1.

Diff: 2

- 46) There can be no current to ground through
- A) a mechanical ground.
 - B) an ac ground.
 - C) a virtual ground.
 - D) an ordinary ground.

Diff: 2

47) The closed-loop input impedance in a noninverting amplifier is

- A) much greater than the open-loop input impedance.
- B) equal to the open-loop input impedance.
- C) sometimes less than the open-loop input impedance.
- D) ideally zero.

Diff: 2

48) What is the value of compensating resistor needed for a noninverting op-amp circuit using 10 k Ω resistors for both R_I and R_F ?

- A) 5 k Ω
- B) 10 k Ω
- C) 20 k Ω
- D) 100 k Ω

Diff: 2

49) The voltage gain of an op-amp is unity at the

- A) cutoff frequency.
- B) unity-gain frequency.
- C) generator frequency.
- D) power bandwidth.

Diff: 2

50) For a given op-amp, which of these is constant?

- A) $f_C(CL)$
- B) feedback voltage
- C) AOL
- D) AOL $f_c(OL)$

Diff: 3

51) If the unit-gain frequency is 10 MHz and the mid-band open-loop voltage gain is 200,000, the cutoff frequency is

- A) 5 kHz.
- B) 50 Hz.
- C) 5 Hz.
- D) 25 MHz.

Diff: 1

Chapter 13 Basic Op-Amp Circuits

- 1) An op-amp comparator has an output dependent upon the polarities of the two inputs.

Diff: 2

- 2) The output voltage of a summing amplifier is proportional to the product of the input voltages.

Diff: 2

- 3) Integration is a mathematical process for determining the area under a curve.

Diff: 2

- 4) A square wave input to an op-amp integrator will produce a sine wave output.

Diff: 2

- 5) Bounding allows the op-amp to have unlimited output voltage up to the value of the supply voltages.

Diff: 2

- 6) An op-amp has an open-loop gain of 100,000. $V_{sat} = +/-12\text{ V}$. A differential signal voltage of $150\text{ }\mu\text{V}_{\text{p-p}}$ is applied between the inputs. The output voltage is

A) 12 V.

B) -12 V.

C) 12 $\text{V}_{\text{p-p}}$.

D) 24 $\text{V}_{\text{p-p}}$.

Diff: 2

- 7) A summing amplifier can add

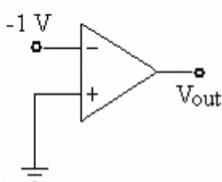
A) dc voltages.

B) ac voltages.

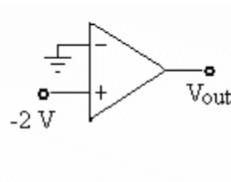
C) dc to ac voltages.

D) All of the above.

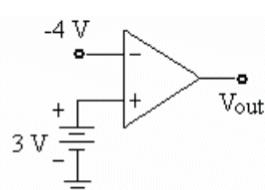
Diff: 2



(a)



(b)



(c)

- 8) Refer to (a) in the figure above. If $V_{CC} = 15\text{ V}$, the approximate output voltage is

A) 1 V.

B) -1 V.

C) 13 V.

D) -13 V.

Diff: 2

9) Refer to (b) in the figure above. If $V_{sat} = \pm 12$ V, the approximate output voltage is

- A) 12 V. B) -12 V. C) 2 V. D) -2 V.

Diff: 2

10) Refer to (c) in the figure above. With the inputs shown, the output voltage would be

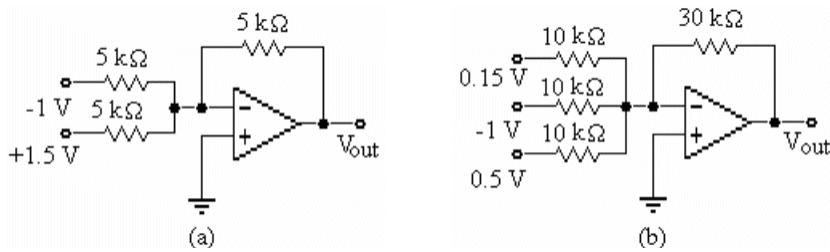
- A) 7 V. B) -7 V. C) $+V_{sat}$. D) $-V_{sat}$.

Diff: 2

11) Each of the following is used to establish a reference voltage on a comparator input except a

- A) voltage divider. B) zener diode.
C) LED. D) battery.

Diff: 2



12) Refer to (a) in the figure above. If a solder splash shorted the two ends of the feedback resistor to each other, the output voltage would be

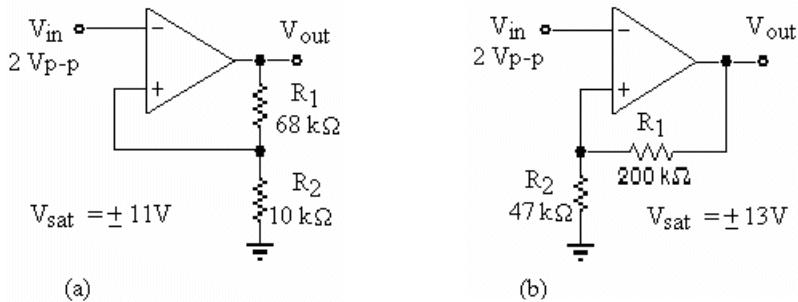
- A) 0.5 V. B) -0.5 V. C) 0 V. D) $-V_{sat}$.

Diff: 3

13) Refer to (b) in the figure above. A voltmeter placed from the inverting input to ground would read

- A) -0.925 V . B) -2.775 V . C) 2.775 V . D) $\approx 0\text{ V}$.

Diff: 3



14) Refer to (a) in the figure above. This circuit is known as a

- A) multivibrator.
- B) zero level detector.
- C) comparator with hysteresis.
- D) noninverting amplifier.

Diff: 2

15) Refer to (b) in the figure above. This type of circuit will usually have

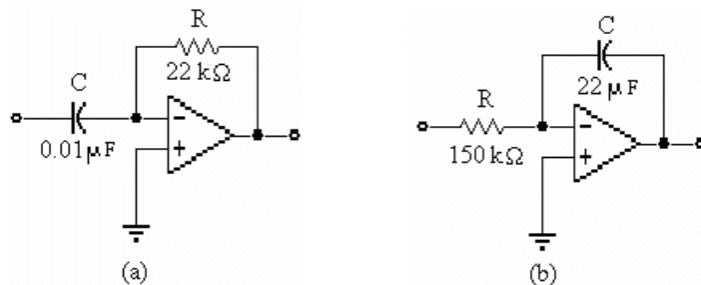
- A) a square wave output if the input is a sine wave.
- B) a triangle wave output.
- C) a ramp output for a square wave input.
- D) None of the above.

Diff: 2

16) Refer to (b) in the figure above. The output voltage with the inputs as shown is

- A) $+V_{sat}$.
- B) $-V_{sat}$.
- C) 26 Vp-p.
- D) 17.06 Vp-p.

Diff: 3



17) See (a) in the figure above. This circuit is known as

- A) a noninverting amplifier.
- B) an integrator.
- C) a differentiator.
- D) a summing amplifier.

Diff: 2

18) Refer to the figure above. Which of these circuits is known as an integrator?

- A) (a) B) (b) C) Neither of the above.

Diff: 2

19) Refer to (b) in the figure above. A square wave input is applied to this circuit. The output voltage is most likely to be

- A) a square wave.
 - B) a triangle wave.
 - C) a sine wave.
 - D) no output.

Diff: 2

20) A Schmitt trigger is a comparator with

- A) hysteresis.
 - B) one trigger point.
 - C) two trigger points.
 - D) A and C above.

Diff: 2

21) An op-amp has an open-loop gain of 90,000. $V_{sat} = \pm 13$ V. A differential voltage of 0.1 V_{p-p} is applied between the inputs. The output voltage is

- A) 13 V. B) -13 V. C) 13 V_{p-p.} D) 26 V_{p-p.}

Diff: 3

22) The output of a Schmitt trigger is a

- A) triangle wave. B) sine wave. C) sawtooth. D) square wave.

Diff: 2

23) An integrator circuit

- A) uses a capacitor in its feedback circuit.
 - B) produces a ramp voltage at its output for a step input voltage.
 - C) uses an inductor in its feedback circuit.
 - D) A and B above.

Diff: 2

24) A differentiator circuit

- A) uses a resistor in its feedback circuit.
 - B) uses a capacitor in its feedback circuit.
 - C) produces a square wave at its output for a triangle wave input.
 - D) A and C above.

Diff: 2

25) Hysteresis voltage is defined as

- A) the voltage of the lower trigger point.
- B) the voltage of the upper trigger point.
- C) the difference in voltage between the upper and the lower trigger points.
- D) the sum of voltages of the upper and the lower trigger points.

Diff: 2

26) A comparator is an example of a(n)

- A) active filter.
- B) current source.
- C) linear circuit.
- D) nonlinear circuit.

Diff: 2

27) If the input to a comparator is a sine wave, the output is a

- A) ramp voltage.
- B) sine wave.
- C) rectangular wave.
- D) sawtooth wave.

Diff: 2

28) A zero crossing detector is a

- A) comparator with no output.
- B) comparator with a trip point referenced to zero.
- C) peak detector.
- D) limiter.

Diff: 2

29) A window comparator

- A) has only one usable threshold.
- B) uses hysteresis to speed up response.
- C) clamps the input positively.
- D) detects an input voltage between two limits.

Diff: 2

30) A Schmitt trigger has

- A) only one trip point.
- B) only negative feedback.
- C) two slightly different trip points.
- D) a triangular output.

Diff: 2

31) A Schmitt trigger is a comparator with

- A) negative feedback.
- B) positive feedback.
- C) Neither A nor B.
- D) Both A and B.

Diff: 2

32) The _____ circuit overcomes the problem of false switching caused by noise on the input(s).

- A) input buffer
- B) Schmitt trigger
- C) input noise eliminator
- D) differentiator

Diff: 2

33) The amount of hysteresis in a Schmitt trigger is defined by

$$A) V_{UTP} - V_{LTP}. \quad B) V_{UTP} \times V_{LTP}. \quad C) \frac{V_{UTP}}{V_{LTP}}. \quad D) V_{UTP} + V_{LTP}.$$

Diff: 3

34) Output bounding is the process of _____ the output voltage range of a comparator.

- A) extending
- B) limiting
- C) comparing
- D) filtering

Diff: 2

35) If all the resistors in a summing amplifier are equal, the output will be equal to the

- A) average of the individual inputs.
- B) inverted average of the individual inputs.
- C) sum of the individual inputs.
- D) inverted sum of the individual inputs.

Diff: 2

36) If the value of resistor R_f in a averaging amplifier circuit is equal to the value of one input resistor divided by the number of inputs, the output will be equal to

- A) average of the individual inputs.
- B) inverted average of the individual inputs.
- C) sum of the individual inputs.
- D) inverted sum of the individual inputs.

Diff: 3

37) The _____ input makes the summing amplifier circuit possible.

- A) virtual ground at the noninverting
- B) virtual ground at the inverting
- C) low voltage
- D) high voltage

Diff: 3

- 38) A D/A converter is an application of the
- A) adjustable bandwidth circuit.
 - B) noninverting amplifier.
 - C) voltage-to-current converter.
 - D) scaling adder.

Diff: 2

- 39) In an op-amp integrator, the current through the input resistor is into the
- A) inverting input.
 - B) noninverting input.
 - C) bypass capacitor.
 - D) feedback capacitor.

Diff: 2

- 40) A mathematical operation that determines the rate of change of a curve is called
- A) differentiation.
 - B) integration.
 - C) curve averaging.
 - D) linear regression.

Diff: 2

- 41) A mathematical operation for finding the area under the curve of a graph is called
- A) differentiation.
 - B) integration.
 - C) curve averaging.
 - D) linear regression.

Diff: 2

- 42) The formula $I_C = \left[\frac{V_C}{t} \right] C$ shows that for a given capacitor, if the voltage changes at a constant rate with respect to time, then current will
- A) increase.
 - B) decrease.
 - C) be constant.
 - D) decrease logarithmically.

Diff: 3

- 43) The output of an op-amp differentiator with a rectangular input is a
- A) series of positive and negative spikes.
 - B) sine wave.
 - C) ramp voltage.

Diff: 2

- 44) A bounded comparator uses _____ in the feedback circuit.
- A) equal-valued resistors
 - B) zener diodes
 - C) an inductor
 - D) a resonant filter

Diff: 2

- 45) A two-input summing amplifier has input voltages of 3 V and 4 V. If R_f is open, the output voltage will be approximately

C) $+V_{sat}$. D) $-V_{sat}$.

Diff: 3

- 46) An R/2R ladder circuit would be found in a

C) Schmitt trigger circuit. D) D/A converter circuit.

Diff: 2

Chapter 14 Special-Purpose Op-Amp Circuits

- 1) A basic instrumentation amplifier has three op-amps.

Diff: 2

- 2) One of the key characteristics of an instrumentation amplifier is its low input impedance.

Diff: 2

- 3) The voltage gain of an instrumentation amplifier is set with an external resistor.

Diff: 2

- 4) A basic isolation amplifier has two electrically isolated sections.

Diff: 2

- 5) Most modern isolation amplifiers use transformer coupling for isolation.

Diff: 2

- 6) OTA stands for operational transistor amplifier.

Diff: 2

- 7) A log amplifier has a JFET in the feedback loop.

Diff: 2

- 8) An antilog amplifier has a BJT in series with the input.

Diff: 2

- 9) The main purpose of an instrumentation amplifier is to amplify common mode voltage.

Diff: 2

- 10) The OTA is a voltage-to-current amplifier.

Diff: 2

- 11) Linear signal compression scales down all signal levels by the same amount.

Diff: 2

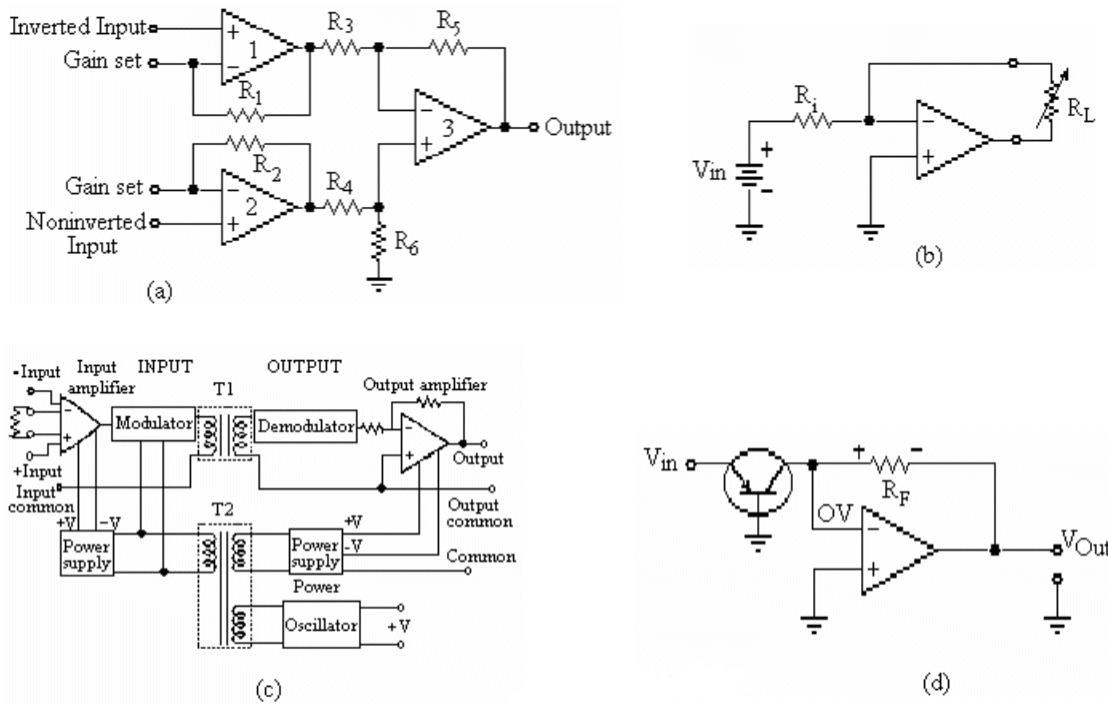
- 12) The OTA has a _____ input impedance and a _____ CMRR.

A) high, low

B) low, high

C) high, high

Diff: 2



13) Refer to the figure above. Which of these circuits is known as an antilog amplifier?

- A) (a) B) (b) C) (c) D) (d)

Diff: 2

14) Refer to the figure above. Which of these circuits is known as a constant-current source?

- A) (a) B) (b) C) (c) D) (d)

Diff: 2

15) Refer to the figure above. Which of these circuits is known as an isolation amplifier?

- A) (a) B) (b) C) (c) D) (d)

Diff: 2

16) Refer to the figure above. Which of these circuits is known as an instrumentation amplifier?

- A) (a) B) (b) C) (c) D) (d)

Diff: 2

17) Refer to (a) in the figure above. If $R_1 = R_2 = 30 \text{ k}\Omega$ and the closed loop gain is 450, the value of the external gain-setting resistor R_G is

- A) 133.63 $\text{k}\Omega$.
 B) 133.63 Ω .
 C) 13.36 Ω .
 D) None of the above.

Diff: 2

18) Refer to (a) in the figure above. If $R_1 = R_2 = 28 \text{ k}\Omega$ and $R_G = 100 \Omega$, the A_{cl} would be

- A) 5.60. B) 56.1. C) 561. D) 560.

Diff: 2

19) Refer to (b) in the figure above. If $V_{in} = 5 \text{ V}$ and $R_{in} = 22 \text{ k}\Omega$, the current thru the load R_L would be

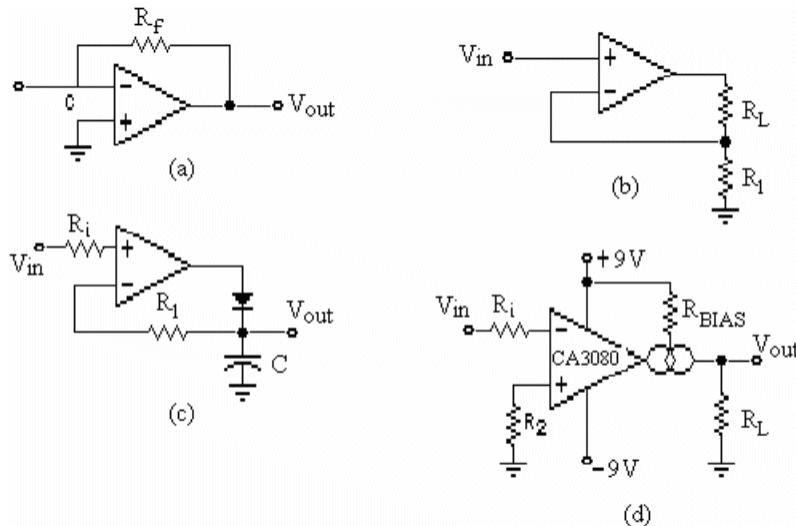
- A) 227.27 mA. B) 2.27 mA. C) 22.72 mA. D) 227.27 μA .

Diff: 2

20) Refer to (d) in the figure above. If $V_{in} = 200 \text{ mV}$, $R_F = 52 \text{ k}$, and $I_{EBO} = 50 \text{ nA}$, the V_{out} would be

- A) 7.75 mV. B) -5.41 mV. C) -7.75 V. D) -775 mV.

Diff: 2



21) Refer to the figure above. Which of these circuits is known as a voltage-to-current converter?

- A) (a) B) (b) C) (c) D) (d)

Diff: 2

22) Refer to the figure above. Which of these circuits is known as a current-to-voltage converter?

- A) (a) B) (b) C) (c) D) (d)

Diff: 2

23) Refer to the figure above. Which of these circuits contains an OTA?

- A) (a) B) (b) C) (c) D) (d)

Diff: 2

24) Refer to the figure above. Which of these circuits is known as a peak detector?

- A) (a) B) (b) C) (c) D) (d)

Diff: 2

25) Refer to (b) in the figure above. If $R_L = 20 \text{ k}\Omega$, $R_1 = 1.2 \text{ k}\Omega$, and $V_{in} = 2.5 \text{ V}$, the load current I_L would be

- A) 20.83 mA. B) 2.083 mA. C) 2.083 A. D) 208.3 μA .

Diff: 2

26) Refer to (d) in the figure above. If $g_m = 25 \text{ mS}$ and $R_L = 25 \text{ k}\Omega$, the voltage gain would be

- A) 625. B) 62.5.
C) 6.25. D) Not enough information is given.

Diff: 2

27) The input signal for an instrumentation amplifier usually comes from

- A) an inverting amplifier. B) a filtered dc power supply.
C) a differential amplifier. D) a Wheatstone bridge.

Diff: 2

28) Instrumentation amplifiers are well suited for environments with

- A) no signal and no noise.
B) high signal levels that need to be attenuated.
C) no power supply voltages.
D) small signals superimposed on larger common-mode voltages.

Diff: 3

29) An instrumentation amplifier has a high

- A) output impedance. B) power gain.
C) CMRR. D) supply voltage.

Diff: 2

30) An input transducer converts

- A) voltage to current.
B) current to voltage.
C) an electrical quantity to a nonelectrical quantity.
D) a nonelectrical quantity to an electrical quantity.

Diff: 2

- 31) In some respects an isolation amplifier is nothing more than an elaborate
- A) op-amp.
 - B) instrumentation amplifier.
 - C) rectifier and filter.
 - D) Both A and B above.

Diff: 2

- 32) The primary function of the oscillator in an isolation amplifier is to
- A) convert dc to high frequency ac.
 - B) convert dc to low frequency ac.
 - C) rectify high frequency ac to dc.
 - D) produce dual polarity dc voltages for the input to the demodulator.

Diff: 3

- 33) The voltage gain of an OTA can be calculated using the formula

$$\begin{array}{ll} \text{A) } AV = \frac{R_f}{R_i}. & \text{B) } AV = g_m R_L. \\ \text{C) } AV = \left[\frac{R_f}{R_i} \right] + 1. & \text{D) } AV = \frac{2R_f}{R_i}. \end{array}$$

Diff: 2

- 34) If an operational transconductance amplifier (OTA) is used as a nonlinear mixer and an audio signal is mixed with an RF signal, the output will be a(n) _____ signal.
- A) square wave
 - B) triangular wave
 - C) frequency modulated (FM)
 - D) amplitude modulated (AM)

Diff: 3

- 35) When using an OTA in a Schmitt-trigger configuration, the trigger points are controlled by
- A) the I_{OUT} .
 - B) the I_{BIAS} .
 - C) the V_{OUT} .
 - D) Both A and B above.

Diff: 3

- 36) An antilog amplifier is formed by connecting a pn junction (diode or BJT) to the
- A) input.
 - B) output.
 - C) feedback loop.
 - D) inverting and noninverting inputs.

Diff: 3

37) To scale down large signal voltages without obscuring lower signal voltages, _____ should be used.

- A) signal compression
- B) logarithmic signal compression
- C) natural logarithmic signal compression
- D) antilogarithmic signal compression

Diff: 3

38) A voltage-to-current converter is used in applications where it is necessary to have an output load current that is controlled by

- A) input voltage.
- B) input resistance.
- C) output resistance.
- D) input frequency.

Diff: 3

39) The output of a peak detector is always

- A) 70.7% of input.
- B) equal to the max value of the peak level received since the last reset pulse.
- C) equal to the min value of the peak level received since the last reset pulse.
- D) None of the above.

Diff: 2

40) Which of the following correctly describes the relationship between bandwidth and gain for an instrumentation amplifier?

- A) Instrumentation amplifiers have no bandwidth since they can only amplify dc.
- B) Bandwidth and gain are both zero.
- C) Bandwidth increases as gain increases.
- D) Bandwidth decreases as gain increases.

Diff: 3

41) Isolation amplifiers can accomplish isolation using

- A) transformer coupling.
- B) optical coupling.
- C) capacitive coupling.
- D) All of the above.

Diff: 2

42) The voltage gain of the input stage of an isolation amplifier is 12. If the output stage has a gain of 6, the total voltage gain is

- A) 6.
- B) 18.
- C) 72.
- D) 144.

Diff: 2

- 43) The total voltage gain of an isolation amplifier is 49. If the voltage gain of the input and output stages are equal, the voltage gain for each stage is

A) 4.9.

B) 7.

C) 24.5.

D) 98.

Diff: 3

- 44) Log amplifiers are used to

A) compress an analog signal.

B) linearize an exponential output from a transducer.

C) perform analog multiplication and division.

D) All of the above.

Diff: 2

- 45) What is the required value of feedback resistance needed in a current-to-voltage converter where each 100 μ A of input current needs to result in an output of 1 V?

A) 1 k Ω

B) $10\text{ k}\Omega$

C) $1 \text{ M}\Omega$

D) $10 \text{ M}\Omega$

46) The current applied to a current-to-voltage converter circuit changes from 4 to 20 mA. If R_f is 625 Ω , what is the change in output voltage?

A) 1 V

B) 5 V

C) 10 V

D) 20 V

Diff: 2

Chapter 15 Active Filters

- 1) The bandwidth of a band-pass filter is the difference between the two cutoff frequencies.

Diff: 2

- 2) Butterworth filters have a roll-off of 40 dB/decade and a widely varying output in the passband.

Diff: 2

- 3) A high-pass filter passes high frequencies easily and attenuates all others.

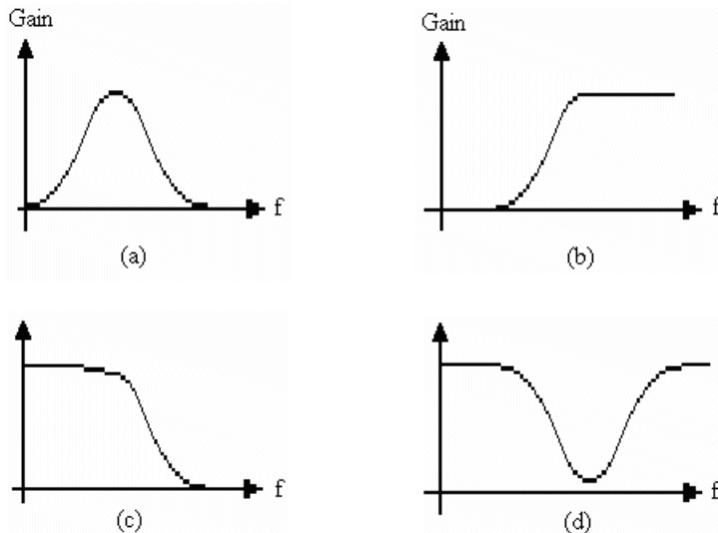
Diff: 2

- 4) A low-pass filter attenuates low frequencies.

Diff: 2

- 5) A band-pass filter passes all frequencies within a specified band and blocks all other frequencies.

Diff: 2



- 6) Refer to (a) in the figure above. This is the frequency response curve for a

- A) low-pass filter.
- B) high-pass filter.
- C) band-pass filter.
- D) band-stop filter.

Diff: 2

- 7) Refer to (b) in the figure above. This is the frequency response curve for a

 - A) low-pass filter.
 - B) high-pass filter.
 - C) band-pass filter.
 - D) band-stop filter.

Diff: 2

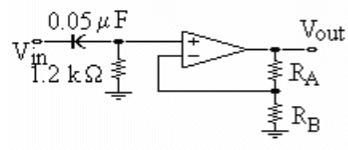
- 8) Refer to (c) in the figure above. This is the frequency response curve for a
A) low-pass filter. B) high-pass filter.
C) band-pass filter. D) band-stop filter.

Diff: 2

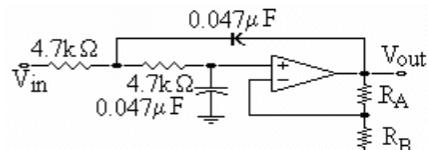
- 9) Refer to (d) in the figure above. This is the frequency response curve for a

 - A) low-pass filter.
 - B) high-pass filter.
 - C) band-pass filter.
 - D) band-stop filter.

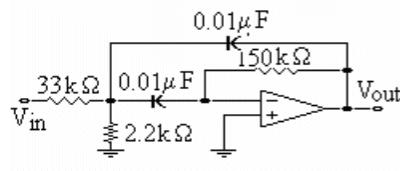
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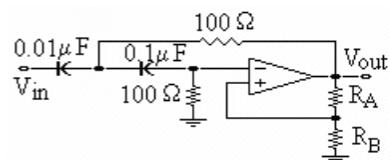
(a)



(b)



(c)



(d)

- 10) Refer to the figure above. Identify the active single-pole high-pass filter.

Diff: 2

- 11) Refer to the figure above. Identify the high-pass filter with a 40 dB/decade roll-off.

Diff: 2

- 12) Refer to the figure above. The low-pass filter with a 20 dB/decade roll-off is

Diff: 2

13) Refer to the figure above. The band-pass filter is

A) (a)

B) (b)

C) (c)

D) (d)

Diff: 2

14) Refer to the figure above. The low-pass filter with a roll-off of 40 dB/decade is

A) (a)

B) (b)

C) (c)

D) (d)

Diff: 2

15) Refer to (a) in the figure above. This circuit was checked for proper operation and f_C was correct but the voltage gain is 1. The cause of this problem might be that

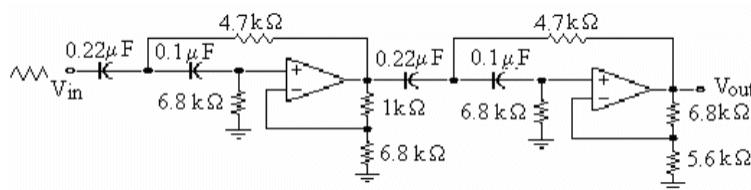
A) the $1.2\text{ k}\Omega$ resistor is open.

B) the capacitor is shorted.

C) R_A is open.

D) R_B is open.

Diff: 3



16) Refer to the figure above. This circuit is known as a _____ and the roll-off rate is _____.

A) low-pass filter, 60 dB/decade

B) high-pass filter, 20 dB/decade

C) high-pass filter, 80 dB/decade

D) band-pass filter, 80 dB/decade

Diff: 3

17) Refer to the figure above. The cutoff frequency for the first filter section is _____ the cutoff frequency for the second section.

A) equal to

B) higher than

C) lower than

D) None of the above.

Diff: 2

18) Another name for a band-stop filter is a(n) _____ filter.

A) low-cut

B) all-stop.

C) notch

D) all-pass

Diff: 2

- 19) A high-pass active filter has a cutoff frequency of 1.23 kHz. The bandwidth of this filter is
- A) 2.46 kHz.
 - B) 1.23 kHz.
 - C) 644 Hz.
 - D) Cannot determine.

Diff: 2

- 20) A low-pass filter with a roll-off rate of 60 dB/decade is needed. The best combination to use is
- A) a 2-pole filter followed by another 2-pole.
 - B) two single-pole filters in series.
 - C) a 2-pole filter followed by a 1-pole.
 - D) None of the above.

Diff: 2

- 21) A high-pass filter has $R = 47 \text{ k}\Omega$ and $C = 0.002 \mu\text{F}$. The cutoff frequency is
- A) 1.69 kHz.
 - B) 10.6 kHz.
 - C) 3.39 Hz.
 - D) None of the above.

Diff: 2

- 22) A pole is a network that contains
- A) a resistor and a capacitor.
 - B) a resistor and an inductor.
 - C) a capacitor and an inductor.
 - D) two resistors and one inductor.

Diff: 2

- 23) A maximally flat frequency response is a common name for
- A) Chebyshev.
 - B) Bessel.
 - C) Butterworth.
 - D) Colpitts.

Diff: 2

- 24) A single RC circuit produces a roll-off rate of
- A) -20 dB/decade.
 - B) -6 dB/octave.
 - C) -40 dB/decade.
 - D) A and B above.

Diff: 3

- 25) A low-pass filter has a cutoff frequency of 1.23 kHz. Determine the bandwidth of the filter.
- A) 2.46 kHz
 - B) 1.23 kHz
 - C) 644 Hz
 - D) Not enough information is given.

Diff: 3

26) Above the cutoff frequency of a low-pass filter, the output voltage

- A) does not change.
- B) doubles for every 1 kHz increase in frequency.
- C) increases.
- D) decreases.

Diff: 3

27) The center frequency of a band-pass filter is always equal to the

- A) bandwidth.
- B) geometric average of the cutoff frequencies.
- C) bandwidth divided by Q.
- D) 3-dB frequency.

Diff: 1

28) Band-pass filters are designed to pass a band of frequencies between

- | | |
|----------------------------|--------------------------------|
| A) f_{c1} and f_{c2} . | B) a band-start and band-stop. |
| C) 1 kHz and 10 kHz. | D) 1 kHz and 10 MHz. |

Diff: 2

29) Low-Q filters are _____ circuits, and high-Q filters are _____ circuits.

- | | |
|-------------------------|-------------------------------------|
| A) band-pass, band-stop | B) wide band-pass, narrow band-pass |
| C) low pass, high pass | D) low order, high order |

Diff: 2

30) A notch filter is a(n)

- | | |
|-----------------------|------------------------|
| A) all-pass filter. | B) band-pass circuit. |
| C) band-stop circuit. | D) time-delay circuit. |

Diff: 2

31) The type of filter response with a rippled passband is the

- | | |
|-----------------------|---------------|
| A) Butterworth. | B) Chebyshev. |
| C) Inverse Chebyshev. | D) Bessel. |

Diff: 2

32) The filter response characteristic that distorts pulses the least is the

- | | | | |
|-----------------|---------------|--------------|------------|
| A) Butterworth. | B) Chebyshev. | C) Elliptic. | D) Bessel. |
|-----------------|---------------|--------------|------------|

Diff: 3

- 33) The filter with the slowest roll-off rate is the
A) Butterworth. B) Chebyshev. C) Elliptic. D) Bessel.
Diff: 2
- 34) The damping factor (DF) of an active filter determined by
A) the positive feedback of the circuit. B) the negative feedback of the circuit.
C) the number of poles. D) the Q of the circuit.
Diff: 2
- 35) If a Butterworth filter has 9 second-order stages, its rolloff rate is
A) 20 dB per decade. B) 40 dB per decade.
C) 180 dB per decade. D) 360 dB per decade.
Diff: 2
- 36) Sallen-Key filters are also called
A) VCVS filters. B) multiple feedback filters.
C) biquadratic filters. D) state-variable filters.
Diff: 2
- 37) By cascading low-pass filters, _____ can be improved.
A) bandwidth B) roll-off rate C) Q-rating D) phase shift
Diff: 2
- 38) A multiple-feedback band-pass filter
A) uses a minimum of two op-amps.
B) is used for a narrow band (high Q) filter.
C) is used for a wide band (low Q) filter.
D) is also known as a Sallen-Key filter.
Diff: 3
- 39) The state-variable filter
A) is difficult to tune.
B) uses fewer than three op-amps.
C) has high component sensitivity.
D) has a low-pass, high-pass and band-pass output.
Diff: 2

40) The Q of a state-variable filter is controlled by the

- A) ratio of $\frac{R_5}{R_6}$.
- B) product of $R_5 \times R_6$.
- C) ratio of the feedback resistors.
- D) Both A and C above.

Diff: 3

41) The lowest frequency that an active low-pass filter can pass is

- A) determined by the unity gain bandwidth of the op-amp.
- B) determined by the feedback capacitor value.
- C) determined by the damping factor.
- D) 0 Hz.

Diff: 2

42) The Q of a band-pass filter is

- A) the ratio of the center frequency to the bandwidth.
- B) not related to the damping factor.
- C) the difference between the two op-amp power supply voltages.
- D) the quiescent current specification of the op-amp input stage.

Diff: 2

43) A band-stop filter is also known as

- A) a band-reject filter.
- B) a notch filter.
- C) a band-elimination filter.
- D) All of the above.

Diff: 2

44) Which of the following is not an advantage of active filters over passive filters?

- A) Active filters provide filtering with gain.
- B) Active filters have minimal loading due to a high input impedance.
- C) Active filters require no power to operate.
- D) Active filters have a low output impedance.

Diff: 3

45) What is the value of resistance needed with a $0.01 \mu\text{F}$ capacitor for a critical frequency of 23.4 kHz?

- A) 680Ω
- B) $2.34 \text{ k}\Omega$
- C) $18 \text{ k}\Omega$
- D) $132.9 \text{ k}\Omega$

Diff: 2

Chapter 16 Oscillators

- 1) To operate properly, an oscillator requires an external ac input signal.

Diff: 2

- 2) An oscillator can produce many types of outputs such as sine, triangle, or square waves.

Diff: 2

- 3) Positive feedback is required for an oscillator to operate properly.

Diff: 2

- 4) Crystal oscillators are very stable.

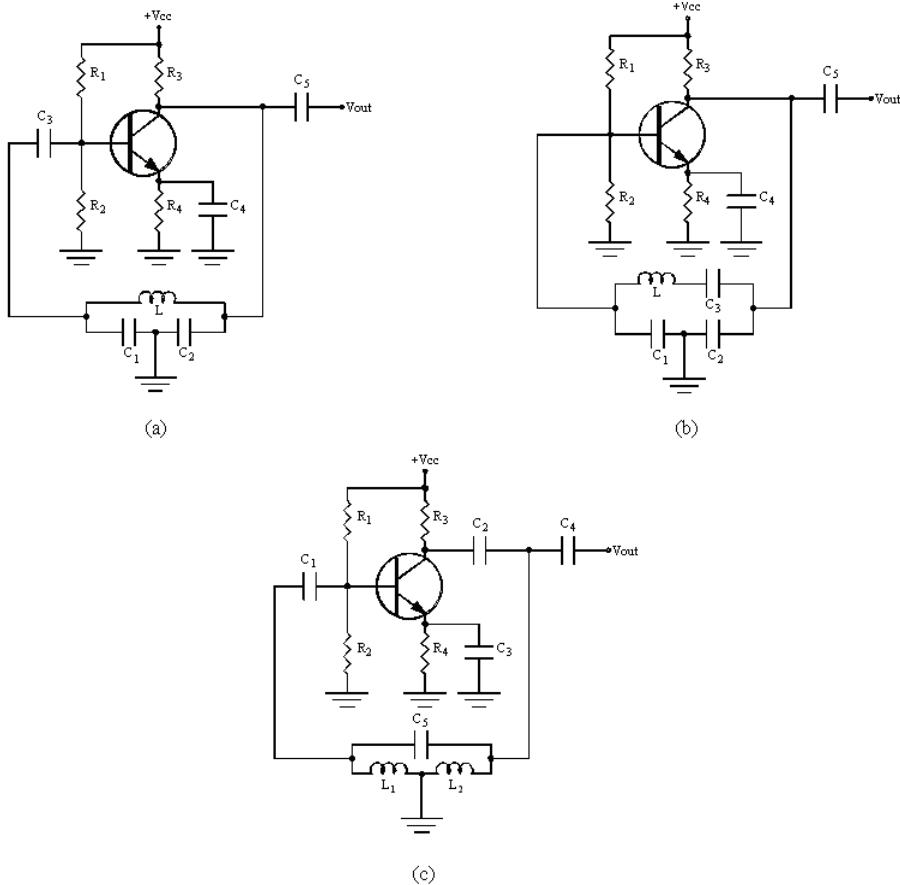
Diff: 2

- 5) An RC phase-shift oscillator uses feedback from a tank circuit.

Diff: 2

- 6) The Twin-T Oscillator is a popular choice because it works well over a wide range of frequencies.

Diff: 2



7) Refer to the figure above. Which of these circuits is known as a Colpitts oscillator?

- | | |
|--------|-----------------------|
| A) (a) | B) (b) |
| C) (c) | D) None of the above. |

Diff: 2

8) Refer to the figure above. Which of these circuits is known as a Clapp oscillator?

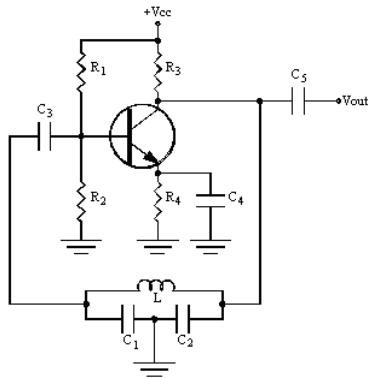
- | | |
|--------|-----------------------|
| A) (a) | B) (b) |
| C) (c) | D) None of the above. |

Diff: 2

9) Refer to the figure above. Which of these circuits is known as a Hartley oscillator?

- | | |
|--------|-----------------------|
| A) (a) | B) (b) |
| C) (c) | D) None of the above. |

Diff: 2



10) Refer to the figure above. If C_5 were to open

- A) the resonant frequency would be higher than normal.
- B) the resonant frequency would be lower than normal.
- C) there would be no signal present at V_{out} .
- D) the circuit would draw no current from $+V_{cc}$.

Diff: 2

11) Of the following oscillator circuit components, the one that exhibits the piezoelectric effect is the

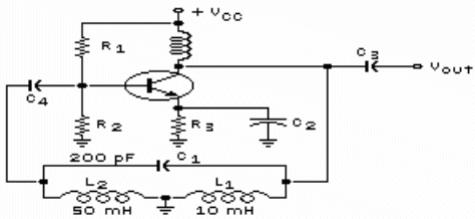
- A) inductor.
- B) capacitor.
- C) crystal.
- D) resistor.

Diff: 2

12) A very stable oscillator is needed to operate on a single frequency. A good choice might be a

- A) Hartley.
- B) VCO.
- C) crystal.
- D) Clapp.

Diff: 2



13) Refer to the figure above. If the value of $V_{CC} = 5$ V, the output voltage would be

- A) a square wave of 10 V p-p.
- B) a square wave that varies between 0 V and 5 V.
- C) a sine wave.
- D) 5 V dc.

Diff: 2

14) Nonsinusoidal oscillators produce

- A) sine waves only.
- B) triangle waves.
- C) square waves.
- D) Either B or C above.

Diff: 2

15) The 555 timer contains

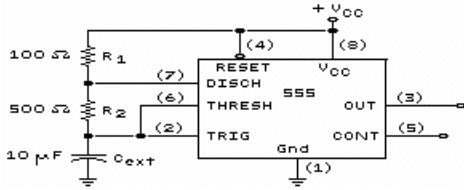
- A) 2 comparators.
- B) 3 comparators.
- C) 4 comparators.
- D) 5 comparators.

Diff: 2

16) A stable type of oscillator is

- A) the Clapp oscillator.
- B) the Hartley oscillator.
- C) the crystal oscillator.
- D) None of the above.

Diff: 2



17) Refer to the figure above. To reduce the duty cycle to less than 50%, which of the following circuit changes would be necessary?

- A) Reduce the size of R_1 .
- B) Reduce the size of R_2 .
- C) Increase the size of R_1 .
- D) Connect a diode in parallel with R_2 .

Diff: 2

18) A circuit that can change the frequency of oscillation with an application of a dc voltage is sometimes called a(n)

- A) voltage-controlled oscillator.
- B) crystal oscillator.
- C) Hartley oscillator.
- D) astable multivibrator.

Diff: 2

19) Which of the following is not an essential requirement of a feedback oscillator?

- A) Positive feedback network
- B) Negative feedback network
- C) Phase shift around the feedback loop of 0°
- D) Amplifier circuit

Diff: 2

20) In order to sustain oscillations in a feedback oscillator, the gain should be _____ so the product of $A_V \times B$ equals _____.

- A) reduced, one
- B) reduced, less than one
- C) increased, more than one
- D) increased, much greater than one

Diff: 2

21) The voltage that starts a feedback oscillator is caused by

- A) ripple from the power supply.
- B) thermal noise in resistors.
- C) the input signal from a generator.
- D) positive feedback.

Diff: 2

- 22) A Wien-bridge oscillator uses
- A) positive feedback.
 - B) negative feedback.
 - C) both types of feedback.
 - D) an LC tank circuit.

Diff: 2

- 23) The RC feedback network used in the Wien-bridge oscillator has a maximum output voltage when
- A) $X_C = X_L$.
 - B) $X_L = R$.
 - C) $R_1 = R_2$ and $X_{C1} = X_{C2}$.
 - D) $R = 0 \Omega$.

Diff: 3

- 24) The closed-loop voltage gain, A_{CL} , for a Wien-bridge oscillator is
- A) 3, after the oscillations have built up.
 - B) slightly greater than 1.
 - C) less than 1.
 - D) exactly 1.

Diff: 2

- 25) In order for feedback oscillators to operate properly, the gain has to be
- A) 1/4.
 - B) self-adjusting.
 - C) stabilized.
 - D) nonlinear.

Diff: 2

- 26) The phase-shift oscillator usually has
- A) two lead or lag circuits.
 - B) three lead or lag circuits.
 - C) no RC sections.
 - D) no feedback loop.

Diff: 2

- 27) One way to recognize a Colpitts oscillator is by the
- A) tapped inductors in the tank circuit.
 - B) tapped capacitors in the tank circuit.
 - C) three lag networks in the feedback path.
 - D) lead/lag network in the feedback path.

Diff: 2

- 28) One way to recognize a Hartley oscillator is by the
- A) transformer used for feedback.
 - B) three lead networks in the feedback path.
 - C) tapped capacitors in the tank circuit.
 - D) tapped inductors in the tank circuit.

Diff: 2

- 29) When Q decreases in a Colpitts oscillator, the frequency of oscillation
- A) decreases.
 - B) remains the same.
 - C) increases.
 - D) is unpredictable.

Diff: 2

- 30) The Hartley oscillator uses
- A) only resistors and capacitors.
 - B) two inductors.
 - C) a tungsten lamp.
 - D) a tickler coil.

Diff: 2

- 31) Which of the following cannot be used as the amplifier element within an oscillator?
- A) BJT
 - B) thermistor
 - C) FET
 - D) op-amp

Diff: 2

- 32) Which type of LC oscillator uses a tickler coil in the feedback path?
- A) Colpitts
 - B) Hartley
 - C) Armstrong
 - D) Clapp

Diff: 2

- 33) Which of the following oscillator types does not use any inductors?
- A) Wien-bridge
 - B) Hartley oscillator
 - C) Colpitts oscillator
 - D) Clapp oscillator

Diff: 2

- 34) In a Colpitts oscillator, which component(s) determine the feedback fraction, B?
- A) The resistors R₁ and R₂ in the base circuit
 - B) The RF choke in the collector circuit
 - C) The capacitors C₁ and C₂ in the tank circuit
 - D) The inductor in the tank circuit

Diff: 3

- 35) The Q of a crystal
- A) is extremely low.
 - B) is about 10 or so in most cases.
 - C) is extremely high.
 - D) None of the above.

Diff: 2

36) A crystal's fundamental frequency depends upon

- A) crystal thickness.
- B) type of cut.
- C) mechanical dimensions.
- D) All of the above.

Diff: 2

37) The higher resonant frequencies of a crystal are called

- A) undertones.
- B) overtones.
- C) octaves.
- D) decades.

Diff: 2

Chapter 17 Voltage Regulators

- 1) Switching regulators are very efficient.

Diff: 2

- 2) A zener diode is sometimes used as a voltage regulator.

Diff: 2

- 3) Line regulation is the percentage change in input voltage for a given change in output voltage.

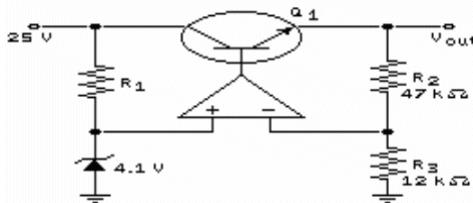
Diff: 2

- 4) In a shunt regulator, the control element is in series with the load.

Diff: 2

- 5) Most voltage regulators include some kind of protection circuitry.

Diff: 2



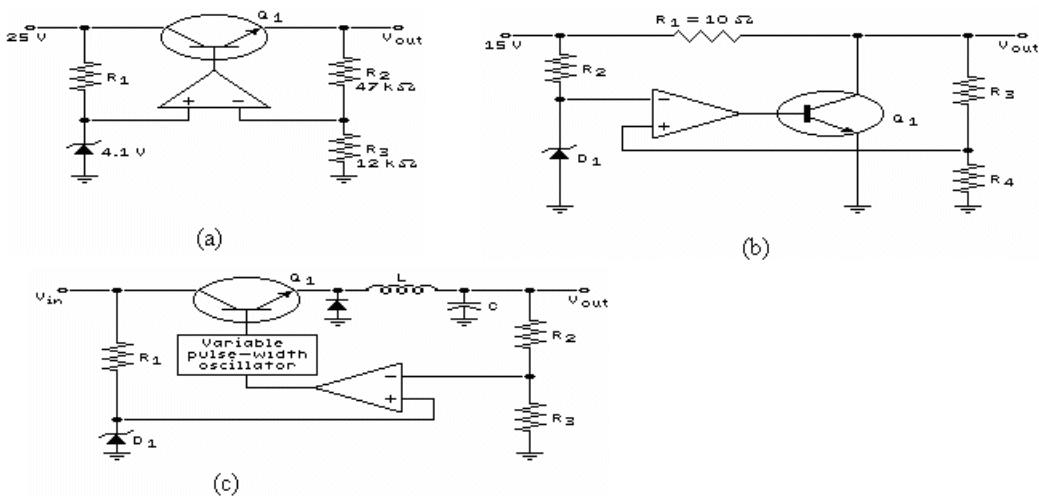
- 6) Refer to the figure above. If the zener had a voltage rating of 3.7 V, V_{out} would be

Diff: 2

- 7) Refer to the figure above. If a wire clipping were to short Q1 emitter to collector, the problem that might result is

- A) R₂ would open. B) V_{OUT} would increase to 25 V.
C) Q₁ would fail. D) the zener would open.

Diff: 3



8) Refer to the figure above. Which of these circuits is known as a shunt regulator?

Diff: 2

9) Refer to the figure above. Which of these circuits is known as a step-up switching regulator?

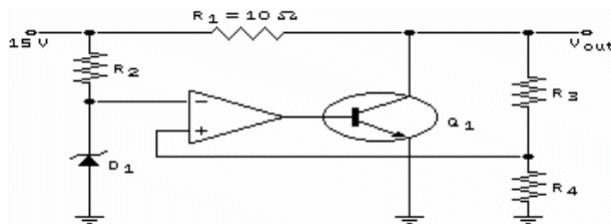
- A) (a) B) (b)
C) (c) D) None of the above.

Diff: 2

10) Refer to the figure above. Which of these circuits is known as a series regulator?

- A) (a) B) (b)
C) (c) D) None of the above.

Diff: 2



11) Refer to the figure above. The purpose for the op-amp is to

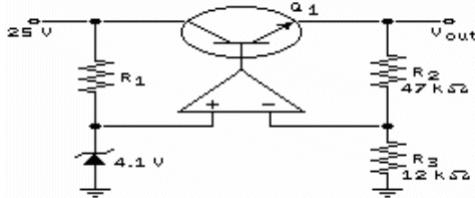
- A) supply a reference voltage.
 - B) sense the error signal.
 - C) limit the input voltage to the circuit.
 - D) amplify the error signal.

Diff: 2

12) Refer to the figure above. An increase in V_{OUT} will cause Q1 to

- A) conduct less.
- B) conduct the same.
- C) conduct more.
- D) open.

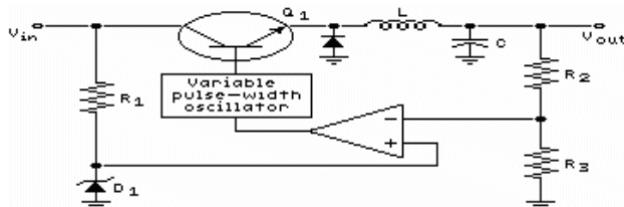
Diff: 3



13) Refer to the figure above. To increase the current handling capability of this regulator, beyond the 5 A rating of the transistor, the reasonable thing to do would be to

- A) place another transistor in series with Q1.
- B) increase the value of the zener diode.
- C) place another transistor in parallel with Q1.
- D) change the values of R2 and R3.

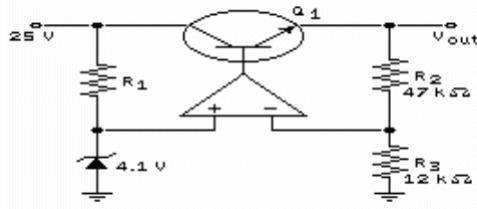
Diff: 2



14) Refer to the figure above. If the output voltage tends to increase due to a decrease in load current, the transistor will conduct for _____ time each cycle.

- A) a longer
- B) a shorter
- C) the same
- D) exactly half the

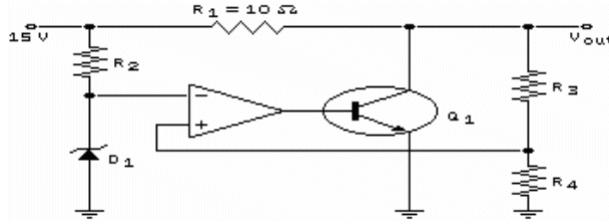
Diff: 2



15) Refer to the figure above. This circuit is brought in for repair. The measured output voltage was 25 V under all load conditions. A possible cause of this symptom might be that

- A) R₂ has opened.
- B) Q₁ base-emitter has opened.
- C) R₃ has opened.
- D) V_{in} has decreased.

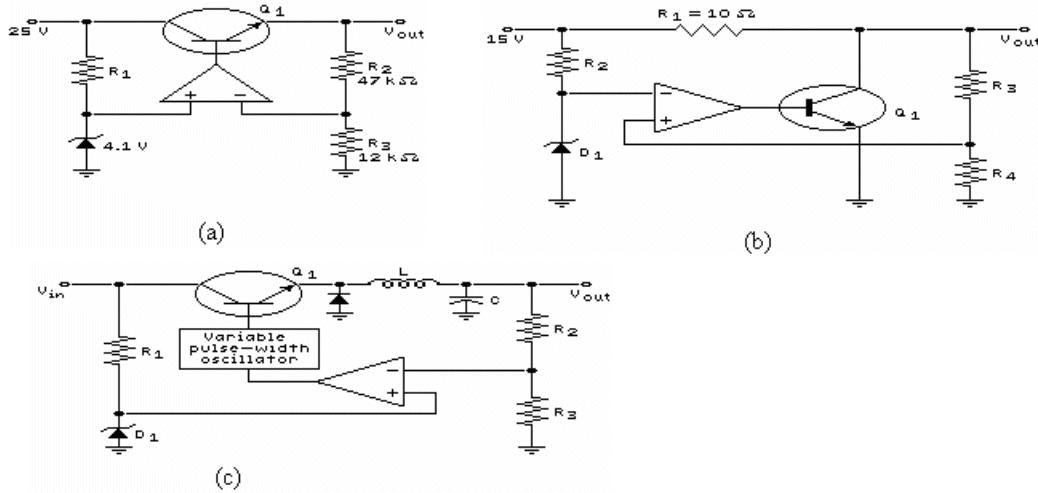
Diff: 3



16) Refer to the figure above. If R₁ opened, V_{OUT} would

- A) increase.
- B) decrease to zero.
- C) remain the same.
- D) Cannot be determined.

Diff: 2



17) Refer to the figure above. In all of these circuits, the zener is used

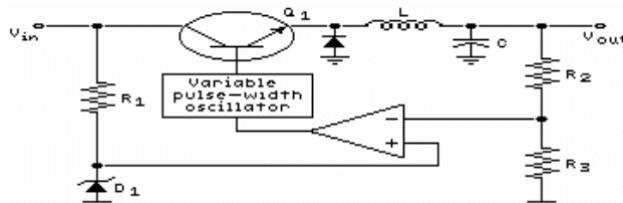
- A) to sense the change in output voltage.
- B) as a reference voltage.
- C) to supply the op-amp with V_{CC}.
- D) to regulate the output voltage directly.

Diff: 2

18) Refer to the figure above. The circuit that will also regulate the output voltage when V_{in} varies is

- A) (a).
- B) (b).
- C) (c).
- D) All of the above.

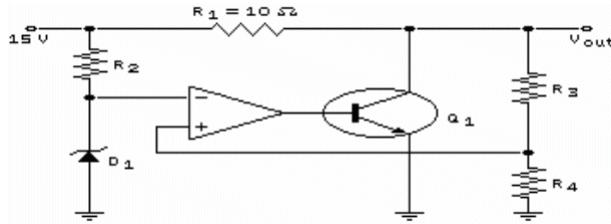
Diff: 2



19) Refer to the figure above. This circuit operates at a relatively _____ frequency and its efficiency is _____.

- A) low, low
- B) low, high
- C) high, high
- D) high, low

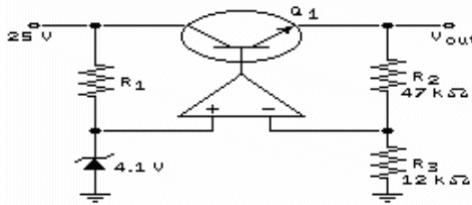
Diff: 2



20) Refer to the figure above. The purpose for the diode D₁ is to

- A) supply a reference voltage.
- B) amplify the error signal.
- C) sense the error signal.
- D) limit the input voltage to the circuit.

Diff: 2



21) Refer to the figure above. If a solder splash shorted the ends of R₁ to each other, the result would be that

- A) the op-amp would fail.
- B) Q1 would open.
- C) the output voltage would not change.
- D) the zener would fail.

Diff: 3

22) A voltage regulator with a no-load dc output of 15 V is connected to a load with a resistance of 12 Ω. If the load voltage decreases to 14.5 V, the percent regulation would be

- A) 96.7%.
- B) 3.33%.
- C) 3.45%.
- D) 100%.

Diff: 2

23) An advantage of a switching regulator is

- A) less heat and wasted power.
- B) the circuit is very efficient.
- C) voltages can be stepped-up or stepped-down.
- D) All of the above.
- E) None of the above.

Diff: 2

24) A voltage regulator has a no-load output of 18 V and a full load output of 17.3 V. The percent load regulation is

- A) 0.25%. B) 96.1%. C) 4.05%. D) 1.04%.

Diff: 2

25) A voltage regulator with a no-load output dc voltage of 12 V is connect to a load with a resistance of $10\ \Omega$. If the load resistance decreases to $7.5\ \Omega$, the load voltage will decrease to 10.9 V. The load current will be _____ and the percent load regulation is _____.

- A) 1.45 A, 90.8% B) 1.45 A, 10.09% C) 1.6 A, 90.8% D) 1.6 A, 9.17%

Diff: 2

26) An increase of line voltage into a power supply usually produces

- A) a decrease in load resistance.
B) an increase in load voltage.
C) a decrease in efficiency.
D) less power dissipation in the rectifier diodes.

Diff: 2

27) _____ is a measurement of how well the power supply maintains a constant output voltage with changes in input voltage.

- A) Voltage control B) Load voltage control
C) Load regulation D) Line regulation

Diff: 2

28) If the output of a voltage regulator varies from 15 to 14.7 V between the minimum and maximum load current, the load regulation is

- A) 0. B) 1%. C) 2%. D) 5%.

Diff: 2

29) If the output of a voltage regulator varies from 20 to 19.8 V when the line voltage varies over its specified range, the load regulation is

- A) 0. B) 1%. C) 2%. D) 5%.

Diff: 2

30) A series regulator is an example of a

- A) linear regulator. B) switching regulator.
C) shunt regulator. D) ac-to-dc converter.

Diff: 2

31) Without current limiting, a shorted load will probably

- A) produce zero load current.
- B) destroy diodes and transistors.
- C) have a load voltage equal to the zener voltage.
- D) have too little load current.

Diff: 2

32) Simple current limiting may produce too much heat in the

- A) zener diode.
- B) load resistor.
- C) pass transistor.
- D) ambient air.

Diff: 2

33) With foldback current limiting, the load voltage approaches zero, and the load current approaches

- A) a small value.
- B) infinity.
- C) the zener current.
- D) a destructive level.

Diff: 3

34) If the load is shorted, the pass transistor has the least power dissipation when the regulator has

- A) foldback limiting.
- B) low efficiency.
- C) buck topology.
- D) a high zener voltage.

Diff: 2

35) Switching regulator configurations include

- A) step-down.
- B) inverting.
- C) step-up.
- D) All of the above.

Diff: 2

36) An advantage of shunt regulation is

- A) built-in short-circuit protection.
- B) low power dissipation in the pass transistor.
- C) high efficiency.
- D) little wasted power.

Diff: 2

- 37) To get more output voltage from a step-down switching regulator, you have to
- A) decrease the duty cycle.
 - B) decrease the input voltage.
 - C) increase the duty cycle.
 - D) increase the switching frequency.
- Diff: 3*
- 38) A _____ maintains a constant output voltage by controlling the duty cycle of a switch in series with the load.
- A) shunt regulator
 - B) linear regulator
 - C) series regulator
 - D) switching regulator
- Diff: 2*
- 39) Switching regulators have _____ than linear regulators.
- A) more heat-sinking requirements
 - B) simpler circuitry
 - C) lower efficiency
 - D) greater efficiency
- Diff: 2*
- 40) In a step-up regulator, the output voltage is filtered with a
- A) choke-input filter.
 - B) capacitor-input filter.
 - C) diode.
 - D) voltage divider.
- Diff: 2*
- 41) The 7912 produces a regulated output voltage of
- A) +5 V.
 - B) +9 V.
 - C) -12 V.
 - D) +12 V.
- Diff: 2*
- 42) The 7800 series of voltage regulators produces an output voltage that is
- A) positive.
 - B) negative.
 - C) either positive or negative.
 - D) unregulated.
- Diff: 2*
- 43) The LM317 regulator provides a(n)
- A) fixed positive output voltage.
 - B) adjustable positive output voltage.
 - C) fixed negative output voltage.
 - D) adjustable negative output voltage.
- Diff: 2*

- 44) The main difference between the 78XX and 79XX series regulators is that

 - A) the 78XX series is adjustable and the 79XX series is fixed.
 - B) the 78XX series is fixed and the 79XX series is adjustable.
 - C) the 78XX series provides a positive fixed output voltage and the 79XX series provides a negative fixed output voltage.
 - D) the 78XX series provides a negative fixed output voltage and the 79XX series provides a positive fixed output voltage.

Diff: 2

- 45) A 7805 regulator has a +20 V input. If the input and output pins of the regulator are shorted together by a solder bridge, the output voltage will be

A) 0 V. B) 0.7 V. C) +5 V. D) +20 V.

Diff: 3

Chapter 18 Communications

- 1) Balanced modulation is used in certain types of communications such as AM broadcast systems, but is not used in single side-band systems.

Diff: 2

- 2) Fiber-optic cables have wider bandwidth, but are more susceptible to interference.

Diff: 2

- 3) *Scattering* is the loss of optical signal into the cladding of the fiber-optic cable.

Diff: 2

- 4) Combining an audio signal with an RF carrier in a nonlinear device is called

A) neutralization. B) demodulation. C) filtering. D) modulation.

Diff: 2

- 5) The process of modifying a high frequency carrier by the information to be transmitted is called

A) modulation. B) multiplexing.
C) detection. D) discrimination.

Diff: 2

- 6) Mixing two signals by a nonlinear process is called

A) sum and product frequencies. B) heterodyning.
C) spectrum modulation. D) bandwidth discrimination.

Diff: 3

- 7) The outline of the peaks of the modulated carrier has the shape of the information signal, and is called the

A) envelope. B) lower-side frequency.
C) RF index. D) duty cycle.

Diff: 2

- 8) Higher modulating frequencies are amplified more than the lower frequencies at the transmitting end of an FM system by a process called

A) pre-emphasis. B) full duplex. C) de-emphasis. D) filtering.

Diff: 3

9) The quadrant classification of a linear multiplier indicates the number of _____ that the multiplier can handle.

- A) input polarity combinations
- B) output polarity combinations
- C) transfer characteristics
- D) scale factors

Diff: 3

10) The purpose of a balanced modulator is to eliminate

- A) the upper side-band.
- B) the lower side-band.
- C) both side-bands.
- D) the carrier.

Diff: 2

11) The product of two sinusoidal signals is called

- A) balanced modulation.
- B) lower side frequency.
- C) suppressed-carrier modulation.
- D) Both A and C above.

Diff: 2

12) If you receive an AM signal modulated by a pure sinusoidal signal in the audio frequency range, you will hear

- A) a single tone.
- B) static.
- C) distortion.
- D) nothing.

Diff: 2

13) A mixer is basically a frequency

- A) doubler.
- B) converter.
- C) demodulator.
- D) modulator.

Diff: 2

14) A basic IF Amplifier always has

- A) a tuned (resonant) circuit on the input.
- B) a tuned (resonant) circuit on the output.
- C) a tuned (resonant) circuit on both the input and output.
- D) None of the above.

Diff: 2

15) The main difference between an FM receiver and an AM receiver is the method used to recover the audio signal from the

- A) modulated IF.
- B) carrier.
- C) mixer.
- D) detector.

Diff: 2

16) The phase detector in a PLL is followed by a low-pass filter. The low-pass filter passes the _____ and rejects all other frequencies.

- A) input signal
- B) feedback signal
- C) sum of the input and feedback signals
- D) difference of the input and feedback signals

Diff: 2

17) In a PLL, to obtain lock, the signal frequency must come within the

- A) lock range.
- B) closed range.
- C) capture range.
- D) deviation range.

Diff: 2

18) For a PLL, the capture range is

- A) always greater than the lock range.
- B) always the same as the lock range.
- C) usually less than the lock range.
- D) always two times the lock range.

Diff: 2

19) A PLL can be used as a(n)

- A) series voltage regulator.
- B) FM demodulator.
- C) audio amplifier.
- D) Both B and C above.

Diff: 2

20) A phase detector has

- A) one input signal and two output signals.
- B) two input signals and one output signal.
- C) no input signals.
- D) three output signals.

Diff: 2

21) The bandwidth of the low-pass filter in a PLL determines the

- A) capture range.
- B) lock range.
- C) free-running frequency.
- D) phase difference.

Diff: 2

22) Most VCO's used in PLL's operate on the principle of

- A) variable power.
- B) variable inductance.
- C) variable reactance.
- D) phase detection.

Diff: 2

23) The IF amplifiers within an FM radio receiver are tuned to

- A) 455 kHz.
- B) 4.55 MHz.
- C) 10.7 MHz.
- D) 100.7 MHz.

Diff: 2

24) The signal loss that occurs when photons interact with the molecules of the core in a fiber-optic cable is called

- A) refraction.
- B) absorption.
- C) scattering.
- D) scattering.

Diff: 3

Answer Key

CHAPTER 1

- 1) FALSE
- 2) FALSE
- 3) TRUE
- 4) FALSE
- 5) TRUE
- 6) C
- 7) B
- 8) A
- 9) A
- 10) D
- 11) D
- 12) C
- 13) B
- 14) D
- 15) A
- 16) C
- 17) B
- 18) A
- 19) C
- 20) A
- 21) C
- 22) B
- 23) D
- 24) B
- 25) B
- 26) A
- 27) B
- 28) D
- 29) A
- 30) A
- 31) D
- 32) A
- 33) B
- 34) D
- 35) D
- 36) A
- 37) C
- 38) C
- 39) A

CHAPTER 2

- 1) TRUE
- 2) FALSE
- 3) TRUE
- 4) FALSE
- 5) FALSE
- 6) D
- 7) D
- 8) A
- 9) C
- 10) D
- 11) B
- 12) B
- 13) C
- 14) D
- 15) B
- 16) D
- 17) B
- 18) A
- 19) C
- 20) B
- 21) C
- 22) D
- 23) E
- 24) B
- 25) D
- 26) B
- 27) A
- 28) C
- 29) B
- 30) A
- 31) B
- 32) C
- 33) D
- 34) C
- 35) C
- 36) B
- 37) A
- 38) C
- 39) B
- 40) D
- 41) B
- 42) D
- 43) B
- 44) A

CHAPTER 3

- 1) TRUE
- 2) FALSE
- 3) C
- 4) B
- 5) C
- 6) A
- 7) A
- 8) A
- 9) D
- 10) D
- 11) D
- 12) D
- 13) B
- 14) B
- 15) B
- 16) A
- 17) D
- 18) E
- 19) C
- 20) B
- 21) D
- 22) E
- 23) C
- 24) A
- 25) B
- 26) A
- 27) D
- 28) D
- 29) A
- 30) C
- 31) D
- 32) C
- 33) A
- 34) B
- 35) B
- 36) B
- 37) A
- 38) B
- 39) B
- 40) D
- 41) C
- 42) C
- 43) B
- 44) A
- 45) A
- 46) B

CHAPTER 4

- 1) TRUE
- 2) FALSE
- 3) FALSE
- 4) TRUE
- 5) TRUE
- 6) TRUE
- 7) TRUE
- 8) D
- 9) C
- 10) A
- 11) B
- 12) D
- 13) C
- 14) B
- 15) B
- 16) D
- 17) C
- 18) A
- 19) C
- 20) A
- 21) A
- 22) D
- 23) C
- 24) A
- 25) D
- 26) B
- 27) C
- 28) B
- 29) B
- 30) C
- 31) B
- 32) B
- 33) B
- 34) C
- 35) C
- 36) C
- 37) A
- 38) C
- 39) B
- 40) D
- 41) A
- 42) C
- 43) B
- 44) B
- 45) B
- 46) B
- 47) D

CHAPTER 5

- 1) TRUE
- 2) FALSE
- 3) FALSE
- 4) TRUE
- 5) TRUE
- 6) C
- 7) C
- 8) D
- 9) B
- 10) E
- 11) D
- 12) C
- 13) B
- 14) D
- 15) B
- 16) A
- 17) C
- 18) B
- 19) C
- 20) B
- 21) D
- 22) B
- 23) D
- 24) C
- 25) A
- 26) C
- 27) B
- 28) C
- 29) C
- 30) D
- 31) A
- 32) B
- 33) C
- 34) B
- 35) B
- 36) A
- 37) D
- 38) D
- 39) A
- 40) A
- 41) B
- 42) B
- 43) D

CHAPTER 6

- 1) FALSE
- 2) TRUE
- 3) TRUE
- 4) FALSE
- 5) FALSE
- 6) D
- 7) C
- 8) C
- 9) A
- 10) B
- 11) B
- 12) D
- 13) A
- 14) D
- 15) C
- 16) D
- 17) D
- 18) C
- 19) A
- 20) D
- 21) B
- 22) C
- 23) A
- 24) B
- 25) C
- 26) C
- 27) A
- 28) B
- 29) B
- 30) B
- 31) A
- 32) B
- 33) B
- 34) B
- 35) A
- 36) C
- 37) B
- 38) C
- 39) A
- 40) A
- 41) A
- 42) C
- 43) D
- 44) D
- 45) B
- 46) B
- 47) B
- 48) B
- 49) B
- 50) B
- 51) A
- 52) C
- 53) D

54) C
55) A
56) B
57) B
58) A
59) D
60) C

CHAPTER 7

- 1) FALSE
2) FALSE
3) FALSE
4) C
5) C
6) B
7) D
8) C
9) A
10) D
11) A
12) D
13) A
14) C
15) D
16) C
17) B
18) B
19) D
20) B
21) B
22) C
23) C
24) A
25) C
26) C
27) C
28) D
29) A
30) D
31) C
32) C
33) C
34) A
35) B
36) B
37) C
38) B
39) C
40) A
41) C
42) C
43) D
44) A
45) B
46) C
47) D
48) B
- 1) TRUE
2) FALSE
3) TRUE
4) TRUE
5) FALSE
6) TRUE
7) FALSE
8) TRUE
9) FALSE
10) A
11) A
12) B
13) D
14) B
15) C
16) D
17) A
18) B
19) D
20) C
21) C
22) B
23) A
24) B
25) B
26) B
27) C
28) A
29) B
30) C
31) A
32) A
33) D
34) C
35) D
36) D
37) C
38) D
39) C
40) B
41) B
42) A
43) B
44) D
45) D
46) A
47) D
48) C
49) D

CHAPTER 8

CHAPTER 9

- 1) FALSE
- 2) FALSE
- 3) TRUE
- 4) TRUE
- 5) FALSE
- 6) TRUE
- 7) FALSE
- 8) FALSE
- 9) TRUE
- 10) FALSE
- 11) FALSE
- 12) TRUE
- 13) FALSE
- 14) FALSE
- 15) TRUE
- 16) C
- 17) D
- 18) D
- 19) C
- 20) A
- 21) B
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- 48) D
- 49) C
- 50) D
- 51) A
- 52) C
- 53) C

- 54) A
- 55) A
- 56) B
- 57) D
- 58) C

CHAPTER 10

- 1) TRUE
- 2) TRUE
- 3) TRUE
- 4) FALSE
- 5) FALSE
- 6) FALSE
- 7) D
- 8) C
- 9) A
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- 37) D
- 38) C
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- 40) A
- 41) D
- 42) A
- 43) C
- 44) B
- 45) D
- 46) C
- 47) A

CHAPTER 11

- 1) TRUE
- 2) FALSE
- 3) TRUE
- 4) TRUE
- 5) FALSE
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- 7) E
- 8) B
- 9) D
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- 37) D
- 38) C
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- 40) A
- 41) D
- 42) A
- 43) C
- 44) B
- 45) D
- 46) C
- 47) A

CHAPTER 12

- 1) TRUE
- 2) TRUE
- 3) FALSE
- 4) TRUE
- 5) FALSE
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- 8) B
- 9) A
- 10) D
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- 38) A
- 39) C
- 40) B
- 41) C
- 42) C
- 43) A
- 44) A
- 45) B
- 46) C
- 47) A
- 48) A
- 49) B
- 50) D
- 51) B

CHAPTER 13

- 1) TRUE
- 2) FALSE
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- 4) FALSE
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- 39) D
- 40) A
- 41) B
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- 43) A
- 44) B
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- 46) D

CHAPTER 14

- 1) TRUE
- 2) FALSE
- 3) TRUE
- 4) TRUE
- 5) FALSE
- 6) FALSE
- 7) FALSE
- 8) TRUE
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- 39) B
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- 42) C
- 43) B
- 44) D
- 45) B
- 46) C

CHAPTER 15

- 1) TRUE
- 2) FALSE
- 3) TRUE
- 4) FALSE
- 5) TRUE
- 6) C
- 7) B
- 8) A
- 9) D
- 10) A
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- 38) C
- 39) D
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- 41) D
- 42) A
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- 45) A

CHAPTER 16

- 1) FALSE
- 2) TRUE
- 3) TRUE
- 4) TRUE
- 5) FALSE
- 6) FALSE
- 7) A
- 8) B
- 9) C
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- 27) B
- 28) D
- 29) A
- 30) B
- 31) B
- 32) C
- 33) A
- 34) C
- 35) C
- 36) D
- 37) B

CHAPTER 17

- 1) TRUE
- 2) TRUE
- 3) FALSE
- 4) FALSE
- 5) TRUE
- 6) B
- 7) B
- 8) B
- 9) D
- 10) A
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- 36) A
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- 42) A
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- 45) D

CHAPTER 18

- 1) FALSE
- 2) FALSE
- 3) TRUE
- 4) D
- 5) A
- 6) B
- 7) A
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- 24) B