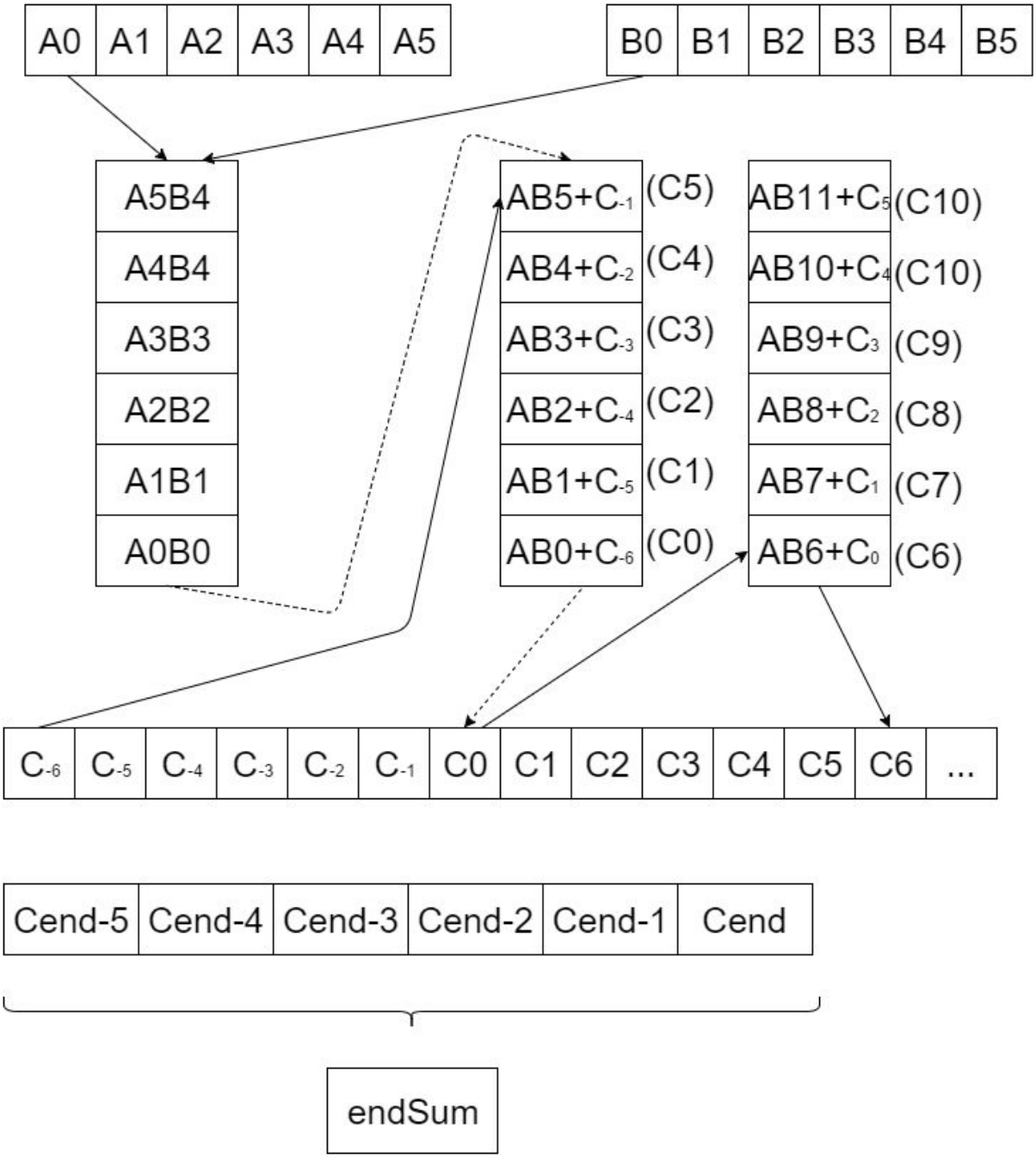
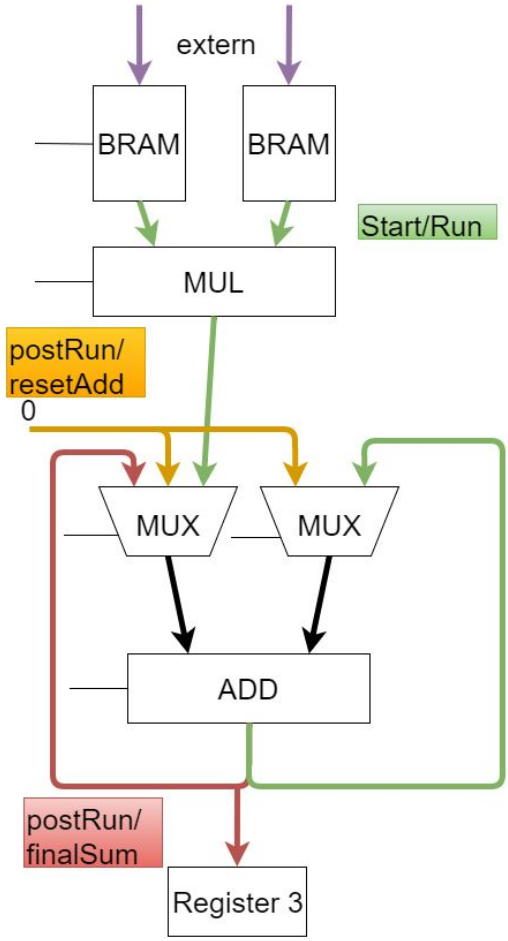
Gewichtete Summe

Analyse:

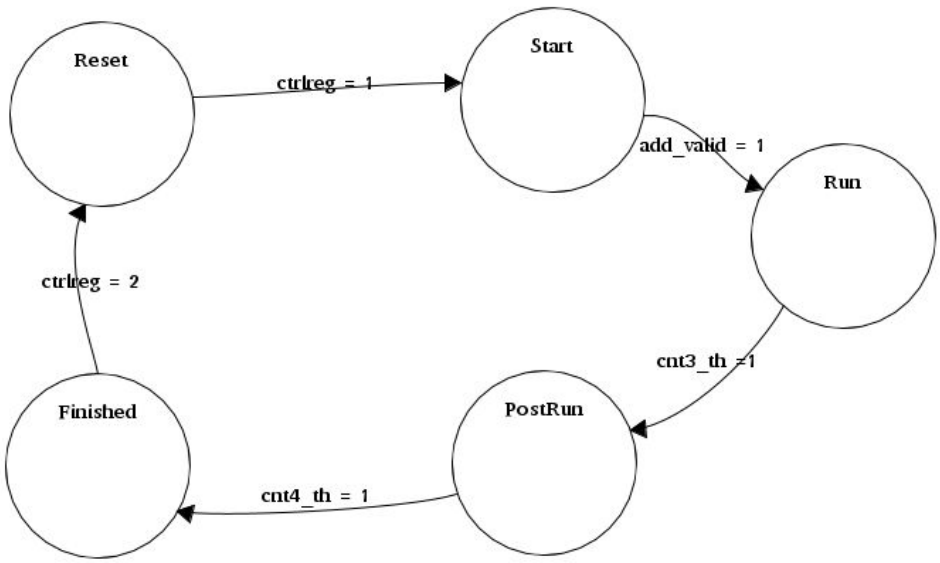


Es werden durch die Latenz von 6 Zyklen 6 unterschiedliche Summe gebildet, die nacheinander am Ausgang anliegen. Am Ende müssen die ebenfalls addiert werden.

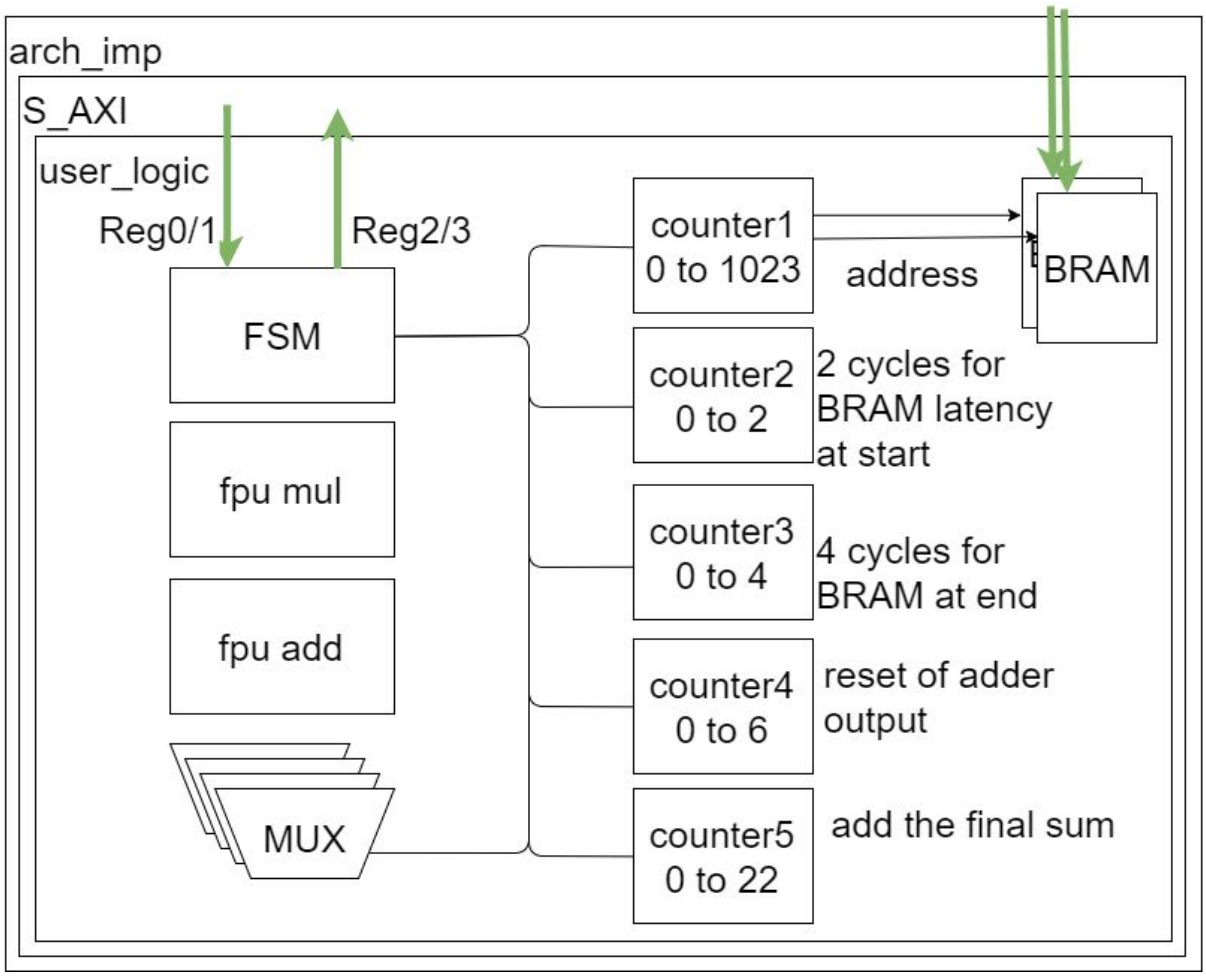
Datenfluss:



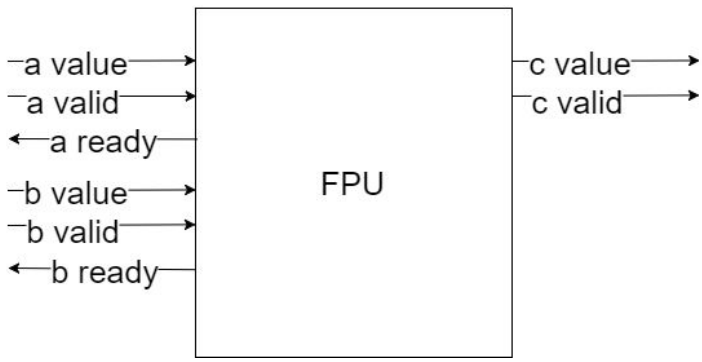
FSM



Modulübersicht:



FPU



Funktionale Beschreibung:

The default FSM state is RESET. In this state the values, counters and output is set to a default value. When the user send the control sequence to start the calculation (01 on register 0) the state changed to START and the counter 1 and 2 will be activated. Counter 1 counts the address for the blockram, counter 2 delay the valid input signals for the multiply FPU for 2 cycles. A state sequence in register 2 (0x00000002) display the user that the calculation has started. 6 cycles after the first valid values for the multiply FPU the add FPU get the first valid values. Further 6 cycles the

add FPU output the first valid value. With that the FSM switch in state RUN. When counter 1 reach the threshold of 1023 values the counter 3 will start counting. When counter 3 reach the threshold 4 the valid signals for the multiply FPU are set to false and the FSM switch to the POSTRUN state. When the first invalid value from the multiply FPU occur (6 cycles later) the input MUX of the adder switch to the output of the adder and counter 5 start to count. Both Inputs of the adder sample now the output of the adder. But the valid signals will be manipulated the calculate the final sum of the 6 values. The input a valid of the adder gets direct the output add_valid. The input b_valid gets only true when a is not ready and the add_valid output is true. When a is not ready it means that is has sampled a value and wait for the input of b. With the control the adder calculate the final sum without any further control. First value get sampled in a and the second is in b when the adder output it. When counter 5 reach his threshold of 22 the output of the adder is copied in register 3 for the user. Furthermore the counter 4 start to count and the mux switch to reset fpus. In that case the adder gets valid values 0.0 for 6 cycles to reset the adder output. When counter 4 reach his threshold the FSM switch to state FINISHED. A controlsequence for the user in register 2 (0x00000003) display the finished calculation. With a controlsequence in register 0 (02) the state switch to RESET and a new calculation can start. The picture show the startprocess of the calculation.

Waveforms:

Anfang: Waveform_start.png

Ende: waveform_end.png

markierte finale Summenbildung: finSum.png

Design:

design.png