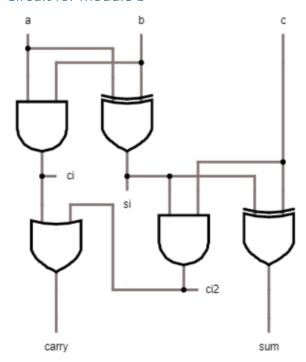
Part1

Module	Timing	Critical path
a) 10-bit number bitwise AND	0.05	Input i -> output i
b) 3:2 adder with "&", " ", "^", "~"	0.18	Input b -> output carry
c) 3:2 adder with "+"	0.18	Input b -> output carry
d) 10-bit adder with "+"	1.02	Input a[0] -> sum[10]
e) 11 5-bit adder with "+"	1.18	Input in3[0] -> sum[4]
f) 11-input adder from hw1/part7	0.72	Input num[4] -> output out[3]
g) 8-bit x 8-bit multiplier	1.48	Input b[2] -> out[14]
h) 16-bit x 16-bit multiplier	3.21	Input a[1] -> out[31]

Circuit for module b



Output of testbench for B

```
Elaborating the design hierarchy:
     Building instance overlay tables: ..... Done
     Generating native compiled code:
          worklib.block b:v <0x7defade4>
                streams: 0, words:
           worklib.tbench:vt <0x29346618>
                streams: 4, words: 2988
     Building instance specific data structures.
     Loading native compiled code:
                                  ..... Done
     Design hierarchy summary:
                           Instances Unique
          Modules:
                                  2
                                         2
          Registers:
                                 2
                                         2
                                 8
          Scalar wires:
           Initial blocks:
                                 1
                                         1
          Cont. assignments: 0
Pseudo assignments: 3
                                         5
                                         3
           Simulation timescale: 10ps
     Writing initial simulation snapshot: worklib.tbench:vt
Loading snapshot worklib.tbench:vt ...... Done
ncsim> source /apps/Cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> run
a b c | cout sum
000
      0
           0
001 0
            1
010 0 1
0 1 1 1 0
100 0 1
1011
          0
1 1 0 1
           0
1 1 1 1
            1
ncsim: *W,RNQUIE: Simulation is complete.
ncsim> exit
TOOL: ncverilog 15.20-s031: Exiting on Feb 14, 2018 at 16:22:50 PST (total:
00:00:02)
```

Subpart A code

```
module block_a (
    input [9:0] a,
    input [9:0] b,
    output [9:0] out
    );

assign out = a & b;
endmodule
```

Subpart B code

```
module block_b(
   input a,
   input b,
   input c,
```

```
output carry,
output sum
);
wire ci, si, ci2;

assign ci = a & b;
assign si = a ^ b;
assign ci2 = si & c;
assign sum = si ^ c;
assign carry = ci | ci2;
endmodule
```

Subpart C code

```
module block_c (
    input a,
    input b,
    input c,
    output carry,
    output sum
    );
    assign {carry, sum} = a + b + c;
endmodule
```

Subpart D code

```
module block_d (
    input [9:0] a,
    input [9:0] b,
    output [10:0] sum
    );
    assign sum = {a[9], a} + {b[9], b};
endmodule
```

Subpart E code

```
//HW2 part 1 e
//An adder which adds 11 5-bit numbers using verilog "+" and produces a 5-bit
sum

`timescale 1ns/10ps

module block_e (
    input [4:0] in0,
    input [4:0] in1,
    input [4:0] in2,
    input [4:0] in3,
    input [4:0] in4,
    input [4:0] in5,
    input [4:0] in6,
```

Subpart F code

```
//adder for 11 single-bit numbers
`timescale 1ns/10ps
module fulladder(
   input a,
   input b,
   input cin,
   output cout,
   output s
);
   wire ci, si, ci2;
   assign ci = a & b;
   assign si = a ^ b;
   assign ci2 = si & cin;
   assign s = si ^ cin;
   assign cout = ci | ci2;
endmodule
module adder42(
   input a,
   input b,
   input c,
   input d,
   input ci,
   output co,
   output c1,
   output s
   );
   wire so;
   fulladder FA1(.a (a),.b (b),.cin (c),.cout (co),.s (so));
   fulladder FA2(.a (so),.b (d),.cin (ci),.cout (c1),.s (s));
```

```
endmodule
module cdma (
  input [10:0] num,
  output reg [4:0] out
);
wire GND; //ground pin
assign GND = 1'b0;
//STAGE 1
  wire [1:0] st11, st12, st13, st14; //stage output
  fulladder FA11 (
    .a (num[0]),
    .b (num[1]),
    .cin (num[2]),
    .cout (st11[1]),
    .s (st11[0])
  );
  fulladder FA12 (
    .a (num[3]),
    .b (num[4]),
    .cin (num[5]),
    .cout (st12[1]),
    .s (st12[0])
  );
  fulladder FA13 (
    .a (num[6]),
    .b (num[7]),
    .cin (num[8]),
    .cout (st13[1]),
    .s (st13[0])
  );
  //half adder
  assign st14 = {num[9] & num[10], num[9] ^ num[10]};
//STAGE 2
  wire [2:0] st21;
  wire [1:0] st22; //stage output
  wire co; //carry between 4:2 adders
  adder42 A21 (
    .a (st11[0]),
    .b (st12[0]),
    .c (st13[0]),
    .d (st14[0]),
    .ci (GND),
    .co (co),
    .c1 (st21[1]),
    .s (st21[0])
  );
```

```
adder42 A22 (
    .a (st11[1]),
    .b (st12[1]),
    .c (st13[1]),
    .d (st14[1]),
    .ci (co),
    .co (st21[2]),
    .c1 (st22[1]),
    .s (st22[0])
  );
//STAGE 3 and 4
  reg [3:0] st3;
  always @(st21 or st22) begin
    st3 = st21 + {st22,1'b0};
//
      out = 5'b10101 + {st3, 1'b0};
    case (st3)
      4'b0000: out = 5'b10101; //0 -11
      4'b0001: out = 5'b10111; //1 -9
      4'b0010: out = 5'b11001; //2
                                    -7
      4'b0011: out = 5'b11011; //3
                                    -5
      4'b0100: out = 5'b11101; //4 -3
      4'b0101: out = 5'b11111; //5
                                    -1
      4'b0110: out = 5'b00001; //6 +1
      4'b0111: out = 5'b00011; //7 + 3
      4'b1000: out = 5'b00101; //8 +5
      4'b1001: out = 5'b00111; //9 +7
      4'b1010: out = 5'b01001; //10 +9
      4'b1011: out = 5'b01011; //11 +11
      default: out = 5'b00000; //def 0
    endcase
  end
endmodule
```

Subpart G code

```
module block_g (
   input [7:0] a,
   input [7:0] b,
   output [15:0] out
   );
   assign out = a * b;
endmodule // block_g
```

Subpart H code

```
module block_h (
   input [15:0] a,
   input [15:0] b,
   output [31:0] out
   );
```

```
assign out = a * b;
endmodule // block_h
```

Part 2

Dot diagram

· - signal, s - sign extend, ○ - inverted signal, b - MSB of multiplier (b[7]), x - repetition of the dot to the right.

Code for 8-bit x 8-bit multiplier

```
//HW2 P2
//
`timescale 1ns/10ps
//add necessary simple adders
module ha (
    input a,
    input b,
    output c,
    output s
    );
    assign s = a ^ b;
    assign c = a \& b;
endmodule //ha
module fa (
    input a,
    input b,
    input c,
    output carry,
```

```
output sum
   );
   assign carry = (a \& b) | ((a ^ b) \& c);
    assign sum = a ^ b ^ c;
endmodule //fa
module add42(
    input a,
    input b,
    input c,
    input d,
   input ci,
   output co, //carry out
   output cc, //carry to next add42
   output s
   );
   wire s internal;
   fa abc (.a (a), .b (b), .c (c), .carry(cc), .sum (s_internal));
    fa scc (.a (s_internal), .b (d), .c (ci), .carry(co), .sum (s));
endmodule //add42
//main module
module mult (
    input [7:0] a,
    input [7:0] b,
   input clk,
   output reg [15:0] out
);
// input clk sync
   reg [7:0] a_r, b_r;
   always @(posedge clk) begin
       a_r <= #1 a;
       b r <= #1 b;
   end
// stage 1. encoding
   //stage's output
   wire [7:0] p0,p1,p2,p3,p4,p5,p6,p7;
   //always @(a r or b r) begin
   assign p0 = a_r \& \{b_r[0], b_r[0], b_r[0], b_r[0], b_r[0], b_r[0], b_r[0]\};
   assign p1 = a_r \& \{b_r[1], b_r[1], b_r[1], b_r[1], b_r[1], b_r[1], b_r[1], b_r[1]\};
   assign p2 = a_r & \{b_r[2], b_r[2], b_r[2], b_r[2], b_r[2], b_r[2], b_r[2], b_r[2]\};
   assign p3 = a_r \& \{b_r[3], b_r[3], b_r[3], b_r[3], b_r[3], b_r[3], b_r[3]\};
   assign p4 = a_r & {b_r[4], b_r[4], b_r[4], b_r[4], b_r[4], b_r[4], b_r[4], b_r[4]};
   assign p5 = a_r & \{b_r[5], b_r[5], b_r[5], b_r[5], b_r[5], b_r[5], b_r[5], b_r[5]\};
   assign p6 = a_r & \{b_r[6], b_r[6], b_r[6], b_r[6], b_r[6], b_r[6], b_r[6], b_r[6]\};
    assign p7 = (~a_r) & \{b_r[7], b_r[7], b_r[7], b_r[7], b_r[7], b_r[7], b_r[7], b_r[7],
b_r[7]};
   //end
// stage 2. CSA
   //stage's output
   wire [11:0] st2 p0;
   wire [12:2] st2_p1;
   wire [15:4] st2 p2;
```

```
wire [15:6] st2_p3;
    wire [7:0] st2 c1; //carry between top 4:2 adders
    wire [9:0] st2_c2; //carry between bottom 4:2 adders
    assign st2_p0[0] = p0[0];
    assign st2_p2[4] = p4[0];
    //top row
          st2_t_col1 (.a (p0[1]), .b (p1[0]),
.c (st2_p1[2]), .s (st2_p0[1]));
          st2_t_col2 (.a (p0[2]), .b (p1[1]), .c (p2[0]),
.carry (st2_p1[3]), .sum (st2_p0[2]));
    add42 st2_t_col3 (.a (p0[3]), .b (p1[2]), .c (p2[1]), .d (p3[0]), .ci (1'b0),
.cc (st2_c1[0]), .co (st2_p1[4]), .s (st2_p0[3]));
    add42 st2_t_col4 (.a (p0[4]), .b (p1[3]), .c (p2[2]), .d (p3[1]), .ci (st2_c1[0]),
.cc (st2_c1[1]), .co (st2_p1[5]), .s (st2_p0[4]));
    add42 st2_t_col5 (.a (p0[5]), .b (p1[4]), .c (p2[3]), .d (p3[2]), .ci (st2_c1[1]),
.cc (st2_c1[2]), .co (st2_p1[6]), .s (st2_p0[5]));
    add42 st2_t_col6 (.a (p0[6]), .b (p1[5]), .c (p2[4]), .d (p3[3]), .ci (st2_c1[2]),
.cc (st2 c1[3]), .co (st2 p1[7]), .s (st2 p0[6]));
    add42 st2_t_col7 (.a (p0[7]), .b (p1[6]), .c (p2[5]), .d (p3[4]), .ci (st2_c1[3]),
.cc (st2_c1[4]), .co (st2_p1[8]), .s (st2_p0[7]));
add42 st2_t_col8 (.a (p0[7]), .b (p1[7]), .c (p2[6]), .d (p3[5]), .ci (st2_c1[4]),
.cc (st2_c1[5]), .co (st2_p1[9]), .s (st2_p0[8]));
    add42 st2_t_col9 (.a (p0[7]), .b (p1[7]), .c (p2[7]), .d (p3[6]), .ci (st2_c1[5]),
.cc (st2_c1[6]), .co (st2_p1[10]), .s (st2_p0[9]));
    add42 st2_t_col10 (.a (p0[7]), .b (p1[7]), .c (p2[7]), .d (p3[7]), .ci (st2_c1[6]),
.cc (st2_c1[7]), .co (st2_p1[11]), .s (st2_p0[10]));
    add42 st2_t_col11 (.a (p0[7]), .b (p1[7]), .c (p2[7]), .d (p3[7]), .ci (st2_c1[7]),
                 .co (st2_p1[12]), .s (st2_p0[11]));
.cc (),
    //bottom row
    add42 \ st2\_b\_col5 \ (.a \ (p4[1]), .b \ (p5[0]), .c \ (b\_r[7]), .d \ (b\_r[7]), .ci \ (1'b0), .cc
(st2_c2[8]), .co (st2_p3[6]), .s (st2_p2[5]));
    add42 st2_b_col6 (.a (p4[2]), .b (p5[1]), .c (p6[0]), .d (b_r[7]), .ci (st2_c2[8]),
.cc (st2 c2[9]), .co (st2 p3[7]), .s (st2 p2[6]));
    add42 st2_b_col7 (.a (p4[3]), .b (p5[2]), .c (p6[1]), .d (p7[0]), .ci (st2_c2[9]),
.cc (st2_c2[0]), .co (st2_p3[8]), .s (st2_p2[7]));
    add42 st2_b_col8 (.a (p4[4]), .b (p5[3]), .c (p6[2]), .d (p7[1]), .ci (st2_c2[0]),
.cc (st2_c2[1]), .co (st2_p3[9]), .s (st2_p2[8]));
add42 st2_b_col9 (.a (p4[5]), .b (p5[4]), .c (p6[3]), .d (p7[2]), .ci (st2_c2[1]),
.cc (st2_c2[2]), .co (st2_p3[10]), .s (st2_p2[9]));
    add42 st2_b_col10 (.a (p4[6]), .b (p5[5]), .c (p6[4]), .d (p7[3]), .ci (st2_c2[2]),
.cc (st2_c2[3]), .co (st2_p3[11]), .s (st2_p2[10]));
    add42 st2_b_col11 (.a (p4[7]), .b (p5[6]), .c (p6[5]), .d (p7[4]), .ci (st2_c2[3]),
.cc (st2_c2[4]), .co (st2_p3[12]), .s (st2_p2[11]));
    add42 st2_b_col12 (.a (p4[7]), .b (p5[7]), .c (p6[6]), .d (p7[5]), .ci (st2_c2[4]),
.cc (st2_c2[5]), .co (st2_p3[13]), .s (st2_p2[12]));
    add42 st2_b_col13 (.a (p4[7]), .b (p5[7]), .c (p6[7]), .d (p7[6]), .ci (st2_c2[5]),
.cc (st2_c2[6]), .co (st2_p3[14]), .s (st2_p2[13]));
    add42 st2_b_col14 (.a (p4[7]), .b (p5[7]), .c (p6[7]), .d (p7[7]), .ci (st2_c2[6]),
.cc (st2_c2[7]), .co (st2_p3[15]), .s (st2_p2[14]));
    add42 st2_b_col15 (.a (p4[7]), .b (p5[7]), .c (p6[7]), .d (p7[7]), .ci (st2_c2[7]),
.cc (),
                 .co (),
                                    .s (st2_p2[15]));
// stage 3. CSA cont
    //stage output
```

```
wire [15:0] st3_p0; //row 0
    wire [15:3] st3 p1; //row 1
    wire [8:0] st3_c; //carry between 4:2 adders
    //pass through bits
    assign st3 p0[1:0] = st2 p0[1:0];
    ha st_b_col2
                     (.a (st2_p0[2]), .b (st2_p1[2]),
.c (st3 p1[3]),
                 .s (st3 p0[2]);
    ha st_b_col3
                     (.a (st2_p0[3]), .b (st2_p1[3]),
.c (st3_p1[4]), .s (st3_p0[3]));
                     (.a (st2 p0[4]), .b (st2 p1[4]), .c (st2 p2[4]),
    fa st_b_col4
.carry (st3_p1[5]), .sum (st3_p0[4]));
                     (.a (st2_p0[5]), .b (st2_p1[5]), .c (st2_p2[5]),
    fa st b col5
.carry (st3 p1[6]), .sum (st3 p0[5]));
    add42 st_b_col6 (.a (st2_p0[6]), .b (st2_p1[6]), .c (st2_p2[6]), .d (st2_p3[6]),
                .cc (st3_c[0]), .co (st3_p1[7]), .s (st3_p0[6]));
.ci (1'b0),
    add42 st_b_col7 (.a (st2_p0[7]), .b (st2_p1[7]), .c (st2_p2[7]),
                                                                         .d (st2_p3[7]),
.ci (st3_c[0]), .cc (st3_c[1]), .co (st3_p1[8]), .s (st3_p0[7]));
    add42 st b col8 (.a (st2 p0[8]), .b (st2 p1[8]), .c (st2 p2[8]),
                                                                         .d (st2 p3[8]),
.ci (st3_c[1]), .cc (st3_c[2]), .co (st3_p1[9]), .s (st3_p0[8]));
    add42 st_b_col9 (.a (st2_p0[9]), .b (st2_p1[9]), .c (st2_p2[9]),
                                                                         .d (st2 p3[9]),
.ci (st3_c[2]), .cc (st3_c[3]), .co (st3_p1[10]), .s (st3_p0[9]));
    add42 st_b_col10 (.a (st2_p0[10]), .b (st2_p1[10]), .c (st2_p2[10]), .d
(st2 p3[10]), .ci (st3 c[3]), .cc (st3 c[4]), .co (st3 p1[11]), .s (st3 p0[10]));
    add42 st_b_col11 (.a (st2_p0[11]), .b (st2_p1[11]), .c (st2_p2[11]), .d
(st2_p3[11]), .ci (st3_c[4]), .cc (st3_c[5]), .co (st3_p1[12]), .s (st3_p0[11]));
    add42 st_b_col12 (.a (st2_p0[11]), .b (st2_p1[12]), .c (st2_p2[12]), .d
(st2_p3[12]), .ci (st3_c[5]), .cc (st3_c[6]), .co (st3_p1[13]), .s (st3_p0[12]));
    add42 st b col13 (.a (st2 p0[11]), .b (st2 p1[12]), .c (st2 p2[13]), .d
(st2_p3[13]), .ci (st3_c[6]), .cc (st3_c[7]), .co (st3_p1[14]), .s (st3_p0[13]));
    add42 st_b_col14 (.a (st2_p0[11]), .b (st2_p1[12]), .c (st2_p2[14]), .d
(st2_p3[14]), .ci (st3_c[7]), .cc (st3_c[8]), .co (st3_p1[15]), .s (st3_p0[14]));
    add42 st_b_col15 (.a (st2_p0[11]), .b (st2_p1[12]), .c (st2_p2[15]), .d
(st2_p3[15]), .ci (st3_c[8]), .cc (),
                                             .co (),
                                                               .s (st3_p0[15]));
// stage 5. CPA
    reg [15:0] out_c;
    always @(st3_p0 or st3_p1) begin
        out c = st3 p0 + \{st3 p1, 3'b000\};
// output clk sync
    always @(posedge clk) begin
        out <= #1 out c;
    end
endmodule
```

Testbench for multiplier

```
//test bench for 8x8 multiplier

`timescale 1ns/10ps

module tbench();
```

```
reg [7:0] a, b;
    wire [15:0] out;
    reg clk;
    integer i;
    reg [7:0] a_tst [23:0], b_tst [23:0];
    reg [15:0] o tst [23:0];
    mult block (.a (a), .b (b), .out (out), .clk (clk));
    initial begin
        //tracer
        $recordfile("mult test");
        $recordvars(tbench);
        //fill test cases
        a_tst[0] = 8'b0000_0000; b_tst[0] = 8'b0000_0000; o_tst[0] =
16'b0000 0000 0000 0000; //
                                  0 x
        a tst[1] = 8'b0000_0001; b_tst[1] = 8'b0111_1111; o_tst[1] =
16'b0000 0000 0111 1111; //
                                 1 x max pos
        a tst[2] = 8'b0000 0001; b tst[2] = 8'b1000 0000; o tst[2] =
16'b1111 1111 1000 0000; //
                                  1 x max neg
        a tst[3] = 8'b0111 1111; b tst[3] = 8'b0000 0001; o tst[3] =
16'b0000_0000_0111_1111; // max pos x
        a_tst[4] = 8'b1000_0000; b_tst[4] = 8'b0000_0001; o_tst[4] =
16'b1111_1111_1000_0000; // max neg x
        a_tst[5] = 8'b0111_1111; b_tst[5] = 8'b0111_1111; o_tst[5] =
16'b0011 1111 0000 0001; // max pos x max pos
        a_tst[6] = 8'b0111_1111; b_tst[6] = 8'b1000_0000; o_tst[6] =
16'b1100 0000 1000 0000; // max pos x max neg
        a_tst[7] = 8'b1000_0000; b_tst[7] = 8'b0111_1111; o_tst[7] =
16'b1100 0000 1000 0000; // max neg x max pos
        a_tst[8] = 8'b1000_0000; b_tst[8] = 8'b1000_0000; o_tst[8] =
16'b0100_0000_0000_0000; // max neg x max neg
        a tst[9] = 8'b0010 1000; b tst[9] = 8'b0010 0000; o tst[9] =
                          // 40 x 32 = 1280
16'b0000 0101 0000 0000;
        a tst[10] = 8'b1111 0001; b tst[10] = 8'b1000 0111; o tst[10] =
16'b0000 0111 0001 0111; // -15 x -121 = 1815
        a_tst[11] = 8'b0001_1110; b_tst[11] = 8'b1111_1111; o_tst[11] =
16'b1111 1111 1110 0010; // 30 x -1 = -30
        a_tst[12] = 8'b1111_1111; b_tst[12] = 8'b1111_1111; o_tst[12] =
16'b0000_0000_0000_0001; // -1 \times -1 = 1
        a tst[13] = 8'b1111 1111; b tst[13] = 8'b0010 1101; o tst[13] =
16'b1111 1111 1101 0011; // -1 x 45 = -45
        a_tst[14] = 8'b0000_0000; b_tst[14] = 8'b0110_0100; o_tst[14] =
16'b0000 0000 0000 0000; //
                             0 \times 100 = 0
        a_tst[15] = 8'b0110_0100; b_tst[15] = 8'b0000_0000; o_tst[15] =
16'b0000_0000_0000_0000; // 100 x 0 = 0
        a tst[16] = 8'b0000 0001; b tst[16] = 8'b1111 1111; o tst[16] =
16'b1111\ 1111\ 1111\ 1111;\ //\ 1\ x\ -1\ =\ -1
        a tst[17] = 8'b1111 1111; b tst[17] = 8'b0000 0001; o tst[17] =
16'b1111 1111 1111 1111; // -1 x 1 = -1
        a tst[18] = 8'b0110 \ 0100; b tst[18] = 8'b0110 \ 0100; o tst[18] =
16'b0010 0111 0001 0000; // 100 x 100 = 10000
```

```
a_tst[19] = 8'b1100_1101; b_tst[19] = 8'b0101_0011; o_tst[19] =
16'b1110 1111 0111 0111; // -51 x 83 = -4233
        a_tst[20] = 8'b1100_0111; b_tst[20] = 8'b1010_0011; o_tst[20] =
16'b0001_0100_1011_0101; // -57 x -93 = 5301
        a_tst[21] = 8'b1101_1101; b_tst[21] = 8'b0100_1110; o_tst[21] =
16'b1111_0101_0101_0110; // -35 \times 78 = -2730
        a tst[22] = 8'b1011 1000; b tst[22] = 8'b0101 1011; o tst[22] =
16'b1110_0110_0110_1000; // -72 x 91 = -6552
        a_tst[23] = 8'b0100_0000; b_tst[23] = 8'b0001_1101; o_tst[23] =
16'b0000 0111 0100 0000; // 64 x 29 = 1856
        //start tests
        clk = 1'b0;
        for (i = 0; i < 24; i = i + 1) begin
            a = a tst[i];
            b = b_tst[i];
            #10
            clk = 1'b1; //start
            #10
            clk = 1'b0;
            #10
            clk = 1'b1; //read answer
            #10
            clk = 1'b0;
            if (out == o tst[i])
                $display("%d) %b x %b = %b",i,a,b,out);
                $display("%d) %b x %b got %b expected %b",i,a,b,out,o tst[i]);
        end
    end
    // generate a clock. osc inverts clock every #10
    //always begin
        #10;
                              // wait for initial block to initialize clock
    //
    //
        clk = \sim clk;
    //end
endmodule
```

Test output (passed)

```
errors: 0, warnings: 0
            Caching library 'worklib' ..... Done
      Elaborating the design hierarchy:
      Building instance overlay tables: ..... Done
      Generating native compiled code:
            worklib.fa:v <0x52bf646d>
                  streams:
                            0, words:
            worklib.ha:v <0x52cafae2>
                  streams: 0, words:
            worklib.mult:v <0x3cc69217>
                  streams: 8, words: 4009
            worklib.tbench:vt <0x0100204a>
                  streams: 3, words: 11212
      Building instance specific data structures.
      Loading native compiled code:
                                   ..... Done
      Design hierarchy summary:
                             Instances Unique
            Modules:
                                  98
            Registers:
                                   11
                                          11
            Scalar wires:
                                  142
                                 66
            Expanded wires:
            Vectored wires:
                                  3
            Always blocks:
                                   3
                                           3
            Initial blocks:
                                   1
                                           1
            Cont. assignments:
                                  2
                                          15
            Pseudo assignments:
                                           3
            Simulation timescale: 10ps
      Writing initial simulation snapshot: worklib.tbench:vt
Loading snapshot worklib.tbench:vt ...... Done
ncsim> source /apps/Cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> run
         1) 00000001 x 01111111 = 0000000001111111
         2) 00000001 x 10000000 = 11111111110000000
         3) 01111111 x 00000001 = 0000000001111111
         4) 10000000 x 00000001 = 11111111110000000
         5) 01111111 x 01111111 = 00111111100000001
         6) 01111111 x 10000000 = 1100000010000000
         7) 10000000 x 01111111 = 1100000010000000
         8) 10000000 x 10000000 = 010000000000000
         9) 00101000 x 00100000 = 0000010100000000
        10) 11110001 x 10000111 = 0000011100010111
        11) 00011110 x 11111111 = 1111111111100010
        13) 11111111 x 00101101 = 1111111111010011
        14) 00000000 x 01100100 = 0000000000000000
        15) 01100100 x 00000000 = 0000000000000000
        16) 00000001 x 11111111 = 111111111111111
        17) 11111111 x 00000001 = 111111111111111
        18) 01100100 x 01100100 = 0010011100010000
        19) 11001101 x 01010011 = 1110111101110111
        20) 11000111 x 10100011 = 0001010010110101
        21) 11011101 x 01001110 = 1111010101010110
        22) 10111000 x 01011011 = 1110011001101000
        23) 01000000 x 00011101 = 0000011101000000
ncsim: *W,RNQUIE: Simulation is complete.
ncsim> exit
```

Test output (failed)

For this test, purposely make mistake at CPA, by giving not enough bit-shift for second carry-save value. Put 2 zeros, instead of three.

```
ncverilog +access+r -l mult.logv -f mult.vfv
ncverilog(64): 15.20-s031: (c) Copyright 1995-2017 Cadence Design Systems, Inc.
file: mult.vt
      module worklib.tbench:vt
            errors: 0, warnings: 0
file: mult.v
      module worklib.ha:v
            errors: 0, warnings: 0
      module worklib.fa:v
            errors: 0, warnings: 0
      module worklib.add42:v
            errors: 0, warnings: 0
      module worklib.mult:v
            errors: 0, warnings: 0
            Caching library 'worklib' ..... Done
      Elaborating the design hierarchy:
      Building instance overlay tables: ..... Done
      Generating native compiled code:
            worklib.fa:v <0x52bf646d>
                  streams:
                            0, words:
            worklib.ha:v <0x52cafae2>
                  streams:
                            0, words:
            worklib.mult:v <0x3cc69217>
                  streams: 8, words: 4026
            worklib.tbench:vt <0x0100204a>
                  streams: 3, words: 11212
      Building instance specific data structures.
      Loading native compiled code:
                                     ..... Done
      Design hierarchy summary:
                             Instances Unique
            Modules:
                                   98
            Registers:
                                   11
                                           11
            Scalar wires:
                                 142
                                 66
            Expanded wires:
            Vectored wires:
                                   3
            Always blocks:
                                    3
                                           3
            Cont. assignments:
                                   1
                                           1
                                   2
                                          15
            Pseudo assignments:
                                   3
                                           3
            Simulation timescale: 10ps
      Writing initial simulation snapshot: worklib.tbench:vt
Loading snapshot worklib.tbench:vt ...... Done
ncsim> source /apps/Cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> run
         1) 00000001 x 01111111 = 0000000001111111
         2) 00000001 x 10000000 got 11111111101000000 expected 11111111110000000
         3) 01111111 x 00000001 = 0000000001111111
         4) 10000000 x 00000001 = 11111111110000000
         5) 01111111 x 01111111 got 0011000001001101 expected 0011111100000001
         6) 01111111 x 10000000 got 1100000001000000 expected 1100000010000000
         7) 10000000 x 01111111 got 011110001000000 expected 1100000010000000
```

```
8) 10000000 x 10000000 got 0011111111000000 expected 0100000000000000
          9) 00101000 x 00100000 = 0000010100000000
         10) 11110001 x 10000111 got 1111111011010111 expected 0000011100010111
         11) 00011110 x 11111111 got 1111110000111010 expected 11111111111100010
         12) 11111111 x 11111111 got 100000000001101 expected 0000000000000001
         13) 11111111 x 00101101 got 1111111110101011 expected 11111111111010011
         14) 00000000 x 01100100 = 0000000000000000
         15) 01100100 x 00000000 = 0000000000000000
         16) 00000001 x 11111111 = 111111111111111
         17) 11111111 x 00000001 = 111111111111111
         18) 01100100 x 01100100 = 0010011100010000
         19) 11001101 x 01010011 got 1101111101110111 expected 11101111011110111
         20) 11000111 x 10100011 got 1111110000101101 expected 0001010010110101
         21) 11011101 x 01001110 got 11101010110101 expected 11110101010110
         22) 10111000 x 01011011 got 1011101101101000 expected 1110011001101000
         23) 01000000 x 00011101 = 0000011101000000
ncsim: *W,RNQUIE: Simulation is complete.
ncsim> exit
```

Area report

```
************
Report : area
Design : mult
Version: J-2014.09-SP2
Date : Sun Feb 18 18:40:42 2018
Information: Updating design information... (UID-85)
Library(s) Used:
    NangateOpenCellLibrary (File:
/software/Synopsys/DesignCompiler/EEC281/lib/nangate45/NangateOpenCellLibrary.db)
Number of ports:
                                             33
Number of nets:
                                            357
Number of cells:
                                            314
Number of combinational cells:
                                            282
Number of sequential cells:
                                             32
Number of macros/black boxes:
                                              0
Number of buf/inv:
                                             24
Number of references:
Combinational area:
                                    381,443996
Buf/Inv area:
                                     13.566000
Noncombinational area: 13.566000

Nacro/Black Box area: 0.000000

Net Interconnect area: undefined (Wire load has zero net area)
Total cell area:
                                     526.147991
Total area:
                             undefined
```

Timing report

Report : timing

```
-path full
       -delay max
       -nworst 10
       -max paths 10
Design : mult
Version: J-2014.09-SP2
Date : Sun Feb 18 18:40:43 2018
************
Operating Conditions: typical Library: NangateOpenCellLibrary
Wire Load Model Mode: top
  Startpoint: b_r_reg[0] (rising edge-triggered flip-flop clocked by clk)
  Endpoint: out reg[15]
           (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max
  Des/Clust/Port Wire Load Model Library
                  5K_hvratio_1_1 NangateOpenCellLibrary
  Point
                                       Incr Path
  clock clk (rise edge)
                                     0.00 0.00
 clock network delay (ideal) 0.00
b_r_reg[0]/CK (DFF_X1) 0.00
b_r_reg[0]/QN (DFF_X1) 0.11
                                                0.00
                                                0.00 r
                                      0.11 0.11 f
0.07 0.18 r
  U328/ZN (NOR2_X1)
  U259/Z (XOR2 X1)
                                      0.09
                                                0.27 r
  U157/Z (XOR2_X1)
                                      0.10
                                                0.37 r
                                               0.47 r
0.56 r
0.62 f
  U156/Z (XOR2 X1)
                                       0.10
  U154/Z (XOR2_X1)
                                       0.10
                                       0.06
  U286/ZN (XNOR2_X1)
  U153/Z (XOR2_X1)
                                        0.09
                                                0.70 f
  U1 4/CO (FA_X1)
                                        0.11
                                                0.81 f
                                                0.90 f
  U1 5/CO (FA X1)
                                        0.09
                                                 1.00 f
  U1 6/C0 (FA X1)
                                       0.09
  U1 7/CO (FA X1)
                                        0.09
                                                1.09 f
  U1 8/CO (FA X1)
                                        0.09
                                                1.18 f
  U1 9/C0 (FA X1)
                                        0.09
                                                1.28 f
  U1_10/C0 (FA_X1)
                                       0.09
                                                 1.37 f
                                        0.09
                                                1.46 f
  U1_11/CO (FA_X1)
  U1 12/CO (FA X1)
                                        0.09
                                                1.55 f
  U1 13/CO (FA X1)
                                                1.65 f
                                        0.09
  U1 14/CO (FA X1)
                                        0.09
                                                 1.74 f
                                       0.13
  U1_15/S (FA_X1)
                                                 1.87 r
  out reg[15]/D (DFF X1)
                                        0.01
                                                 1.88 r
  data arrival time
                                                 1.88
                                 4.00
0.00
-0.20
  clock clk (rise edge)
                                                 4.00
  clock network delay (ideal)
                                                 4.00
  clock uncertainty
                                                 3.80
  out reg[15]/CK (DFF X1)
                                      0.00
                                                 3.80 r
  library setup time
                                      -0.03
                                                 3.77
  data required time
                                                  3.77
  _____
```

```
data required time
                                              3.77
data arrival time
                                              -1.88
slack (MET)
                                              1.89
Startpoint: b r reg[0] (rising edge-triggered flip-flop clocked by clk)
Endpoint: out_reg[15]
         (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
Des/Clust/Port Wire Load Model Library
-----
       5K_hvratio_1_1 NangateOpenCellLibrary
mult
                                    Incr
Point
                                             Path
-----
                              0.00 0.00
0.00 0.00
0.00 0.00 r
0.11 0.11 f
0.07 0.18 r
0.09 0.27 r
0.10 0.37 r
clock clk (rise edge)
clock network delay (ideal)
b r reg[0]/CK (DFF X1)
b_r_reg[0]/QN (DFF_X1)
U328/ZN (NOR2 X1)
U259/Z (XOR2_X1)
U157/Z (XOR2 X1)
U156/Z (XOR2_X1)
                                    0.10
                                            0.47 r
U154/Z (XOR2_X1)
                                             0.56 r
                                    0.10
U286/ZN (XNOR2 X1)
                                    0.06
                                             0.62 f
U153/Z (XOR2_X1)
                                    0.09
                                             0.70 f
                                    0.10
U1 4/CO (FA X1)
                                             0.81 f
U1_5/CO (FA_X1)
                                    0.09
                                             0.90 f
                                          0.99 f
1.09 f
1.18 f
U1 6/CO (FA X1)
                                    0.09
U1_7/CO (FA_X1)
                                    0.09
                                    0.09
U1_8/CO (FA_X1)
U1_9/CO (FA_X1)
                                    0.09
                                             1.27 f
U1 10/CO (FA X1)
                                    0.09
                                             1.37 f
                                    0.09 1.46 f
0.09 1.55 f
0.09 1.64 f
0.09 1.74 f
0.13 1.87 r
0.01 1.88 r
U1 11/CO (FA X1)
U1 12/CO (FA X1)
U1 13/CO (FA X1)
U1 14/CO (FA X1)
U1 15/S (FA X1)
out_reg[15]/D (DFF_X1)
data arrival time
                                              1.88
clock clk (rise edge)
                                   4.00
                                              4.00
clock network delay (ideal)
                               0.00
-0.20
                                    0.00
                                              4.00
clock uncertainty
                                              3.80
out reg[15]/CK (DFF X1)
                                   0.00
                                              3.80 r
library setup time
                                   -0.03
                                             3.77
data required time
______
data required time
                                              3.77
data arrival time
______
slack (MET)
                                              1.89
```

```
Startpoint: b_r_reg[0] (rising edge-triggered flip-flop clocked by clk)
Endpoint: out reg[15]
         (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
Des/Clust/Port Wire Load Model Library
-----
               5K_hvratio_1_1 NangateOpenCellLibrary
mult
Point
                                  Incr
                                            Path
                     0.00 0.00
clock clk (rise edge)
                                  0.00
                                            0.00
clock network delay (ideal)
                                  0.00
                                           0.00 r
b_r_reg[0]/CK (DFF_X1)
                                  0.11
                                           0.11 f
b r reg[0]/QN (DFF X1)
                                            0.18 r
U328/ZN (NOR2_X1)
                                  0.07
U259/Z (XOR2 X1)
                                            0.27 r
                                   0.09
U157/Z (XOR2_X1)
                                            0.37 r
                                   0.10
                                            0.47 r
U156/Z (XOR2 X1)
                                   0.10
U154/Z (XOR2 X1)
                                   0.10
                                            0.56 r
U286/ZN (XNOR2 X1)
                                    0.06
                                            0.62 f
U153/Z (XOR2 X1)
                                    0.09
                                            0.70 f
                                           0.81 f
U1_4/CO (FA_X1)
                                    0.11
U1 5/CO (FA X1)
                                    0.09
                                            0.90 f
U1_6/CO (FA_X1)
                                    0.09
                                            1.00 f
U1_7/CO (FA_X1)
                                    0.09
                                            1.09 f
                                    0.09
0.09
                                            1.18 f
U1 8/CO (FA X1)
U1 9/CO (FA X1)
                                            1.27 f
U1 10/CO (FA X1)
                                    0.09
                                            1.36 f
U1_11/CO (FA_X1)
                                   0.09
                                            1.46 f
                                           1.55 f
1.64 f
U1 12/CO (FA X1)
                                    0.09
U1_13/CO (FA_X1)
                                   0.09
U1_14/CO (FA_X1)
                                   0.09
                                            1.74 f
U1_15/S (FA_X1)
                                   0.13
                                            1.87 r
out reg[15]/D (DFF X1)
                                    0.01
                                            1.88 r
data arrival time
                                             1.88
clock clk (rise edge)
clock network delay (ideal) 0.00
clock uncertainty -0.20
out_reg[15]/CK (DFF_X1) 0.00
-0.03
                                          4.00
                                  4.00
                                            4.00
                                            3.80
                                             3.80 r
                                             3.77
data required time
_____
data required time
                                             3.77
data arrival time
                                            -1.88
_____
slack (MET)
                                             1.89
Startpoint: b_r_reg[0] (rising edge-triggered flip-flop clocked by clk)
Endpoint: out reg[15]
         (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
```

mult	Wire Load Model	Library	
mare	5K_hvratio_1_1	Nangate0	OpenCellLibrary
Point		Incr	Path
clock clk (rise ed		0.00	0.00
clock network dela	<u> </u>	0.00	0.00
b_r_reg[0]/CK (DF		0.00	0.00 r
b_r_reg[0]/QN (DF		0.11	0.11 f
U328/ZN (NOR2_X1)	- ·	0.07	0.18 r
U259/Z (XOR2_X1)		0.09	0.27 r
U157/Z (XOR2_X1)		0.10	0.37 r
U156/Z (XOR2_X1)		0.10	0.47 r
U154/Z (XOR2_X1)		0.10	0.56 r
U286/ZN (XNOR2_X1))	0.06	0.62 f
U153/Z (XOR2_X1)		0.09	0.70 f
U1_4/CO (FA_X1)		0.11	0.81 f
U1_5/CO (FA_X1)		0.09	0.90 f
U1_6/CO (FA_X1)		0.09	1.00 f
U1_7/CO (FA_X1)		0.09	1.09 f
U1_8/CO (FA_X1)		0.09	1.18 f
U1_9/CO (FA_X1)		0.09	1.28 f
U1_10/CO (FA_X1)		0.09	1.36 f
U1_11/CO (FA_X1)		0.09	1.46 f
U1_12/CO (FA_X1)		0.09	1.55 f
U1_13/CO (FA_X1)		0.09	1.64 f
U1_14/CO (FA_X1)		0.09	1.74 f
U1_15/S (FA_X1)		0.13	1.87 r
out_reg[15]/D (DFI	F X1)	0.01	1.88 r
data arrival time	_ /		1.88
clock clk (rise ed	dge)	4.00	4.00
clock network dela	ay (ideal)	0.00	4.00
clock uncertainty		-0.20	3.80
out_reg[15]/CK (DF		0.00	3.80 r
library setup time	2	-0.03	3.77
data required time	e 		3.77
data required time			3.77
data arrival time			-1.88
slack (MET)			1.89

clock clk (rise e		0.00	0.00
clock network del		0.00	0.00
b_r_reg[0]/CK (DF	– <i>i</i>	0.00	0.00 r
b_r_reg[0]/QN (DF	_ ,	0.11	0.11 f
U328/ZN (NOR2_X1))	0.07	0.18 r
U259/Z (XOR2_X1)		0.09	0.27 r
U157/Z (XOR2_X1)		0.10	0.37 r
U156/Z (XOR2_X1)		0.10	0.47 r
U154/Z (XOR2_X1)		0.10	0.56 r
U286/ZN (XNOR2_X1	1)	0.06	0.62 f
U153/Z (XOR2_X1)	•	0.09	0.70 f
U1_4/CO (FA_X1)		0.11	0.81 f
U1_5/CO (FA_X1)		0.09	0.90 f
U1_6/CO (FA_X1)		0.09	0.99 f
U1_7/CO (FA_X1)		0.09	1.09 f
U1_8/C0 (FA_X1)		0.09	1.18 f
U1_9/C0 (FA_X1)		0.09	1.27 f
U1_10/C0 (FA_X1)		0.09	1.36 f
U1_11/CO (FA_X1)		0.09	1.46 f
U1_12/C0 (FA_X1)		0.09	1.55 f
U1_13/C0 (FA_X1)		0.09	
U1_14/CO (FA_X1)		0.09	1.74 f
U1_15/S (FA_X1)		0.13	1.87 r
out_reg[15]/D (DF	FF_X1)	0.01	1.88 r
data arrival time	– <i>i</i>		1.88
clock clk (rise e	edge)	4.00	4.00
clock network del		0.00	4.00
clock uncertainty		-0.20	3.80
out_reg[15]/CK ([0.00	3.80 r
library setup tim		-0.03	3.77
data required tim			3.77
	me		3.77
data required tim			
data required time	9		-1.88
data arrival time	e 		-1.88 1.89
	2		
data arrival time slack (MET) Startpoint: b_r_r Endpoint: out_reg	reg[0] (rising edge-t		1.89
data arrival time	reg[0] (rising edge-t g[15]	-flop clocke	1.89
data arrival time slack (MET) Startpoint: b_r_r Endpoint: out_reg	reg[0] (rising edge-t g[15] g edge-triggered flip	-flop clocke Library	1.89 ip-flop clocked by clk) ed by clk)
data arrival time slack (MET) Startpoint: b_r_r Endpoint: out_reg	reg[0] (rising edge-t g[15] g edge-triggered flip Wire Load Model	-flop clocke Library	1.89 ip-flop clocked by clk) ed by clk)
data arrival time	reg[0] (rising edge-t g[15] g edge-triggered flip Wire Load Model 5K_hvratio_1_1	Library Nangate Incr	1.89 ip-flop clocked by clk) ed by clk) OpenCellLibrary Path
data arrival time	reg[0] (rising edge-t g[15] g edge-triggered flip Wire Load Model 5K_hvratio_1_1	Library Nangate Incr	1.89 ip-flop clocked by clk) ed by clk) OpenCellLibrary Path 0.00
data arrival time	reg[0] (rising edge-t g[15] g edge-triggered flip Wire Load Model 5K_hvratio_1_1	Library Nangate Incr 0.00 0.00	1.89 ip-flop clocked by clk) ed by clk) OpenCellLibrary Path 0.00 0.00
data arrival time	reg[0] (rising edge-t g[15] g edge-triggered flip Wire Load Model 5K_hvratio_1_1 edge) lay (ideal)	Library NangateO Incr 0.00 0.00	1.89 Lip-flop clocked by clk) Lip-flop clocked by clk) DipenCellLibrary Path 0.00 0.00 0.00 r
data arrival time	reg[0] (rising edge-tg[15] g edge-triggered flip Wire Load Model 5K_hvratio_1_1 edge) lay (ideal) FF_X1) FF_X1)	Library NangateO Incr 0.00 0.00 0.00 0.11	1.89 Lip-flop clocked by clk) Lip-flop clocked by clk) DipenCellLibrary Path 0.00 0.00 0.00 0.00 r 0.11 f
data arrival time	reg[0] (rising edge-tg[15] g edge-triggered flip Wire Load Model 5K_hvratio_1_1 edge) lay (ideal) FF_X1) FF_X1)	Library NangateO Incr 0.00 0.00	1.89 Lip-flop clocked by clk) Lip-flop clocked by clk) DipenCellLibrary Path 0.00 0.00 0.00 r

U157/Z (XOR2_X	(1)	0.10	0.37 r	
U156/Z (XOR2_X	(1)	0.10	0.47 r	
U154/Z (XOR2_X	(1)	0.10	0.56 r	
U286/ZN (XNOR2	2 X1)	0.06	0.62 f	
U153/Z (XOR2_X	_ ,	0.09	0.70 f	
U1_4/CO (FA_X1	·	0.11	0.81 f	
U1_5/CO (FA_X1		0.09	0.90 f	
U1_6/CO (FA_X1	•	0.09	1.00 f	
U1_7/CO (FA_X1	•	0.09	1.00 f	
	•			
U1_8/C0 (FA_X1		0.09	1.18 f	
U1_9/CO (FA_X1	•	0.09	1.27 f	
U1_10/C0 (FA_X	•	0.09	1.36 f	
U1_11/CO (FA_X		0.09	1.46 f	
U1_12/CO (FA_X	•	0.09	1.55 f	
U1_13/CO (FA_X		0.09		
U1_14/CO (FA_X	(1)	0.09		
U1_15/S (FA_X1	.)	0.13	1.87 r	
out_reg[15]/D	(DFF X1)	0.01	1.88 r	
data arrival t			1.88	
			_,	
clock clk (ris	se edge)	4.00	4.00	
	delay (ideal)		4.00	
clock uncertai		-0.20	3.80	
	(DFF_X1)	0.00		
library setup		-0.03		
data required	time		3.77	
data required	time		3 77	
data required			3.77 -1.88	
data arrival t			-1.88	
data arrival t	ime		-1.88	
data arrival t slack (MET) Startpoint: b_ Endpoint: out_	r_reg[0] (rising edge-t reg[15] ing edge-triggered flip k	riggered fli -flop clocke	-1.88 1.89 p-flop clocked by clk)	
data arrival t slack (MET) Startpoint: b_ Endpoint: out_	ime r_reg[0] (rising edge-t _reg[15] ing edge-triggered flip _k	riggered fli -flop clocke	-1.88 1.89 p-flop clocked by clk)	
data arrival t slack (MET) Startpoint: b_ Endpoint: out_	r_reg[0] (rising edge-t reg[15] ing edge-triggered flip k	riggered fli -flop clocke Library	-1.88 1.89 p-flop clocked by clk)	
data arrival to slack (MET) Startpoint: b_Endpoint: out_(ris Path Group: cl Path Type: max Des/Clust/Port	r_reg[0] (rising edge-t reg[15] ing edge-triggered flip k : Wire Load Model	riggered fli -flop clocke Library	-1.88 1.89 p-flop clocked by clk) d by clk)	
data arrival tslack (MET) Startpoint: b_ Endpoint: out_	r_reg[0] (rising edge-t reg[15] sing edge-triggered flip k : Wire Load Model 5K_hvratio_1_1	riggered fli -flop clocke Library NangateO	-1.88 1.89 p-flop clocked by clk) d by clk)	
data arrival t	r_reg[0] (rising edge-t reg[15] sing edge-triggered flip k Wire Load Model 5K_hvratio_1_1	riggered fli -flop clocke Library NangateO Incr0.00	-1.88 1.89 p-flop clocked by clk) d by clk) penCellLibrary Path 0.00	
data arrival t	r_reg[0] (rising edge-t reg[15] sing edge-triggered flip k Wire Load Model 5K_hvratio_1_1	riggered fli -flop clocke Library NangateO Incr 0.00 0.00	-1.88 1.89 p-flop clocked by clk) d by clk) penCellLibrary Path 0.00 0.00	
data arrival t	r_reg[0] (rising edge-t reg[15] ing edge-triggered flip k : Wire Load Model 	riggered fli -flop clocke Library NangateO Incr 0.00 0.00 0.00	-1.88 1.89 p-flop clocked by clk) d by clk) penCellLibrary Path 0.00 0.00 0.00 r	
data arrival t	r_reg[0] (rising edge-t reg[15] ing edge-triggered flip k : Wire Load Model 	riggered fli -flop clocke Library NangateO Incr 0.00 0.00 0.00 0.11	-1.88 1.89 p-flop clocked by clk) d by clk) penCellLibrary Path 0.00 0.00 0.00 r 0.11 f	
data arrival tassistance (MET) Startpoint: b_Endpoint: out	r_reg[0] (rising edge-treg[15] ing edge-triggered flip.k Wire Load Model 5K_hvratio_1_1 se edge) delay (ideal) (DFF_X1) (DFF_X1) X1)	riggered fli -flop clocke Library NangateO Incr 0.00 0.00 0.00 0.11 0.07	-1.88 1.89 p-flop clocked by clk) d by clk) penCellLibrary Path 0.00 0.00 0.00 r 0.11 f 0.18 r	
data arrival t	r_reg[0] (rising edge-treg[15] ing edge-triggered flip k Wire Load Model SK_hvratio_1_1 ee edge) delay (ideal) (DFF_X1) (DFF_X1) X1) X1)	riggered fli -flop clocke Library NangateO Incr 0.00 0.00 0.00 0.11 0.07 0.09	-1.88 1.89 p-flop clocked by clk) d by clk) penCellLibrary Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r	
data arrival t	r_reg[0] (rising edge-treg[15]) ing edge-triggered flip k Wire Load Model 5K_hvratio_1_1 ee edge) delay (ideal) (DFF_X1) (DFF_X1) X1) X1)	riggered fli -flop clocke Library NangateO Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10	-1.88 1.89 p-flop clocked by clk) d by clk) penCellLibrary Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r	
data arrival t	r_reg[0] (rising edge-t reg[15] sing edge-triggered flip k Wire Load Model SK_hvratio_1_1 se edge) delay (ideal) (DFF_X1) (DFF_X1) X1) (1)	riggered fli -flop clocke Library NangateO Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10 0.10	-1.88	
data arrival table slack (MET) Startpoint: b_Endpoint: out	r_reg[0] (rising edge-t reg[15] sing edge-triggered flip k Wire Load Model SK_hvratio_1_1 se edge) delay (ideal) (DFF_X1) (DFF_X1) X1) (1) (1)	riggered fli -flop clocke Library NangateO Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10	-1.88 1.89 p-flop clocked by clk) d by clk) penCellLibrary Path 0.00 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r	
data arrival table slack (MET) Startpoint: b_Endpoint: out	r_reg[0] (rising edge-treg[15]) ing edge-triggered flip k Wire Load Model 5K_hvratio_1_1 se edge) delay (ideal) (DFF_X1) (DFF_X1) (X1) (X1) (X1) (X1) (X1) (X1) (X1) (Library NangateO Incr 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10 0.10 0.06	-1.88 1.89 p-flop clocked by clk) d by clk) penCellLibrary Path 0.00 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f	
data arrival table slack (MET) Startpoint: b_Endpoint: out	r_reg[0] (rising edge-treg[15]) ing edge-triggered flip k Wire Load Model 5K_hvratio_1_1 se edge) delay (ideal) (DFF_X1) (DFF_X1) (X1) (X1) (X1) (X1) (X1) (X1) (X1) (riggered fli -flop clocke Library NangateO Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10	-1.88 1.89 p-flop clocked by clk) d by clk) penCellLibrary Path 0.00 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r	

U1_5/CO (FA_X1)		0.09	0.90 f	
U1_6/CO (FA_X1)		0.09		
U1_7/CO (FA_X1)		0.09		
U1_8/CO (FA_X1)		0.09		
U1_9/CO (FA_X1)		0.09		
U1_10/CO (FA_X1)		0.09	1.36 f	
U1_11/CO (FA_X1)		0.09	1.46 f	
U1_12/CO (FA_X1)		0.09	1.55 f	
U1_13/C0 (FA_X1)		0.09	1.64 f	
U1 14/CO (FA X1)		0.09	1.74 f	
U1_15/S (FA_X1)		0.13	1.87 r	
out_reg[15]/D (DI	FF X1)	0.01	1.88 r	
data arrival time			1.88	
clock clk (rise	edge)	4.00	4.00	
clock network de		0.00		
clock uncertainty		-0.20		
		0.00		
<pre>out_reg[15]/CK (I library setup tir</pre>	me	-0.03		
		-0.03	3.77	
data required tir				
data required tir	me		3.77	
data arrival time			-1.88	
			1.89	
Endpoint: out_reg (rising Path Group: clk			ip-flop clocked by clk)	
Startpoint: b_r_ı Endpoint: out_reı (risinı Path Group: clk Path Type: max	g[15] g edge-triggered flip	-flop clock		
Startpoint: b_r_n Endpoint: out_reg	g[15] g edge-triggered flip Wire Load Model	Library	ed by clk)	
Startpoint: b_r_n Endpoint: out_reg	g[15] g edge-triggered flip	Library	ed by clk)	
Startpoint: b_r_n Endpoint: out_reg	g[15] g edge-triggered flip Wire Load Model	Library	ed by clk) OpenCellLibrary	
Startpoint: b_r_r Endpoint: out_reg	g[15] g edge-triggered flip Wire Load Model 5K_hvratio_1_1 edge)	Library Nangate Incr	OpenCellLibrary Path 0.00	
Startpoint: b_r_n Endpoint: out_reg	g[15] g edge-triggered flip Wire Load Model 5K_hvratio_1_1 edge) lay (ideal)	Library Nangate	Path 0.000 0.00	
Startpoint: b_r_r Endpoint: out_reg	g[15] g edge-triggered flip Wire Load Model 5K_hvratio_1_1 edge) lay (ideal)	Library Nangate Incr	OpenCellLibrary Path 0.00	
Startpoint: b_r_n Endpoint: out_reg	g[15] g edge-triggered flip Wire Load Model	Library Nangate Incr 0.00 0.00	Path 0.000 0.00	
Startpoint: b_r_n Endpoint: out_reg	g[15] g edge-triggered flip Wire Load Model	Library Nangate Incr 0.00 0.00	Path 0.000 0.000 0.000 0.000	
Startpoint: b_r_d Endpoint: out_reg	g[15] g edge-triggered flip Wire Load Model	Library Nangate Incr 0.00 0.00 0.00 0.11	Path 0.00 0.00 0.00 0.11 f	
Startpoint: b_r_r Endpoint: out_reg	g[15] g edge-triggered flip Wire Load Model	Library Nangate Incr 0.00 0.00 0.00 0.11 0.07	Path	
Startpoint: b_r_r Endpoint: out_reg	g[15] g edge-triggered flip Wire Load Model	Library Nangate Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10	Path	
Startpoint: b_r_r Endpoint: out_reg	g[15] g edge-triggered flip Wire Load Model	Library Nangate Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10 0.10	Path	
Startpoint: b_r_r Endpoint: out_reg	g[15] g edge-triggered flip Wire Load Model	Library Nangate Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r	
Startpoint: b_r_r Endpoint: out_reg	g[15] g edge-triggered flip Wire Load Model	Library Nangate Incr 0.00 0.00 0.01 0.07 0.09 0.10 0.10 0.10 0.10 0.06	Path 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f	
Startpoint: b_r_I Endpoint: out_reg	g[15] g edge-triggered flip Wire Load Model	Library Nangate Incr 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10 0.10 0.06 0.09	Path 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f 0.70 f	
Startpoint: b_r_I Endpoint: out_reg	g[15] g edge-triggered flip Wire Load Model	Library Nangate Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10 0.10 0.06 0.09 0.11	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f 0.70 f 0.81 f	
Startpoint: b_r_I Endpoint: out_reg	g[15] g edge-triggered flip Wire Load Model	Library Nangate Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10 0.10 0.10 0.10 0.06 0.09 0.11	Path 0.00 0.00 0.00 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f 0.70 f 0.81 f 0.90 f	
Startpoint: b_r_r Endpoint: out_res	g[15] g edge-triggered flip Wire Load Model	Library Nangate Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10 0.10 0.10 0.10 0.10	Path 0.00 0.00 0.00 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f 0.70 f 0.81 f 0.90 f 0.99 f	
Startpoint: b_r_r Endpoint: out_reg	g[15] g edge-triggered flip Wire Load Model	Library Nangate Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10 0.10 0.10 0.10 0.06 0.09 0.11 0.09 0.09	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f 0.70 f 0.81 f 0.90 f 0.99 f 1.09 f	
Startpoint: b_r_r Endpoint: out_res	g[15] g edge-triggered flip Wire Load Model	Library Nangate Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10 0.10 0.10 0.06 0.09 0.11 0.09 0.09 0.09 0.09	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f 0.70 f 0.81 f 0.90 f 0.99 f 1.09 f 1.18 f	
Startpoint: b_r_r Endpoint: out_reg	g[15] g edge-triggered flip Wire Load Model	Library Nangate Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10 0.10 0.10 0.10 0.06 0.09 0.11 0.09 0.09	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f 0.70 f 0.81 f 0.90 f 0.99 f 1.09 f	

UL11/CO (FA XI)					
UI_12/CO (FA_X1) UI_13/CO (FA_X1) UI_14/CO (FA_X1) UI_14/CO (FA_X1) UI_14/CO (FA_X1) UI_14/CO (FA_X1) UI_15/S	U1 11/CO (FA X1)		0.09	1.46 f	
UL_13/CO (FA_XI) UL_14/CO (FA_XI) UL_14/CO (FA_XI) UL_15/S (FA_XI) UL_18/S (FA				1.55 f	
UL_14/CO (FA_X1) UL_15/S (FA_X			0.09	1.64 f	
UL_15/S (FA_XI)' 0.13 1.87 r out reg[5]70 (DFF_XI) 0.01 1.88 r data arrival time 1.88 clock clk (rise edge) 4.00 4.00 clock network delay (ideal) 0.00 4.00 clock uncertainty -0.20 3.80 r out_reg[15]/CK (DFF_XI) 0.00 3.80 r library setup time -0.03 3.77 d data required time 3.77 d data required time 3.77 d data arrival time -1.88 slack (MET) 1.89 Startpoint: b_r_reg[0] (rising edge-triggered flip-flop clocked by clk) Path Group: clk Path Group: clk Path Type: max Des/Clust/Port Wire Load Model Library mult SK_hvratio_1 NangateOpenCellLibrary Point Incr Path Clock clk (rise edge) 0.00 0.00 clock network delay (ideal) 0.00 0.00 b_r_reg[0]/CK (DFF_XI) 0.11 0.11 f.11 f.11 0.11					
out_reg[15]/0 (DFF_X1) 0.01 1.88 r data arrival time 1.88 clock clk (rise edge) 4.00 4.00 clock network delay (ideal) 0.00 4.00 clock uncertainty -0.20 3.80 out_reg[15]/CK (DFF_X1) 0.00 3.80 r library setup time -0.03 3.77 data required time 3.77 data required time 3.77 data arrival time -1.88 slack (MET) 1.89 Startpoint: b_r_reg[0] (rising edge-triggered flip-flop clocked by clk) Fendpoint: out_reg[15] (rising edge-triggered flip-flop clocked by clk) Path Group: clk Path Group: clk Path Type: max Des/Clust/Port Wire Load Model Library mult 5K_hvratio_1 NangateOpenCellLibrary Point Incr Path clock clk (rise edge) 0.00 0.00 clock network delay (ideal) 0.00 0.00 b_r_reg[0]/0N (DFF_X1) 0.11 0.11 fl 01259/Z (XOR2 X1) 0.09 <			0.13	1.87 r	
1.88		F X1)			
Clock clk (rise edge)			0.01		
Clock network delay (ideal)	data arrivai time			1.00	
Clock network delay (ideal)	clock clk (rise a	dge)	1 00	1 00	
Clock uncertainty					
out reg[15]/CK (DFF_X1) 0.00 3.80 r library setup time -0.03 3.77 data required time 3.77 data arrival time -1.88					
1bhrary setup time	•				
data required time		_ /			
			-0.03		
Startpoint: b_r_reg[0] (rising edge-triggered flip-flop clocked by clk)					
Startpoint: b_r_reg[0] (rising edge-triggered flip-flop clocked by clk)	•				
Startpoint: b_r_reg[0] (rising edge-triggered flip-flop clocked by clk) Endpoint: out_reg[15]					
Startpoint: b_r_reg[0] (rising edge-triggered flip-flop clocked by clk) Endpoint: out_reg[15]					
Indpoint: out_reg[15]	STACK (MET)			1.09	
Point Incr Path clock clk (rise edge) 0.00 0.00 clock network delay (ideal) 0.00 0.00 b_r_reg[0]/CK (DFF_X1) 0.00 0.00 r b_r_reg[0]/CK (DFF_X1) 0.11 0.11 f U328/ZN (NOR2_X1) 0.07 0.18 r U259/Z (XOR2_X1) 0.09 0.27 r U157/Z (XOR2_X1) 0.10 0.37 r U156/Z (XOR2_X1) 0.10 0.37 r U156/Z (XOR2_X1) 0.10 0.56 r U286/ZN (XNOR2_X1) 0.10 0.56 r U286/ZN (XNOR2_X1) 0.10 0.56 r U165/Z (XOR2_X1) 0.10 0.56 r U165/Z (XOR2_X1) 0.00 0.70 f U1 4/CO (FA_X1) 0.09 0.70 f U1 -4/CO (FA_X1) 0.11 0.81 f U1_5/CO (FA_X1) 0.09 0.90 f U1_6/CO (FA_X1) 0.09 0.90 f U1_6/CO (FA_X1) 0.09 1.00 f U1_7/CO (FA_X1) 0.09 1.09 f U1_8/CO (FA_X1) 0.09 1.28 f U1_9/CO (FA_X1) 0.09 1.28 f U1_9/CO (FA_X1) 0.09 1.28 f U1_10/CO (FA_X1) 0.09 1.55 f U1_11/CO (FA_X1) 0.09 1.55 f U1_11/CO (FA_X1) 0.09 1.64 f U1_12/CO (FA_X1) 0.09 1.74 f U1_15/S (FA_X1) 0.09 1.74 f					
clock clk (rise edge)	Path Type: max	Wire Load Model	Library		
clock clk (rise edge) 0.00 0.00 clock network delay (ideal) 0.00 0.00 b_r_reg[0]/CK (DFF_X1) 0.00 0.00 r b_r_reg[0]/QN (DFF_X1) 0.11 0.11 f U328/ZN (NOR2_X1) 0.07 0.18 r U259/Z (XOR2_X1) 0.09 0.27 r U157/Z (XOR2_X1) 0.10 0.37 r U156/Z (XOR2_X1) 0.10 0.47 r U154/Z (XOR2_X1) 0.10 0.56 r U286/ZN (XNOR2_X1) 0.06 0.62 f U153/Z (XOR2_X1) 0.09 0.70 f U1_4/CO (FA_X1) 0.11 0.81 f U1_5/CO (FA_X1) 0.09 0.90 f U1_6/CO (FA_X1) 0.09 1.09 f U1_7/CO (FA_X1) 0.09 1.28 f U1_9/CO (FA_X1) 0.09 1.37 f U1_10/CO (FA_X1) 0.09 1.37 f U1_11/CO (FA_X1) 0.09 1.55 f U1_11/CO (FA_X1) 0.09 1.55 f U1_13/CO (FA_X1) 0.09 1.74 f U1_15/S (FA_X1) 0.13 1.87 r	Path Type: max Des/Clust/Port)penCellLibrary	
clock network delay (ideal) 0.00 0.00 b_r_reg[0]/CK (DFF_X1) 0.00 0.00 r b_r_reg[0]/QN (DFF_X1) 0.11 0.11 f U328/ZN (NOR2_X1) 0.07 0.18 r U259/Z (XOR2_X1) 0.09 0.27 r U157/Z (XOR2_X1) 0.10 0.37 r U156/Z (XOR2_X1) 0.10 0.47 r U156/Z (XOR2_X1) 0.10 0.56 r U286/ZN (XNOR2_X1) 0.06 0.62 f U153/Z (XOR2_X1) 0.09 0.70 f U1_4/CO (FA_X1) 0.09 0.70 f U1_4/CO (FA_X1) 0.09 0.90 f U1_5/CO (FA_X1) 0.09 1.00 f U1_7/CO (FA_X1) 0.09 1.09 f U1_8/CO (FA_X1) 0.09 1.28 f U1_10/CO (FA_X1) 0.09 1.28 f U1_11/CO (FA_X1) 0.09 1.55 f U1_11/CO (FA_X1) 0.09 1.55 f U1_13/CO (FA_X1) 0.09 1.74 f U1_15/S (FA_X1) 0.09 1.74 f U1_15/S (FA_X1) 0.13 1.87 r	Path Type: max Des/Clust/Port mult Point	5K_hvratio_1_1	NangateO	Path	
b_r_reg[0]/CK (DFF_X1)	Path Type: max Des/Clust/Port mult Point	5K_hvratio_1_1	Nangate(Path	
b_r_reg[0]/QN (DFF_X1) U328/ZN (NOR2_X1) U259/Z (XOR2_X1) U157/Z (XOR2_X1) U156/Z (XOR2_X1) U157/C (FA_X1) U157/C	Path Type: max Des/Clust/Port mult Point clock clk (rise e	5K_hvratio_1_1 dge)	NangateO	Path 0.00	
U328/ZN (NOR2_X1) U259/Z (XOR2_X1) U157/Z (XOR2_X1) U156/Z (XOR2_X1) U156/Z (XOR2_X1) U156/Z (XOR2_X1) U156/Z (XOR2_X1) U154/Z (XOR2_X1) U154/Z (XOR2_X1) U154/Z (XOR2_X1) U155/Z (XOR2_X1) U155/Z (XOR2_X1) U166	Path Type: max Des/Clust/Port mult Point clock clk (rise e	5K_hvratio_1_1 cup dge) ay (ideal)	NangateO Incr 0.00 0.00	Path 0.00 0.00	
U259/Z (XOR2_X1) 0.09 0.27 r U157/Z (XOR2_X1) 0.10 0.37 r U156/Z (XOR2_X1) 0.10 0.47 r U154/Z (XOR2_X1) 0.10 0.56 r U286/ZN (XNOR2_X1) 0.06 0.62 f U153/Z (XOR2_X1) 0.09 0.70 f U1_4/CO (FA_X1) 0.11 0.81 f U1_5/CO (FA_X1) 0.09 0.90 f U1_7/CO (FA_X1) 0.09 1.00 f U1_8/CO (FA_X1) 0.09 1.18 f U1_9/CO (FA_X1) 0.09 1.28 f U1_10/CO (FA_X1) 0.09 1.37 f U1_11/CO (FA_X1) 0.09 1.55 f U1_12/CO (FA_X1) 0.09 1.55 f U1_13/CO (FA_X1) 0.09 1.74 f U1_15/S (FA_X1) 0.09 1.74 f U1_15/S (FA_X1) 0.13 1.87 r	Path Type: max Des/Clust/Port mult Point clock clk (rise e clock network del b_r_reg[0]/CK (DF	5K_hvratio_1_1 dge) ay (ideal) F_X1)	Nangate(Incr 0.00 0.00 0.00	Path 0.00 0.00 0.00 r	
U157/Z (XOR2_X1) U156/Z (XOR2_X1) U154/Z (XOR2_X1) U154/Z (XOR2_X1) U158/Z (XOR2_X1) U10.10 U10.10 U10.56 r U10.286/ZN (XNOR2_X1) U10.286/ZN (XNOR2_X1) U10.29 U10.20 U10.	Path Type: max Des/Clust/Port mult Point clock clk (rise e clock network del b_r_reg[0]/CK (DF b_r_reg[0]/QN (DF	5K_hvratio_1_1 dge) ay (ideal) F_X1) F_X1)	NangateO Incr 0.00 0.00 0.00 0.00 0.11	Path 0.00 0.00 0.00 r 0.11 f	
U156/Z (XOR2_X1) U154/Z (XOR2_X1) U154/Z (XOR2_X1) U286/ZN (XNOR2_X1) U153/Z (XOR2_X1) U153/Z (XOR2_X1) U10.4/CO (FA_X1) U11.5/CO (Path Type: max Des/Clust/Port mult Point clock clk (rise e clock network del b_r_reg[0]/CK (DF b_r_reg[0]/QN (DF U328/ZN (NOR2_X1)	5K_hvratio_1_1 dge) ay (ideal) F_X1) F_X1)	NangateO Incr 0.00 0.00 0.00 0.11 0.07	Path 0.00 0.00 0.00 r 0.11 f 0.18 r	
U154/Z (XOR2_X1) 0.10 0.56 r U286/ZN (XNOR2_X1) 0.06 0.62 f U153/Z (XOR2_X1) 0.09 0.70 f U1_4/CO (FA_X1) 0.11 0.81 f U1_5/CO (FA_X1) 0.09 0.90 f U1_6/CO (FA_X1) 0.09 1.00 f U1_7/CO (FA_X1) 0.09 1.09 f U1_8/CO (FA_X1) 0.09 1.18 f U1_9/CO (FA_X1) 0.09 1.28 f U1_10/CO (FA_X1) 0.09 1.37 f U1_11/CO (FA_X1) 0.09 1.55 f U1_13/CO (FA_X1) 0.09 1.64 f U1_13/CO (FA_X1) 0.09 1.74 f U1_15/S (FA_X1) 0.13 1.87 r	Path Type: max Des/Clust/Port mult Point clock clk (rise e clock network del b_r_reg[0]/CK (DF b_r_reg[0]/QN (DF U328/ZN (NOR2_X1)	5K_hvratio_1_1 dge) ay (ideal) F_X1) F_X1)	NangateO Incr 0.00 0.00 0.00 0.11 0.07 0.09	Path 0.00 0.00 0.00 r 0.11 f 0.18 r	
U154/Z (XOR2_X1) U286/ZN (XNOR2_X1) U153/Z (XOR2_X1) U10.4/CO (FA_X1) U11.4/CO (FA_X1) U11.5/CO (FA_X1) U11.6/CO (FA_X1) U11.6/CO (FA_X1) U11.8/CO (FA_X1) U11.9/CO (FA_X1) U11.9/CO (FA_X1) U11.10/CO (FA_X1) U11.10/CO (FA_X1) U11.11/CO (FA_X1)	Path Type: max Des/Clust/Port mult Point clock clk (rise e clock network del b_r_reg[0]/CK (DF b_r_reg[0]/QN (DF U328/ZN (NOR2_X1) U259/Z (XOR2_X1)	5K_hvratio_1_1 dge) ay (ideal) F_X1) F_X1)	NangateO Incr 0.00 0.00 0.00 0.11 0.07 0.09	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r	
U286/ZN (XNOR2_X1) 0.06 0.62 f U153/Z (XOR2_X1) 0.09 0.70 f U1_4/CO (FA_X1) 0.11 0.81 f U1_5/CO (FA_X1) 0.09 0.90 f U1_6/CO (FA_X1) 0.09 1.00 f U1_7/CO (FA_X1) 0.09 1.18 f U1_9/CO (FA_X1) 0.09 1.28 f U1_10/CO (FA_X1) 0.09 1.37 f U1_11/CO (FA_X1) 0.09 1.46 f U1_12/CO (FA_X1) 0.09 1.55 f U1_13/CO (FA_X1) 0.09 1.64 f U1_14/CO (FA_X1) 0.09 1.74 f U1_15/S (FA_X1) 0.13 1.87 r	Path Type: max Des/Clust/Port mult Point clock clk (rise e clock network del b_r_reg[0]/CK (DF b_r_reg[0]/QN (DF U328/ZN (NOR2_X1) U259/Z (XOR2_X1) U157/Z (XOR2_X1)	5K_hvratio_1_1 dge) ay (ideal) F_X1) F_X1)	NangateO Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r	
U153/Z (XOR2_X1) 0.09 0.70 f U1_4/C0 (FA_X1) 0.11 0.81 f U1_5/C0 (FA_X1) 0.09 0.90 f U1_6/C0 (FA_X1) 0.09 1.00 f U1_7/C0 (FA_X1) 0.09 1.8 f U1_8/C0 (FA_X1) 0.09 1.28 f U1_10/C0 (FA_X1) 0.09 1.37 f U1_11/C0 (FA_X1) 0.09 1.46 f U1_12/C0 (FA_X1) 0.09 1.55 f U1_13/C0 (FA_X1) 0.09 1.64 f U1_14/C0 (FA_X1) 0.09 1.74 f U1_15/S (FA_X1) 0.13 1.87 r	Path Type: max Des/Clust/Port mult Point clock clk (rise e clock network del b_r_reg[0]/CK (DF b_r_reg[0]/QN (DF U328/ZN (NOR2_X1) U259/Z (XOR2_X1) U156/Z (XOR2_X1)	5K_hvratio_1_1 dge) ay (ideal) F_X1) F_X1)	NangateO Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10 0.10	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r	
U1_4/CO (FA_X1) U1_5/CO (FA_X1) U1_5/CO (FA_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_	Path Type: max Des/Clust/Port mult Point clock clk (rise e clock network del b_r_reg[0]/CK (DF b_r_reg[0]/QN (DF U328/ZN (NOR2_X1) U259/Z (XOR2_X1) U157/Z (XOR2_X1) U156/Z (XOR2_X1) U154/Z (XOR2_X1)	5K_hvratio_1_1 dge) ay (ideal) F_X1) F_X1)	NangateO Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r	
U1_5/CO (FA_X1) U1_6/CO (FA_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_11/CO (FA_X1) U1_12/CO (FA_X1) U1_13/CO (FA_X1) U1_13/CO (FA_X1) U1_14/CO (FA_X1) U1_15/S (FA_X1)	Path Type: max Des/Clust/Port mult Point clock clk (rise e clock network del b_r_reg[0]/CK (DF b_r_reg[0]/QN (DF U328/ZN (NOR2_X1) U157/Z (XOR2_X1) U156/Z (XOR2_X1) U154/Z (XOR2_X1) U286/ZN (XNOR2_X1)	5K_hvratio_1_1 dge) ay (ideal) F_X1) F_X1)	NangateO Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10 0.06	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f	
U1_6/CO (FA_X1) U1_7/CO (FA_X1) 0.09 1.00 f U1_7/CO (FA_X1) 0.09 1.18 f U1_9/CO (FA_X1) 0.09 1.28 f U1_10/CO (FA_X1) 0.09 1.37 f U1_11/CO (FA_X1) 0.09 1.46 f U1_12/CO (FA_X1) 0.09 1.55 f U1_13/CO (FA_X1) 0.09 1.64 f U1_14/CO (FA_X1) 0.09 1.74 f U1_15/S (FA_X1) 0.13 1.87 r	Path Type: max Des/Clust/Port mult Point clock clk (rise e clock network del b_r_reg[0]/CK (DF b_r_reg[0]/QN (DF U328/ZN (NOR2_X1) U157/Z (XOR2_X1) U157/Z (XOR2_X1) U154/Z (XOR2_X1) U286/ZN (XNOR2_X1 U153/Z (XOR2_X1) U153/Z (XOR2_X1)	5K_hvratio_1_1 dge) ay (ideal) F_X1) F_X1)	NangateO Incr 0.00 0.00 0.01 0.07 0.09 0.10 0.10 0.10 0.06 0.09	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f 0.70 f	
U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_11/CO (FA_X1) U1_12/CO (FA_X1) U1_12/CO (FA_X1) U1_13/CO (FA_X1) U1_14/CO (FA_X1) U1_15/S (FA_X1)	Path Type: max Des/Clust/Port	5K_hvratio_1_1 dge) ay (ideal) F_X1) F_X1)	NangateO Incr 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10 0.06 0.09 0.11	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f 0.70 f 0.81 f	
U1_8/CO (FA_X1) 0.09 1.18 f U1_9/CO (FA_X1) 0.09 1.28 f U1_10/CO (FA_X1) 0.09 1.37 f U1_11/CO (FA_X1) 0.09 1.46 f U1_12/CO (FA_X1) 0.09 1.55 f U1_13/CO (FA_X1) 0.09 1.64 f U1_14/CO (FA_X1) 0.09 1.74 f U1_15/S (FA_X1) 0.13 1.87 r	Path Type: max Des/Clust/Port	5K_hvratio_1_1 dge) ay (ideal) F_X1) F_X1)	NangateO Incr 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10 0.10 0.06 0.09 0.11 0.09	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f 0.70 f 0.81 f 0.90 f	
U1_9/CO (FA_X1) 0.09 1.28 f U1_10/CO (FA_X1) 0.09 1.37 f U1_11/CO (FA_X1) 0.09 1.46 f U1_12/CO (FA_X1) 0.09 1.55 f U1_13/CO (FA_X1) 0.09 1.64 f U1_14/CO (FA_X1) 0.09 1.74 f U1_15/S (FA_X1) 0.13 1.87 r	Path Type: max Des/Clust/Port	5K_hvratio_1_1 dge) ay (ideal) F_X1) F_X1)	NangateO Incr 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10 0.10 0.10 0.06 0.09 0.11 0.09 0.09	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f 0.70 f 0.81 f 0.90 f 1.00 f	
U1_10/C0 (FA_X1) 0.09 1.37 f U1_11/C0 (FA_X1) 0.09 1.46 f U1_12/C0 (FA_X1) 0.09 1.55 f U1_13/C0 (FA_X1) 0.09 1.64 f U1_14/C0 (FA_X1) 0.09 1.74 f U1_15/S (FA_X1) 0.13 1.87 r	Path Type: max Des/Clust/Port	5K_hvratio_1_1 dge) ay (ideal) F_X1) F_X1)	NangateO Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10 0.10 0.06 0.09 0.11 0.09 0.09 0.09	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.09 f	
U1_11/CO (FA_X1)	Path Type: max Des/Clust/Port	5K_hvratio_1_1 dge) ay (ideal) F_X1) F_X1)	NangateO Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10 0.10 0.06 0.09 0.11 0.09 0.09 0.09 0.09	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.09 f 1.18 f	
U1_12/CO (FA_X1) 0.09 1.55 f U1_13/CO (FA_X1) 0.09 1.64 f U1_14/CO (FA_X1) 0.09 1.74 f U1_15/S (FA_X1) 0.13 1.87 r	Path Type: max Des/Clust/Port	5K_hvratio_1_1 dge) ay (ideal) F_X1) F_X1)	NangateO Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10 0.10 0.06 0.09 0.11 0.09 0.09 0.09 0.09 0.09 0.09	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.09 f 1.18 f 1.28 f	
U1_13/C0 (FA_X1) 0.09 1.64 f U1_14/C0 (FA_X1) 0.09 1.74 f U1_15/S (FA_X1) 0.13 1.87 r	Path Type: max Des/Clust/Port	5K_hvratio_1_1 dge) ay (ideal) F_X1) F_X1)	NangateO Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10 0.10 0.06 0.09 0.11 0.09 0.09 0.09 0.09 0.09 0.09	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.09 f 1.18 f 1.28 f 1.37 f	
U1_14/C0 (FA_X1) 0.09 1.74 f U1_15/S (FA_X1) 0.13 1.87 r	Path Type: max Des/Clust/Port mult Point clock clk (rise e clock network del b_r_reg[0]/CK (DF b_r_reg[0]/QN (DF U328/ZN (NOR2_X1) U157/Z (XOR2_X1) U156/Z (XOR2_X1) U156/Z (XOR2_X1) U156/Z (XOR2_X1) U158/ZN (XNOR2_X1) U1286/ZN (XNOR2_X1) U1_5/CO (FA_X1) U1_5/CO (FA_X1) U1_5/CO (FA_X1) U1_7/CO (FA_X1) U1_7/CO (FA_X1) U1_9/CO (FA_X1) U1_19/CO (FA_X1) U1_11/CO (FA_X1) U1_11/CO (FA_X1)	5K_hvratio_1_1 dge) ay (ideal) F_X1) F_X1)	NangateO Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10 0.10 0.06 0.09 0.11 0.09 0.09 0.09 0.09 0.09 0.09	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.09 f 1.18 f 1.28 f 1.37 f 1.46 f	
U1_14/CO (FA_X1) 0.09 1.74 f U1_15/S (FA_X1) 0.13 1.87 r	Path Type: max Des/Clust/Port	5K_hvratio_1_1 dge) ay (ideal) F_X1) F_X1)	NangateO Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10 0.10 0.06 0.09 0.11 0.09 0.09 0.09 0.09 0.09 0.09	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.09 f 1.18 f 1.28 f 1.37 f 1.46 f	
U1_15/S (FA_X1) 0.13 1.87 r	Path Type: max Des/Clust/Port	5K_hvratio_1_1 dge) ay (ideal) F_X1) F_X1)	NangateO Incr 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10 0.10 0.06 0.09 0.11 0.09 0.09 0.09 0.09 0.09 0.09	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.09 f 1.18 f 1.28 f 1.37 f 1.46 f 1.55 f	
	Path Type: max Des/Clust/Port	5K_hvratio_1_1 dge) ay (ideal) F_X1) F_X1)	NangateO Incr 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10 0.10 0.06 0.09 0.11 0.09 0.09 0.09 0.09 0.09 0.09	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.09 f 1.18 f 1.28 f 1.37 f 1.46 f 1.55 f 1.64 f	
	Path Type: max Des/Clust/Port	5K_hvratio_1_1 dge) ay (ideal) F_X1) F_X1)	NangateO Incr 0.00 0.00 0.00 0.11 0.07 0.09 0.10 0.10 0.10 0.10 0.06 0.09 0.11 0.09 0.09 0.09 0.09 0.09 0.09	Path 0.00 0.00 0.00 r 0.11 f 0.18 r 0.27 r 0.37 r 0.47 r 0.56 r 0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.09 f 1.18 f 1.28 f 1.37 f 1.46 f 1.55 f 1.64 f 1.74 f	

data arrival time	e		1.88
alack alk /====	odgo)	4 00	4 00
clock clk (rise		4.00	4.00
clock network de		0.00	4.00
clock uncertainty		-0.20	3.80
out_reg[15]/CK (0.00	3.80 r
library setup tim		-0.03	3.77
data required ti	me 		3.77
data required tim			3.77
data arrival time	e		-1.88
slack (MET)			1.89
Endpoint: out_re			ip-flop clocked by clk) ed by clk)
Des/Clust/Port	Wire Load Model	Library	
mult	5K_hvratio_1_1	Nangate(OpenCellLibrary
Point		Incr	
clock clk (rise		0.00	
clock network de		0.00	0.00
b_r_reg[0]/CK (D		0.00	0.00 r
b_r_reg[0]/QN (DI		0.11	0.11 f
		0.07	0.11
U328/ZN (NOR2_X1))	0.07	0.18 r
U259/Z (XOR2_X1)		0.09	0.27 r
U157/Z (XOR2_X1)		0.10	0.37 r
U156/Z (XOR2_X1)		0.10	0.47 r
U154/Z (XOR2_X1)		a 1a	0.56
		0.10	0.56 r
U286/ZN (XNOR2_X:	1)	0.06	
` -	1)		0.62 f
U153/Z (XOR2_X1)	1)	0.06 0.09	0.62 f 0.70 f
U153/Z (XOR2_X1) U1_4/CO (FA_X1)	1)	0.06 0.09 0.11	0.62 f 0.70 f 0.81 f
U153/Z (XOR2_X1) U1_4/CO (FA_X1) U1_5/CO (FA_X1)	1)	0.06 0.09 0.11 0.09	0.62 f 0.70 f 0.81 f 0.90 f
U153/Z (XOR2_X1) U1_4/CO (FA_X1) U1_5/CO (FA_X1) U1_6/CO (FA_X1)	1)	0.06 0.09 0.11 0.09 0.09	0.62 f 0.70 f 0.81 f 0.90 f 1.00 f
U153/Z (XOR2_X1) U1_4/CO (FA_X1) U1_5/CO (FA_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1)	1)	0.06 0.09 0.11 0.09 0.09 0.09	0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.09 f
U153/Z (XOR2_X1) U1_4/CO (FA_X1) U1_5/CO (FA_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1)	1)	0.06 0.09 0.11 0.09 0.09 0.09	0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.09 f 1.18 f
U153/Z (XOR2_X1) U1_4/CO (FA_X1) U1_5/CO (FA_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1)	1)	0.06 0.09 0.11 0.09 0.09 0.09 0.09	0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.09 f 1.18 f 1.28 f
U153/Z (XOR2_X1) U1_4/CO (FA_X1) U1_5/CO (FA_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_19/CO (FA_X1)	1)	0.06 0.09 0.11 0.09 0.09 0.09 0.09 0.09	0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.18 f 1.28 f 1.37 f
U153/Z (XOR2_X1) U1_4/CO (FA_X1) U1_5/CO (FA_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1)	1)	0.06 0.09 0.11 0.09 0.09 0.09 0.09 0.09	0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.18 f 1.28 f 1.37 f 1.46 f
U153/Z (XOR2_X1) U1_4/CO (FA_X1) U1_5/CO (FA_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_12/CO (FA_X1)	1)	0.06 0.09 0.11 0.09 0.09 0.09 0.09 0.09 0.09	0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.18 f 1.28 f 1.37 f 1.46 f 1.55 f
U153/Z (XOR2_X1) U1_4/CO (FA_X1) U1_5/CO (FA_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_12/CO (FA_X1)	1)	0.06 0.09 0.11 0.09 0.09 0.09 0.09 0.09	0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.18 f 1.28 f 1.37 f 1.46 f
U153/Z (XOR2_X1) U1_4/CO (FA_X1) U1_5/CO (FA_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_12/CO (FA_X1) U1_13/CO (FA_X1)	1)	0.06 0.09 0.11 0.09 0.09 0.09 0.09 0.09 0.09	0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.18 f 1.28 f 1.37 f 1.46 f 1.55 f
U153/Z (XOR2_X1) U1_4/CO (FA_X1) U1_5/CO (FA_X1) U1_5/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_12/CO (FA_X1) U1_13/CO (FA_X1) U1_13/CO (FA_X1) U1_14/CO (FA_X1)	1)	0.06 0.09 0.11 0.09 0.09 0.09 0.09 0.09 0.09	0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.09 f 1.18 f 1.28 f 1.37 f 1.46 f 1.55 f 1.65 f
U153/Z (XOR2_X1) U1_4/CO (FA_X1) U1_5/CO (FA_X1) U1_5/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_12/CO (FA_X1) U1_13/CO (FA_X1) U1_13/CO (FA_X1) U1_14/CO (FA_X1) U1_15/S (FA_X1)		0.06 0.09 0.11 0.09 0.09 0.09 0.09 0.09 0.09	0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.09 f 1.18 f 1.28 f 1.37 f 1.46 f 1.55 f 1.65 f 1.74 f 1.87 r
U286/ZN (XNOR2_X: U153/Z (XOR2_X1) U1_4/CO (FA_X1) U1_5/CO (FA_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_12/CO (FA_X1) U1_13/CO (FA_X1) U1_13/CO (FA_X1) U1_15/S (FA_X1) U1_15/S (FA_X1) out_reg[15]/D (Didata arrival time	FF_X1)	0.06 0.09 0.11 0.09 0.09 0.09 0.09 0.09 0.09	0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.18 f 1.28 f 1.37 f 1.46 f 1.55 f 1.65 f 1.74 f
U153/Z (XOR2_X1) U1_4/CO (FA_X1) U1_5/CO (FA_X1) U1_5/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_11/CO (FA_X1) U1_12/CO (FA_X1) U1_13/CO (FA_X1) U1_13/CO (FA_X1) U1_15/S (FA_X1) U1_15/S (FA_X1) Out_reg[15]/D (DIdata arrival time	FF_X1) e	0.06 0.09 0.11 0.09 0.09 0.09 0.09 0.09 0.09	0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.09 f 1.18 f 1.28 f 1.37 f 1.46 f 1.55 f 1.65 f 1.74 f 1.87 r 1.88 r 1.88
U153/Z (XOR2_X1) U1_4/CO (FA_X1) U1_5/CO (FA_X1) U1_5/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_12/CO (FA_X1) U1_12/CO (FA_X1) U1_13/CO (FA_X1) U1_13/CO (FA_X1) U1_15/S (FA_X1) U1_15/S (FA_X1) out_reg[15]/D (Didata arrival time	FF_X1) e edge)	0.06 0.09 0.11 0.09 0.09 0.09 0.09 0.09 0.09	0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.09 f 1.18 f 1.28 f 1.37 f 1.46 f 1.55 f 1.65 f 1.74 f 1.87 r 1.88 r 1.88
U153/Z (XOR2_X1) U1_4/CO (FA_X1) U1_5/CO (FA_X1) U1_5/CO (FA_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_12/CO (FA_X1) U1_13/CO (FA_X1) U1_13/CO (FA_X1) U1_15/S (FA_X1) Out_reg[15]/D (Didata arrival time clock clk (rise clock network decored)	FF_X1) e edge) lay (ideal)	0.06 0.09 0.11 0.09 0.09 0.09 0.09 0.09 0.09	0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.09 f 1.18 f 1.28 f 1.37 f 1.46 f 1.55 f 1.65 f 1.74 f 1.87 r 1.88 r 1.88
U153/Z (XOR2_X1) U1_4/CO (FA_X1) U1_5/CO (FA_X1) U1_5/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_12/CO (FA_X1) U1_12/CO (FA_X1) U1_13/CO (FA_X1) U1_13/CO (FA_X1) U1_15/S (FA_X1) U1_15/S (FA_X1) out_reg[15]/D (Didata arrival time	FF_X1) e edge) lay (ideal)	0.06 0.09 0.11 0.09 0.09 0.09 0.09 0.09 0.09	0.62 f 0.70 f 0.81 f 0.90 f 1.00 f 1.09 f 1.18 f 1.28 f 1.37 f 1.46 f 1.55 f 1.65 f 1.74 f 1.87 r 1.88 r 1.88

```
      library setup time
      -0.03
      3.77

      data required time
      3.77

      data arrival time
      -1.88

      slack (MET)
      1.89
```

Part 3

Dot diagram

Code for Booth-2 encoding 8-bit x 8-bit multiplier

```
//HW2 P2
//
`timescale 1ns/10ps
//add necessary simple adders
module ha (
    input a,
    input b,
    output c,
    output s
    );
    assign s = a ^ b;
    assign c = a \& b;
endmodule //ha
module fa (
    input a,
    input b,
    input c,
    output carry,
    output sum
    );
```

```
assign carry = (a \& b) | ((a ^ b) \& c);
   assign sum = a ^ b ^ c;
endmodule //fa
module add42(
   input a,
   input b,
   input c,
   input d,
   input ci,
   output co, //carry out
   output cc, //carry to next add42
   output s
   );
   wire s internal;
   fa abc (.a (a), .b (b), .c (c), .carry(cc), .sum (s_internal));
   fa scc (.a (s_internal), .b (d), .c (ci), .carry(co), .sum (s));
endmodule //add42
module booth2 (
   input [2:0] section,
   input [7:0] number,
   output reg [8:0] code,
   output reg invert
   );
   always @(section or number) begin
       case (section)
          3'b000: {code, invert} = 10'b0;
          3'b001: {code, invert} = {number[7], number, 1'b0};
          3'b010: {code, invert} = {number[7], number, 1'b0};
          3'b011: {code, invert} = {number, 2'b0};
          3'b100: {code, invert} = {~number, 2'b11};
          3'b101: {code, invert} = {~number[7], ~number, 1'b1};
          3'b110: {code, invert} = {~number[7], ~number, 1'b1};
          3'b111: {code, invert} = 10'b0;
       endcase
   end
endmodule
//main module
module mult (
   input [7:0] a,
   input [7:0] b,
   input clk,
   output reg [15:0] out
);
// input clk sync
   reg [7:0] a_r, b_r;
   always @(posedge clk) begin
       a_r <= #1 a;
```

```
b r <= #1 b;
    end
// stage 1. encoding
    //stage's output
    wire [8:0] p0,p1,p2,p3; //partial products
    wire [3:0] p4;
                            //invert bits for PPs
    booth2 B0 (.section (\{b_r[1:0], 1'b0\}), .number (a_r), .code (p0), .invert (p4[0]));
    booth2 B1 (.section (b r[3:1]),
                                             .number (a_r), .code (p1), .invert (p4[1]));
    booth2 B2 (.section (b_r[5:3]),
                                            .number (a_r), .code (p2), .invert (p4[2]));
    booth2 B3 (.section (b_r[7:5]),
                                             .number (a_r), .code (p3), .invert (p4[3]));
// stage 2. CSA
    //stage's output
    wire [15:0] st2 p0;
    wire [15:3] st2 p1;
    wire [2:0] st2_p2; //columns 1, 5, 6
    wire [8:0] st2 c; //carry between 4:2 adders
    //pass through
    assign st2 p2[0] = p0[1]; //column 1
    assign st2 p2[2] = p4[3]; //column 6
    //top row
          st2_t_col0 (.a (p0[0]), .b (p4[0]),
.c (st2_p0[1]), .s (st2_p0[0]));
          st2_t_col2 (.a (p0[2]), .b (p1[0]), .c (p4[1]),
.carry (st2_p0[3]), .sum (st2_p0[2]));
          st2_t_col3 (.a (p0[3]), .b (p1[1]),
.c (st2 p0[4]), .s (st2 p1[3]));
    add42 st2_t_col4 (.a (p0[4]), .b (p1[2]), .c (p2[0]), .d (p4[2]), .ci (1'b0),
.cc (st2_p0[5]), .co (st2_p1[5]), .s (st2_p1[4]));
          st2_t_col5 (.a (p0[5]), .b (p1[3]), .c (p2[1]),
.carry (st2_p0[6]), .sum (st2_p2[1]));
    add42 st2_t_col6 (.a (p0[6]), .b (p1[4]), .c (p2[2]), .d (p3[0]), .ci (1'b0),
.cc (st2_c[0]), .co (st2_p0[7]), .s (st2_p1[6]));
add42 st2_t_col7 (.a (p0[7]), .b (p1[5]), .c (p2[3]), .d (p3[1]), .ci (st2_c[0]),
.cc (st2_c[1]), .co (st2_p0[8]), .s (st2_p1[7]));
    add42 st2_t_col8 (.a (p0[8]), .b (p1[6]), .c (p2[4]), .d (p3[2]), .ci (st2_c[1]),
.cc (st2_c[2]), .co (st2_p0[9]), .s (st2_p1[8]));
    add42 st2_t_col9 (.a (p0[8]), .b (p1[7]), .c (p2[5]), .d (p3[3]), .ci (st2_c[2]),
.cc (st2_c[3]), .co (st2_p0[10]), .s (st2_p1[9]));
    add42 st2_t_col10 (.a (p0[8]), .b (p1[8]), .c (p2[6]), .d (p3[4]), .ci (st2_c[3]),
.cc (st2 c[4]), .co (st2 p0[11]), .s (st2 p1[10]));
    add42 st2_t_col11 (.a (p0[8]), .b (p1[8]), .c (p2[7]), .d (p3[5]), .ci (st2_c[4]),
.cc (st2_c[5]), .co (st2_p0[12]), .s (st2_p1[11]));
    add42 st2_t_col12 (.a (p0[8]), .b (p1[8]), .c (p2[8]), .d (p3[6]), .ci (st2_c[5]),
.cc (st2_c[6]), .co (st2_p0[13]), .s (st2_p1[12]));
    add42 st2_t_col13 (.a (p0[8]), .b (p1[8]), .c (p2[8]), .d (p3[7]), .ci (st2_c[6]),
.cc (st2_c[7]), .co (st2_p0[14]), .s (st2_p1[13]));
    add42 st2_t_col14 (.a (p0[8]), .b (p1[8]), .c (p2[8]), .d (p3[8]), .ci (st2_c[7]),
.cc (st2_c[8]), .co (st2_p0[15]), .s (st2_p1[14]));
    add42 st2_t_col15 (.a (p0[8]), .b (p1[8]), .c (p2[8]), .d (p3[8]), .ci (st2_c[8]),
                                  .s (st2_p1[15]));
.cc (),
                .co (),
// stage 3. CSA cont
    //stage output
```

```
wire [15:0] st3_p0;
   wire [15:6] st3 p1;
   wire [4:2] st3_p2; //part of st3_p1 at column 4,3,2
   //pass through bits
   assign st3_p0[0] = st2_p0[0];
   assign st3 p0[2] = st2 p0[2];
   assign st3_p0[3] = st2_p0[3];
   assign st3 p0[4] = st2 p0[4];
   assign st3_p2[3] = st2_p1[3];
   assign st3_p2[4] = st2_p1[4];
   ha st_b_col1 (.a (st2_p0[1]), .b (st2_p2[0]),
                                                                       .c (st3_p2[2]),
.s (st3 p0[1]));
   fa st_b_col5 (.a (st2_p0[5]), .b (st2_p1[5]), .c (st2_p2[1]), .carry (st3_p0[6]),
.sum (st3_p0[5]));
   fa st_b_col6 (.a (st2_p0[6]), .b (st2_p1[6]), .c (st2_p2[2]), .carry (st3_p0[7]),
.sum (st3 p1[6]));
   ha st_b_col7 (.a (st2_p0[7]), .b (st2_p1[7]),
                                                                       .c (st3_p0[8]),
.s (st3 p1[7]));
   ha st_b_col8 (.a (st2_p0[8]), .b (st2_p1[8]),
                                                                       .c (st3_p0[9]),
.s (st3 p1[8]));
   ha st_b_col9 (.a (st2_p0[9]), .b (st2_p1[9]),
                                                                       .c (st3_p0[10]),
.s (st3_p1[9]));
   ha st_b_col10 (.a (st2_p0[10]), .b (st2_p1[10]),
                                                                       .c (st3_p0[11]),
.s (st3_p1[10]));
   ha st_b_col11 (.a (st2_p0[11]), .b (st2_p1[11]),
                                                                       .c (st3_p0[12]),
.s (st3 p1[11]));
   ha st_b_col12 (.a (st2_p0[12]), .b (st2_p1[12]),
                                                                       .c (st3_p0[13]),
.s (st3 p1[12]));
   ha st_b_col13 (.a (st2_p0[13]), .b (st2_p1[13]),
                                                                       .c (st3_p0[14]),
.s (st3_p1[13]));
   ha st_b_col14 (.a (st2_p0[14]), .b (st2_p1[14]),
                                                                       .c (st3_p0[15]),
.s (st3_p1[14]));
   ha st_b_col15 (.a (st2_p0[15]), .b (st2_p1[15]),
                                                                       .c (),
.s (st3 p1[15]));
// stage 5. CPA
    reg [15:0] out_c;
   always @(st3 p0 or st3 p1) begin
        out_c = st3_p0 + {st3_p1, 1'b0, st3_p2, 2'b00};
    end
// output clk sync
    always @(posedge clk) begin
        out <= #1 out_c;
    end
endmodule
```

Test output (passed)

```
ncverilog +access+r -l mult.logv -f mult.vfv
ncverilog(64): 15.20-s031: (c) Copyright 1995-2017 Cadence Design Systems, Inc.
file: mult.vt
module worklib.tbench:vt
errors: 0, warnings: 0
```

```
file: mult.v
      module worklib.ha:v
            errors: 0, warnings: 0
      module worklib.fa:v
            errors: 0, warnings: 0
      module worklib.add42:v
            errors: 0, warnings: 0
      module worklib.booth2:v
            errors: 0, warnings: 0
      module worklib.mult:v
            errors: 0, warnings: 0
            Caching library 'worklib' ..... Done
      Elaborating the design hierarchy:
      Building instance overlay tables: ..... Done
      Generating native compiled code:
            worklib.booth2:v <0x77c08669>
                  streams: 1, words: 764
            worklib.fa:v <0x52bf646d>
                            0, words:
                  streams:
            worklib.ha:v <0x52cafae2>
                  streams:
                            0, words:
            worklib.mult:v <0x6cc97f80>
                  streams: 9, words: 2381
            worklib.tbench:vt <0x0100204a>
                  streams: 3, words: 11212
      Building instance specific data structures.
      Loading native compiled code:
                                     ..... Done
      Design hierarchy summary:
                             Instances Unique
            Modules:
                                   55
            Registers:
                                   19
                                           13
            Scalar wires:
                                   92
            Expanded wires:
                                   36
            Vectored wires:
                                  11
            Always blocks:
                                   7
                                   1
            Initial blocks:
                                            1
                                   0
            Cont. assignments:
                                           12
            Pseudo assignments:
                                    6
                                            6
            Simulation timescale: 10ps
      Writing initial simulation snapshot: worklib.tbench:vt
Loading snapshot worklib.tbench:vt ...... Done
ncsim> source /apps/Cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> run
         1) 00000001 x 01111111 = 0000000001111111
         2) 00000001 x 10000000 = 11111111110000000
         3) 01111111 x 00000001 = 0000000001111111
         4) 10000000 x 00000001 = 11111111110000000
         5) 01111111 x 01111111 = 0011111100000001
         6) 01111111 x 10000000 = 1100000010000000
         7) 10000000 x 01111111 = 1100000010000000
         8) 10000000 x 10000000 = 0100000000000000
         9) 00101000 x 00100000 = 0000010100000000
        10) 11110001 x 10000111 = 0000011100010111
        11) 00011110 x 11111111 = 1111111111100010
        12) 11111111 x 11111111 = 00000000000000001
        13) 11111111 x 00101101 = 1111111111010011
```

Test output (failed)

For this test, the Booth-2 encoder outputs wrong inverting bit on the beginning of string of 1's

```
ncverilog +access+r -l mult.logv -f mult.vfv
ncverilog(64): 15.20-s031: (c) Copyright 1995-2017 Cadence Design Systems, Inc.
file: mult.vt
      module worklib.tbench:vt
            errors: 0, warnings: 0
file: mult.v
      module worklib.ha:v
            errors: 0, warnings: 0
      module worklib.fa:v
            errors: 0, warnings: 0
      module worklib.add42:v
            errors: 0, warnings: 0
      module worklib.booth2:v
            errors: 0, warnings: 0
      module worklib.mult:v
            errors: 0, warnings: 0
            Caching library 'worklib' ..... Done
      Elaborating the design hierarchy:
      Building instance overlay tables: ..... Done
      Generating native compiled code:
            worklib.booth2:v <0x77c08669>
                   streams:
                             1, words:
                                         764
            worklib.fa:v <0x52bf646d>
                   streams:
                             0. words:
                                           0
            worklib.ha:v <0x52cafae2>
                   streams:
                             0, words:
            worklib.mult:v <0x6cc97f80>
                   streams: 9, words: 2381
            worklib.tbench:vt <0x0100204a>
                   streams: 3, words: 11212
      Building instance specific data structures.
      Loading native compiled code:
                                       ..... Done
      Design hierarchy summary:
                              Instances Unique
            Modules:
                                     55
                                              6
                                     19
            Registers:
                                             13
            Scalar wires:
                                     92
            Expanded wires:
                                     36
                                              4
            Vectored wires:
                                     11
            Always blocks:
                                     7
                                              4
            Initial blocks:
                                      1
                                              1
```

```
Cont. assignments:
                                            12
            Pseudo assignments:
                                             6
            Simulation timescale: 10ps
      Writing initial simulation snapshot: worklib.tbench:vt
Loading snapshot worklib.tbench:vt ...... Done
ncsim> source /apps/Cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> run
         1) 00000001 x 01111111 = 0000000001111111
         2) 00000001 x 10000000 got 11111111101000000 expected 11111111110000000
         3) 01111111 x 00000001 = 0000000001111111
         4) 10000000 x 00000001 = 11111111110000000
         5) 01111111 x 01111111 = 0011111100000001
         6) 01111111 x 10000000 got 1100000001000000 expected 1100000010000000
         7) 10000000 x 01111111 = 1100000010000000
         8) 10000000 x 10000000 got 0011111111000000 expected 0100000000000000
         9) 00101000 x 00100000 got 0000010011110000 expected 0000010100000000
        10) 11110001 x 10000111 got 0000011011010111 expected 0000011100010111
        11) 00011110 x 11111111 = 1111111111100010
        12) 11111111 x 11111111 = 00000000000000001
        13) 11111111 x 00101101 = 1111111111010011
        14) 00000000 x 01100100 got 1111111111110000 expected 0000000000000000
        15) 01100100 x 00000000 = 0000000000000000
        16) 00000001 x 11111111 = 111111111111111
        17) 11111111 x 00000001 = 111111111111111
        18) 01100100 x 01100100 got 0010011100000000 expected 0010011100010000
        19) 11001101 x 01010011 = 1110111101110111
        20) 11000111 x 10100011 got 00010100101010 expected 0001010010110101
        21) 11011101 x 01001110 got 11110101010101 expected 111101010101010
        22) 10111000 x 01011011 = 1110011001101000
        23) 01000000 x 00011101 = 0000011101000000
ncsim: *W,RNQUIE: Simulation is complete.
ncsim> exit
```

Area report

```
***********
Report : area
Design : mult
Version: J-2014.09-SP2
Date : Sun Feb 18 22:13:38 2018
Information: Updating design information... (UID-85)
Library(s) Used:
   NangateOpenCellLibrary (File:
/software/Synopsys/DesignCompiler/EEC281/lib/nangate45/Nangate0penCellLibrary.db)
Number of ports:
                                         33
Number of nets:
                                        322
Number of cells:
                                        279
Number of combinational cells:
                                        247
Number of sequential cells:
                                         32
Number of macros/black boxes:
                                         0
Number of buf/inv:
                                         14
Number of references:
                                         18
```

Combinational area: 372.133996 Buf/Inv area: 7.980000 Noncombinational area: 144.703995 Macro/Black Box area: 0.000000 Net Interconnect area: undefined (Wire load has zero net area)

Total cell area: 516.837991

Total area: undefined

Timing report

************ Report : timing -path full -delay max -nworst 10 -max_paths 10 Design : mult Version: J-2014.09-SP2 Date : Sun Feb 18 22:13:39 2018 *********** Operating Conditions: typical Library: NangateOpenCellLibrary Wire Load Model Mode: top Startpoint: b_r_reg[3] (rising edge-triggered flip-flop clocked by clk) Endpoint: out_reg[15] (rising edge-triggered flip-flop clocked by clk) Path Group: clk Path Type: max Des/Clust/Port Wire Load Model Library ----mult 5K hvratio 1 1 NangateOpenCellLibrary

marc	3K_HV1 dc10_1_1	Nangaccc	peneciilion ar y
Point		Incr	Path
clock clk (rise	edge)	0.00	0.00
clock network de	lay (ideal)	0.00	0.00
b_r_reg[3]/CK (DF	F_X1)	0.00	0.00 r
b_r_reg[3]/Q (DFF	X1)	0.17	0.17 r
U378/Z (XOR2_X1)		0.17	0.34 r
U333/ZN (NOR2_X1))	0.03	0.37 f
U396/Z (MUX2_X1)		0.08	0.45 f
U103/Z (XOR2_X1)		0.08	0.54 f
U102/Z (XOR2_X1)		0.08	0.62 f
U101/ZN (NAND2_X	L)	0.05	0.67 r
U285/ZN (OAI21_X	L)	0.05	0.72 f
U261/ZN (XNOR2_X	L)	0.07	0.79 f
U91/Z (XOR2_X1)		0.09	0.87 f
U1_6/CO (FA_X1)		0.11	0.98 f
U1_7/CO (FA_X1)		0.09	1.08 f
U1_8/CO (FA_X1)		0.09	1.17 f
U1_9/CO (FA_X1)		0.09	1.26 f
U1_10/C0 (FA_X1)		0.09	1.35 f

U1_11/CO (FA_X1)		0.09	1.45 f	
U1_12/CO (FA_X1)		0.09	1.54 f	
U1_13/C0 (FA_X1)		0.09	1.63 f	
U1_14/CO (FA_X1)		0.09	1.73 f	
U1_15/S (FA_X1)		0.13	1.86 r	
out_reg[15]/D (DF	F Y1)	0.01	1.87 r	
data arrival time		0.01	1.87	
aca arrivai cime			1.07	
clock clk (rise e	dge)	4.00	4.00	
clock network del		0.00		
clock network der	· · · · · · · · · · · · · · · · · · ·	-0.20		
_		0.00		
ut_reg[15]/CK (D	_ /			
library setup tim		-0.03		
data required tim	e 		3.77	
data required tim			3.77	
data required time data arrival time			-1.87	
slack (MET)			1.90	
Des/Clust/Port	Wire Load Model	Library		
	Wire Load Model 5K_hvratio_1_1)penCellLibrary	
nult Point	5K_hvratio_1_1	Nangate(Path	
nult Point clock clk (rise e	5K_hvratio_1_1 dge)	Nangate(Incr 0.00	Path 	
mult Point clock clk (rise e	5K_hvratio_1_1 dge)	Nangate(Incr 0.00	Path 	
mult Point clock clk (rise e clock network del	5K_hvratio_1_1 dge) ay (ideal)	Nangate(Incr 0.00 0.00	Path 0.00 0.00	
mult Point clock clk (rise e clock network del b_r_reg[3]/CK (DF	5K_hvratio_1_1 dge) ay (ideal) F_X1)	Nangate(Incr 0.00 0.00 0.00	Path 0.00 0.00 0.00 0.00 r	
mult Point clock clk (rise e clock network del b_r_reg[3]/CK (DF b_r_reg[3]/Q (DFF	5K_hvratio_1_1 dge) ay (ideal) F_X1)	Incr 0.00 0.00 0.00 0.00	Path 0.00 0.00 0.00 r 0.17 r	
mult Point clock clk (rise e clock network del b_r_reg[3]/CK (DF b_r_reg[3]/Q (DFF U378/Z (XOR2_X1)	5K_hvratio_1_1 dge) ay (ideal) F_X1) _X1)	Nangate(Incr 0.00 0.00 0.00 0.17 0.17	Path 0.00 0.00 0.00 r 0.17 r 0.34 r	
mult Point clock clk (rise e clock network del b_r_reg[3]/CK (DF b_r_reg[3]/Q (DFF U378/Z (XOR2_X1) U333/ZN (NOR2_X1)	5K_hvratio_1_1 dge) ay (ideal) F_X1) _X1)	Nangate(Incr 0.00 0.00 0.00 0.17 0.17 0.03	Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f	
mult Point clock clk (rise e clock network del b_r_reg[3]/CK (DF b_r_reg[3]/Q (DFF U378/Z (XOR2_X1) U333/ZN (NOR2_X1) U396/Z (MUX2_X1)	5K_hvratio_1_1 dge) ay (ideal) F_X1) _X1)	Nangate(Incr 0.00 0.00 0.00 0.17 0.17 0.03 0.08	Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f 0.45 f	
mult Point clock clk (rise e clock network del b_r_reg[3]/CK (DF b_r_reg[3]/Q (DFF U378/Z (XOR2_X1) U333/ZN (NOR2_X1) U396/Z (MUX2_X1) U103/Z (XOR2_X1)	5K_hvratio_1_1 dge) ay (ideal) F_X1) _X1)	Nangate(Incr 0.00 0.00 0.00 0.17 0.17 0.03 0.08 0.08	Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f 0.45 f 0.54 f	
mult Point	5K_hvratio_1_1 dge) ay (ideal) F_X1) _X1)	Nangate(Incr 0.00 0.00 0.00 0.17 0.17 0.03 0.08 0.08	Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f 0.45 f 0.54 f 0.62 f	
mult Point	5K_hvratio_1_1 dge) ay (ideal) F_X1) _X1)	Nangate(Incr 0.00 0.00 0.00 0.17 0.17 0.03 0.08 0.08 0.08	Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f 0.45 f 0.45 f 0.62 f 0.67 r	
mult Point	5K_hvratio_1_1 dge) ay (ideal) F_X1) _X1)	Nangate(Incr 0.00 0.00 0.00 0.17 0.17 0.03 0.08 0.08 0.08 0.08	Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f 0.45 f 0.45 f 0.62 f 0.62 f 0.67 r 0.72 f	
mult Point	5K_hvratio_1_1 dge) ay (ideal) F_X1) _X1)	Nangate(Incr 0.00 0.00 0.17 0.17 0.03 0.08 0.08 0.08 0.08 0.05 0.05	Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f 0.45 f 0.62 f 0.62 f 0.67 r 0.72 f 0.79 f	
mult Point	5K_hvratio_1_1 dge) ay (ideal) F_X1) _X1)	Nangate(Incr 0.00 0.00 0.17 0.17 0.03 0.08 0.08 0.08 0.09	Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f 0.45 f 0.62 f 0.62 f 0.67 r 0.72 f 0.79 f 0.87 f	
mult Point	5K_hvratio_1_1 dge) ay (ideal) F_X1) _X1)	Nangate(Incr 0.00 0.00 0.17 0.17 0.03 0.08 0.08 0.08 0.09 0.05 0.07 0.09 0.11	Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f 0.45 f 0.62 f 0.62 f 0.67 r 0.72 f 0.79 f 0.87 f 0.98 f	
mult Point	5K_hvratio_1_1 dge) ay (ideal) F_X1) _X1)	Nangate(Incr 0.00 0.00 0.17 0.17 0.03 0.08 0.08 0.08 0.09 0.05 0.07 0.09	Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f 0.45 f 0.62 f 0.62 f 0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f	
mult Point	5K_hvratio_1_1 dge) ay (ideal) F_X1) _X1)	Nangate(Incr 0.00 0.00 0.17 0.17 0.03 0.08 0.08 0.08 0.09 0.05 0.07 0.09 0.11	Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f 0.45 f 0.62 f 0.62 f 0.67 r 0.72 f 0.79 f 0.87 f 0.98 f	
mult Point	5K_hvratio_1_1 dge) ay (ideal) F_X1) _X1)	Nangate(Incr 0.00 0.00 0.17 0.17 0.03 0.08 0.08 0.08 0.09 0.05 0.07 0.09	Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f 0.45 f 0.62 f 0.62 f 0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f	
Point	5K_hvratio_1_1 dge) ay (ideal) F_X1) _X1)	Nangate(Incr 0.00 0.00 0.00 0.17 0.17 0.03 0.08 0.08 0.08 0.09 0.05 0.07 0.09 0.11 0.09 0.09	Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f 0.45 f 0.54 f 0.62 f 0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f 1.17 f 1.26 f	
Point	5K_hvratio_1_1 dge) ay (ideal) F_X1) _X1)	Nangate(Incr 0.00 0.00 0.00 0.17 0.17 0.03 0.08 0.08 0.08 0.09 0.05 0.05 0.07 0.09 0.11 0.09 0.09 0.09	Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f 0.45 f 0.54 f 0.62 f 0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f 1.17 f 1.26 f 1.35 f	
Point	5K_hvratio_1_1 dge) ay (ideal) F_X1) _X1)	Nangate(Incr 0.00 0.00 0.00 0.17 0.17 0.03 0.08 0.08 0.08 0.09 0.05 0.05 0.05 0.07 0.09 0.11 0.09 0.09 0.09 0.09	Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f 0.45 f 0.54 f 0.62 f 0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f 1.17 f 1.26 f 1.35 f 1.45 f	
Point	5K_hvratio_1_1 dge) ay (ideal) F_X1) _X1)	Nangate(Incr 0.00 0.00 0.17 0.17 0.03 0.08 0.08 0.08 0.05 0.05 0.05 0.07 0.09 0.11 0.09 0.09 0.09 0.09	Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f 0.45 f 0.54 f 0.62 f 0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f 1.17 f 1.26 f 1.35 f 1.45 f 1.54 f	
mult Point	5K_hvratio_1_1 dge) ay (ideal) F_X1) _X1)	Nangate(Incr 0.00 0.00 0.17 0.17 0.17 0.03 0.08 0.08 0.08 0.09 0.09 0.09 0.09 0.09 0.09 0.09 0.09 0.09 0.09	Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f 0.45 f 0.54 f 0.62 f 0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f 1.17 f 1.26 f 1.35 f 1.45 f 1.54 f 1.63 f	
mult Point	5K_hvratio_1_1 dge) ay (ideal) F_X1) _X1)	Nangate(Incr 0.00 0.00 0.00 0.17 0.17 0.03 0.08 0.08 0.08 0.09 0.09 0.09 0.09 0.09 0.09 0.09 0.09 0.09 0.09 0.09	Path 0.00 0.00 r 0.17 r 0.34 r 0.37 f 0.45 f 0.62 f 0.67 r 0.72 f 0.79 f 0.87 f 0.87 f 0.98 f 1.08 f 1.17 f 1.26 f 1.35 f 1.45 f 1.54 f 1.54 f 1.54 f 1.73 f	
mult Point	5K_hvratio_1_1 dge) ay (ideal) F_X1) _X1)	Nangate(Incr 0.00 0.00 0.17 0.17 0.17 0.03 0.08 0.08 0.08 0.09 0.09 0.09 0.09 0.09 0.09 0.09 0.09 0.09 0.09	Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f 0.45 f 0.54 f 0.62 f 0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f 1.17 f 1.26 f 1.35 f 1.45 f 1.54 f 1.63 f	

data arrival time	2		1.87
alack alk /====	odgo)	4 00	4 00
clock clk (rise		4.00	4.00
clock network de		0.00	4.00
clock uncertainty	•	-0.20	3.80
out_reg[15]/CK ([0.00	3.80 r
library setup tir		-0.03	3.77
data required tir	ne 		3.77
data required tir			3.77
data arrival time	е		-1.87
slack (MET)			1.90
Endpoint: out_re			ip-flop clocked by clk) ed by clk)
Des/Clust/Port	Wire Load Model	Library	
mult	5K_hvratio_1_1	Nangate(OpenCellLibrary
Point		Incr	
clock clk (rise		0.00	
clock network de		9 99	9 99
b_r_reg[3]/CK (DI		0.00	0.00 r
b_r_reg[3]/Q (DFI		0.17	0.17 r
		0.17	0.17 1
U378/Z (XOR2_X1)	、	0.17	0.34 r
U333/ZN (NOR2_X1))		
U396/Z (MUX2_X1)			0.45 f
U103/Z (XOR2_X1)			0.54 f
()		0 08	0.62 f
U102/Z (XOR2_X1)		0.00	***= *
	1)	0.05	
U101/ZN (NAND2_X			
U101/ZN (NAND2_X: U285/ZN (OAI21_X:	1)	0.05	0.67 r 0.72 f
U101/ZN (NAND2_X: U285/ZN (OAI21_X: U261/ZN (XNOR2_X:	1)	0.05 0.05 0.07	0.67 r 0.72 f 0.79 f
U101/ZN (NAND2_X: U285/ZN (OAI21_X: U261/ZN (XNOR2_X: U91/Z (XOR2_X1)	1)	0.05 0.05 0.07 0.09	0.67 r 0.72 f 0.79 f 0.87 f
U101/ZN (NAND2_X: U285/ZN (OAI21_X: U261/ZN (XNOR2_X: U91/Z (XOR2_X1) U1_6/CO (FA_X1)	1)	0.05 0.05 0.07 0.09 0.11	0.67 r 0.72 f 0.79 f 0.87 f 0.98 f
U101/ZN (NAND2_X: U285/ZN (OAI21_X: U261/ZN (XNOR2_X: U91/Z (XOR2_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1)	1)	0.05 0.05 0.07 0.09 0.11 0.09	0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f
U101/ZN (NAND2_X: U285/ZN (OAI21_X: U261/ZN (XNOR2_X: U91/Z (XOR2_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1)	1)	0.05 0.05 0.07 0.09 0.11 0.09 0.09	0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f 1.17 f
U101/ZN (NAND2_X: U285/ZN (OAI21_X: U261/ZN (XNOR2_X: U91/Z (XOR2_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1)	1)	0.05 0.05 0.07 0.09 0.11 0.09 0.09	0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f 1.17 f 1.26 f
U101/ZN (NAND2_X: U285/ZN (OAI21_X: U261/ZN (XNOR2_X: U91/Z (XOR2_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_19/CO (FA_X1) U1_10/CO (FA_X1)	1)	0.05 0.05 0.07 0.09 0.11 0.09 0.09 0.09	0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f 1.17 f 1.26 f 1.35 f
U101/ZN (NAND2_X: U285/ZN (OAI21_X: U261/ZN (XNOR2_X: U91/Z (XOR2_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1)	1)	0.05 0.05 0.07 0.09 0.11 0.09 0.09 0.09	0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f 1.17 f 1.26 f 1.35 f 1.45 f
U101/ZN (NAND2_X: U285/ZN (OAI21_X: U261/ZN (XNOR2_X: U91/Z (XOR2_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_11/CO (FA_X1) U1_12/CO (FA_X1)	1)	0.05 0.05 0.07 0.09 0.11 0.09 0.09 0.09 0.09	0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f 1.17 f 1.26 f 1.35 f 1.45 f 1.54 f
U101/ZN (NAND2_X: U285/ZN (OAI21_X: U261/ZN (XNOR2_X: U91/Z (XOR2_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_11/CO (FA_X1) U1_12/CO (FA_X1)	1)	0.05 0.05 0.07 0.09 0.11 0.09 0.09 0.09	0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f 1.17 f 1.26 f 1.35 f 1.45 f
U101/ZN (NAND2_X: U285/ZN (OAI21_X: U261/ZN (XNOR2_X: U91/Z (XOR2_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_11/CO (FA_X1) U1_12/CO (FA_X1) U1_13/CO (FA_X1)	1)	0.05 0.05 0.07 0.09 0.11 0.09 0.09 0.09 0.09	0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f 1.17 f 1.26 f 1.35 f 1.45 f 1.54 f
U101/ZN (NAND2_X: U285/ZN (OAI21_X: U261/ZN (XNOR2_X: U91/Z (XOR2_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_12/CO (FA_X1) U1_13/CO (FA_X1) U1_13/CO (FA_X1) U1_14/CO (FA_X1)	1)	0.05 0.05 0.07 0.09 0.11 0.09 0.09 0.09 0.09	0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f 1.17 f 1.26 f 1.35 f 1.45 f 1.54 f 1.63 f
U101/ZN (NAND2_X: U285/ZN (OAI21_X: U261/ZN (XNOR2_X: U91/Z (XOR2_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_12/CO (FA_X1) U1_13/CO (FA_X1) U1_13/CO (FA_X1) U1_14/CO (FA_X1) U1_15/S (FA_X1)	1)	0.05 0.05 0.07 0.09 0.11 0.09 0.09 0.09 0.09 0.09 0.09	0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f 1.17 f 1.26 f 1.35 f 1.45 f 1.54 f 1.63 f 1.73 f 1.86 r
U101/ZN (NAND2_X: U285/ZN (OAI21_X: U261/ZN (XNOR2_X: U91/Z (XOR2_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_11/CO (FA_X1) U1_12/CO (FA_X1) U1_13/CO (FA_X1) U1_13/CO (FA_X1) U1_15/S (FA_X1) Out_reg[15]/D (DI	1) 1) FF_X1)	0.05 0.05 0.07 0.09 0.11 0.09 0.09 0.09 0.09 0.09	0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f 1.17 f 1.26 f 1.35 f 1.45 f 1.54 f 1.63 f 1.73 f
U102/Z (XOR2_X1) U101/ZN (NAND2_X: U285/ZN (OAI21_X: U261/ZN (XNOR2_X: U91/Z (XOR2_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_12/CO (FA_X1) U1_13/CO (FA_X1) U1_13/CO (FA_X1) U1_15/S (FA_X1) U1_15/S (FA_X1) Out_reg[15]/D (DI data arrival time	1) 1) FF_X1) e	0.05 0.05 0.07 0.09 0.11 0.09 0.09 0.09 0.09 0.09 0.09	0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f 1.17 f 1.26 f 1.35 f 1.45 f 1.54 f 1.63 f 1.73 f 1.86 r 1.87 r 1.87
U101/ZN (NAND2_X: U285/ZN (OAI21_X: U261/ZN (XNOR2_X: U91/Z (XOR2_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_8/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_12/CO (FA_X1) U1_13/CO (FA_X1) U1_13/CO (FA_X1) U1_15/S (FA_X1) U1_15/S (FA_X1) Out_reg[15]/D (DIdata arrival time	1) 1) FF_X1) e edge)	0.05 0.05 0.07 0.09 0.11 0.09 0.09 0.09 0.09 0.09 0.09	0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f 1.17 f 1.26 f 1.35 f 1.45 f 1.45 f 1.63 f 1.73 f 1.86 r 1.87 r 1.87
U101/ZN (NAND2_X: U285/ZN (OAI21_X: U261/ZN (XNOR2_X: U91/Z (XOR2_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_12/CO (FA_X1) U1_12/CO (FA_X1) U1_13/CO (FA_X1) U1_13/CO (FA_X1) U1_15/S (FA_X1) Out_reg[15]/D (DIdata arrival time clock clk (rise clock network dei	fF_X1) e edge) lay (ideal)	0.05 0.05 0.07 0.09 0.11 0.09 0.09 0.09 0.09 0.09 0.09	0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f 1.17 f 1.26 f 1.35 f 1.45 f 1.54 f 1.63 f 1.73 f 1.86 r 1.87 r 1.87
U101/ZN (NAND2_X: U285/ZN (OAI21_X: U261/ZN (XNOR2_X: U91/Z (XOR2_X1) U1_6/CO (FA_X1) U1_7/CO (FA_X1) U1_9/CO (FA_X1) U1_10/CO (FA_X1) U1_11/CO (FA_X1) U1_12/CO (FA_X1) U1_13/CO (FA_X1) U1_13/CO (FA_X1) U1_15/S (FA_X1) U1_15/S (FA_X1) Out_reg[15]/D (DIdata arrival time	fF_X1) e edge) lay (ideal)	0.05 0.05 0.07 0.09 0.11 0.09 0.09 0.09 0.09 0.09 0.09	0.67 r 0.72 f 0.79 f 0.87 f 0.98 f 1.08 f 1.17 f 1.26 f 1.35 f 1.45 f 1.45 f 1.63 f 1.73 f 1.86 r 1.87 r 1.87

library setup tim data required tim	ne	-0.03	3.77	
data required tim			3.77	
data arrival time			-1.87	
slack (MET)			1.90	
Endpoint: out_reg			p-flop clocked by clk)	
Des/Clust/Port	Wire Load Model	-		
	5K_hvratio_1_1		penCellLibrary	
Point		Incr		
clock clk (rise e		0.00		
	ay (ideal)			
b_r_reg[3]/CK (DF			0.00 r	
b_r_reg[3]/Q (DFF		0.17		
U378/Z (XOR2_X1)		0.17		
U333/ZN (NOR2_X1)	1	0.03		
U396/Z (MUX2_X1)		0.08		
U103/Z (XOR2_X1)		0.08		
U102/Z (XOR2_X1)	١		0.62 f	
U101/ZN (NAND2_X1	*	0.05		
U285/ZN (OAI21_X1	•	0.05		
U261/ZN (XNOR2_X1	-)	0.07		
U91/Z (XOR2_X1)		0.09	0.87 f	
U1_6/CO (FA_X1)		0.11	0.98 f	
U1_7/C0 (FA_X1)		0.09	1.08 f	
U1_8/CO (FA_X1)		0.09	1.17 f	
U1_9/CO (FA_X1)		0.09	1.26 f	
U1_10/CO (FA_X1)		0.09	1.35 f	
U1_11/CO (FA_X1)		0.09	1.45 f	
U1_12/CO (FA_X1)		0.09	1.54 f	
U1_13/CO (FA_X1)		0.09	1.63 f	
U1_14/CO (FA_X1)		0.09	1.73 f	
U1_15/S (FA_X1)		0.13	1.86 r	
out_reg[15]/D (DF	F_X1)	0.01	1.87 r	
data arrival time			1.87	
clock clk (rise e		4.00	4.00	
clock network del	· · · · · · · · · · · · · · · · · · ·	0.00	4.00	
clock uncertainty		-0.20	3.80	
out_reg[15]/CK (D	_ ,	0.00	3.80 r	
library setup tim		-0.03	3.77	
data required tim	1e 		3.77	
data required tim			3.77	
data arrival time	1		-1.87	

```
slack (MET)
                                                1.90
Startpoint: b_r_reg[3] (rising edge-triggered flip-flop clocked by clk)
Endpoint: out_reg[15]
         (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
Des/Clust/Port Wire Load Model
                                   Library
                                     NangateOpenCellLibrary
mult
                5K_hvratio_1_1
Point
                                     Incr
                                                Path
                                     0.00 0.00
clock clk (rise edge)
                                0.00
0.00
clock network delay (ideal)
                                              0.00
b r reg[3]/CK (DFF X1)
                                               0.00 r
b_r_reg[3]/Q (DFF_X1)
                                    0.17
                                               0.17 r
                                    0.17
                                              0.34 r
U378/Z (XOR2 X1)
U333/ZN (NOR2 X1)
                                     0.03
                                              0.37 f
                                     0.08
U396/Z (MUX2 X1)
                                              0.45 f
                                             0.54 f
0.62 f
U103/Z (XOR2 X1)
                                     0.08
U102/Z (XOR2_X1)
                                     0.08
U101/ZN (NAND2 X1)
                                     0.05
                                              0.67 r
U285/ZN (OAI21_X1)
                                     0.05
                                              0.72 f
U261/ZN (XNOR2_X1)
                                     0.07
                                              0.79 f
U91/Z (XOR2 X1)
                                     0.09
                                               0.87 f
U1_6/CO (FA_X1)
                                     0.11
                                              0.98 f
U1 7/CO (FA X1)
                                     0.09
                                               1.07 f
U1_8/CO (FA_X1)
                                     0.09
                                               1.17 f
U1 9/CO (FA X1)
                                     0.09
                                              1.26 f
U1_10/CO (FA_X1)
                                     0.09
                                               1.35 f
                                     0.09
U1_11/CO (FA_X1)
                                               1.44 f
U1_12/CO (FA_X1)
                                     0.09
                                               1.54 f
U1 13/CO (FA X1)
                                              1.63 f
                                     0.09
U1 14/CO (FA X1)
                                     0.09
                                               1.72 f
U1 15/S (FA X1)
                                     0.13
                                               1.86 r
out reg[15]/D (DFF X1)
                                     0.01
                                               1.87 r
data arrival time
                                               1.87
clock clk (rise edge)
                                    4.00
                                               4.00
clock network delay (ideal)
                                    0.00
                                               4.00
clock uncertainty
                                    -0.20
                                               3.80
out_reg[15]/CK (DFF_X1)
                                     0.00
                                               3.80 r
library setup time
                                    -0.03
                                                3.77
data required time
                                               3.77
_____
data required time
                                                3.77
data arrival time
                                               -1.87
slack (MET)
                                                1.90
Startpoint: b_r_reg[3] (rising edge-triggered flip-flop clocked by clk)
Endpoint: out reg[15]
         (rising edge-triggered flip-flop clocked by clk)
```

	Wire Load Model		
mult	5K_hvratio_1_1		OpenCellLibrary
Point		Incr	Path
clock clk (rise e		0.00	
clock network del	ay (ideal)	0.00	0.00
b_r_reg[3]/CK (DF		0.00	0.00 r
b_r_reg[3]/Q (DFF		0.17	0.17 r
J378/Z (XOR2_X1)	- /	0.17	0.34 r
J333/ZN (NOR2_X1)		0.03	
U396/Z (MUX2_X1)		0.08	
U103/Z (XOR2 X1)			0.54 f
U102/Z (XOR2_X1)		0.08	
U101/ZN (NAND2_X1))	0.05	
U285/ZN (OAI21_X1	•	0.05	
U261/ZN (XNOR2_X1	•	0.03	0.79 f
U91/ZN (XNOK2_X1 U91/Z (XOR2_X1)	.,	0.09	0.87 f
U1 6/CO (FA X1)		0.11	0.98 f
U1_7/CO (FA_X1)		0.09	1.07 f
U1_7/CO (FA_X1)		0.09	1.17 f
U1_8/CO (FA_X1)		0.09	1.17 T
U1_9/CO (FA_X1)		0.09	1.35 f
		0.09	1.44 f
U1_11/CO (FA_X1)			
U1_12/CO (FA_X1)		0.09	1.54 f
U1_13/CO (FA_X1)		0.09	1.63 f
U1_14/CO (FA_X1)		0.09	1.72 f
U1_15/S (FA_X1)	- V4.	0.13	1.86 r
out_reg[15]/D (DF data arrival time		0.01	1.87 r 1.87
clock clk (rise e	dge)	4.00	4.00
clock network del		0.00	4.00
clock uncertainty	- '	-0.20	3.80
out_reg[15]/CK (D		0.00	
library setup tim		-0.03	
data required tim	ie		3.77
data required tim	 le		3.77
data arrival time			-1.87
			1.90

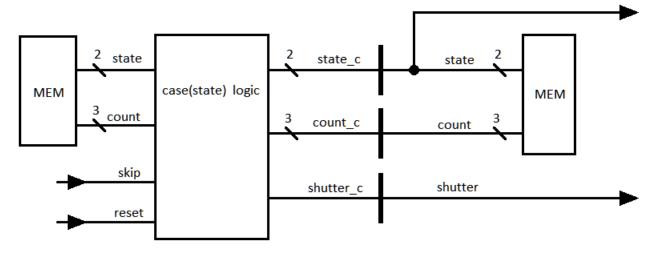
Point		Incr	Path	
clock clk (rise e	edge)	0.00	0.00	
clock network del	ay (ideal)	0.00	0.00	
b_r_reg[3]/CK (DF	F_X1)	0.00	0.00 r	
b_r_reg[3]/Q (DFF	:_X1)	0.17	0.17 r	
U378/Z (XOR2_X1)		0.17	0.34 r	
U333/ZN (NOR2_X1)	ı	0.03	0.37 f	
U396/Z (MUX2_X1)		0.08	0.45 f	
U103/Z (XOR2_X1)		0.08	0.54 f	
U102/Z (XOR2_X1)		0.08	0.62 f	
U101/ZN (NAND2_X1	•	0.05	0.67 r	
U285/ZN (OAI21_X1	•	0.05	0.72 f	
U261/ZN (XNOR2_X1	-)	0.07	0.79 f	
U91/Z (XOR2_X1)		0.09 0.11	0.87 f 0.98 f	
U1_6/CO (FA_X1) U1 7/CO (FA X1)		0.09	1.07 f	
U1_8/CO (FA_X1)		0.09	1.07 f	
U1_9/CO (FA_X1)		0.09	1.17 T 1.26 f	
U1_10/CO (FA_X1)		0.09	1.35 f	
U1_11/CO (FA_X1)		0.09	1.44 f	
U1_12/CO (FA_X1)		0.09	1.54 f	
U1_13/CO (FA_X1)		0.09	1.63 f	
U1_14/CO (FA_X1)		0.09	1.72 f	
U1_15/S (FA_X1)		0.13	1.86 r	
out_reg[15]/D (DF	F X1)	0.01	1.87 r	
data arrival time			1.87	
clock clk (rise e	edge)	4.00	4.00	
clock network del	- '	0.00	4.00	
clock uncertainty		-0.20	3.80	
out_reg[15]/CK ([0.00	3.80 r	
library setup tim		-0.03	3.77	
data required tin 	1 0 		3.77	
			3.77	
	<u> </u>		-1.87	
slack (MET)			1.90	
slack (MET) Startpoint: b_r_r Endpoint: out_re	e reg[3] (rising edge-t	riggered fl	-1.87 1.90 ip-flop clocked by clk)	
	Wire Load Model	•		
	5K_hvratio_1_1		OpenCellLibrary	
Point		Incr	Path	
clock clk (rise e	edge)	0.00	0.00	
			0.00 0.00	

$b_r_eg[3]/Q$ (DFF	X1)	0.17	0.17 r
U378/Z (XOR2_X1)		0.17	0.34 r
U333/ZN (NOR2_X1))	0.03	0.37 f
U396/Z (MUX2_X1)		0.08	0.45 f
U103/Z (XOR2_X1)		0.08	0.54 f
U102/Z (XOR2_X1)		0.08	0.62 f
• — •			
U101/ZN (NAND2_X1	•	0.05	0.67 r
U285/ZN (OAI21_X1		0.05	0.72 f
U261/ZN (XNOR2_X1	L)	0.07	0.79 f
U91/Z (XOR2_X1)		0.09	0.87 f
U1_6/CO (FA_X1)		0.11	0.98 f
U1_7/CO (FA_X1)		0.09	1.07 f
U1_8/CO (FA_X1)		0.09	1.17 f
U1_9/C0 (FA_X1)		0.09	1.26 f
U1_10/C0 (FA_X1)		0.09	1.35 f
_			
U1_11/C0 (FA_X1)		0.09	1.44 f
U1_12/C0 (FA_X1)		0.09	1.54 f
U1_13/C0 (FA_X1)		0.09	
U1_14/C0 (FA_X1)		0.09	
U1_15/S (FA_X1)		0.13	1.86 r
out_reg[15]/D (DF	F X1)	0.01	1.87 r
data arrival time			1.87
.1	. 4	4 00	4.00
clock clk (rise		4.00	4.00
clock network del		0.00	4.00
clock uncertainty		-0.20	3.80
out_reg[15]/CK ([OFF_X1)	0.00	3.80 r
Out_1 cg[13]/ ck (t			
library setup tim		-0.03	3.77
	ne ne		
library setup tim	ne 		3.77 3.77
library setup tim data required tim data required tim	ne ne ne		3.77 3.77 3.77
library setup tim	ne ne ne e		3.77 3.77
library setup tim data required tim data required tim data arrival time	ne ne ne		3.77 3.77 3.77
library setup tim data required tim data required tim data arrival time slack (MET) Startpoint: b_r_r Endpoint: out_reg	ne ne ne e e 	riggered fla	3.77 3.77
library setup tim data required tim data required tim data arrival time slack (MET) Startpoint: b_r_r Endpoint: out_reg	ne ne ne reg[3] (rising edge-tr g[15] g edge-triggered flip-	riggered fla	3.77 3.77 -1.87 -1.90 ip-flop clocked by clk)
library setup tim data required tim data required tim data arrival time slack (MET) Startpoint: b_r_r Endpoint: out_reg	reg[3] (rising edge-trg[15] g edge-triggered flip-	riggered fla	3.77 3.77 -1.87 -1.90 ip-flop clocked by clk)
library setup tim data required tim data required tim data arrival time slack (MET) Startpoint: b_r_r Endpoint: out_reg	reg[3] (rising edge-trg[15] g edge-triggered flip- Wire Load Model 5K_hvratio_1_1	riggered fla flop clocke Library NangateO	3.77 3.77 3.77 -1.87 1.90 Ap-flop clocked by clk) Apd by clk) AppenCellLibrary Path
library setup tim data required tim data required tim data arrival time slack (MET) Startpoint: b_r_r Endpoint: out_reg	reg[3] (rising edge-trg[15] g edge-triggered flip- Wire Load Model 5K_hvratio_1_1	riggered fla flop clocke Library Nangate Incr	3.77 3.77 -1.87 -1.90 Ap-flop clocked by clk) ed by clk) OpenCellLibrary Path 0.00
library setup tim data required tim data required tim data arrival time slack (MET) Startpoint: b_r_r Endpoint: out_reg (rising Path Group: clk Path Type: max Des/Clust/Port mult Point clock clk (rise eclock network del	me me me me me gg[3] (rising edge-tr gg[15] g edge-triggered flip- Wire Load Model 5K_hvratio_1_1	Library Nangate Incr 0.00 0.00	3.77 3.77 -1.87 -1.90 Ap-flop clocked by clk) ed by clk) OpenCellLibrary Path 0.00 0.00
library setup tim data required tim data required tim data arrival time slack (MET) Startpoint: b_r_r Endpoint: out_reg (rising Path Group: clk Path Type: max Des/Clust/Port	me me me me me me me gg[3] (rising edge-tr gg[15] g edge-triggered flip- Wire Load Model 5K_hvratio_1_1 edge) Lay (ideal) FF_X1)	Library Nangate Incr 0.00 0.00	3.77 3.77 -1.87 1.90 Ap-flop clocked by clk) Apd by clk) AppenCellLibrary Path 0.00 0.00 0.00 r
library setup tim data required tim data required tim data arrival time slack (MET) Startpoint: b_r_r Endpoint: out_reg	me me me me me me me gg[3] (rising edge-tr gg[15] g edge-triggered flip- Wire Load Model 5K_hvratio_1_1 edge) Lay (ideal) FF_X1)	Library Nangate Incr 0.00 0.00 0.00 0.17	3.77 3.77 -1.87 1.90 Ap-flop clocked by clk) Apdroced by clk) AppenCellLibrary Path 0.00 0.00 0.00 0.00 r 0.17 r
library setup tim data required tim data required tim data arrival time slack (MET) Startpoint: b_r_r Endpoint: out_reg	me m	Library Nangate Incr 0.00 0.00 0.00 0.17 0.17	3.77 3.77 -1.87 -1.90 Ap-flop clocked by clk) ApdrocellLibrary Path 0.00 0.00 0.00 r 0.17 r 0.34 r
library setup tim data required tim data required tim data arrival time slack (MET) Startpoint: b_r_r Endpoint: out_reg	me m	Library Nangate Incr 0.00 0.00 0.17 0.17 0.03	3.77 3.77 -1.87 -1.90 Ap-flop clocked by clk) ApdrecellLibrary Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f
library setup tim data required tim data required tim data arrival time slack (MET) Startpoint: b_r_r Endpoint: out_reg	me m	Library Nangate Incr 0.00 0.00 0.00 0.17 0.17	3.77 3.77 -1.87 -1.90 Ap-flop clocked by clk) ApdrocellLibrary Path 0.00 0.00 0.00 r 0.17 r 0.34 r
library setup tim data required tim data required tim data arrival time slack (MET) Startpoint: b_r_r Endpoint: out_reg	me m	Library Nangate Incr 0.00 0.00 0.17 0.17 0.03	3.77 3.77 -1.87 -1.90 Ap-flop clocked by clk) ApdrecellLibrary Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f

	<u> </u>	0.05	^	
U101/ZN (NAND2_X1	•	0.05	0.67 r	
U285/ZN (OAI21_X1)		0.05	0.72 f	
U261/ZN (XNOR2_X1	.)	0.07		
U91/Z (XOR2_X1)		0.09	0.87 f	
U1_6/CO (FA_X1)		0.11	0.98 f	
U1_7/CO (FA_X1)		0.09	1.08 f	
U1_8/CO (FA_X1)		0.09	1.17 f	
U1_9/CO (FA_X1)		0.09	1.26 f	
U1_10/CO (FA_X1)		0.09	1.35 f	
U1_11/CO (FA_X1)		0.09	1.44 f	
U1 12/C0 (FA X1)		0.09	1.54 f	
U1_13/C0 (FA_X1)		0.09	1.63 f	
U1_14/C0 (FA_X1)		0.09	1.72 f	
U1_15/S (FA_X1)		0.13	1.86 r	
out_reg[15]/D (DF		0.01	1.87 r	
data arrival time			1.87	
clock clk (rise e	dge)	4.00	4.00	
	ay (ideal)			
clock uncertainty		-0.20		
out_reg[15]/CK (D		0.00		
		-0.03		
library setup tim		-0.03		
data required tim	e 		3.77	
data required tim			3.77	
			-1.87	
data arrival time slack (MET)			1.90	
slack (MET) Startpoint: b_r_r Endpoint: out_reg	eg[3] (rising edge-t	riggered fli	1.90 ip-flop clocked by clk)	
slack (MET) Startpoint: b_r_r Endpoint: out_reg	eg[3] (rising edge-t [15] edge-triggered flip	riggered fli -flop clocke	1.90 ip-flop clocked by clk)	
Startpoint: b_r_r Endpoint: out_reg	eg[3] (rising edge-t [15] edge-triggered flip Wire Load Model	riggered fli -flop clocke Library	1.90 ip-flop clocked by clk) ed by clk)	
Startpoint: b_r_r Endpoint: out_reg	eg[3] (rising edge-t [15] edge-triggered flip Wire Load Model	riggered fli -flop clocke Library NangateO	1.90 ip-flop clocked by clk) ed by clk) OpenCellLibrary	
Startpoint: b_r_r Endpoint: out_reg	eg[3] (rising edge-t [15] edge-triggered flip Wire Load Model	riggered fli -flop clocke Library	1.90 ip-flop clocked by clk) ed by clk)	
Startpoint: b_r_r Endpoint: out_reg	eg[3] (rising edge-t [15] edge-triggered flip Wire Load Model 	riggered fli -flop clocke Library NangateO	1.90 ip-flop clocked by clk) ed by clk) OpenCellLibrary Path	
Startpoint: b_r_r Endpoint: out_reg	eg[3] (rising edge-t [15] edge-triggered flip Wire Load Model 5K_hvratio_1_1	riggered fli -flop clocke Library NangateO Incr0.00	1.90 Ap-flop clocked by clk) Ped by clk) OpenCellLibrary Path 0.00	
Startpoint: b_r_r Endpoint: out_reg	eg[3] (rising edge-t [15] edge-triggered flip Wire Load Model 	riggered fli -flop clocke Library NangateO Incr 0.00 0.00	1.90 Ap-flop clocked by clk) Ped by clk) PenCellLibrary Path 0.00 0.00	
slack (MET) Startpoint: b_r_r Endpoint: out_reg	eg[3] (rising edge-t [15] edge-triggered flip Wire Load Model 	riggered fli -flop clocke Library NangateO Incr 0.00 0.00 0.00	1.90 ip-flop clocked by clk) ed by clk) OpenCellLibrary Path 0.00 0.00 0.00 r	
slack (MET) Startpoint: b_r_r Endpoint: out_reg	eg[3] (rising edge-t [15] edge-triggered flip Wire Load Model 	riggered fli -flop clocke Library NangateO Incr 0.00 0.00 0.00 0.00 0.17	1.90 Ap-flop clocked by clk) AppenCellLibrary Path 0.00 0.00 0.00 0.17 r	
slack (MET) Startpoint: b_r_r Endpoint: out_reg	eg[3] (rising edge-t [15] edge-triggered flip Wire Load Model 	riggered fli -flop clocke Library NangateO Incr 0.00 0.00 0.00 0.17 0.17	1.90 Ap-flop clocked by clk) AppenCellLibrary Path 0.00 0.00 0.00 0.00 r 0.17 r 0.34 r	
slack (MET) Startpoint: b_r_r Endpoint: out_reg	eg[3] (rising edge-t [15] edge-triggered flip Wire Load Model 	riggered fli -flop clocke Library NangateO Incr 0.00 0.00 0.00 0.00 0.17	1.90 Ap-flop clocked by clk) AppenCellLibrary Path 0.00 0.00 0.00 0.17 r	
Startpoint: b_r_r Endpoint: out_reg	eg[3] (rising edge-t [15] edge-triggered flip Wire Load Model 	riggered fli -flop clocke Library NangateO Incr 0.00 0.00 0.00 0.17 0.17 0.03	1.90 ip-flop clocked by clk) ed by clk) OpenCellLibrary Path 0.00 0.00 0.00 0.17 r 0.34 r 0.37 f	
slack (MET) Startpoint: b_r_r Endpoint: out_reg	eg[3] (rising edge-t [15] edge-triggered flip Wire Load Model 	riggered fli -flop clocke Library NangateO Incr 0.00 0.00 0.00 0.17 0.17 0.03 0.08	1.90 Ap-flop clocked by clk) AppenCellLibrary Path	
slack (MET) Startpoint: b_r_r Endpoint: out_reg	eg[3] (rising edge-t [15] edge-triggered flip Wire Load Model 	riggered fli -flop clocke Library NangateO Incr 0.00 0.00 0.00 0.17 0.17 0.03 0.08 0.08	1.90 Ap-flop clocked by clk) AppenCellLibrary Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f 0.45 f 0.54 f	
slack (MET) Startpoint: b_r_r Endpoint: out_reg	eg[3] (rising edge-t :[15] edge-triggered flip Wire Load Model 	riggered fli -flop clocke Library NangateO Incr 0.00 0.00 0.00 0.17 0.17 0.03 0.08 0.08 0.08	1.90 Ap-flop clocked by clk) AppenCellLibrary Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f 0.45 f 0.54 f 0.62 f	
slack (MET) Startpoint: b_r_r Endpoint: out_reg	eg[3] (rising edge-t [15] edge-triggered flip Wire Load Model 	Library Nangate Incr -0.00 0.00 0.17 0.17 0.03 0.08 0.08 0.08 0.08 0.05	1.90 ip-flop clocked by clk) ed by clk) OpenCellLibrary Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f 0.45 f 0.54 f 0.62 f 0.67 r	
slack (MET) Startpoint: b_r_r Endpoint: out_reg	eg[3] (rising edge-t [15] edge-triggered flip Wire Load Model 	Library Nangate Incr -0.00 0.00 0.17 0.17 0.03 0.08 0.08 0.08 0.08 0.08 0.05 0.05	1.90 Ap-flop clocked by clk) AppenCellLibrary Path	
slack (MET) Startpoint: b_r_r Endpoint: out_reg	eg[3] (rising edge-t [15] edge-triggered flip Wire Load Model 	Library Nangate Incr -0.00 0.00 0.17 0.17 0.03 0.08 0.08 0.08 0.08 0.05	1.90 ip-flop clocked by clk) ed by clk) OpenCellLibrary Path 0.00 0.00 0.00 r 0.17 r 0.34 r 0.37 f 0.45 f 0.54 f 0.62 f 0.67 r	
slack (MET) Startpoint: b_r_r Endpoint: out_reg	eg[3] (rising edge-t [15] edge-triggered flip Wire Load Model 	Library Nangate Incr -0.00 0.00 0.17 0.17 0.03 0.08 0.08 0.08 0.08 0.08 0.05 0.05	1.90 Ap-flop clocked by clk) AppenCellLibrary Path	
slack (MET) Startpoint: b_r_r Endpoint: out_reg	eg[3] (rising edge-t [15] edge-triggered flip Wire Load Model 	riggered fli -flop clocke Library NangateO Incr 0.00 0.00 0.17 0.17 0.03 0.08 0.08 0.08 0.08 0.05 0.05 0.07	1.90 Ap-flop clocked by clk) AppenCellLibrary Path	

U1_8/CO (FA_X1)	0.09	1.17 f	
U1_9/C0 (FA_X1)	0.09	1.26 f	
U1_10/CO (FA_X1)	0.09	1.35 f	
U1_11/CO (FA_X1)	0.09	1.44 f	
U1_12/CO (FA_X1)	0.09	1.54 f	
U1_13/CO (FA_X1)	0.09	1.63 f	
U1_14/CO (FA_X1)	0.09	1.72 f	
U1_15/S (FA_X1)	0.13	1.86 r	
out_reg[15]/D (DFF_X1)	0.01	1.87 r	
data arrival time		1.87	
clock clk (rise edge)	4.00	4.00	
clock network delay (ideal)	0.00	4.00	
clock uncertainty	-0.20	3.80	
out_reg[15]/CK (DFF_X1)	0.00	3.80 r	
library setup time	-0.03	3.77	
data required time		3.77	
data required time		3.77	
data arrival time		-1.87	

Part 4
Pipelined block diagram

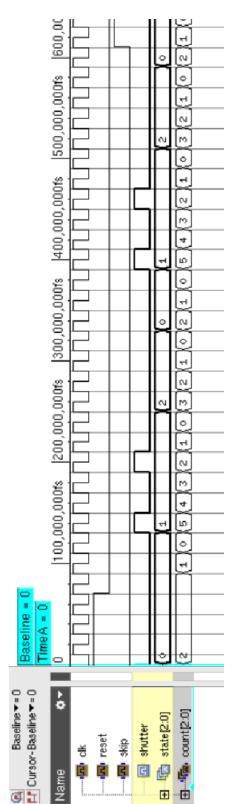


Code for state machine

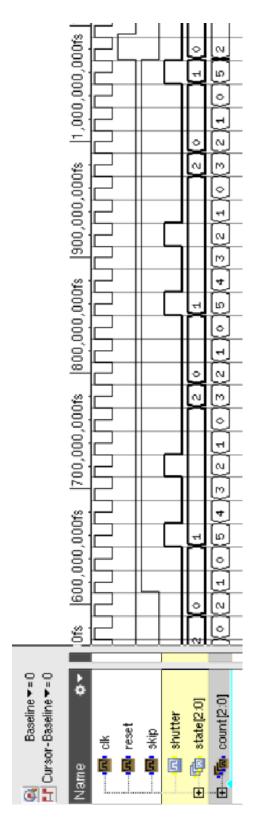
```
//hw2 p4
module machine (
    input reset,
    input clk,
    input skip,
    output reg shutter,
    output reg [2:0] state
);
    parameter IDLE = 2'b00;
    parameter CAMERA_ON = 2'b01;
    parameter PROCESS = 2'b10;
    reg [1:0] state_c;
    reg [2:0] count, count_c;
    reg shutter_c;
    always @(state or count or reset or clk or skip) begin
        //default
        count_c = count;
        state_c = state;
        shutter_c = shutter;
        case(state)
            IDLE: begin
                if (count == 3'b000) begin
                    state_c = CAMERA_ON;
                    count_c = 3'b101; //6 cycles
                    shutter_c = 1'b1;
                end else
                    count_c = count - 3'b001;
            end
            CAMERA_ON: begin
                if (count == 3'b000) begin
                    state_c = PROCESS;
                    count_c = 3'b011; // 4 cycles
                    shutter_c = 1'b0;
                end else begin
                    shutter_c = (count == 3'b011);
                    count_c = count - 3'b001;
                end
            end
            PROCESS: begin
                if (skip == 1'b1 || count == 3'b000) begin
                    state_c = IDLE;
                    count_c = 3'b010;
                end else begin
                    count_c = count - 3'b001;
                end
            end
            default: begin
                count_c = 3'b010;
                state_c = IDLE;
                shutter_c = 1'b0;
            end
        endcase
    end
    always @(posedge clk or posedge reset) begin
        if (reset) begin
            // reset
```

```
count <= #1 3'b010;
    state <= #1 IDLE;
    shutter <= #1 1'b0;
end
else begin
    count <= #1 count_c;
    state <= #1 state_c;
    shutter <= #1 shutter_c;
end
end
end</pre>
```

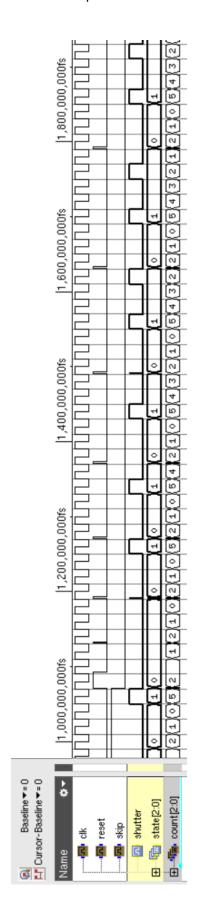
Test waveforms



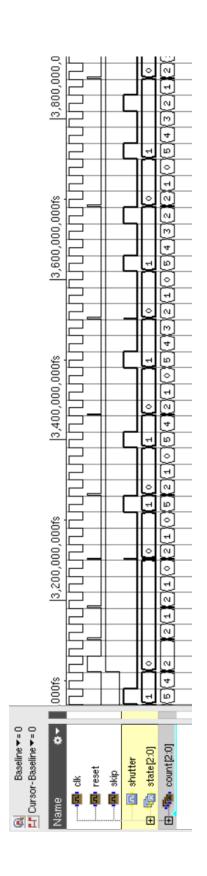
Waveform for normal operation with skip = 0



Waveform for normal operation with skip = 1



Waveform for reset tests with skip = 0



Waveform for reset tests with skip = 1

Code for test bench

```
//testbench for state machine
module test();
    reg clk, reset, skip;
    wire shutter;
    wire [2:0] state;
    integer cycle = 0;
    machine camera (
        .clk (clk),
        .reset (reset),
        .skip (skip),
        .shutter (shutter),
        .state (state)
    );
    initial begin
        $recordfile("machine_test");
        $recordvars(test);
        clk = 1'b0;
        reset = 1'b1;
        skip = 1'b0;
    end
    //clock
    always begin
        #10; //initial begin
        clk = \sim clk;
    end
    //logic
    always @(posedge clk) begin
        cycle <= #1 cycle + 1;</pre>
        case (cycle)
            //start circuit with skip = 0
            3: reset <= #1 1'b0;</pre>
            //skip = 1 on 3rd iteration
            30: skip <= #1 1'b1;
            //testing reset with skip = 0
            53: {reset, skip} <= #1 2'b10;
            53: begin reset <= #1 1'b1; reset <= #3 1'b0; end // @ IDLE 0
            54: begin reset <= #1 1'b1; reset <= #3 1'b0; end // @ IDLE 1
            56: begin reset <= #1 1'b1; reset <= #3 1'b0; end // @ IDLE 2
            59: begin reset <= #1 1'b1; reset <= #3 1'b0; end // @ CAMERA_ON 0
            63: begin reset <= #1 1'b1; reset <= #3 1'b0; end // @ CAMERA_ON 1
            68: begin reset <= #1 1'b1; reset <= #3 1'b0; end // @ CAMERA ON 2
            74: begin reset <= #1 1'b1; reset <= #3 1'b0; end // @ CAMERA ON 3
            81: begin reset <= #1 1'b1; reset <= #3 1'b0; end // @ CAMERA ON 4
            89: begin reset <= #1 1'b1; reset <= #3 1'b0; end // @ CAMERA_ON 5
```

```
98: begin reset <= #1 1'b1; reset <= #3 1'b0; end // @ PROCESS 0
            108: begin reset <= #1 1'b1; reset <= #3 1'b0; end// @ PROCESS 1
            119: begin reset <= #1 1'b1; reset <= #3 1'b0; end// @ PROCESS 2
           131: begin reset <= #1 1'b1; reset <= #3 1'b0; end// @ PROCESS 3
           150: begin reset <= #5 1'b1; reset <= #6 1'b0; end// @ some place in cycle
           //testing reset with skip = 1
           155: {reset, skip} <= #1 2'b11;
           156: reset <= #1 1'b0;
           157: begin reset <= #1 1'b1; reset <= #3 1'b0; end // @ IDLE 1
           159: begin reset <= #1 1'b1; reset <= #3 1'b0; end // @ IDLE 2
           162: begin reset <= #1 1'b1; reset <= #3 1'b0; end // @ CAMERA_ON 0
           166: begin reset <= #1 1'b1; reset <= #3 1'b0; end // @ CAMERA ON 1
           171: begin reset <= #1 1'b1; reset <= #3 1'b0; end // @ CAMERA ON 2
           177: begin reset <= #1 1'b1; reset <= #3 1'b0; end // @ CAMERA_ON 3
           184: begin reset <= #1 1'b1; reset <= #3 1'b0; end // @ CAMERA ON 4
            192: begin reset <= #1 1'b1; reset <= #3 1'b0; end // @ CAMERA_ON 5
           101: begin reset <= #1 1'b1; reset <= #3 1'b0; end // @ PROCESS 0
            211: begin reset <= #1 1'b1; reset <= #3 1'b0; end // @ IDLE 0
           222: begin reset <= #1 1'b1; reset <= #3 1'b0; end // @ IDLE 1
           234: begin reset <= #1 1'b1; reset <= #3 1'b0; end // @ PROCESS 3
           //finish
           238: reset <= #1 1'b1;
       endcase
       //finish simulation
       if (cycle > 240)
           $finish;
   end
endmodule
```