Chapter 1 – Computer Systems Overview

True / False Questions:

1. The operating system acts as an interface between the computer hardware and the human user.
2. One of the processor's main functions is to exchange data with memory.
3. User-visible registers are typically accessible to system programs but are not typically available to application programs.
4. Data registers are general purpose in nature, but may be restricted to specific tasks such as performing floating-point operations.
5. The Program Status Word contains status information in the form of condition codes, which are bits typically set by the programmer as a result of program operation.
6. The processing required for a single instruction on a typical computer system is called the Execute Cycle.
7. A fetched instruction is normally loaded into the Instruction Register (IR).
8. An interrupt is a mechanism used by system modules to signal the processor that normal processing should be temporarily suspended.
9. To accommodate interrupts, an extra fetch cycle is added to the instruction cycle.
10. The minimum information that must be saved before the processor transfers control to the interrupt handler routine is the program status word (PSW) and the location of the current instruction.
11. One approach to dealing with multiple interrupts is to disable all interrupts while an interrupt is being processed.
12. Multiprogramming allows the processor to make use of idle time caused by long-wait interrupt handling.
13. In a two-level memory hierarchy, the Hit Ratio is defined as the fraction of all memory accesses found in the slower memory.
14. Cache memory exploits the principle of locality by providing a small, fast memory between the processor and main memory.
15. In cache memory design, block size refers to the unit of data exchanged between cache and main memory
16. The primary problem with programmed I/O is that the processor must wait for the I/O module to become ready and must repeatedly interrogate the status of the I/O module while waiting.

Multiple Choice Questions:

1. The general role of an operating system is to: B
   a. Act as an interface between various computers
   b. Provide a set of services to system users
   c. Manage files for application programs
   d. None of the above
2. The four main structural elements of a computer system are:
   a. Processor, Registers, I/O Modules & Main Memory
   b. Processor, Registers, Main Memory & System Bus
   c. Processor, Main Memory, I/O Modules & System Bus
   d. None of the above

3. The two basic types of processor registers are:
   a. User-visible and Control/Status registers b. Control and Status registers
   c. User-visible and user-invisible registers d. None of the above
4. Address registers may contain:
   a. Memory addresses of data b. Memory addresses of instructions
   c. Partial memory addresses d. All of the above
5. A Control/Status register that contains the address of the next instruction to be fetched is called the:
   a. Instruction Register (IR) b. Program Counter (PC)
   c. Program Status Word (PSW) d. All of the above
6. The two basic steps used by the processor in instruction processing are:
   a. Fetch and Instruction cycles b. Instruction and Execute cycles
   c. Fetch and Execute cycles d. None of the above
7. A fetched instruction is normally loaded into the:
   a. Instruction Register (IR) b. Program Counter (PC)
   c. Accumulator (AC) d. None of the above
8. A common class of interrupts is:
   a. Program b. Timer c. I/O d. All of the above
9. When an external device becomes ready to be serviced by the processor, the device sends this type of signal to the processor:
   a. Interrupt signal b. Halt signal c. Handler signal d. None of the above
10. Information that must be saved prior to the processor transferring control to the interrupt handler routine includes:
   a. Processor Status Word (PSW)
   b. Processor Status Word (PSW) & Location of next instruction
   c. Processor Status Word (PSW) & Contents of processor registers
   d. None of the above
11. One accepted method of dealing with multiple interrupts is to:
   a. Define priorities for the interrupts
   b. Disable all interrupts except those of highest priority
   c. Service them in round-robin fashion
   d. None of the above
12. In a uniprocessor system, multiprogramming increases processor efficiency by:
   a. Increasing processor speed
   b. Taking advantage of time wasted by long wait interrupt handling
   c. Eliminating all idle processor cycles
   d. All of the above
13. As one proceeds down the memory hierarchy (i.e., from inboard memory to offline storage), the following condition(s) apply:
   a. Increasing cost per bit b. Decreasing capacity
   c. Increasing access time d. All of the above
14. Small, fast memory located between the processor and main memory is called:
   a. WORM memory b. Cache memory
   c. CD-RW memory d. None of the above
15. When a new block of data is written into cache memory, the following determines which cache location the block will occupy:

a. Block size b. Cache size c. Write policy d. None of the above

16. Direct Memory Access (DMA) operations require the following information from the processor:
    a. Address of I/O device b. Starting memory location to read from or write to
    c. Number of words to be read or written d. All of the above

Fill-In-The-Blank Questions:

1. An operating system exploits the hardware resources of one or more processors to provide a set of services to _____.
2. Each location in Main Memory contains a _____字_____ that can be interpreted as either an instruction or data.
3. Registers that are used by system programs to minimize main memory references by optimizing register use are called _____寄存器_____.
4. A special type of address register, required by a system that implements user-visible stack addressing, is called a _____栈指针_____.
5. The _____指令寄存器_____ contains the most recently fetched instruction.
6. The processing required for a single instruction is called a(n) _____指令_____ cycle.
7. A fetched instruction is normally loaded into the _____指令寄存器_____.
8. An arithmetic overflow condition resulting from some instructional execution will generate a(n) _____ interrupt.
9. To accommodate interrupts, a(n)_____基本指令周期_____ is added to the basic instruction cycle.
10. The _____程序计数器_____ is part of the information that must be saved prior to the processor transferring control to the interrupt handler routine, and it tells the processor where to return control to the previously interrupted program
11. A drawback to the disable interrupt strategy of dealing with multiple interrupts is that it doesn't account for _____.
12. The concept of multiple programs taking turns in execution is known as _____多道程序设计_____.
13. The memory design dilemma (regarding cost vs. capacity vs. access time) is solved by employing a(n) _____层次存储器_____.
14. _____缓存存储器_____ exploits the principle of locality by providing a small, fast memory between the processor and main memory.
15. The _____替换策略_____ chooses, within the constraints of the mapping function, which block to replace when a new block is to be loaded and all cache slots are already filled.
16. Interrupt-driven I/O, although more efficient than simple Programmed I/O, still requires the use of the _____直接存储器_____ to transfer data between memory and an I/O module.