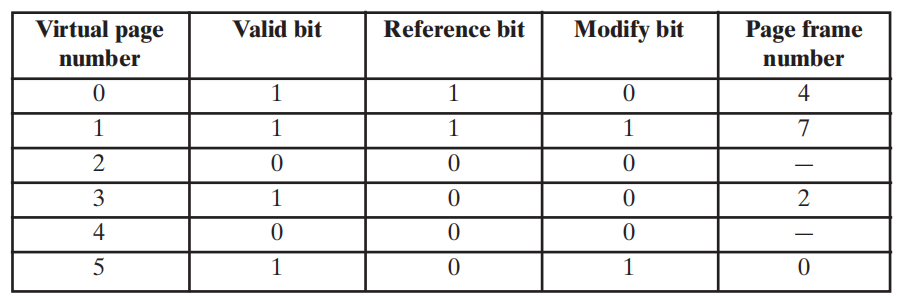
**第八章作业**

**（6月16日（周二）21:00提交）**

**1.** Suppose the page table for the process currently executing on the processor looks like the following. All numbers are decimal, everything is numbered starting from zero, and all addresses are memory byte addresses. The page size is 1024 bytes.



**a.** Describe exactly how, in general, a virtual address generated by the CPU is translated into a physical main memory address.

**b.** What physical address, if any, would each of the following virtual addresses correspond to? (Do not try to handle any page faults, if any.)

**(i)** 1052

**(ii)** 2221

**(iii)** 5499

**2.** Consider a paged virtual memory system with 32-bit virtual addresses and 1K-byte pages. Each page table entry requires 32 bits. It is desired to limit the page table size to one page.

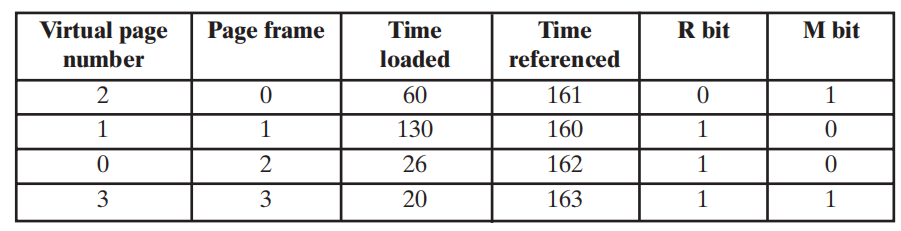
**a.** How many levels of page tables are required?

**b.** What is the size of the page table at each level? Hint: One page table size is smaller.

**c.** The smaller page size could be used at the top level or the bottom level of the page table hierarchy. Which strategy consumes the least number of pages?

**3.** A process has four page frames allocated to it. (All the following numbers are decimal, and everything is numbered starting from zero). The time of the last loading of a page into each page frame, the time of last access to the page in each page frame, the virtual page number in each page frame, and the referenced (R) and modified (M)

bits for each page frame are as shown (the times are in clock ticks from the process start at time 0 to the event — not the number of ticks since the event to the present).



A page fault to virtual page 4 has occurred at time 164.Which page frame will have its contents replaced for each of the following memory management policies? Explain why in each case.

**a.** FIFO (first-in-first-out)

**b.** LRU (least recently used)

**c.** Clock

**d.** Optimal (Use the following reference string.)

**e.** Given the aforementioned state of memory just before the page fault, consider the following virtual page reference string:

4, 0, 0, 0, 2, 4, 2, 1, 0, 3, 2

How many page faults would occur if the working set policy with LRU were used with a window size of 4 instead of a fixed allocation? Show clearly when each page fault would occur.

**4.** four page frames in main memory. The following page trace occurs:

1, 0, 2, 2, 1, 7, 6, 7, 0, 1, 2, 0, 3, 0, 4, 5, 1, 5, 2, 4, 5, 6, 7, 6, 7, 2, 4, 2, 7, 3, 3, 2, 3

**a.** Show the successive pages residing in the four frames using the LRU replacement policy. Compute the hit ratio in main memory.Assume that the frames are initially empty.

**b.** Repeat part (a) for the FIFO replacement policy.

**c.** Compare the two hit ratios and comment on the effectiveness of using FIFO to approximate LRU with respect to this particular trace.

**5.** Assuming a page size of 4 Kbytes and that a page table entry takes 4 bytes, how many levels of page tables would be required to map a 64-bit address space, if the top level page table fits into a single page?

**6.** Assume that a task is divided into four equal-sized segments and that the system builds an eight-entry page descriptor table for each segment. Thus, the system has a combination of segmentation and paging. Assume also that the page size is 2 Kbytes.

**a.** What is the maximum size of each segment?

**b.** What is the maximum logical address space for the task?

**c.** Assume that an element in physical location 00021ABC is accessed by this task.

What is the format of the logical address that the task generates for it? What is the maximum physical address space for the system?

**7.** Consider a paged logical address space (composed of 32 pages of 2 Kbytes each) mapped into a 1-Mbyte physical memory space.

**a.** What is the format of the processor’s logical address?

**b.** What is the length and width of the page table (disregarding the “access rights”bits)?

**c.** What is the effect on the page table if the physical memory space is reduced by half?