Maxence Bouvier, PhD

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I discovered AI's potential six years ago at IBM, inspiring my Ph.D. studies to build energy-efficient machine learning vision systems. At Sony, I have been working on multimodel transformer models for low power vision systems. I supervised many successful internship projects which helped me patent several ideas. I'm now eager to create AI solutions that can impact millions.

EXPERIENCE

- **SONY** Zurich, Switzerland

  Senior AI Research Engineer *Aug 2023 - Present*
  - **Sparsity Exploitation in Transformers**
    - Engineered an asynchronous PointNet-based embedding, enabling continuous spatio-temporal data conversion into dense tensors for seamless, ongoing feeding of Transformer models - (*1 paper, 1 patent.*)
    - Designed a NPU-adapted sparse scaled-dot-product-attention per-block module for highly efficient sparse attention in Transformers, achieving moer than 50% FLOPs reduction during inference and higher accuracy.
  - **SLAM Enhanced AI Training**: Enhanced performance by incorporating a cutting-edge SLAM pipeline for multi-modal training process, achieving 6x faster model convergence and a 15% boost in accuracy.

  AI Research Engineer *June 2022 - Aug 2023*
  - **SW/HW Co-Design Automation with Neural Architecture Search**
    - Built an AI-driven, Hardware-Aware Neural Architecture Search framework. Enabled to automatically reduce model to 8% FLOP cost while losing only 4% relative accuracy.
    - Integrated a Design Space Exploration software in thas NAS to estimate energy and latency of model execution.
  - **Transformer Hardware Acceleration Survey**: Conducted a Transformer acceleration study, guiding Sony's AI advancements; featured in CTO's strategic report.
  - **SW/HW Co-Design Automation with Neural Architecture Search**
    - Implemented an AI model leveraging CNN and Transformer architectures to enhance video sequence continuity through advanced frame generation. - (*1 patent.*)
    - Built a live demo of the model, from image sensor to application. This led to 2 major collaborations with other teams.
    - Converted to the model as an API to simplify sharing across teams and projects.

- **STMicroelectronics** Grenoble, France

  Hardware Design Engineer *Apr 2021 - May 2023*
  - **CPU Deisgn and Automation**
    - Created a toolbox to automate component assembly of the Trace and Debug subsystem with ARM's Armv9-A SoC modules.
    - Developed an RTL generator for STM32 MPU SoC, streamline the design of a multi-clock domain reset and clock control for over 300 peripherals.
  - **CPU Benchmarking**: Conducted CoreMark benchmarking on a multi-core MPU SoC, highlighting significant performance gains (up to 6x) through compiler updates.

- **CEA LETI** Grenoble, France

  Doctoral Researcher on AI and Hardware Design *Apr 2018 - Apr 2021*
  - **Neuromorphic Hardware Analysis**: Conducted a comprehensive bibliographic study on scalable, multi-chip, distributed neuromorphic hardware, leading to a widely cited publication in ACM JETC. - (*1 paper*.)
  - **ULP IC Design for Sparse AI Acceleration**: Built a 28nm FDSOI ultra-low power sparse AI accelerator, setting energy efficiency records and enabling seamless Event-Based pixel grid integration. - (*1 paper, 2 patents.*)
  - **EB VIO/SLAM Pipeline and Object Detection Innovation**: Developed an Event-Based VIO/SLAM pipeline with ego-motion compensation, leading to a patent and a solution for moving objects detection. - (*1 patent.*)

- **IBM Research** Yorktown Heights, NY, USA

  Intern Hardware Engineer *Feb 2017 - Aug 2017*
  - Automated wafer-scale memory device characterization, reducing execution time from days to hours.
  - Contributed to the optimization of PCM technologies for Compute-in-Memory-based AI accelerarion. - (*1 paper, 1 patent.*)

SKILLS

- **Languages**: Python, C, C++, SystemVerilog, VHDL, MATLAB, LaTeX
- **Libraries**: PyTorch, ONNX, Numpy, Pandas, ROS, OpenCV
- **Softwares**: Git, VScode, EDA (Cadence, Synopsys, Mentor), PowerPoint Expert

EDUCATION

- **Grenoble Alpes University** | *Ph.D. in Computer Science* *Apr 2018 – Apr 2021* | Grenoble, France
- **EPFL** | *"M.Eng. in Electronics (Highest Honors)"* *Sep 2015 – Sep 2017* | Lausanne, Switzerland
- **Grenoble Institute of Technology** | *B.Eng. in Electronics* *Sep 2012 – Sep 2015* | Grenoble, France