Maxence Bouvier

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Experience

- **Sony** — Zurich, Switzerland

  Senior AI Research Engineer — *Aug 2023 - Present*

  - **Sparsity Exploitation in Transformers**
    - Engineered an asynchronous PointNet-based embedding, enabling continuous spatio-temporal data conversion into dense tensors for seamless, ongoing feeding of Transformer models - *Publication (WIP).*
    - Designed a NPU-adapted sparse scaled-dot-product-attention per-block module for highly efficient sparse attention in Transformers, achieving moer than 50% FLOPs reduction during inference and higher accuracy.
  - **SLAM Enhanced AI Training**: Optimized the training pipeline by integrating a state-of-the-art SLAM pipeline with ego-motion compensation, leading to 6x faster model convergence and a 15% increase in accuracy.

  AI Research Engineer — *June 2022 - Aug 2023*

  - **SW/HW Co-Design Automation with Neural Architecture Search**
    - Built an AI-driven, Hardware-Aware Neural Architecture Search framework. Enabled to automatically reduce model to 8% FLOP cost while losing only 4% relative accuracy.
    - Integrated a Design Space Exploration software in thas NAS to estimate energy and latency of model execution.
  - **Transformer Hardware Acceleration Survey**: Conducted a Transformer acceleration study, guiding Sony's AI advancements; featured in CTO's strategic report. - (Attended ISSCC23)
  - **Vision Transformer Design**: Implemented an AI model leveraging CNN and Transformer architectures to enhance video sequence continuity through advanced frame generation. *(1 patent).*

- **STMicroelectronics** — Grenoble, France

  Hardware Design Engineer — *Apr 2021 - May 2023*

  - **CPU Design**: Built Trace and Debug subsystem for ARM's Armv9-A SoC from scratch and created a Python library for automated component assembly.
  - **Reset and Clock Controller Generator**: Developed an RTL generator for STM32 MPU SoC, automating multi-clock domain reset and clock control for over 300 peripherals.
  - **CPU Benchmarking**: Conducted CoreMark benchmarking on a multi-core MPU SoC, highlighting significant performance gains (up to 6x) through compiler updates.

- **CEA LETI** — Grenoble, France

  Doctoral Researcher on AI and Hardware Design — *Apr 2018 - Apr 2021*

  - **Neuromorphic Hardware Analysis**: Conducted a comprehensive bibliographic study on scalable, multi-chip, distributed neuromorphic hardware, leading to a widely cited survey in ACM JETC.
  - **ULP IC Design for Neuromorphic Acceleration**: Built a 28nm FDSOI ultra-low power neuromorphic accelerator, setting energy efficiency records and enabling seamless EB pixel grid integration. *(1 paper, 2 patents.)*
  - **EB VIO/SLAM Pipeline and Object Detection Innovation**: Developed an Event-Based VIO/SLAM pipeline with ego-motion compensation, leading to a patent and improved perception accuracy. - *1 patent.*

- **IBM Research** — Yorktown Heights, NY, USA

  Intern Hardware Engineer — *Feb 2017 - Aug 2017*

  - Automated wafer-scale memory device characterization, reducing execution time from days to hours.
  - Contributed to the optimization of PCM technologies for Compute-in-Memory AI accelerarion. - *1 paper, 1 patent.*

Programming Skills

- **Languages**: Python, C, C++, SystemVerilog, VHDL, MATLAB
- **Technologies**: PyTorch, ONNX, ROS, Xilinx FPGAs,
- **Tools**: Git, VScode, EDA (Cadence, Synopsys, Mentor), LaTeX

Education

- **Grenoble Alpes University** — *Ph.D. in Computer Science* — *Apr 2018 – Apr 2021* — Grenoble, France
- **EPFL** — *"M.Eng. in Electronics (Highest Honors)"* — *Sep 2015 – Sep 2017* — Lausanne, Switzerland
- **Grenoble Institute of Technology** — *B.Eng. in Electronics* — *Sep 2015 – Sep 2017* — Grenoble, France