

Maxence Bouvier, PhD

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I discovered AI's potential six years ago at IBM, inspiring my Ph.D. studies to build energy-efficient machine learning vision systems. At Sony, I have been leading a project on multimodal transformer models for low power vision systems. I mentored many successful students during their thesis and internships, which helped me patent several ideas. I'm now eager to create AI solutions that will impact millions.

EXPERIENCE

• SONY

Senior AI Research Engineer

Zurich, Switzerland

Aug 2023 - Present

◦ Sparsity Exploitation in Transformers

- * Engineered an asynchronous PointNet-based embedding, enabling continuous spatio-temporal data conversion into dense tensors for seamless, ongoing feeding of Transformer models - (*1 paper, 1 patent.*)
- * Designed an NPU-compatible sparse scaled-dot-product-attention per-block module for highly efficient sparse attention in Transformers, achieving more than 50% FLOPs reduction during inference and higher accuracy.

◦ SLAM Enhanced AI Training:

Enhanced performance by incorporating a cutting-edge SLAM pipeline for multi-modal training process, achieving 6x faster model convergence and a 15% boost in accuracy.

AI Research Engineer

June 2022 - Aug 2023

◦ SW/HW Co-Design Automation with Neural Architecture Search

- * Built an AI-driven, Hardware-Aware Neural Architecture Search framework. Enabled to automatically reduce model to 8% FLOP cost while losing only 4% relative accuracy.

- * Integrated a Design Space Exploration software in the NAS loop to estimate energy and latency of model execution.

◦ Transformer Hardware Acceleration Survey:

Conducted a literature study, featured in CTO's strategic report.

◦ Vision Transformer for Image Generation

- * Implemented an AI model leveraging CNN and Transformer architectures to realize advanced frame generation. - (*1 patent.*)

- * Built a live demo of the model, from image sensor to application. This led to 2 major collaborations with other teams.

- * Converted the model as an API to simplify sharing across teams and projects.

◦ Software Maintainer:

Responsible for the CI of a few Python libraries shared among teams.

• STMicroelectronics

Hardware Design Engineer

Grenoble, France

Apr 2021 - May 2023

◦ CPU Design and Automation

- * Created a toolbox to automate component assembly of the Trace and Debug subsystem with ARM's Armv9-A SoC modules.
- * Developed an RTL generator for STM32 MPU SoC, streamlining the design of a multi-clock domain reset and clock control for over 300 peripherals.

◦ CPU Benchmarking:

Conducted CoreMark benchmarking on a multi-core MPU SoC, highlighting significant performance gains (up to 6x) through compiler updates.

• CEA LETI

Doctoral Researcher on AI and Hardware Design

Grenoble, France

Apr 2018 - Apr 2021

◦ Neuromorphic Hardware Analysis:

Conducted a comprehensive bibliographic study on scalable, multi-chip, distributed neuromorphic hardware, leading to a widely cited publication in ACM JETC. - (*1 paper.*)

◦ ULP NPU Design:

Built (RTL design, synthesis and layout) an ultra-low power sparse AI accelerator, setting energy efficiency records (2.86pJ/OP in 28nm) and enabling seamless integration for 3D-stacked imagers. - (*1 paper, 2 patents.*)

◦ EB VIO/SLAM Pipeline and Object Detection Innovation:

Developed an Event-Based VIO/SLAM pipeline with ego-motion compensation, leading to a solution for detecting moving objects. - (*1 patent.*)

• IBM Research

Intern Hardware Engineer

Yorktown Heights, NY, USA

Feb 2017 - Aug 2017

- Automated wafer-scale memory device characterization, reducing execution time from days to hours.

- Contributed to the optimization of PCM technologies for Compute-in-Memory-based AI acceleration. - (*1 paper, 1 patent.*)

SKILLS

• Languages:

Python, C, C++, MATLAB, SystemVerilog, VHDL, LaTeX

• Libraries:

PyTorch, ONNX, Numpy, Pandas, ROS, OpenCV

• Softwares:

Git, GitLab CI, EDA (Cadence, Synopsys, Mentor), VSCode, PowerPoint Expert

EDUCATION

• Grenoble Alpes University | *Ph.D. in Computer Science*

Apr 2018 – Apr 2021 | Grenoble, France

• EPFL | *"M.Eng. in Electronics (Highest Honors)"*

Sep 2015 – Sep 2017 | Lausanne, Switzerland

• Grenoble Institute of Technology | *B.Eng. in Electronics*

Sep 2012 – Sep 2015 | Grenoble, France