NOTES:

Initial Design 1/23/2020

Preliminary Design Review 1/24/2020

1. AI85 references scrubbed from design, replaced with MAX78000

2. SIMO and power decoupling modified per Tom Maguire's guidance

3. Confirmed GPIO secondary functions may be assigned on a pin by pin basis

4. Confirmed GPIO is set to input tri-state post reset, VDDIO as source voltage

5. Confirmed Port 3 is a three volt VDDIOH interface only

6. Reset and Port 3.01 to be pulled to 3V, must be allowed to float freely to 3V regardless of power status of any connected peripherals

7. Added debounced PB to WAKEUP port 3.01

8. Touch screen confirmed as required

9. LCD screen does not have to match that of demo kit, would be nice if it did

10. Gokhan to provide connections to integrate power monitor module: one channel to measure DUT drain and one on CNN core

11. Add jumper blocks to all non connectorized peripherals to allow probing, experimentation and substitution of other parts

12. Provisions for canned 3.072 MHz OSC and ext OSC input to feed I2S ext clock

Post initial review 1/31/2020

1. Decision made to investigate alternative power measurement scheme

2. Designed solution around MAX34417 power accumulator

3. MAX32625 selected for display drive and USB data out

Final review 2/10/2020

1. Divorced global reset from RISC V JTAG with jumper

2. Divorced global reset from 625 power metering processor

3. Deleted program button from 625

4. Deleted two navigation buttons from 625

5. Swapped VREGI C6 and C9 on schematic symbol

Design updates 2/19/2020

1. Added BOOST LDO to meet demands of CNN core peak loads

2. Added FET switch to BOOST LDO voltage divider to eliminate voltage divider drain when LDO not required

3. Four ADC channels revert to GPIO in order to control BOOST LDO

4. Spare GPIO P24 routed to same header used for P30, P31

Design updates 2/25/2020

1. Removed differential filter option from ADC inputs

2. Replaced DUT symbol with version matching datasheet VREGI nomenclature

3. Updated VREGI jumper labels to reflect DUT schematic symbol

Revision B 4/28/2020

1. Removed unwanted DNI tags from cut n paste ME11 elements

2. Redesigned reset circuit to compensate for SWD and RSTN on different default voltage domains

Revision B continued 5/08/2020

1. User notes added to CNN boost circuit block

2. Added USB-QSPI interface to drive photo images directly into onboard flash

3. Camera must be unplugged for direct photo load

Revision B continued 5/19/2020

1. I2S OSC changed to 12.288 MHz

2. Be aware that DUT sch symbol shall change to match chip datasheet as soon as that info is provided to me

Revision B continued 5/21/2020

1. Replace CNN booster LDO with buck regulator

2. Accumulator filter changes pending

Revision B continued 5/22/2020

1. Updated block diagram

2. Updated power monitor filter topology

3. Added jumper to break 3v3 input to DUT for current measurement

4. CNN power boost voltage set to 1v2 volts (reverts to 1v1 for later silicon)

Revision C continued 7/08/2020

1. TFT display reset line now driven by p0.19

2. 4 wire option removed from TFT panel

3. Bus switch added to isolate camera and USB SPI bridge

4. x

STANDOFF HOLES

H1 DNI
H2 DNI
H3 DNI
H4 DNI
H5 DNI
H6 DNI
H7 DNI

STANDOFF HARDWARE

BMP1 RB Bump
BMP2 RB Bump
BMP5 RB Bump
BMP7 RB Bump
BMP3 RB Bump
BMP4 RB Bump
BMP6 RB Bump

MST1 STANDOFF
MST2 STANDOFF
MS1 Screw Steel
MS2 Screw Steel
MST3 STANDOFF
MST4 STANDOFF
MS3 Screw Steel
MS4 Screw Steel
MST5 STANDOFF
MST6 STANDOFF
MS5 Screw Steel
MS6 Screw Steel
MST7 STANDOFF
MS7 Screw Steel

PCB1
PCB-00170-C-0

GND BLK TP1
GND BLK TP2
GND BLK TP3
GND BLK TP4

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Title: MAX78000 EV KIT - Notes

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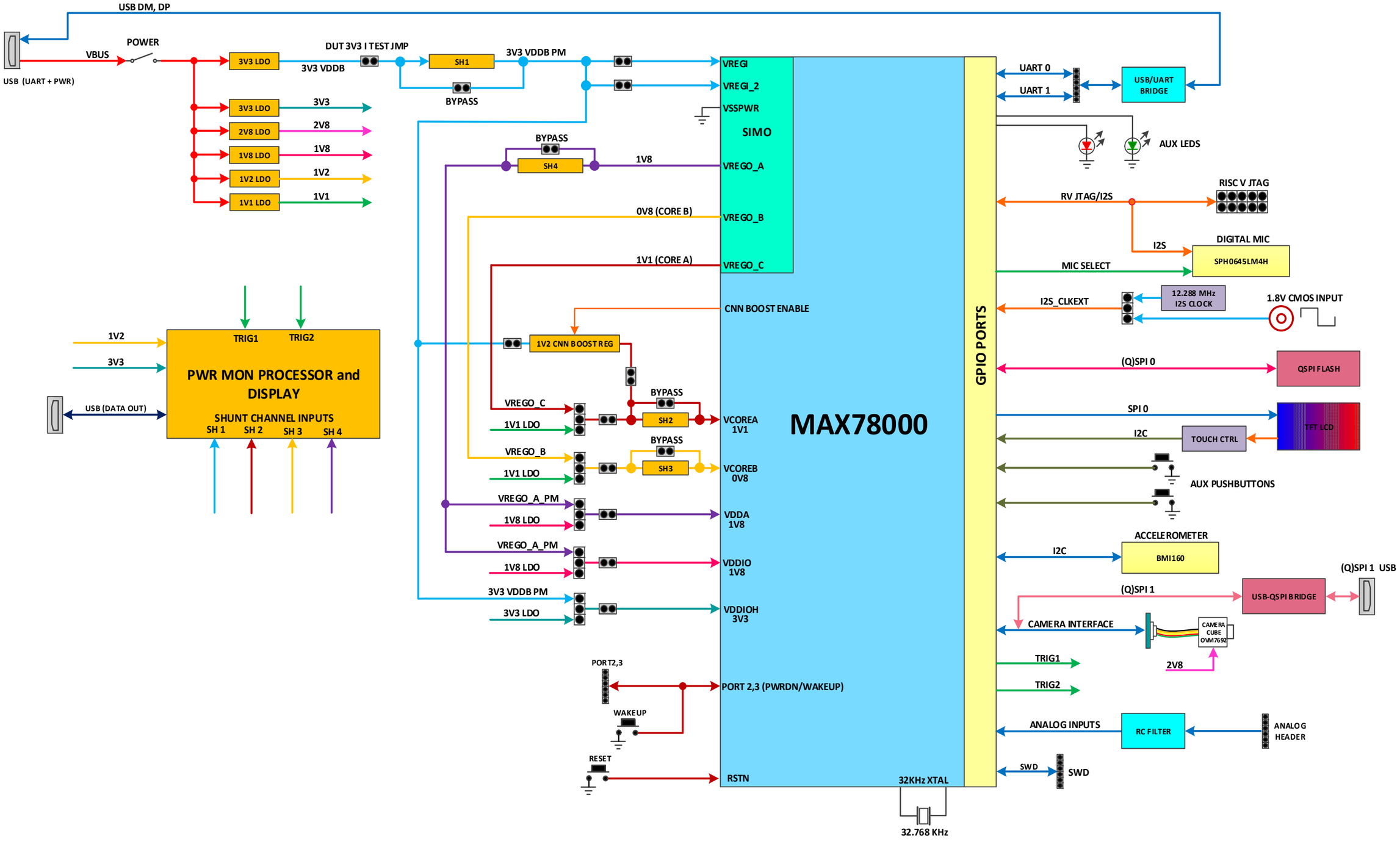

Title: MAX78000 EV KIT - Block Diagram

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Components inside dashed box should be placed as close to the USB connector as practical.

USB/PWR

CN1
47346-0001
VBUS DM DP ID GND GND_4 GND_3 GND_2 GND_1

L1
BLM41PG102SN1L
1806 1500mA

90 ohm differential traces

C1 1uF 0603

C3 100nF 0603

U4
MAX13202EALT+T
VCC GND NC_1 NC_2 IO1 IO2

SW1
SPDT 3A
PWR
OFF ON

5V0
TP5
BLUE

R7
2.7K

D3
BLUE
5V IN

R6 27
R5 27
USBDM0
USBDP0

C4 47pF
C5 47pF

USB <--> UART

U3
FT230XS-R
VCCIO VCC USBDM USBDP
TXD RXD RTS CTS
CBUS0 CBUS1 CBUS2 CBUS3
RESET
3V3OUT
GND GND

C6 100nF 0402
C8 100nF 0402

UART 0 EN

JH1
P0_2 P0_3 P0_0 P0_1
UART0_CTS UART0_RTS UART0_RX UART0_TX
P0_2 P0_3 P0_0 P0_1

UART 1 EN

JH2
P0_12 P0_13
UART1_RX UART1_TX
P0_12 P0_13

OPEN DRAIN LED BUFFER

U2
NL27WZ07DFT2G
A1 A2 GND Y1 Y2 VCC

JP1 LED1 EN
JP2 LED2 EN

R2 100K
R3 100K

C2 100nF 0402

AUXILIARY LEDS

3V3_LDO

LED1
D1 GRN R1 332

LED2
D2 RED R4 470

OPEN DRAIN TASK TRIGGER BUFFER

U5
NL27WZ07DFT2G
A1 A2 GND Y1 Y2 VCC

JP3 TRIG1
JP4 TRIG2
TRIG1 TRIG2
625_P0_2 625_P0_3

C9 100nF 0402

3V3 VDDB (DUT)

U6
MAX8869EUE33
IN_1 IN_2 IN_3 IN_4 OUT_4 OUT_3 OUT_2 OUT_1 RSTOUT SHDN SS SET GND NC1 NC2 NC3 EP

C12 1uF 0402
C10 1uF 0402

JP21
DUT I
3V3_VDDB

1V8 LDO

U7
MAX8869EUE18+
IN_1 IN_2 IN_3 IN_4 OUT_4 OUT_3 OUT_2 OUT_1 RSTOUT SHDN SS SET GND NC1 NC2 NC3 EP

C11 1uF 0402
C13 1uF 0402
1V8_LDO

3V3 LDO (AUX)

U8
MAX8869EUE33
IN_1 IN_2 IN_3 IN_4 OUT_4 OUT_3 OUT_2 OUT_1 RSTOUT SHDN SS SET GND NC1 NC2 NC3 EP

C14 1uF 0402
C16 1uF 0402
3V3_LDO

1V2 LDO (625 CORE)

U9
MAX38902AATA+
IN GND EP EN SELA OUT BYP OUTS SELB

C15 4.7uF 0603
C18 10nF 0402
C17 4.7uF 0603
1V2_LDO

2V8 LDO (CAMERA ANALOG VDD)

U10
MAX8902BATA+T
IN EN POK EP OUT BYP FB GS GND

C21 10uF 0805
C20 10nF 0402
C19 10uF 0805
R9 30K
R11 8.2K
2V8_LN

1V1 LDO

U11
MAX8869EUE33
IN_1 IN_2 IN_3 IN_4 OUT_4 OUT_3 OUT_2 OUT_1 RSTOUT SHDN SS SET GND NC1 NC2 NC3 EP

C22 1uF 0402
R10 3.32K
R12 10K
C23 1uF 0402
1V1_LDO

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Title: MAX78000 EV KIT - PWR Conditioning, UART Bridge, AUX LEDs

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DUT

XU1
MAX78000EXG+ 81P BGA SOCKET

P0_0	UART0_RX	J9	P0.0/UART0A_RX
P0_1	UART0_TX	H9	P0.1/UART0A_TX
P0_2	UART0_CTS	J8	P0.2/TMR0A__IOA/UART0B_CTS
P0_3	UART0_RTS	H8	P0.3/EXT_CLK/TMR0A_IOB/UART0B_RTS
P0_4	QSPI0_SS0	J7	P0.4/SPI0_SS0/TMR0B_IOAN
P0_5	QSPI0_MOSI	H7	P0.5/SPI0_MOSI/TMR0B_IOBN
P0_6	QSPI0_MISO	G7	P0.6/SPI0_MISO/OWM_IO
P0_7	QSPI0_SCK	H6	P0.7/SPI0_SCK/OWM_PE
P0_8	QSPI0_SDIO2	G6	P0.8/SPI0_SDIO2/TMR0B_IOA
P0_9	QSPI0_SDIO3	F6	P0.9/SPI0_SDIO3/TMR0B_IOB
P0_10	QSPI0_SS2	E6	P0.10/I2C0_SCL/SPI0_SS2
P0_11	QSPI0_SS1	D6	P0.11/I2C0_SDA/SPI0_SS1
P0_12	UART1_RX	H5	P0.12/UART1A_RX/TMR1B_IOAN
P0_13	UART1_TX	G5	P0.13/UART1A_TX/TMR1B_IOBN
P0_14	I2S_CLKEXT	F5	P0.14/TMR1A_IOA/I2S_CLKEXT
P0_15	PCIF_VSYNC	E5	P0.15/TMR1A_IOB/PCIF_VSYNC
P0_16	TS_BUSY	D5	P0.16/I2C1_SCL/PT2
P0_17	TS_PENIRQ	H4	P0.17/I2C1_SDA/PT3
P0_18	PCIF_XVCLK	G4	P0.18/PT0/OWM_IO
P0_19	DISP_RS_DC	F4	P0.19/PT1/OWM_PE
P0_20	PCIF_IO0	E4	P0.20/SPI1_SS0/PCIF_D0
P0_21	PCIF_IO1	D4	P0.21/SPI1_MOSI/PCIF_D1
P0_22	PCIF_IO2	J3	P0.22/SPI1_MISO/PCIF_D2
P0_23	PCIF_IO3	H3	P0.23/SPI1_SCK/PCIF_D3
P0_24	PCIF_IO4	G3	P0.24/SPI1_SDIO2/PCIF_D4
P0_25	PCIF_IO5	F3	P0.25/SPI1_SDIO3/PCIF_D5
P0_26	PCIF_IO6	E3	P0.26/TMR2A_IOA/PCIF_D6
P0_27	PCIF_IO7	J2	P0.27/TMR2A_IOB/PCIF_D7
P0_28	SWDIO	H2	P0.28/SWDIO
P0_29	SWCLK	J1	P0.29/SWCLK
P0_30	I2C2_SCL	H1	P0.30/I2C2_SCL/PCIF_D8
P0_31	I2C2_SDA	G2	P0.31/I2C2_SDA/PCIF_D9
P1_0	RV_TCK	G1	P1.0/UART2A_RX/RV_TCK
P1_1	RV_TMS	F1	P1.1/UART2A_TX/RV_TMS
P1_2	RV_TDI	F2	P1.2/I2S_SCK/RV_TDI
P1_3	RV_TDO	E2	P1.3/I2S_WS/RV_TDO
P1_4	I2S_SDI	D2	P1.4/I2S_SDI/TMR3B_IOA
P1_5	GYRO_IRQ1	D3	P1.5/I2S_SDO/TMR3B_IOB
P1_6	GYRO_IRQ2	B1	P1.6/TMR3A_IOA/PCIF_D10
P1_7	MIC-JTAG_B	C2	P1.7/TMR3A_IOB/PCIF_D11
P1_8	PCIF_HSYNC	A2	P1.8/PCIF_HSYNC/RXEV0
P1_9	PCIF_XCLK	B2	P1.9/PCIF_PCLK/TXEV0
P2_0	AIN0	D7	P2.0/AIN0/AINON
P2_1	AIN1	E8	P2.1/AIN1/AIN0P
P2_2	AIN2	E7	P2.2/AIN2/AIN1N
P2_3	AIN3	F9	P2.3/AIN3/AIN1P
P2_4		F8	P2.4/AIN4/AIN2N/LPTMR0B_IOA
P2_5		F7	P2.5/AIN5/AIN2P/LPTMR1_IOA
P2_6		G8	P2.6/LPTMR0_CLK/AIN6/AIN3N/LPUARTB_RX
P2_7		G9	P2.7/LPTMR1_CLK/AIN7/AIN3P/LPUARTB_TX
P3_0		C3	P3.0/PDOWN/WAKEUP
P3_1		B3	P3.1/SQWOUT/WAKEUP

C52 DNI 0402 — Y1 32.768kHz — C57 DNI 0402
B5 32KIN, A5 32KOUT
DUT_3V3_RSTN — B4 RSTN
81BHC80A01

U1
MAX78000EXG+
81P CTBGA

VREGI

TP6 RED

VREGI	C9	JP5 1–2	VREGI
VREGI	C6	JP6 1–2	VREGIA
		JP7 2–1	3V3_VDDB_PM, CNN BOOST
VSSPWR	A9	C24 1uF 0402	C25 47uF 0805
		C26 47uF 0805 DNI	

LXA B9 — L2 2.2uH 0805
LXB A8 — C27 3.3nF 0402
VBST C8

VREGO_A	B8	VREGO_A
VREGO_B	A7	VREGO_B
VREGO_C	B7	VREGO_C

C29 22uF 0603 DNI; C30 22uF 0603; C31 22uF 0603; C32 22uF 0603

VCOREA	D9	VCOREA_PM
VCOREA	E1	

C36 100nF 0201; C37 100nF 0201; C38 1uF 0402; C39 1uF 0402

VCOREB D8 — VCOREB_PM
C43 100nF 0201; C45 1uF 0402

VDDA C7 — VDDA
C47 100nF 0201; C48 1uF 0402
VSSA B6

VDDIOH	J4	VDDIOH
VDDIOH	A3	
VDDIOH	C1	

C53 100nF 0201; C54 100nF 0201; C55 1uF 0402

VDDIO	J5	VDDIO
VDDIO	A4	
VDDIO	D1	

C59 100nF 0201; C60 100nF 0201; C61 1uF 0402

VSS	A1	
VSS	C4	
VSS	C5	
VSS	A6	
VSS	J6	
VSS	E9	

1V2 CNN Power Boost

L5 2.2uH
U30
MAX38642AENT+
A2 LX — OUT B2
A1 IN — RSEL/NC B3
B1 EN — GND A3
6P WLP

C34 100uF; C35 22uF 0603
P2_5 BOOST
C40 22uF 0603; C50 22uF 0603
R17 383K

PWR TEST MATRIX

VREGO_A_PM	JP8	VDDA	1V8_LDO
VREGO_A_PM	JP9	VDDIO	1V8_LDO
3V3_VDDB_PM	JP10	VDDIOH	3V3_LDO
VREGO_B	JP11	VCOREB	1V1_LDO
VREGO_C	JP12	VCOREA	1V1_LDO

(INT / EXT)

POWER ACCUMULATOR

3V3_VDDB — R13 33.2 0603 — C28 4.7uF 0603
VREGI PM BYPASS — JP13 — R14 100 mOhms 1206 — 3V3_VDDB_PM

JP14 2–1 CNN 1V2 — VCOREA
VCOREA PM BYPASS — JP15 — R16 33.2 0603 — R18 100 mOhms 1206 — C41 4.7uF 0603 — VCOREA_PM

VCOREB — R21 33.2 0603 — C46 4.7uF 0603
VCOREB PM BYPASS — JP16 — R22 100 mOhms 1206 — VCOREB_PM

VREGO_A — R24 33.2 0603 — C56 4.7uF 0603
VREG_A PM BYPASS — JP17 — R25 100 mOhms 1206 — VREGO_A_PM

Refer to APPLICATION NOTE 6774 for specific routing guidelines for MAX34417 low level analog

U13
MAX34417ENE+

A3	IN+	SCL	C4 — I2CM0A_SCL — 625_P1_7
A2	1N1-	SDA	D4 — I2CM0A_SDA — 625_P1_6
		ADDR	C2
A1	IN2+	PDNB	B3 — 1V8_LDO
B1	IN2-	SLOW	C3
		VIO	B2 — C44 100nF 0402
D1	IN3+	VDD	A4 — 3V3_LDO
C1	IN3-		C49 100nF 0402
D3	IN4+	GND	B4
D2	1N4-		

RV JTAG

JH4
10P CORTEX DEBUG

1V8_LDO	1	2	RV_TMS — P1_1
	3 VCC — SWDIO/TMS	4	RV_TCK — P1_0
	5 GND — SWDCLK/TCK	6	RV_TDO — P1_3
	7 GND — SWO/TDO	8	RV_TDI — P1_2
	9 KEY — NC/TDI	10	
	GND_DETECT — NRESET		

SWD

JH5
10P CORTEX DEBUG

1V8_LDO — R58 10K

1V8_LDO	1	2	P0_28
	3 VCC — SWDIO/TMS	4	P0_29
	5 GND — SWDCLK/TCK	6	
	7 GND — SWO/TDO	8	
	9 KEY — NC/TDI	10	
	GND_DETECT — NRESET		

JP18 2–1 RV RESET EN

MIC

U15
SPH0645LM4H-B

WS 1, BCLK 4, DATA_OUT 6 — I2S_SDI — P1_4
SELECT 2 — MIC-JTAG_B — P1_7
VDD 5 — 1V8_LDO — C68 220pF 0402; C69 100nF 0402
GND 3
R35 100K; R36 10K

Drive SELECT high to allow MIC to take over the port.
Default is SELECT pulled low keeping MIC pins in a high Z state and allowing RV JTAG communications

RESET

TP7 WHT — RSTN — SW5

OPEN DRAIN RESET BUFFER

U16
NL27WZ07DFT2G
A1 — Y1 6; A2 — Y2 4 — DUT_3V3_RSTN
GND 2 — VCC 5 — 1V8_LDO
C70 100nF 0402

WAKEUP

SW4 P3.1

DEBOUNCE

U17
MAX6816EUS+T
IN 2 — OUT 3
GND 1 — VCC 4 — 3V3_LDO
C71 100nF 0402

OPEN DRAIN WAKEUP BUFFER

U18
NL27WZ07DFT2G
A1 — Y1 6; A2 — Y2 4
GND 2 — VCC 5 — 3V3_LDO
C72 100nF 0402

PB1

P2_6 — R28 49.9K — SW2 P2.6

PB2

P2_7 — R29 49.9K — SW3 P2.7

ADC IN

JH3
8P 2x4

P2_0 AIN0 — R30 0
P2_1 AIN1 — R31 0
P2_2 AIN2 — R33 0
P2_3 AIN3 — R34 0
C62 DNI 0402; C64 DNI 0402; C65 DNI 0402; C66 DNI 0402

A0	1	2	GND
A1	3	4	
A2	5	6	
A3	7	8	

PORT 2,3

JH6
5P 1x5

P2_4 — GND 1, P24 2, P30 3, P31 4, GND 5
P3_0, P3_1

Title: MAX78000 EV KIT - MAX78000, I/O, SWD, JTAG
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MICRO B USB

POWER DATA I/O

J1

L3
BLM21AG121SN1D
0805

C75
1uF
0603

90 ohm differential traces

C76 1uF 0402

U21
MAX13202EALT+T

3V3 VDDB (625)

U19
MAX1818EUT33+T
SOT-23 6P

C73
1uF
0402

C74
4.7uF
0603

VDDB625

POWER DATA PROCESSOR

U20
MAX32625ITK+
68P TQFN 8x8 LS0.4mm

1V8_LDO

R37 2.21K
R38 2.21K
R42 2.21K
R39 2.21K
R40 10K
R41 10K

625_P0_2 TRIG1
625_P0_3 TRIG2
625_P0_4 SPIM0A_SCK
625_P0_5 SPIM0A_MOSI
625_P0_7 SPIM0A_SS0
625_P1_0 DISP_EN
625_P1_6 I2CM0A_SDA
625_P1_7 I2CM0A_SCL
625_DBG_SRST
625_DBG_SWC
625_DBG_SWD

AIN0 AIN1 AIN2 AIN3
P0_0 P0_1 P0_2 P0_3 P0_4 P0_5 P0_6 P0_7
P1_0 P1_1 P1_2 P1_3 P1_4 P1_5 P1_6 P1_7
DP DM
RSTN SRSTN
TCK/SWCLK TMS/SWDIO TDO TDI
32KOUT 32KIN
VSS VSS VSS VSS VSS EP

Y2
32.768KHz

P2_0 P2_1 P2_2 P2_3 P2_4 P2_5 P2_6 P2_7
P3_0 P3_1 P3_2 P3_3 P3_4 P3_5 P3_6 P3_7
P4_0 P4_1 P4_2 P4_3 P4_4 P4_5 P4_6 P4_7

DBG_RX 625_P2_0
DBG_TX 625_P2_1
R_LED 625_P2_4
G_LED 625_P2_5
B_LED 625_P2_6
L 625_P2_7
R 625_P3_0

VDD18 VDD18
VDD12
VDDIOH VDDIOH
VRTC
VDDIO VDDIO
VDDB
VDDB625

C77 1uF 0402
C78 1uF 0402
C79 1uF 0402
C80 1uF 0402
C81 1uF 0402
C82 1uF 0402
C83 1uF 0402
C84 1uF 0402
C85 1uF 0402

1V8_LDO
1V2_LDO
3V3_LDO

625 SWD

J2
TC2050-IDC-NL
MAXDAP
DNI

1V8_LDO
625_DBG_SWD
625_DBG_SWC
VCC SWD GND SWC GND
RST ID DRX NC DTX
625_DBG_SRST
DBG_RX 625_P2_0
DBG_TX 625_P2_1

625 STATUS

D4
SML-LX0404SIUPGUSB

3V3_LDO
COM A
RED K
BLUE K
GREEN K

R43 2.7K R_LED 625_P2_4
R44 1.4K B_LED 625_P2_6
R45 1K G_LED 625_P2_5

Add header to 625 SWD for easy customer access?

PWR MODE SEL

1V8_LDO
R47 10K
SW6 LEFT L 625_P2_7
R46 10K 1V8_LDO
SW7 RIGHT R 625_P3_0

POWER DISPLAY

J3
503480-1000

625_P0_4 SPIM0A_SCK
625_P0_5 SPIM0A_MOSI
625_P0_7 SPIM0A_SS0
625_P1_0 DISP_EN
3V3_LDO

SCLK SI SCS EXTCOMIN DISP VDDA VDD EXTMODE VSS VSSA

C86 100nF 0402
C87 10uF 0805
C88 100nF 0402

U22
LS013B7DH03
10P CON

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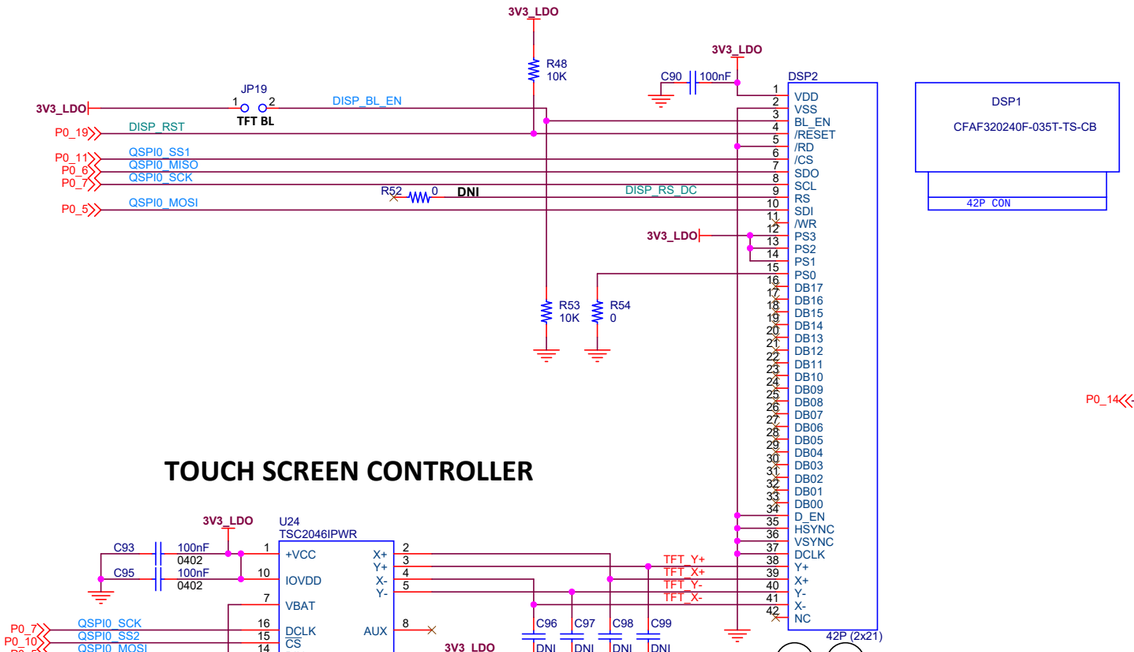
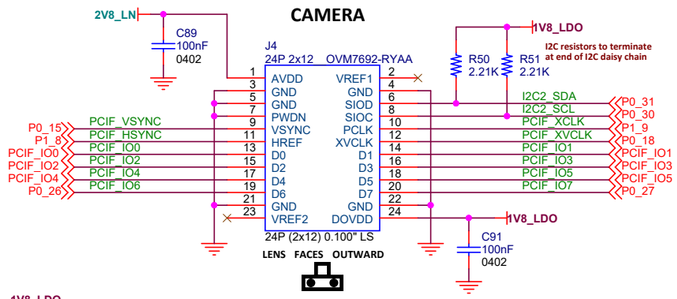
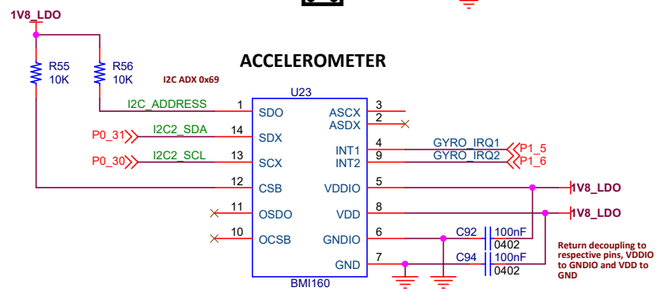
TFT DISPLAY



CAMERA

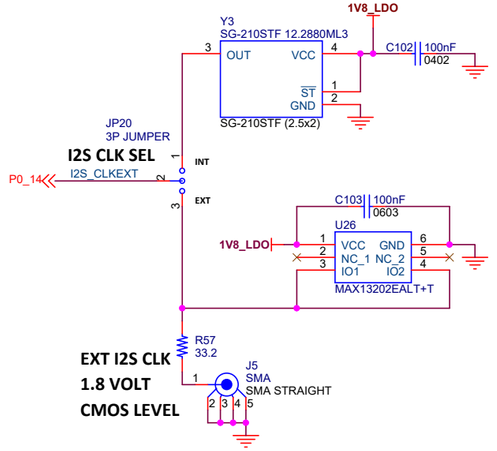


ACCELEROMETER

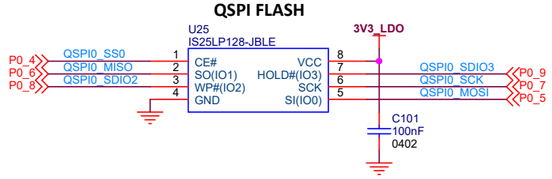


TOUCH SCREEN CONTROLLER

I2S EXTERNAL CLOCK

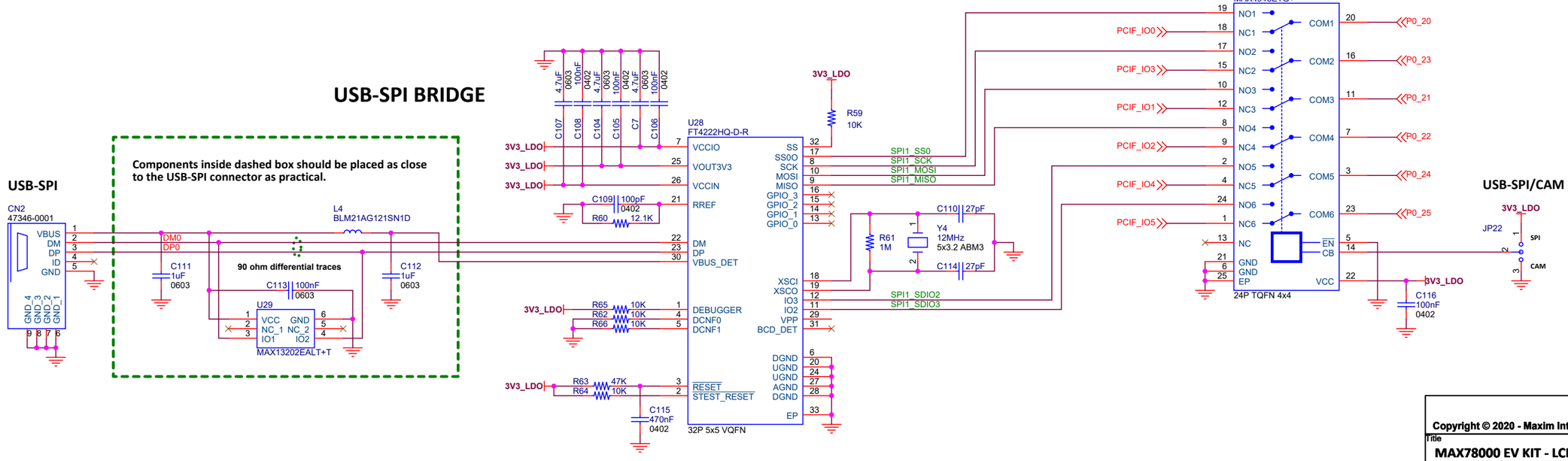


QSPI FLASH



USB-SPI BRIDGE / CAMERA SELECT

USB-SPI BRIDGE



USB-SPI BRIDGE / CAMERA SELECT

USB-SPI/CAM

maxim integrated

Title: MAX78000 EV KIT - LCD, Camera, Flash, Gyro, TS

Size	Document Number	Rev
13x19	SC-00170	C

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