ECE M216A Project, Fall 2024
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Performance Summary

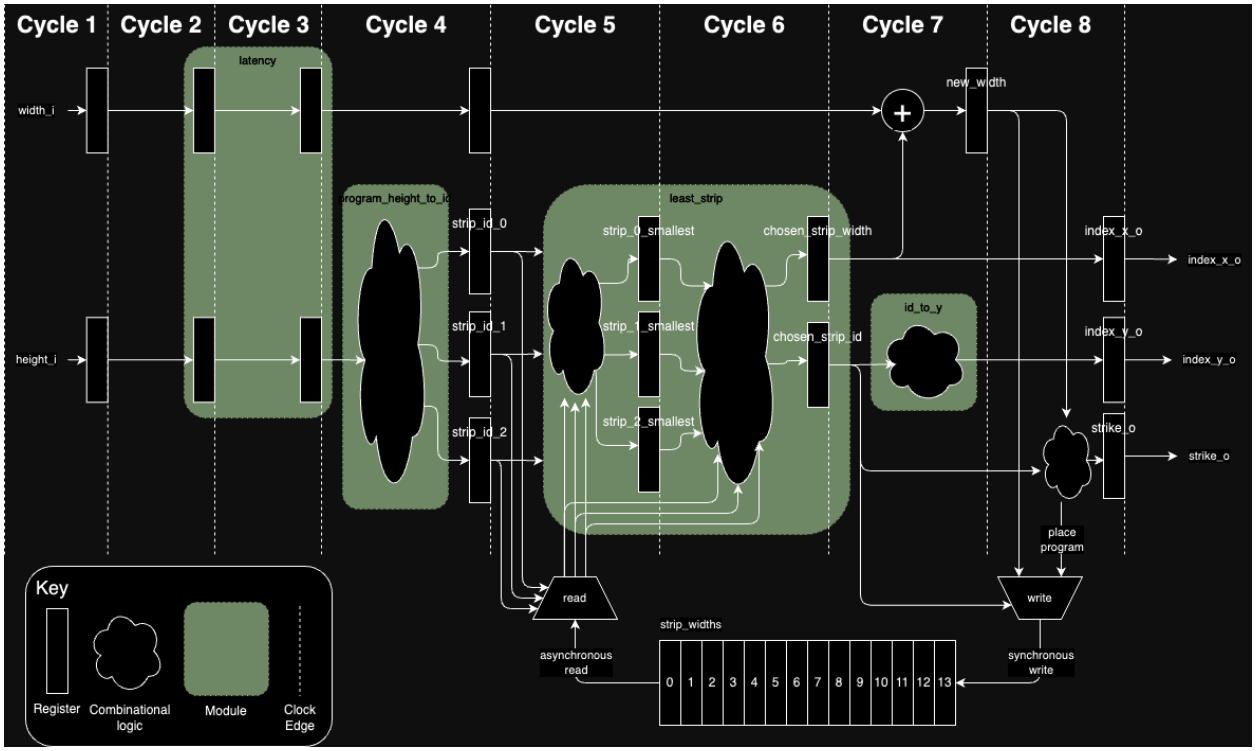
Max Fclk (MHz)	Area (μm^2)	Energy (pJ)	Hold Time Slack (ps)	EA/f	Tclk (1/Fclk)
2173.91	4213.15	1.25	0.01303	2.42	0.46ns

Math can be checked here: https://www.desmos.com/calculator/neb4eqn1uy
Github: https://github.com/MaxwellJung/ecem216a

See next page for architecture.

Architecture

Block Diagram



Key Features

Increase throughput (2+GHz) by inserting registers to break long combinational logic

Modules

- latency
  - Chain of registers to delay signal by N clock cycles
- program_height_to_id
  - Computes up to 3 possible strips a program can fit into
    - First strip ID (strip_id_0) corresponds to higher priority then second strip ID (strip_id_1) which is higher priority then third strip ID (strip_id_2)
    - Strip ID indexed from 1 to 13
      - ID of 0 corresponds to null/error
  - Combinational logic
- least_strip
  - Priority comparator
    - Compares 3 strip IDs and their corresponding widths and outputs the best strip ID and width

        - If widths are equal, break ties in the order strip_id_0 < strip_id_1 < strip_id_2
    - Clocked with latency of 2 clock cycles to increase throughput
- id_to_y
    - Converts strip id to y position on compute array
    - Combinational
- Counter (not shown above)
    - Counts from 1 to 4 to track number of clock cycles since program arrival
    - Output value used to synchronize different register writes

Synchronization
All register writes are synchronized using the value from the counter.

Inputs are registered (consuming 1 clock cycle), then delayed by 2 more clock cycles using the latency module.
On the 4th clock cycle, the height of the program is converted into 3 potential strip IDs.
On the 5th and 6th clock cycle, the best strip out of the 3 potential strips is chosen (valid output on 6th clock cycle).
On the 7th clock cycle, the y position of the strip and the new width of the chosen strip is computed.
On the 8th clock cycle, the new width is written to memory (strip_widths) and the outputs are registered.