Jiajun Wu | PhD Student, HKU

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Introduction

Jiajun Wu is currently a PhD student at the Department of Electrical and Electronic Engineering (EEE), the University of Hong Kong (HKU). His research interests include reconfigurable computing, hardware accelerator and computer architecture.

Education

The University of Hong Kong — PhD Student 2021 — present

- Supervisor: Dr. Hayden Kwok-Hay So
- Research Field: AI Hardware System

Huazhong University of Science and Technology — Bachelor of Engineering 2017 — 2021

- Supervisor: Prof. Chao Wang
- Honored Thesis
- GPA: 3.89/4.0

Experience

Exchange — Singapore University of Technology and Design, Singapore 01/2020 — 02/2020

- **Mentor**: Dr. Shaowei Lin
- **Project**: Study of Advanced Algorithms of Neuromorphic Computing and Hardware Implementation

Research Intern — Zhuhai UM Science & Technology Research Institute, China 07/2020 — 10/2020

- **Mentor**: Dr. Sai Weng Sin
- **Project**: Study of 3D ToF sensor based advanced mixed-signal circuit design

Publications

1. **J. Wu** *et al.*, "An Energy-Efficient Deep Belief Network Processor Based on Heterogeneous Multi-Core Architecture with Transposable Memory and On-Chip Learning," in *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 11, no. 4, pp. 725-738, Dec. 2021.

2. **J. Wu** *et al*., "Efficient Design of Spiking Neural Network with STDP Learning Based on Fast CORDIC," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 6, pp. 2522-2534, June 2021.

3. **J. Wu** *et al*., "An Energy-efficient Multi-core Restricted Boltzmann Machine Processor with On-chip Bio-plausible Learning and Reconfigurable Sparsity," in *2020 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pp. 1-4, 2020.

4. J. Xu, Y. Zhan, Y. Li, **J. Wu**, X. Ji, G. Yu, W. Jiang, R. Zhao and C. Wang, "In-Situ Aging-aware Error Monitoring Scheme for IMPLY-based Memristive Computing-in-Memory Systems," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, July 2021.

5. Q. Wang, Y. Zhan, B. Liu, **J. Wu**, Y. Shi, G. Yu, and C. Wang, "A Reconfigurable Area and Energy Efficient Hardware Accelerator of Five High-order Operators for Vision Sensor Based Robot Systems," in *Proc. of IEEE International Conference on Integrated Circuits, Technologies and Applications*, Nov. 24-26, 2021.

6. B. Liu, Z. Wen, H. Zhu, J. Lai, **J. Wu**, H. Ping, W. Liu, G. Yu, J. Zhang, Z. Liu, H. Zeng and C. Wang, "Energy-Efficient Intelligent Pulmonary Auscultation for Post COVID-19 Era Wearable Monitoring Enabled by Two-Stage Hybrid Neural Network," in *2022 IEEE International Symposium on Circuits and Systems* (ISCAS 2022)

Selected Awards

- **FIRST PRIZE** in TI Cup College Students' Electronic Design Competition (TI 杯全國大學生電子設計競賽)
- **SECOND PRIZE** in Challenge Cup College Students' Extracurricular Academic Science and Technology Works Contest ("挑戰杯"全國大學生課外學術科技作品競賽)
- **SECOND PRIZE** in China University Intelligent Robot Creative Competition (中國高校智能機器人創意大賽)

Skills

- Programming skills: C/C++, Python, Verilog HDL
- EDA Tools: Xilinx Vivado, Vivado HLS, Cadence Toolchain
- Common AI Frameworks: PyTorch, TensorFlow etc.