

# Jiajun Wu

PHD CANDIDATE · ELECTRICAL AND ELECTRONIC ENGINEERING

University of Hong Kong, Main Campus, Pokfulam, Hong Kong

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## Education

### University of Hong Kong (HKU)

Hong Kong SAR

PHD CANDIDATE

2021 - present

- Supervisor: Dr. Hayden Kwok-Hay So
- Research Field: *Hardware Acceleration Systems for AI Applications*

### Huazhong University of Science and Technology (HUST)

China

BENG, INTEGRATED CIRCUIT DESIGN

2017 - 2021

- Honored Thesis & Honored Graduate
- GPA: 3.89/4.0
- Supervisor: Prof. Chao Wang

## Experience

### University of Hong Kong - PhD Candidate

Hong Kong SAR

ADVISOR: DR. HAYDEN KWOK-HAY SO

Sep. 2021 - Present

- Probation: Mixed-Precision DNN Training and Acceleration: An Efficient Algorithm-Hardware Co-Design Approach

### Huazhong University of Science and Technology - Research Assistant

Wuhan, China

ADVISORS: PROF. CHAO WANG AND DR. GUOYI YU

2019-2021

- Research Topic: Energy-Efficient Brain-Inspired Computing

### University of Macau - Research Intern

Zhuhai, China

ADVISOR: PROF. SAI-WENG SIN

Jul. 2020-Oct. 2020

- Research Topic: Analog Computing in the event sensor front-end

### Singapore University of Technology and Design - Visiting Student

Singapore

ADVISOR: DR. SHAOWEI LIN

Jan. 2020-Feb. 2020

- Project: Study of neuromorphic computing in machine learning algorithms

## Publications

### PUBLISHED

- J. Wu**, J. Zhou, Y. Gao, Y. Ding, N. Wong and H. K. -H. So, "MSD: Mixing Signed Digit Representations for Hardware-efficient DNN Acceleration on FPGA with Heterogeneous Resources," 2023 IEEE 31st Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM), Marina Del Rey, CA, USA, 2023, pp. 94-104.
- Y. Ding<sup>1</sup>, **J. Wu**<sup>1</sup>, Y. Gao, M. Wang and H. K. -H. So, "Model-Platform Optimized Deep Neural Network Accelerator Generation through Mixed-Integer Geometric Programming," 2023 IEEE 31st Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM), Marina Del Rey, CA, USA, 2023, pp. 83-93.
- J. Wu**, X. Huang, L. Yang, J. Wang, B. Liu, Z. Wen, J. Li, G. Yu, K. -S. Chong and C. Wang, "An Energy-Efficient Deep Belief Network Processor Based on Heterogeneous Multi-Core Architecture With Transposable Memory and On-Chip Learning," in IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 11, no. 4, pp. 725-738, Dec. 2021
- J. Wu**, Y. Zhan, Z. Peng, X. Ji, G. Yu, R. Zhao and C. Wang, "Efficient Design of Spiking Neural Network With STDP Learning Based on Fast CORDIC," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 6, pp. 2522-2534, June 2021

<sup>1</sup>Equal Contribution

- J. Wu**, X. Huang, L. Yang, L. Wang, J. Wang, Z. Liu, K. -S. Chong, S. Lin and C. Wang, "An Energy-efficient Multi-core Restricted Boltzmann Machine Processor with On-chip Bio-plausible Learning and Reconfigurable Sparsity," 2020 IEEE Asian Solid-State Circuits Conference (A-SSCC), Hiroshima, Japan, 2020, pp. 1-4
- J. Zhou<sup>2</sup>, **J. Wu**<sup>2</sup>, Y. Gao, Y. Ding, C. Tao, B. Li, F. Tu, K. -T. Cheng, H. K. -H. So, and N. Wong, "DyBit: Dynamic Bit-Precision Numbers for Efficient Quantized Neural Network Inference," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (Early Access).
- J. Xu, Y. Zhan, Y. Li, **J. Wu**, X. Ji, G. Yu, W. Jiang, R. Zhao and C. Wang, "In situ aging-aware error monitoring scheme for IMPLY-based memristive computing-in-memory systems," IEEE Transactions on Circuits and Systems I: Regular Papers, 69(1), pp.309-321.
- B. Liu, Z. Wen, H. Zhu, J. Lai, **J. Wu**, H. Ping, W. Liu, G. Yu, J. Zhang, Z. Liu, H. Zeng and C. Wang "Energy-efficient intelligent pulmonary auscultation for post COVID-19 era wearable monitoring enabled by two-stage hybrid neural network," in 2022 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 2220-2224. IEEE, 2022.
- Q. Wang, Y. Zhan, B. Liu, **J. Wu**, Y. Shi, G. Yu, and C. Wang. "A Reconfigurable Area and Energy Efficient Hardware Accelerator of Five High-order Operators for Vision Sensor Based Robot Systems," in 2021 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA), pp. 189-190. IEEE, 2021.

#### ACCEPTED, TO BE PUBLISHED

- M. Song, **J. Wu**, Y. Ding and H. K. -H. So, "SqueezeBlock: A Transparent Weight Compression Scheme for Deep Neural Networks," in International Conference on Field Programmable Technology (FPT) 2023, Yokohama, Japan.

#### UNDER REVIEW

- J. Wu**, M. Song, J. Zhao, J. Zhou, N. Wong and H. K. -H. So, "TATA: Transformer Acceleration with Transformable Arithmetic Processing," in ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS) 2024, under review.

#### Selected Awards

2021	<b>Postgraduate Research Scholarship</b> , University of Hong Kong <b>Honored Thesis &amp; Honored Graduate</b> , Huazhong University of Science and Technology	HK\$ 18,830/m
2019	<b>Second Prize in Challenge Cup College Students' Extracurricular Academic Science and Technology Works Contest</b> , Ministry of Education, P. R. China <b>Second Prize in China University Intelligent Robot Creative Competition</b> , China Association for Science and Technology <b>Third Prize in TI Cup College Students' Electronic Design Competition</b> , Texas Instruments, and Ministry of Education, P. R. China <b>Merit Student</b> , HUST, Huazhong University of Science and Technology	¥ 10,000 ¥ 3,000 ¥ 2,000
2018	<b>First Prize in TI Cup College Students' Electronic Design Competition</b> , Texas Instruments, and Ministry of Education, P. R. China	¥ 500

#### Academic Presentations

- Spring 2023. *MSD: Mixing Signed Digit Representations for Hardware-efficient DNN Acceleration on FPGA with Heterogeneous Resources*. In 2023 IEEE 31st Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM), CA, USA
- Summer 2021. *Energy-efficient DNN Hardware Accelerator with On-chip Learning – A Deep Belief Network Processor Case*. Invited by IEEE CASS-EDS-SSCS HUST Student Branch Chapter, Wuhan, China.
- Autumn 2020. *An Energy-efficient Multi-core Restricted Boltzmann Machine Processor with On-chip Bio-plausible Learning and Reconfigurable Sparsity*. In 2020 IEEE Asian Solid-State Circuits Conference (A-SSCC), Virtual Event.

<sup>2</sup>Equal Contribution

## Teaching Experience \_\_\_\_\_

2023	ELEC3342, Digital system design, Teaching Assistant	HKU
2022	ELEC3342, Digital system design, Teaching Assistant	HKU
2022	ELEC6036, High performance computer architecture, Teaching Assistant	HKU

## Outreach & Professional Development \_\_\_\_\_

- Reviewer of IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)
- IEEE Member
- IEEE Student Member in IEEE CASS-EDS-SSCS HUST Student Branch Chapter