Jiajun Wu | PhD Student, HKU

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Introduction

Jiajun Wu is currently a PhD student at the Department of Electrical and Electronic Engineering (EEE), the University of Hong Kong (HKU). His research interests include reconfigurable computing, hardware accelerator and computer architecture.

Education

PhD Student — The University of Hong Kong 2021 — present

- Supervisor: Dr. Hayden Kwok-Hay So
- Research Field: AI Hardware System

BEng — Huazhong University of Science and Technology 2017 — 2021

- Major: Integrated Circuit Design
- Supervisor: Prof. Chao Wang
- Honored Graduate
- GPA: 3.89/4.0

Experience

Exchange — Singapore University of Technology and Design, Singapore 01/2020 — 02/2020

- Mentor: Dr. Shaowei Lin
- Research Field: Study of Advanced Algorithms of Neuromorphic Computing and Hardware Implementation (Published in **ASSCC 2020**)

Research Intern — Zhuhai UM Science & Technology Research Institute, China 07/2020 — 10/2020

- Mentor: Dr. Sai Weng Sin
- Research Field: Study of 3D ToF sensor based advanced mixed-signal circuit design

Publications

1. **J. Wu** et al., "MSD: Mixing Signed Digit Representations for Hardware-efficient DNN Acceleration on FPGA with Heterogeneous Resources," in *the 31st IEEE International Symposium On Field-Programmable Custom Computing Machines (FCCM 2023)*.

2. Y. Ding[1], **J. Wu**[1] et al., “Model-Platform Optimized Deep Neural Network Accelerator Generation through Mixed-integer Geometric Programming,” in *the 31st IEEE International Symposium On Field-Programmable Custom Computing Machines (FCCM 2023)*.
3. J. Zhou[2], **J. Wu**[2] et al., "DyBit: Dynamic Bit-Precision Numbers for Efficient Quantized Neural Network Inference," *arXiv preprint arXiv:2302.12510 (2023).*
4. **J. Wu** et al., "An Energy-Efficient Deep Belief Network Processor Based on Heterogeneous Multi-Core Architecture with Transposable Memory and On-Chip Learning," in *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 11, no. 4, pp. 725-738, Dec. 2021.
5. **J. Wu** et al., “Efficient Design of Spiking Neural Network with STDP Learning Based on Fast CORDIC,” in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 6, pp. 2522-2534, June 2021.
6. **J. Wu** et al., "An Energy-efficient Multi-core Restricted Boltzmann Machine Processor with On-chip Bioplausible Learning and Reconfigurable Sparsity," in *2020 IEEE Asian Solid-State Circuits Conference (ASSCC)*, pp. 1-4, 2020.
7. J. Xu, Y. Zhan, Y. Li, **J. Wu**, et al., “In-Situ Aging-aware Error Monitoring Scheme for IMPLY-based Memristive Computing-in-Memory Systems,” in *IEEE Transactions on Circuits and Systems I: Regular Papers*, July 2021.
8. B. Liu, Z. Wen, H. Zhu, J. Lai, **J. Wu**, et al., “Energy-Efficient Intelligent Pulmonary Auscultation for Post COVID-19 Era Wearable Monitoring Enabled by Two-Stage Hybrid Neural Network,” in *2022 IEEE International Symposium on Circuits and Systems (ISCAS 2022)*.
9. Q. Wang, Y. Zhan, B. Liu, **J. Wu**, et al., “A Reconfigurable Area and Energy Efficient Hardware Accelerator of Five High-order Operators for Vision Sensor Based Robot Systems,” in *Proc. of IEEE International Conference on Integrated Circuits, Technologies and Applications*, Nov. 24-26, 2021.

Selected Awards

- **FIRST PRIZE** in TI Cup College Students' Electronic Design Competition
- **SECOND PRIZE** in Challenge Cup College Students’ Extracurricular Academic Science and Technology Works Contest
- **SECOND PRIZE** in China University Intelligent Robot Creative Competition

Academic Services

- IEEE member.
- IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I) reviewer.

[1] Equally contributed
[2] Equally contributed