

# Jiajun Wu

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Jiajun Wu is currently a PhD student in the Department of Electrical and Electronic Engineering (EEE), the University of Hong Kong (HKU). His research interests include FPGA system, hardware accelerators, neuromorphic computing, and computer architecture.



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## EDUCATION

### THE UNIVERSITY OF HONG KONG

Hong Kong

**PhD Student in Electrical and Electronic Engineering**, from 09/2021 to present

Supervisor: Prof. Hayden Kwok-Hay So

Current Research Topics:

- AI Hardware Accelerator
- Computer Architecture

### HUAZHONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

(“Double First-Class” initiative, “985” Project)

Wuhan, China

**Bachelor in IC Design and Integrated System**, from 09/2017 to 06/2021 GPA 3.89/4.0

Supervisor: Prof. Chao Wang

Representative Courses:

- CMOS Analog Integrated Circuit
- Processor Architecture
- Fundamentals of Digital Integrated Circuit
- Principles of Embedded System
- Hardware Description Language and Design of Digital System
- Principles of Computer Architecture

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## EXCHANGE & INTERNSHIP

### SINGAPORE UNIVERSITY OF TECHNOLOGY AND DESIGN

Singapore

**Internship**, from 15/01/2020 to 03/02/2020

Supervised by Prof. Shaowei Lin, Singapore University of Technology and Design

Project: Study of Advanced Algorithms of Neuromorphic Computing and Hardware Implementation

### ZHUHAI UM SCIENCE & TECHNOLOGY RESEARCH INSTITUTE / UNIVERSITY OF MACAU

Zhuhai, China

**Internship**, from 28/07/2020 to 31/10/2020

Supervised by Prof. Sai Weng Sin, University of Macau

Project: Study of 3D ToF sensor based advanced mixed-signal circuit design

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## PUBLICATIONS

**J. Wu et al.**, “An Energy-Efficient GALS Multi-core Restricted Boltzmann Machine Processor with On-chip Bi-plausible Learning and Reconfigurable Sparsity”, in *IEEE A-SSCC 2020*, Nov. 2020.

**J. Wu<sup>1</sup>**, Y. Zhan<sup>1</sup> et al., “Efficient Design of Spiking Neural Network With STDP Learning Based on Fast CORDIC,” in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 6, pp. 2522-2534, June 2021.

**J. Wu et al.**, “An Energy-efficient Deep Belief Network Processor Based on Heterogeneous Multi-core Architecture with Transposable Memory and On-chip Learning,” in *IEEE JETCAS*, under review.

J. Xu, Y. Zhan, Y. Li, **J. Wu**, X. Ji, G. Yu, W. Jiang, R. Zhao and C. Wang, “In-Situ Aging-aware Error Monitoring Scheme for IMPLY-based Memristive Computing-in-Memory Systems,” in *IEEE Transactions on Circuits and Systems I: Regular Papers*, in press, 2021.

Q. Wang, Y. Zhan, B. Liu, **J. Wu**, Y. Shi, G. Yu, and C. Wang, “A Reconfigurable Area and Energy Efficient Hardware Accelerator of Five High-order Operators for Vision Sensor Based Robot Systems,” in *Proc. of IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA 2021)*, Nov. 24-26, 2021.

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## RESEARCH EXPERIENCES

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<sup>1</sup> Equally contributed to this work

## **STUDY OF TOF ALGORITHM BASED ADVANCED MIXED-SIGNAL CIS DESIGN**

*Adviser: Prof. Sai Weng Sin*

*Institution: Singapore University of Technology and Design*

Zhuhai, China

July 2020 - present

- The project is still going on. We are studying advanced recognition / classification algorithm based on Time-of-Flight (ToF) sensors and 3D images. Then, we look forward to implementing some energy-efficient accelerator such as NN accelerator, and finally getting a chip design.

## **STUDY OF NEURAL NETWORK BASED NEUROMORPHIC COMPUTING AND HIGH ENERGY EFFICIENT CHIP DESIGN**

*Adviser: Prof. Chao Wang* *Institution: Research Lab of Ultra Low-Power and Intelligent Integrated Circuits*

Wuhan, China

May 2019 - present

- Proposed a reconfigurable and highly efficient Spiking Neural Network (SNN) based on fast-convergence COordinate Rotation DIgital Computer (CORDIC) algorithm is proposed to achieve digital hardware implementation. This work has been summarized into a paper and under review.

## **STUDY OF ADVANCED ALGORITHMS OF NEUROMORPHIC COMPUTING AND HARDWARE IMPLEMENTATION**

*Adviser: Prof. Shaowei Lin*

*Institution: Singapore University of Technology and Design*

Singapore

Jan 2020 - Feb 2020

- Joined the development of VPF and MPN source code and understood its mathematical significance deeply. Implemented basic modules of VPF algorithm's hardware accelerator and verified in RTL simulation level.

## **HIGH RELIABILITY LITHIUM BATTERY SYSTEM WITH INTEGRATED ULTRASONIC SENSOR NETWORK**

*Adviser: Prof. Yue Shen*

*Institution: HUST-WISCO Joint Laboratory*

Wuhan, China

Feb 2019 - May 2019

- Integrated the ultrasonic sensor network into the battery module, using the ultrasonic signal to monitor the state of the battery, obtaining a high-precision state of charge and health, especially the battery gas detection limit is as low as 20 uL, far beyond traditional technology.

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## **COMPETITION AWARDS<sup>2</sup>**

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### **FIRST PRIZE IN TI CUP COLLEGE STUDENTS' ELECTRONIC DESIGN COMPETITION**

*Institution: Science & Technology Innovation Center, HUST*

Aug 2018

### **SECOND PRIZE IN CHALLENGE CUP HUBEI PROVINCE COLLEGE STUDENTS' EXTRACURRICULAR ACADEMIC SCIENCE AND TECHNOLOGY WORKS CONTEST**

*Institution: School of Artificial Intelligence and Automation, HUST*

Mar 2019 - May 2019

### **SECOND PRIZE IN CHINA UNIVERSITY INTELLIGENT ROBOT CREATIVE COMPETITION**

*Institution: School of Artificial Intelligence and Automation, HUST*

Mar 2019 - May 2019

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## **SKILLS**

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**C/C++   Python   FPGA   MATLAB   Verilog-HDL   Embedded System**

- Developed small software apps based on some desktop platforms (e.g., Qt).
- Developed some software-hardware co-design implementations on FPGA, especially with Xilinx devices.
- ALL the source codes of my publications and other works are shared in my GitHub: <https://github.com/MaxwellWjj>

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<sup>2</sup> Only national or provincial high-level competition awards are listed here.