Jiajun Wu | PhD Student in HKU

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Introduction

Jiajun Wu is currently a PhD student in the Department of Electrical and Electronic Engineering (EEE), the University of Hong Kong (HKU). His research interests include reconfigurable computing based on FPGA, hardware accelerator and computer architecture.

Education

The University of Hong Kong — PhD Student, Hong Kong 2021 — present

- Supervisor: Prof. Hayden Kwok-Hay So
- Research Field: AI Hardware System

Huazhong University of Science and Technology — Bachelor, China 2017 — 2021

- Supervisor: Prof. Chao Wang
- Honored Graduate and Honored Thesis
- GPA: 3.89/4.0

Experience

Internship — Singapore University of Technology and Design, Singapore 01/2020 — 02/2020

- Mentor: Dr. Shaowei Lin

- **Project**: Study of Advanced Algorithms of Neuromorphic Computing and Hardware Implementation

Internship — University of Macau, Macau 07/2020 — 10/2020

- **Mentor**: Prof. Sai Weng Sin
- **Project**: Study of 3D ToF sensor based advanced mixed-signal circuit design

Publications

1. **J. Wu** *et al*., "An Energy-efficient Multi-core Restricted Boltzmann Machine Processor with On-chip Bio-plausible Learning and Reconfigurable Sparsity," in *2020 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pp. 1-4, 2020.

2. **J. Wu**[1], Y. Zhan[2] *et al*., “Efficient Design of Spiking Neural Network with STDP Learning Based on Fast CORDIC,” in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 6, pp. 2522-2534, June 2021.

3. **J. Wu** *et al*., "An Energy-efficient Deep Belief Network Processor Based on Heterogeneous Multi-core Architecture with Transposable Memory and On-chip Learning," in *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, September 2021.

4. J. Xu, Y. Zhan, Y. Li, **J. Wu**, X. Ji, G. Yu, W. Jiang, R. Zhao and C. Wang, “In-Situ Aging-aware Error Monitoring Scheme for IMPLY-based Memristive Computing-in-Memory Systems,” in *IEEE Transactions on Circuits and Systems I: Regular Papers*, July 2021.

5. Q. Wang, Y. Zhan, B. Liu, **J. Wu**, Y. Shi, G. Yu, and C. Wang, “A Reconfigurable Area and Energy Efficient Hardware Accelerator of Five High-order Operators for Vision Sensor Based Robot Systems,” in *Proc. of IEEE International Conference on Integrated Circuits, Technologies and Applications*, Nov. 24-26, 2021.

Selected Awards

- FIRST PRIZE in TI Cup College Students' Electronic Design Competition
- SECOND PRIZE in Challenge Cup College Students’ Extracurricular Academic Science and Technology Works Contest
- SECOND PRIZE in China University Intelligent Robot Creative Competition

Skills

- Programming skills: C/C++, Python, Verilog HDL
- EDA Tools: Xilinx Vivado, Vivado HLS, Cadence Toolchain
- Common AI Frameworks: PyTorch, TensorFlow etc.

[1] Equal contribution
[2] Equal contribution