# ASSAM SCIENCE AND TECHNOLOGY UNIVERSITY

## Guwahati

## Course Structure and Syllabus

**ELECTRONICS AND COMMUNICATION ENGINEERING (ECE)**
**SEMESTER VII / ECE /B.TECH**

| Sl No | Sub Code | Subject | Hrs | | | Credits C |
|---|---|---|---|---|---|---|
| | | | L | T | P | |
| | **Theory** | | | | | |
| 1 | EC131701 | Linear Integrated Circuits | 3 | 2 | 0 | 4 |
| 2 | EC131702 | VHDL and Digital System Design | 3 | 0 | 0 | 3 |
| 3 | EC131703 | VLSI Design | 3 | 0 | 0 | 3 |
| 4 | EC131704 | Telecommunication Switching and Transmission System | 3 | 0 | 0 | 3 |
| 5 | **1317E01 | Elective I (Departmental) | 3 | 0 | 0 | 3 |
| 6 | HS1317E02 | Elective II (Humanities) | 2 | 0 | 0 | 2 |
| | **Practical** | | | | | |
| 7 | EC131711 | Linear Integrated Circuits Lab | 0 | 0 | 2 | 1 |
| 8 | EC131712 | VLSI and VHDL Lab | 0 | 0 | 2 | 1 |
| 9 | EC131715 | Project | 0 | 0 | 8 | 4 |
| 10 | EC131721 | Seminar on Summer Training | 0 | 0 | 0 | 1 |
| Total | | | 17 | 2 | 12 | **25** |
| Total Contact Hours : 31 | | | | | | |
| Total Credit : 25 | | | | | | |

| Elective-I Subjects | | |
|---|---|---|
| **Sl No** | **Subject Code** | **Subject** |
| 1 | **1317E01(I) | Embedded System |
| 2 | **1317E01(II) | Information Theory and Coding |
| 3 | **1317E01(III) | Satellite Communication and Remote Sensing |
| 4 | EE1317E01(IV) | Optimization Techniques |
| 5 | **1317E01(V) | Any other subject offered from time to time with the approval of the University |

| Elective-II Subjects | | |
|---|---|---|
| **Sl No** | **Subject Code** | **Subject** |
| 1 | HS1317E02(I) | Value Education, Human Rights and Legislative Procedure |
| 2 | HS1317E02(II) | Any other subject offered from time to time with the approval of the university |
| | | |

**Course Title:** LINEAR INTEGRATED CIRCUITS
**Course Code:** EC131701
**L-T-P-C: 3-2-0-4**

| | |
|---|---|
| Class Hours/week | 4 |
| Expected weeks | 12 |
| Total hrs. of classes | 36+12 =48 |

| MODULE | TOPIC | COURSE CONTENT | HOURS |
|---|---|---|---|
| 1. | **INTRODUCTION** | Op-amp block diagram, symbol, and equivalent diagram, pin diagram, ideal Op-amp, voltage transfer characteristics, dc characteristic: input bias, offset current, offset voltage, Offset error compensation, thermal drift, ac characteristics: frequency response, frequency compensation, slew rate, noise, CMRR | 8 |
| 2. | **NEGATIVE FEEDBACK** | Op-amp as inverting, non-inverting amplifier, voltage follower, loading effect, adder, differential, integrator, differentiator, powering op-amp. | 6 |
| 3. | **CURRENT TO VOLTAGE CONVERTERS** | V-I converters (floating load and grounded load), Current amplifiers, instrumentation amplifier, Log/Antilog Amplifier, Analog multipliers, Electronic analog computation. | 6 |
| 4. | **COMPARATORS** | Voltage limiter, level detectors, window detectors, ON/OFF temperature controller, pulse width modulation, Schmitt trigger, Precision half wave and full wave rectifiers Peak detectors. Sample and hold circuits, clipper, and clamper. | 7 |
| 5. | **SINE WAVE GENERATORS** | 555 timer, multivibrators, Triangular wave generator, Saw-tooth generator, Voltage to frequency and frequency to voltage converters. | 7 |
| 6. | **PERFORMANCE PARAMETERS** | Zener and Avalanche diode voltage references, Compensation methods, Series regulators, IC Voltage Regulators. | 4 |
| 7. | **CONVERTER DEFINITIONS AND SPECIFICATIONS** | Basic DAC techniques, Flash/Parallel, counter type, SAR AD converters. | 4 |
| 8. | **PHASE-LOCKED LOOP (PLL), VOLTAGE CONTROLLED OSCILLATOR (VCO)** | Phase-Locked Loop (PLL), Voltage Controlled Oscillator (VCO) | 2 |
| 9. | **FIRST ORDER ACTIVE FILTERS, SECOND ORDER RESPONSE** | Low-pass, high-pass, band pass and notch, KRC filters, multiple-feedback filters. | 4 |
| | | **TOTAL** | **48** |

## Text books/references:


1. Nergio Franco - Design with Operational Amplifiers and Analog Integrated Circuits, McGraw Hill Book Company.
2. R.F.Coughlin, F.F.Driscoll - Operational AmpIifier and Linear Integrated Circuits, Prentice Hall of India.
3. Ramakant A. Gayakwad- Op-Amps and Linear Integrated Circuits, PHI.
4. D.Roy Choudhury and S. B. Jain- Linear Integrated Circuits, New Age Int.
5. Salivahanan: Linear Integated Circuits, TMH.

**Course Title:** VHDL AND DIGITAL SYSTEM DESIGN
**Course Code:** EC131702
**L-T-P-C: 3-0-0-3**

| | |
|---|---|
| Class Hours/week | 3 |
| Expected weeks | 12 |
| Total hrs. of classes | 36 |

| MODULE | TOPIC | COURSE CONTENT | HOURS |
|---|---|---|---|
| **1.** | **INTRODUCTION** | Basic concepts of hardware description languages. Design process flow, hardware simulation and synthesis. Using VHDL for design synthesis. PLDs, macrocell structures and characteristics of PLDs and CPLDs. Architecture and features of FPGAs. Programming technologies of FPGAs. Inertial and transport delays, Simulation deltas, Signal drivers. Variable assignment, signal assignment, constants. VHDL operators, data objects, data types. | 8 |
| **2.** | **BEHAVIORAL MODELING**<br><br>**DATA FLOW AND STRUCTURAL MODELLING** | Entity declaration, architecture body, process statement, Wait, If, Case, Null, Loop, Exit, Next and Assertion statements.<br><br>Concurrent signal assignment, sequential signal assignment, Multiple drivers, conditional signal assignment, selected signal assignment, block statements, concurrent assertion statement, component declaration, component instantiation. Generate Statements. | 10 |
| **3.** | **GENERICS AND CONFIGURATIONS** | Generics. Default configurations, component configurations.<br>**SUBPROGRAMS AND PACKAGES:** Subprograms – functions, procedures, declarations. Package declarations, package body, use clause, predefined package standard. Design libraries. Test Benches. | 5 |
| **4.** | **DIGITAL SYSTEM DESIGN PROCESS,REGISTER TRANSFER,VHDL DESCRIPTION OF COMBINATIONAL LOGIC CIRCUITS** | Multiplexer, demultiplexer, encoder, decoder, adder, subtractor. Sequential Switching Circuit Design, Algorithmic state Machine approach, Moore and Mealy Machines. VHDL description of sequential logic circuits: Up-down decade counter, sequence detector, sequence generator, multipliers. Power Distribution and noise in digital systems. | 13 |

**Text books/ References:**


1. William J Dally and John W Poulton, Digital Systems Engineering, Cambridge University Press, 2008.
2. William I.Fletcher, An engineering approach to digital design, Prentice Hall of India,
3. Jayaram Bhasker, A VHDL Primer, 3rd edition, Prentice-Hall India, 2009.
4. Skahil, VHDL for Programmable logic- 2nd Ed – Wiley.
5. D. Perry, VHDL, 3rd Ed. - TMH.
6. Zainalabedin Navabi, VHDL Analysis and Modeling of Digital Systems, McGraw Hill, Second Edition, 1998.
7. Brown, Digital Logic with VHDL, TMH

**Course Title:** VLSI DESIGN
**Course Code:** EC131703
**L-T-P-C: 3-0-0-3**

| | |
|---|---|
| Class Hours/week | 3 |
| Expected weeks | 12 |
| Total hrs. of classes | 36 |

| MODULE | TOPIC | COURSE CONTENT | HOURS |
|---|---|---|---|
| **1.** | **INTRODUCTION TO VLSI AND BASIC CONCEPT OF MOS:** | Evolution of VLSI, Technology trends in VLSI, Introduction to MOS Transistor, I-V characteristics of nMOS and pMOS transistors, transconductance ($g_m$), channel length modulation. | 4 |
| **2.** | **VLSI FABRICATION TECHNIQUES** | Wafer fabrication - Wafer processing - Oxidation - Patterning - Silicon gate NMOS process - CMOS process - Nwell - Pwell - Twintub –resistor, capacitor and diode in IC - CMOS Process enhancements - Ion beam techniques - Chemical methods. | 8 |
| **3.** | **ANALOG VLSI:** | Introduction to analog VLSI - Analog circuit building blocks - Switches, active resistors - Current sources and sinks - Current mirrors/amplifiers - MOS & BJT, inverting amplifiers - CMOS and BJT two stage op-amp. | 6 |
| **4.** | **DIGITAL VLSI** | Basic electrical properties of NMOs & CMOS inverters, Stick Diagram & Design rules, Scaling of MOS Circuits, Subsystem Design And Layout, The CMOS structure: NAND and NOR gates, transfer characteristics, System Design And Design Methods; Adder Architectures, Multiplier Architectures, Counter Architectures, ALU Architectures. Latches, Flip-flops, Registers and Register Files, Standard Cell Approach. Moore and Mealy Machines, SRAM Cell, Different DRAM Cells. | 10 |
| **5.** | **ASIC DESIGN AND VHDL** | Architecture and programming technologies of ROMs, EPROMs, Introduction to ASIC, PLA, PAL, Gate arrays, CPLDs and FPGAs, programmable interconnect - Configuration memory. VHDL: Basics of VHDL-Operators, hierarchy procedures and assignments-Timing controls and delays. | 8 |

**TEXTBOOKS:**

1. D. A. Hodges, H. G. Jackson & R. A. Saleh, ***Analysis and Design of Digital Integrated Circuits***, Tata McGraw Hill, 3rd Ed. 2008.
2. D. A. Pucknell & K. Eshraghian, ***Basic VLSI Design,*** Prentice Hall of India, 3rd Ed. 2001.
3. Anguman Sarkar, Swapnadip De & Chandan Kumar Sarkar, ***VLSI Design and EDA Tools***, Scitech Publications (INDIA) Pvt. Ltd.

**REFERENCES:**

1. W. H. Wolf, ***Modern VLSI Design System-on-chip design***, Prentice Hall of India, 3rd Ed. 2004.
2. C. Mead & L. Conway, ***Introduction to VLSI system***, Addison Wesley, 2004.
3. James E.Palmor,Darid E.Perlman., "Introduction to Digital systems" Tata Mc Graw Hill,1996.

**Course Title:** TELECOMMUNICATION SWITCHING AND TRANSMISSION SYSTEM
**Course Code:** EC131704
**L-T-P-C: 3-0-0-3**

| | |
|---|---|
| Class Hours/week | 3 |
| Expected weeks | 12 |
| Total hrs. of classes | 36 |

| MODULE | TOPIC | COURSE CONTENT | HOURS |
|---|---|---|---|
| **1.** | **INTRODUCTION** | Introduction, Switching systems, Classification of Switching Systems, Functions of Switching systems, Evolution of Digital Switching System, Stored Program Control(SPC), Digital Switching system fundamentals; Transmission Media**:** Guided and Unguided | 8 |
| **2.** | **NETWORK SERVICES AND ARCHITECTURE** | Telecommunication Traffic: Introduction, Unit of Traffic Congestion, Traffic Measurement, Mathematical Model, Lost Call system, Queing Systems; Layered Architecture: Need and Advantages, Review of TCP/IP protocol, Review of OSI Model, Network Configuration. | 12 |
| **3.** | **NETWORKS** | Circuit Switched networks, Packet Switched Networks, Structure of a Switch: structure of circuit switch, structure of packet switch, Network Technologies: Core Technologies- IPv4, IPv6; Network access Technologies- MODEM, Digital subscriber line; Remote Access Technologies- Remote logging, Telnet; ATM Networks: Architecture, ATM Cell, ATM Layer, ATM LAN architecture; Quality of Service: Flow characteristics, Techniques to improve QoS; Internet, Architecture of Cellular system. | 10 |
| **4.** | **OPTICAL SYSTEMS** | Components of an optical system, WDM, optical routing. | 6 |

**Text Books / References:**

1. Thiagarajan Viswanathan, "Telecommunication switching systems and network", PHI learning private limited, 1992.
2. J.E.Flood, "Telecommunication switching Traffic & Networks" , Pearson Education, 2002
3. W. Stallings, "Data and Computer Communications", 6th edition, Prentice Hall, 2000.
4. A. S. Tanenbaum, "Computer Networks", 2nd edition, Prentice Hall, 1989.
5. Behrouz A Forouzan, "Data Communications and Networking", 4th edition, Tata Mc Graw Hills & Sons.
6. John C. Bellamy, "Digital Telephony" , 3rd edition, John willey and sons.
7. Gerd Keiser, "Local Area Network", 2nd edition, Tata Mc Graw Hills and Sons.

**Course Title:** ELECTIVE I (Departmental)
**Course Code:** **1317E01(I)
**L-T-P-C: 3-0-0-3**

| | |
|---|---|
| Class Hours/week | 3 |
| Expected weeks | 12 |
| Total hrs. of classes | 36 |

**EMBEDDED SYSTEM**

| MODULE | TOPIC | COURSE CONTENT | HOURS |
|---|---|---|---|
| **1.** | **INTRODUCTION** | What is an embedded system? Overview of embedded systems, embedded system design challenges. Embedded hardware units and devices in a system, Embedded software in a system, Examples of embedded systems, Classification of embedded systems. Processor and memory organization, processor and memory selection. | 4 |
| **2.** | **DEVICES AND COMMUNICATION BUSES FOR DEVICE NETWORKS** | I/O Types and Examples, Serial Communication Devices, Parallel Port Devices, Interfacing Features in Device Ports, Wireless Communication Devices, Timer and Counting Devices, Watchdog Timers, Real Time Clocks. Parallel communication network using the ISA, pci, pci-x and advanced buses. | 10 |
| **3.** | **INTERRUPTS** | Interrupt service routine, Interrupt latency. Polled I/O issues. Thread and device driver concept. Interrupt sources; Interrupt servicing (handling) mechanism, Shared Data Problem, Multiple interrupts, Context and the periods for context switching, interrupt latency and deadline. Preemptive and non-preemptive multitasking. Critical section. Survey of software Architecture, Round Robin, Round Robin with Interrupts, function Queues, scheduling. Direct memory access. Device driver programming, Parallel port device drivers in a system. Serial port device drivers in a system, Timer devices. | 10 |
| **4.** | **REAL TIME OPERATING SYSTEM** | Embedded operating system, Comparison with general purpose OS. RTOS Tasks, states, Semaphores and shared data. Concept of semaphores, problem of sharing data by multiple tasks and routines, inter process communication. More operating systems services - Message Queues, mail Boxes, timers, events, memory management, synchronisation, control blocks.<br>**Scheduling**: conventional scheduling, deadline driven scheduling, rate monotonic scheduling, deadlock, watchdog timer. Encapsulating semaphores and Queues. Hardware software co- | 12 |

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|---|---|---|---|
| | | design aspects in embedded systems. **RTOS programming**: Micro C/OS-II and Vx Works, Types of real- time operating systems, RTOS mC/OS-II, RTOS Vx Works. | |

**Text books/ References:**


1. Raj Kamal, Embedded systems. Architecture, programming and design, Tata McGraw Hill, 2003
2. An Embedded software Primer - David E. Simon: Pearson Education, 1999
3. Jonathan W Valvano, Embedded Microcomputer systems, Real time interfacing, Thomson Brooks/col 2002.
4. Raj Kamal, Microcontrollers architecture, programming, interfacing and system design, pearson education.
5. Embedded System Design: A Unified Hardware/Software Introduction – Frank Vahid, Tony Givargis, John Wiley & Sons, Inc.2002
6. Embedded Systems Architecture – A Comprehensive Guide for Engineers and Programmers , Tammy Noergaard, Elsevier Publication, 2005
7. Embedded C programming, Barnett, Cox & O'cull, Thomson (2005).
8. Shibu, Introduction to to Embedded Systems, TMH

**Course Title:** ELECTIVE I (Departmental)
**Course Code:** **1317E01(II)
**L-T-P-C: 3-0-0-3**

| | |
|---|---|
| Class Hours/week | 3 |
| Expected weeks | 12 |
| Total hrs. of classes | 36 |

**INFORMATION THEORY AND CODING**

| MODULE | TOPIC | COURSE CONTENT | HOURS |
|---|---|---|---|
| 1. | **SOURCE CODING** | Uncertainty and information, average mutual information and entropy, information measures for continuous random variables, source coding theorem, Huffman Code. | 5 |
| 2. | **CHANNEL CAPACITY AND CODING** | Channel models, channel capacity, channel coding, information capacity theorem, Shannon limit. | 5 |
| 3. | **LINEAR AND BLOCK CODES FOR ERROR CORRECTION** | Matrix description of linear block codes, equivalent codes, parity check matrix, decoding of a linear block code, perfect codes, Hamming codes generator. | 6 |
| 4. | **CYCLIC CODE** | Polynomials, division algorithm for polynomials, a method for generating cyclic codes, matrix description of cyclic codes, Golay codes. | 6 |
| 5. | **BCH CODES** | Primitive elements, minimal polynomials, polynomials in terms of minimal polynomials, examples of BCH codes. | 6 |
| 6. | **CONVOLUTION CODES** | Tree codes, Trellis codes, polynomial description of convolution codes, distance notions for convolution codes, the generating function, matrix representation of convolution codes, decoding of convolutional codes, distance and performance bounds for convolution codes, examples of convolution codes, Turbo codes and Turbo decoding. | 8 |

**Texts/ References:**


1. Information Theory, Coding and Cryptography- Ranjan Bose, TMH
2. Information and Coding- N. Abramson, McGraw Hill
3. Introduction to Information Theory- M.Mansurpur, McGraw Hill
4. Information Theory- R.B. Ash, Prentice Hall
5. Error Control Coding- Shu Lin and D.J. Costello, Prentice Hall
6. Digital Communication- Bernard Sklar, Pearson Education

**Course Title:** ELECTIVE I (Departmental)
**Course Code:** **1317E01(III)
**L-T-P-C: 3-0-0-3**

| | |
|---|---|
| Class Hours/week | 3 |
| Expected weeks | 12 |
| Total hrs. of classes | 36 |

**SATELLITE COMMUNICATION AND REMOTE SENSING**

| MODULE | TOPIC | COURSE CONTENT | HOURS |
|---|---|---|---|
| **1.** | **INTRODUCTION** | Historical background, Basic Concepts, Frequency allocation for satellite services, Orbital and Spacecraft problems, Comparison of networks and services, modulation techniques. | 2 |
| **2.** | **ORBITAL MECHANISM** | Two body problem, orbital mechanism, geostationary orbit change in longitude, orbital maneuvers, orbital transfer, orbital perturbation. | 4 |
| **3.** | **LAUNCH VEHICLES** | Launch Vehicles, principles of Rocket propulsion, powered flight, Launch vehicle for communication satellites. | 2 |
| **4.** | **RF LINK** | Noise, the basic RF link, satellite links (up and down), optimization RF link, inter satellite link, noise temperature, antenna temperature, overall temperature, propagation factors, rain attenuation model, Tropospheric and Ionospheric effects. | 6 |
| **5.** | **MULTIPLE ACCESS** | FDMA, TDMA, CDMA techniques, Comparison of multiple access techniques, error controlling codes. | 4 |
| **6.** | **REMOTE SENSING** | Satellite subsystems and satellite link design. AOCS, IT & C, Power system, spacecraft antenna, transponder, Friis transmission equation. GT ratio of earth station.<br>**Remote Sensing**<br>a) Basic of remote sensing, Electromagnetic Radiation principles, Atmospheric window, Indian satellite sensing satellite system, Active, Passive ground based and Space based sensing<br>b) Spatial, spectral radiometric and temporal resolution, satellite sensors, | 18 |

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|---|---|---|---|
| | | detectors and scanning technique. FOV and error sources, image analysis and Interpretation weather RADAR, LIDAR, acoustic sounding systems, TRMM, AURA-MLS, Megha Tropiques, Altimeter, Scattering Radiometer.<br>Ground based and radio occulation techniques, spectral response of water, sea surface temperature, wind speed, colour monitor, clouds, water vapour, convective system, trace gases. | |

**Textbooks/ References:**


1. Satellite Communication- D. Roddy (TMH).
2. Global Navigation Satellite Systems- B.S. Rao (TMH).
3. Remote Sensing and GIS- B. Bhatta (Oxford University Press).
4. Remote Sensing of the Environment- J.R. Jenson (Pearson).
5. Remote Sensing- R.A. Schowendt (Academic Press).

**Course Title:** ELECTIVE I (Departmental)
**Course Code:** EE1317E01(IV)
**L-T-P-C: 3-0-0-3**

| | |
|---|---|
| Class Hours/week | 3 |
| Expected weeks | 12 |
| Total hrs. of classes | 36 |

**OPTIMIZATION TECHNIQUES**

| MODULE | TOPIC | COURSE CONTENT | HOURS |
|---|---|---|---|
| 1. | **INTRODUCTION TO OPTIMIZATION** | Introduction, Historical development, Engineering Application of Optimization, Statement of an Optimization problem-Design Vector, Design Constraints, Constraint Surface, Objective Function Surfaces.<br>Classification of Optimization Problems, Optimization techniques, Engineering Optimization Literature. Problems | 8 |
| 2. | **CLASSICAL OPTIMIZATION TECHNIQUES** | Introduction, single variable Optimization, multi-variable Optimization with no constraints, multivariable Optimization with equality constraints, multivariable Optimization with inequality constraints, convex programming problems. | 7 |
| 3. | **LINEAR PROGRAMMING I: SIMPLEX METHOD** | Introduction, Application of Linear Programming, Standard form of a Linear Programming Problem, Geometry of a Linear Programming Problems, Definitions and Theorem, Solution of a system of Linear simultaneous equation, Pivotal reduction of a general system of equation, motivation of the simplex method, Simplex algorithm, two phases of the simplex method | 7 |
| 4. | **LINEAR PROGRAMMING II: ADDITIONAL TOPICS AND EXTENSIONS** | Revised simplex method, duality in linear programming, decomposition principle, sensitivity or postoptimality analysis, Transportation problem, Karmarkar's Method, quadratic programming. | 7 |
| 5. | **NON-LINEAR PROGRAMMING: ONE DIMENSIONAL MINIMIZATION METHODS** | Introduction, unimodal function, Unrestricted search, exhaustive search, dichotomous search, Interval Halving method, Fibonacci method, | 7 |

**Textbooks/References:**


1. Optimization Theory and Application – SS Rao, Wiley Eastern Ltd, 3rd edition
2. Optimization Techniques-Chander Mohan, Kusum Deep, New Age Science.
3. Optimization Techniques-Paban Kumar Oberoi, Global Vision Publishing House
4. Computer based Optimization Techniques-Tanweer Alam- A.B.Publications
5. Operation Research-An Introduction-TAHA H A,Prentice Hall

**Course Title:** ELECTIVE II (Humanities)
**Course Code:** HS1317E02(I)
**L-T-P-C: 2-0-0-2**

| | |
|---|---|
| Class Hours/week | 2 |
| Expected weeks | 12 |
| Total hrs. of classes | 24 |

**VALUE EDUCATION, HUMAN RIGHTS AND LEGISLATIVE PROCEDURE**

| MODULE | TOPIC | COURSE CONTENT | HOURS |
|---|---|---|---|
| 1. | **VALUES AND SELF DEVELOPMENT** | Social values and individual attitudes, Work ethics, Indian vision of humanism, Moral and non moral valuation, Standards and principles, Value judgments. Importance of cultivation of values, Sense of duty, Confidence, National unity, Patriotism, Love for nature, Discipline. Devotion, Self reliance. | 5 |
| 2. | **PERSONALITY AND BEHAVIOUR DEVELOPMENT** | Soul and scientific attitude, Positive thinking, Integrity and discipline, Punctuality, Love and kindness, Avoiding fault finding, Free from anger, Dignity of labor, Universal brotherhood and religious tolerance, Happiness vs. suffering love for truth, Aware of self destructive habits, Association and cooperation | 4 |
| 3. | **CHARACTER AND COMPETENCE** | Science vs. God, Holy books vs. blind faith, Self management and good health, Science of reincarnation, Equality, Nonviolence, Humility, Role of women, All religions and same message, Mind your mind, Self control | 4 |
| 4. | **HUMAN RIGHTS** | Jurisprudence of human rights nature and definition, Universal protection of human rights, Regional protection of human rights, National level protection of human rights, Human rights and vulnerable groups. | 5 |
| 5. | **LEGISLATIVE PROCEDURES** | Indian constitution, Philosophy, fundamental rights and duties, Legislature, Executive and Judiciary, Constitution and function of parliament, Composition of council of states and house of people, Speaker, Passing of bills, Vigilance, Lokpal and functionaries. | 6 |

**Textbooks:**

1. Chakraborty, S.K., Values and Ethics for Organizations Theory and Practice, Oxford University Press, New Delhi
2. Kapoor, S.K., Human rights under International Law and Indian Law, Prentice Hall of India, New Delhi
3. Basu, D.D., Indian Constitution, Oxford University Press, New Delhi

***Reference Books:***

1. Frankena, W.K., Ethics, Prentice Hall of India, New Delhi,
2. Meron Theodor, Human Rights and International Law Legal Policy Issues, Vol. 1 and 2, Oxford University Press, New Delhi

# PRACTICALS

**Course Title:** LINEAR INTEGRATED CIRCUITS LAB
**Course Code:** EC131711
**L-T-P-C: 0-0-2-1**
**Expected No. of weeks : 12 (approx)**

| EXPERIMENT NO | AIM OF EXPERIMENT | HOURS |
|---|---|---|
| 1 | Design an inverting amplifier whose closed loop gain *A* is 5. | 3 |
| 2 | Design a non-inverting amplifier whose closed loop gain *A* is varying:<br>(a) ***A*** greater than equal to 1 V/V and less than equal to 5 V/V<br>(b) ***A*** greater than equal to 0.5 V/V and less than equal to 2 V/V | 3 |
| 3 | Design an adder circuit. | 3 |
| 4 | Design an integrator circuit. Study the responses for the inputs (i) sine wave (ii) square wave. | 3 |
| 5 | Design a window detector circuit showing three level detectors with indicator. | 3 |
| 6 | Design a half wave precision rectifier. | 3 |
| 7 | Design active filters: low pass, high pass, notch filter. | 3 |
| 8 | Design a digital to analog converter. | 3 |
| 9 | Design an analog to digital converter. | 3 |
| 10 | To study IC Timer 555 and its application. | 3 |
| 11 | Study of Phase Locked Loop NE 565 PLL IC; (i) to find natural frequency of the VCO, (ii) to determine the 'Lock Range'., (iii) to determine the 'Capture Range'. | 3 |
| | **TOTAL** | 33 |

**Course Title:** VLSI AND VHDL LAB
**Course Code:** EC131712
**L-T-P-C: 0-0-2-1**
**Expected No. of weeks : 12 (approx)**

| EXPERIMENT NO | AIM OF EXPERIMENT | HOURS |
|---|---|---|
| 1 | Write dataflow VHDL description of a 4:1 MUX. Simulate and verify the design using ISE simulator. | 3 |
| 2 | Write behavioral VHDL description of a 4:1 MUX using<br>a) CASE statement<br>b) WHEN-ELSE statement<br>Simulate and verify the design using ISE simulator | 3 |
| 3 | Design a full adder using half-adder. Write structural VHDL description of a full adder using half adder circuits. Simulate and verify the design using ISE simulator | 3 |
| 4 | Write structural VHDL description of generic ripple carry adder in VHDL. Use GENERATE statement. Simulate and verify the design using ISE simulator. | 3 |
| 5 | Write behavioral VHDL description of 3:8 address decoder in VHDL. Simulate and verify the design using ISE simulator. | 3 |
| 6 | Write behavioral VHDL description of following flip flops<br>(a) S-R FF<br>(b) J-K FF<br>(c) T FF<br>(d) D FF<br>All flip flops to have preset and clear input terminals. Simulate and verify the design using ISE simulator. | 3 |
| 7 | Write behavioural VHDL description of a decade up-counter having<br>a) synchronous reset and<br>b) asynchronous reset.<br>Simulate and verify the design using ISE simulator. | 3 |
| 8 | Write behavioural VHDL description of a circuit that generates a digital signal of frequency 1Hz from a digital signal of frequency 50MHz. | 3 |
| 9 | Write behavioural VHDL description of a shift register<br>a) Serial IN serial OUT<br>b) Serial IN parallel OUT<br>Simulate and verify the design using ISE simulator | 3 |
| 10 | Write behavioural description of finite state machine in VHDL. Simulate and verify the design using ISE simulator. | |
| | **TOTAL** | 30 |

| | | |
|---|---|---|
| EC131715 | **PROJECT** | L = 0<br>T = 0<br>P = 8<br>C = 4 |
| GUIDELINES WILL BE UPLOADED BY THE UNIVERSITY FROM TIME TO TIME | | |
| EC131721 | **SEMINAR ON SUMMER TRAINING** | L = 0<br>T = 0<br>P = 0<br>C = 1 |
| GUIDELINES WILL BE UPLOADED BY THE UNIVERSITY FROM TIME TO TIME | | |