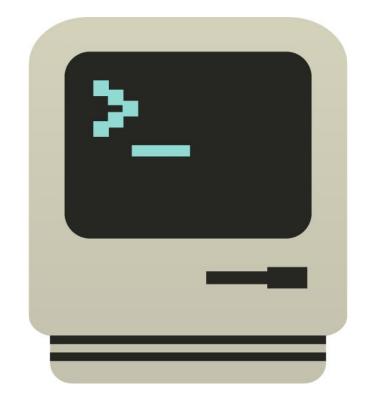
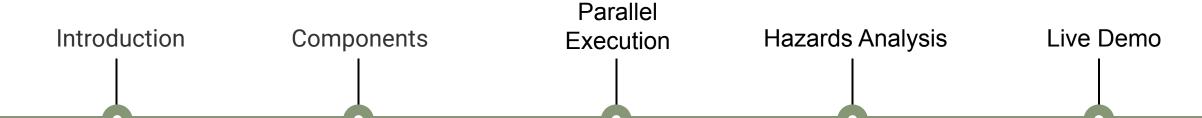
# Project 3 MIPS Simulator



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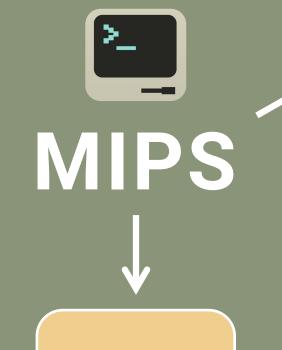
#### Components

CPU

- Register32 RegistersPC and IR
- Fuctional Unit

  IF ID EX

  MEM WB



Mem

- Instruction Mem
- Data Mem

Machine code Input

Display Statistics

### Components

Class cpu{ public:



Registers[]; // 32 Regs, IR, PC Control unit; // 8 control signals Latch value; // for 4 piepeline regs Other flag signals; // for each stage

int FuctionUnit(); // 5 funcs for 5 stages
int hazard\_check(); // at ID stage
void EX\_ALU(data1, data2, ALUOp);

#### CPU

- Cpu.cpp
- Cpu\_unit.cpp
- Cpu\_IF.cpp
- Cpu\_ID.cpp
- Cpu\_EX.cpp
- Cpu\_MEM.cpp
- Cpu\_WB.cpp

#### Components

Mem



Memory.h



Memory.cpp

Class Memory{
public:
 int Mem[]; // IMem and DMem
 void loadMem();
 void showMem();
 void intMem();
 void charMem();

1/0



code.txt



MipsDemo.cpp

#include <fstream>



## How to increase CPU Throughput?



### Consider Pipelining



## Parallel Execution in C++





MipsDemo.cpp

```
while(current<input){
    object.WB();
    object.MEM();
    object.EX();
    object.hazard_check;
    object.ID();
    object.IF();
}</pre>
```

In Specific Order!

### Hazard Analysis

branch

**Control Hazard** 

## 0

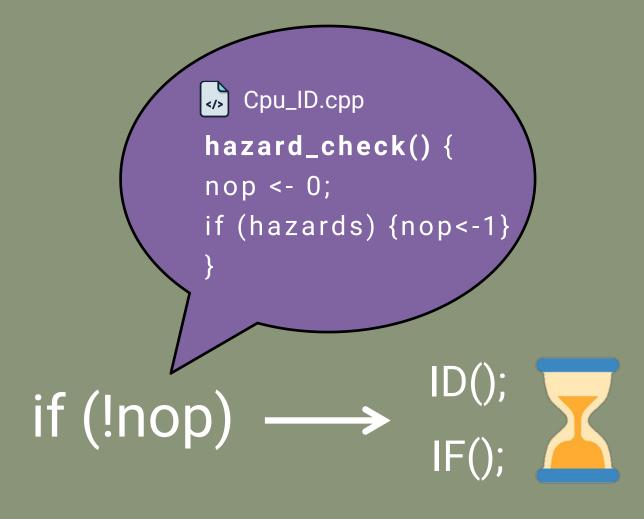
hazard check();

#### Data Hazard

```
rs <- binary2int(IR,25,21)
rt <- binary2int(IR,20,16)

if (regBusy[rs] or
    regBusy[rt]) {
    ......
}</pre>
```

#### Hazards must be taken into account and be resolved



"NOP"



be inserted to ask

IF/ID to stop and wait

## Live Demo!







#### THANK YOU!

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