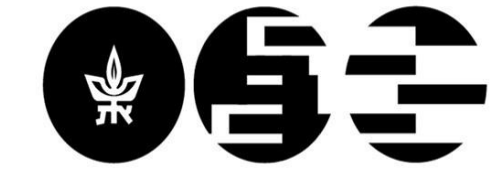

Digital High-Frequency Source on a Chip - Digitally Controlled Oscillator

Project Number: **22-1-12723**

Project Report

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Project Carried Out at: Tel Aviv University and Intel

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Abstract

This project's objective is building a digital phase-locked loop (DPLL), with our team focusing on the design of a digitally controlled oscillator (DCO), which is recognized as the fundamental core of the DPLL.

A DPLL is a closed-loop frequency-control system that compares the phase difference between the input and the output signal of a DCO. The negative feedback loop of the system forces the PLL to be phase locked.

This project contributes to a broader chip manufacturing initiative utilizing Intel's 16 nm FinFET technology aimed at developing a precise on-chip frequency source for advanced wireless communication applications.

The DCO design integrates an inductor and a capacitor bank and matrix controlled by digital switches, targeting a 10 GHz frequency with a 10% tuning range.

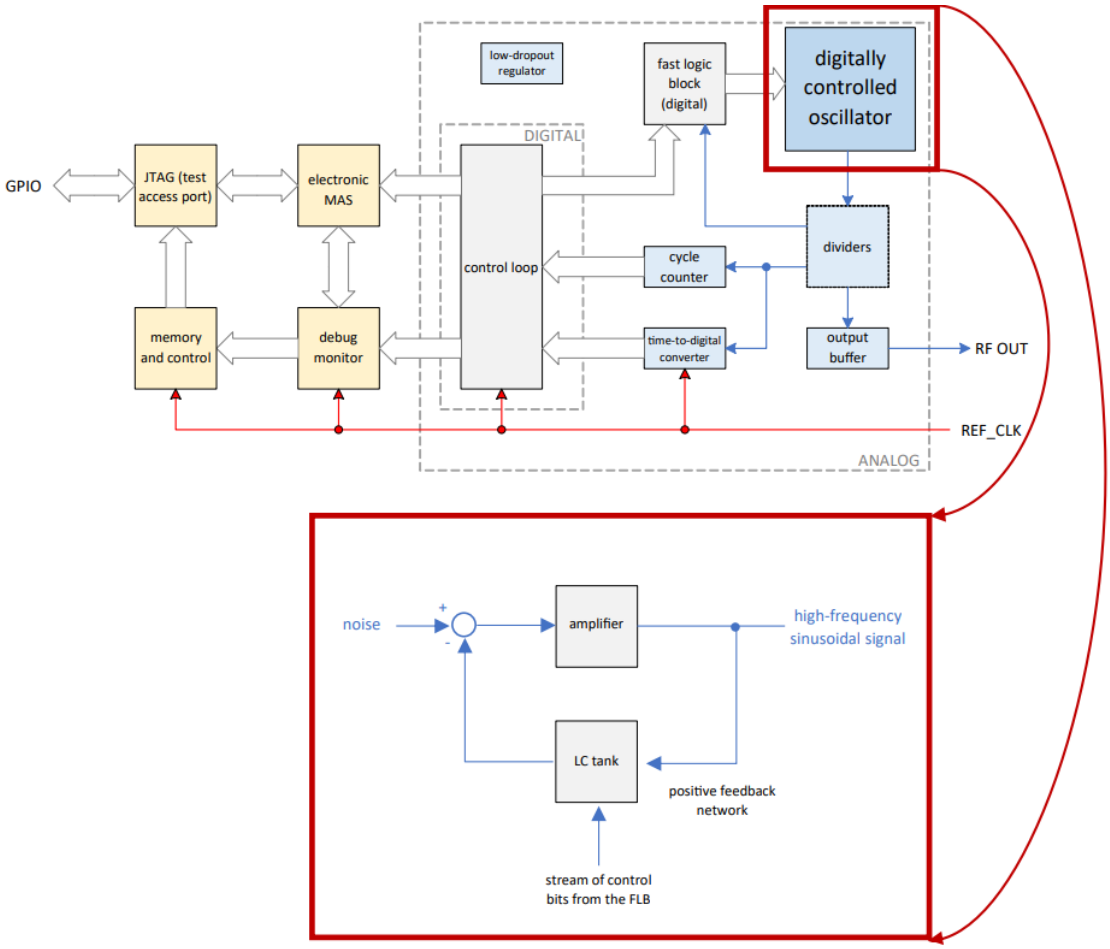

Figure 1: Block diagram of the DCO within the DPLL

1 Introduction

The motivation behind this project lies in designing a digitally controlled oscillator, as the core block of a DPLL, capable of delivering a stable and precisely controlled output frequency that can meet modern communication requirements.
Phase-locked loops are widely employed in digital radio and TV broadcasting, telecommunications, computers, radar systems, power electronics, etc. One can use a PLL to generate stable frequencies, recover signals from a noisy communication channel, or distribute clock signals.
In wireless communication, for example, precise frequency control is essential for ensuring signal integrity and minimizing interference. The DPLL offers the potential to achieve unparalleled levels of frequency precision. This not only meets the demands of emerging communication standards, but also positions the technology for applications such as 5G and beyond, where higher frequencies enable increased data transfer rates and reduced latency.
One alternative to a DCO is a voltage-controlled oscillator (VCO), which is an electronic oscillator whose output frequency is proportional to its input voltage and is determined by the voltage. DCOs operate in a very different way than VCOs, in a result of which DCOs have a much more seamless integration withing an all-digital PLL. This removes the need for additional circuitry to decipher the digital information coming from the loop filter, which would introduce additional noise and complexity. In addition, the digital control of a DCO is less susceptible to noise than that of a VCO.
Withing DCOs, one alternative to an LC oscillator is a ring oscillator, which has the disadvantage of high phase noise and higher power consumption.

2 Theoretical background

2.1 Digital Phase-Locked Loop (DPLL)

A digital phase-locked loop (DPLL) is a control system that aligns the phase of its output signal with that of an input reference signal. It operates as a feedback loop, adjusting the frequency of a digitally controlled oscillator (DCO) to minimize the phase difference between the input and output signals. A DPLL's key components include:

1. **Phase Detector (PD)**: Compares the phase of the input and output signals, generating an error signal proportional to the phase difference.
2. **Loop Filter**: Processes the error signal to smooth out noise and rapid changes.
3. **Digitally Controlled Oscillator (DCO)**: Produces the output frequency, controlled by digital inputs that adjust components like capacitors or inductors.

In a closed loop, the phase detector generates a digital error signal, which is filtered and used to adjust the DCO's frequency. This process continually reduces phase error, locking the output signal's phase and frequency to the reference, maintaining synchronization even with minor disturbances or noise.

2.2 Digitally Controlled Oscillator (DCO)

A digitally controlled oscillator is a key component in digital phase-locked loops (DPLLs) providing a stable and adjustable frequency output. Unlike traditional analog oscillators, which use continuous voltage or current control, DCOs rely on digital control signals to adjust their frequency. This makes DCOs more precise, robust, and suitable for integration in modern digital systems.

A DCO generates a periodic output signal, such as a square wave or sine wave, where the frequency is determined by a set of digital control inputs. These inputs typically adjust the oscillator's resonating circuit, the LC tank, built from passive components like capacitors and inductors, like in our design, or in some cases, ring oscillators formed by a series of inverters. The natural frequency of this core is determined by the values of these components.

A DCO contains digital control logic that receives digital control signals and converts them into discrete adjustments to the oscillator core's components. For example, our DCO uses a switched capacitor bank and matrix, where different capacitor values are

activated based on the control signals. Similarly, an array of inductors can be digitally switched in or out of the circuit to modify the frequency.
The following are several key concepts related to the implementation of an LC tank-based DCO with variable capacitance.

2.2.1 Frequency Tuning

The resonant frequency of an LC tank with an inductance L and capacitance C is given by:

$$(1)\ f = \frac{1}{2\pi\sqrt{LC}}.$$

Differentiating this relation with respect to C, and assuming that the fixed capacitance is much greater than the variable capacitance, we obtain the following relationship between the change in frequency df and the change in capacitance dC_{var} :

$$(2)\ df \approx -2\pi^2 \cdot f_{max}^3 \cdot L \cdot dC_{var}$$

where f_{max} is the upper oscillation frequency.
The capacitance of the individual components can be extracted from an S-parameter analysis using the following relation:

$$(3)\ C = \frac{1}{2\pi f X_C}$$

2.2.2 Temperature-Driven Sub-Band Overlap

Oscillators', the output frequency can drift due to changes in temperature. This can degrade signal stability and accuracy. One of the ways to mitigate the effects of frequency drift is to ensure a frequency overlap between the sub-bands of the oscillator. The desired overlap is calculated as follows:

$$(4)\ OL = \frac{2\chi \cdot dT \cdot f_{min}}{2\pi^2 \cdot {f_{min}}^3 \cdot L \cdot dC_{var}}$$

where χ is the frequency drift, dT is the operational temperature range, f_{min} is the lower oscillation frequency, L is the inductor's inductance, and dC_{var} is the smallest change in capacitance which is used to switch between frequencies.

2.2.3 Phase Noise and Maximum Inductance

Phase noise refers to the random fluctuations or deviations in the phase of the oscillator's output signal over time. In order to maintain it withing acceptable limits, the following inductance limitation can be imposed:

$$(5)\ L_{max} = \frac{\mathcal{L}\{\omega_n\}_{max}\ Q\ \omega_m^2\ V_{DD}^2}{2kT\ \omega_{o,\,max}^3(1+F)}$$

where $\mathcal{L}\{\omega_n\}_{max}$ is the maximum allowed phase noise, Q is the quality factor, ω_n is the offset from the output angular frequency, V_{DD} is the supply voltage, k is the Boltzmann constant, T is the operational temperature, $\omega_{o,max}$ is the upper angular frequency of oscillation, and F is the noise figure of the active devices.

In order to extract the inductance from an S-parameter analysis, the following formula is used:

$$(6)\ L = \frac{X_L}{2\pi f}$$

2.2.4 Q Factor

The Q factor (quality factor) measures how efficiently an oscillator stores energy relative to how much it loses per cycle. A higher Q factor results in better frequency stability, lower phase noise, and a more precise output signal.
The Q factor depends on component quality (inductors and capacitors), CMOS technology integration and operating frequency. In a practical RLC resonator (LC tank), the following equations hold:

$$(7)\ Q_L = \frac{\omega L}{R_L}$$

$$(8)\ Q_C = \frac{1}{\omega C R_C}$$

$$(9)\ Q_T = \left(\frac{1}{Q_L} + \frac{1}{Q_C}\right)^{-1}$$

where Q_L, Q_C, and Q_T are the inductor, capacitor, and total Q factors, respectively. ω is the resonance frequency in radians per second, L is the inductance, C is the capacitance, and R_L and R_C are the series resistances of the inductor and the capacitor, respectively.

3 Simulation

In order to simulate our design, a schematic of a cross-coupled oscillator was assembled. Non-ideal components were chosen from the analog library. The parameters of the components were determined using formula (1) with the goal to achieve a lower oscillation frequency of 8.55 GHz and an upper oscillation frequency of 11.235 GHz, considering that the desired range of the DCO is 9.5 GHz – 10.5 GHz and taking 10% below and 7% above as a spare.

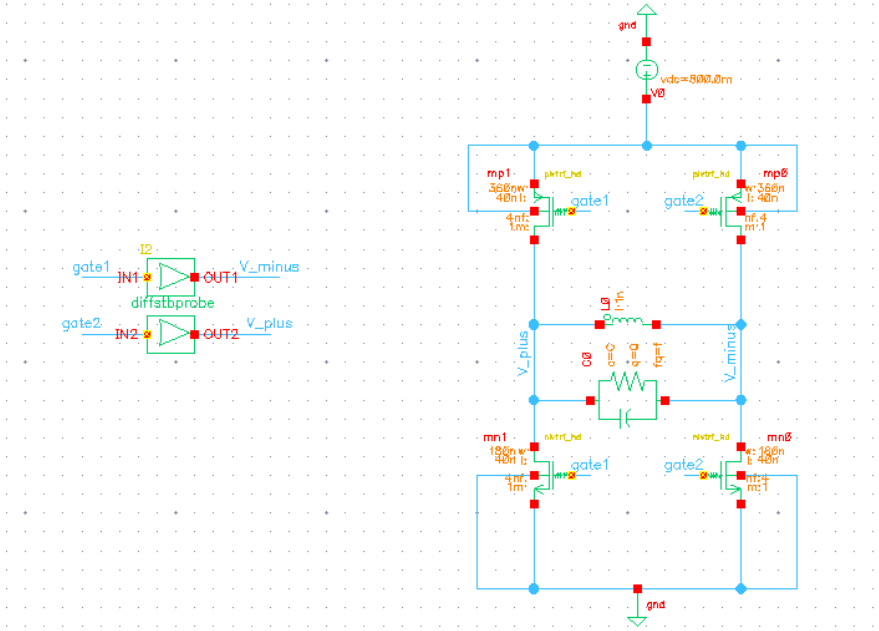

Figure 3: Schematic of a cross-coupled oscillator

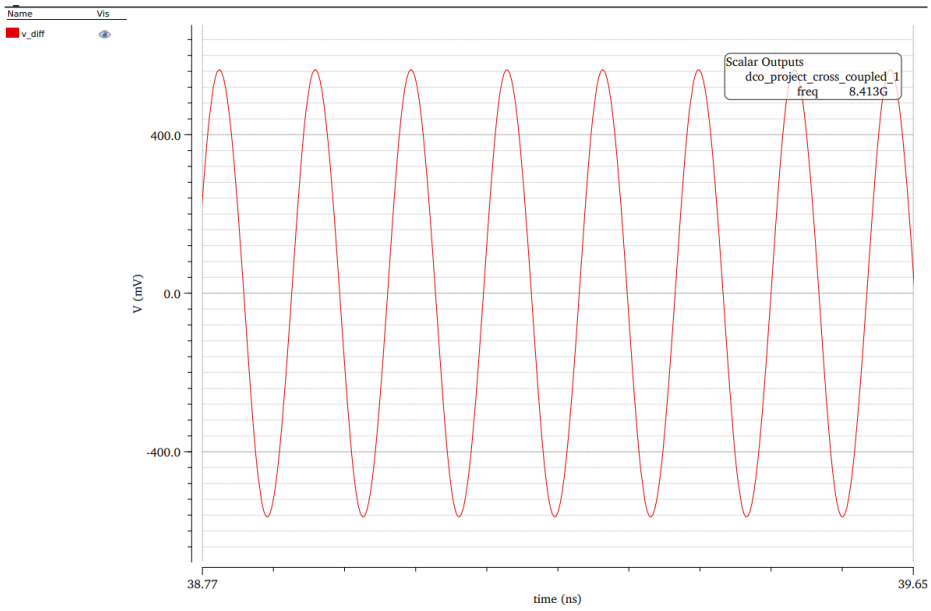

Figure 2: Simulation of the oscillations - lower frequency

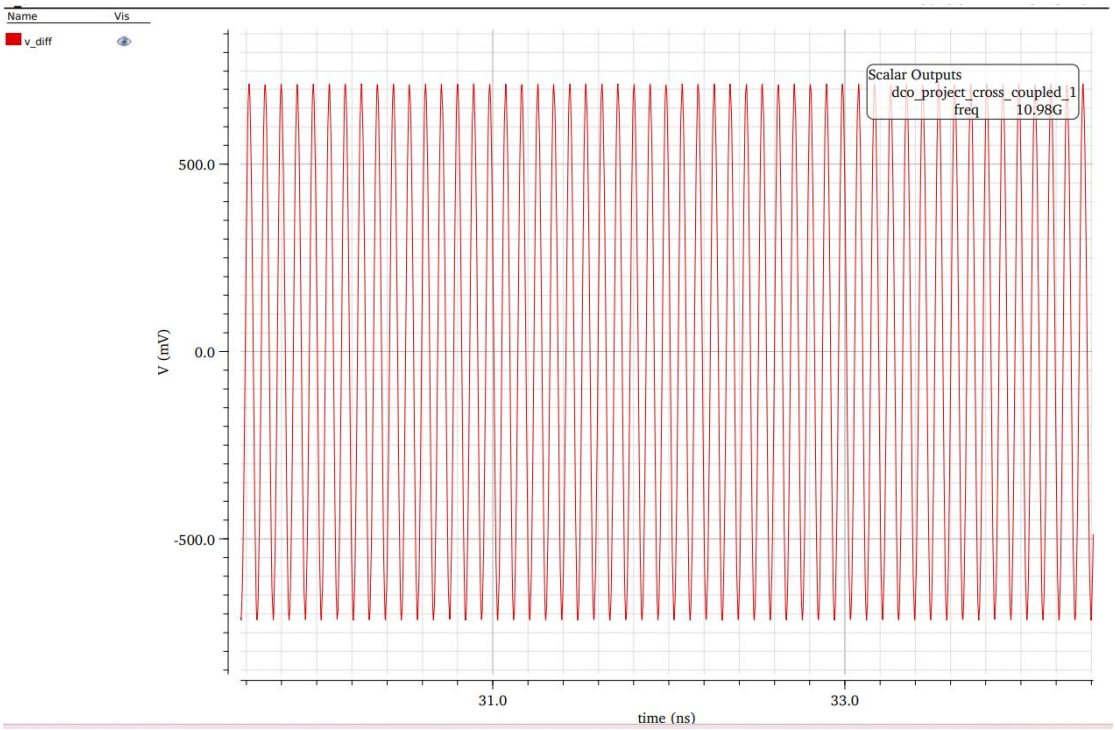

Figure 4: Simulation of the oscillations - upper frequency

Name	Type	Details	Value
v_plus	signal	/V_plus	
v_minus	signal	/V_minus	
Loop Gain Phase	expr	phaseDegUnwrapped(getData("loopGain" ?result "stb"))	
Loop Gain dB20	expr	db(mag(getData("loopGain" ?result "stb")))	
v_diff	expr	(VT("/V_plus") - VT("/V_minus"))	
freq	expr	frequency(v_diff)	8.413G

Figure 5: Simulation results - lower frequency

Name	Type	Details	Value
v_plus	signal	/V_plus	
v_minus	signal	/V_minus	
Loop Gain Phase	expr	phaseDegUnwrapped(getData("loopGain" ?result "stb"))	
Loop Gain dB20	expr	db(mag(getData("loopGain" ?result "stb")))	
v_diff	expr	(VT("/V_plus") - VT("/V_minus"))	
freq	expr	frequency(v_diff)	10.98G

Figure 6: Simulation results - upper frequency

As expected, the results are not ideal since non-ideal components are used.

4 Implementation

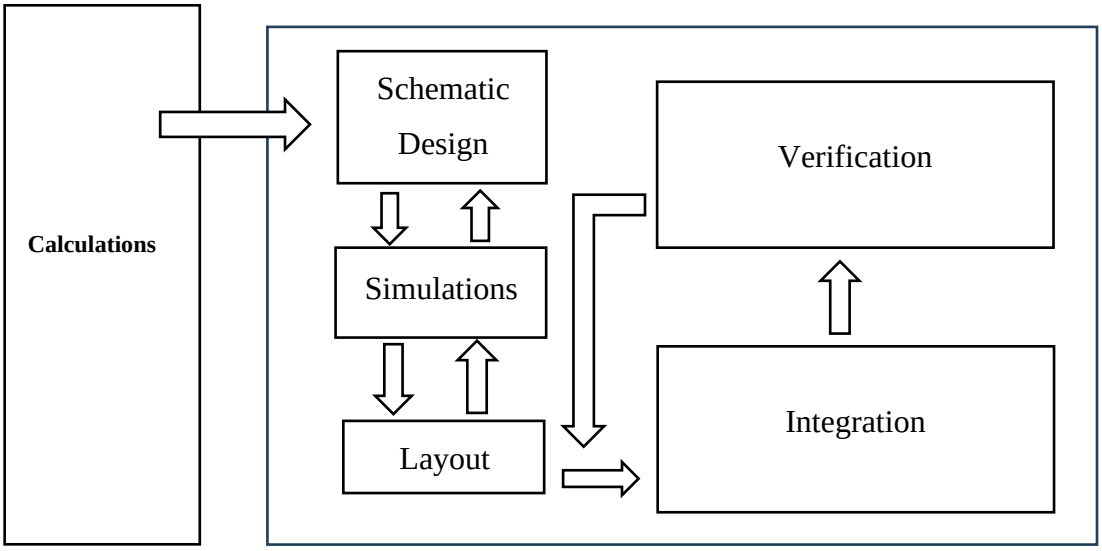

Figure 7: The Implementation methodology

To implement The DCO, several platforms are used:

1. GitHub - The project is a part of a bigger project (The DPLL).
   This platform is a collaborative platform used for version control and project management.
2. Cadence Virtuoso – A major part of the project was conducted in Cadence Virtuoso, starting from the design stage, through the simulation, implementation and running tests. The following tools and technologies we used:
   a. Intel 16 nm FinFET technology – chip implementation and testing
   b. The Calibre RVE is – layout editing
   c. The Cadence Quantus Extraction Solution –extraction

In this project, some of the components are built from scratch to meet the specifications.

The DCO circuit is made of two main sub-blocks: the LC tank and the amplifier.

4.1 The LC tank

This sub-block is made of an inductor, a capacitor bank and a capacitor matrix. The **LC tank** forms the core of the oscillator in a DCO, with the **inductor and capacitor bank and matrix** defining the resonant frequency.

All of the blocks have been verified using DRC and LVS checks, as well as simulations.

4.1.1 Block A – The Inductor

The inductor determines the tank's resonant frequency in combination with the capacitor bank and matrix. According to formula (5), the maximal inductor's inductance is extracted and equal to 5.8nH. To make the implementation of the capacitor matrix simpler, the inductance is chosen to be 1.2nH. The inductor is implemented and built by us to achieve this result.

The inductor is 150μmx150μm and is made of gmb metal and the connector is a gm0 metal. These are high metals – to accomplish not only the required size, but also a relatively high quality factor (Q) and reduced parasitics.

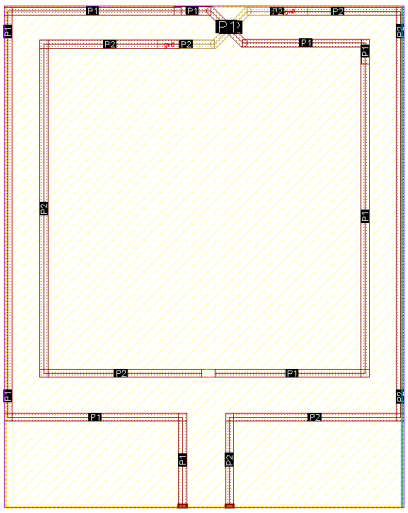

Figure 8: Layout of 1.2nH inductor

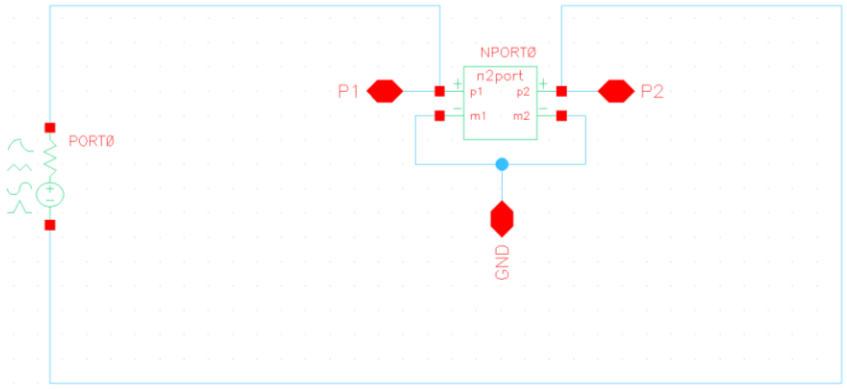

Figure 9: Schematic of the inductor for SP simulation

Name	Type	Details	Value
Z11 reOhm	expr	real(zpm('sp 1 1))	
Z11 imOhm	expr	imag(zpm('sp 1 1))	
L_10.5G	expr	abs(value((imag(zpm('sp 1 1)) / (xval(zpm('sp 1 1)) * 3.14 * 2)) 1.05e+10))	1.238n
Q_10.5g	expr	value((- (imag(zpm('sp 1 1)) / (- real(zpm('sp 1 1))))) 1.05e+10)	20.08

Figure 10: S-parameter calculation of the inductor size and the Q using formulas (6), (7) respectively.

The graph of the simulation can be found in Appendix B.

By varying the **capacitance**, the DCO can achieve precise frequency control while benefiting from the **high-quality factor** of the LC tank for better stability and performance.

4.1.2 Block B – The Capacitor Matrix

The main goal of the capacitor matrix is to perform the fine frequency tunning with the resolution of 1.1MHz. It is made of 256 cells that can be selectively connected or disconnected to create a desired total capacitance to adjust the frequency.
The difference in capacitance between the ON and OFF-states of a single cell, ΔC , is extracted using formula (2) and equal to 32.7aF. The target ΔC is around 50aF, including spare due to parasitics.
Each cell consists of two capacitors and two transistors. The capacitors are the basic building blocks of the cell and were implemented by us to achieve the required ΔC.
They are of type MoM, 0.75μmx0.70μm each, and are made of three metal layers: Metal 4, Metal 5 and Metal 6. All layouts of the matrix are presented in Appendix C.

4.1.2.1 A single capacitor

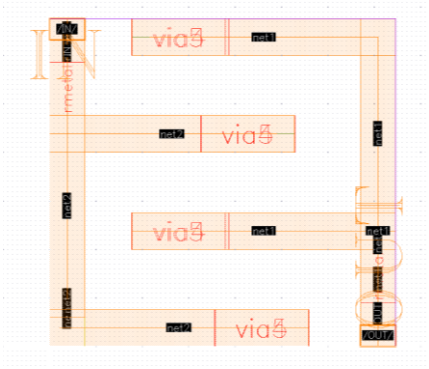

Figure 13: Layout of the ~250aFcapacitor.

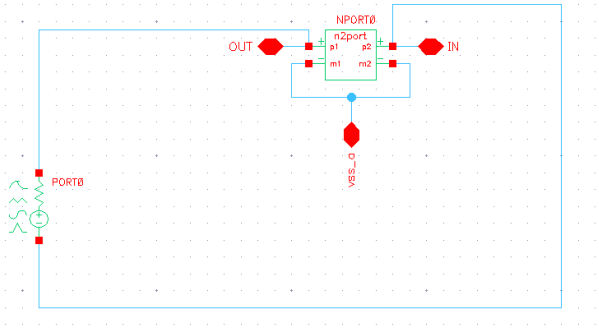

Figure 12: Schematic of a single capacitor for SP simulation

Name	Type	Details	Value
Z11 imOhm	expr	imag(zpm('sp 1 1))	
Z11 reOhm	expr	real(zpm('sp 1 1))	
C_10.5G	expr	abs(value((1 / (xval(zpm('sp 1 1)) * imag(zpm('sp 1 1)) * 3.14 * 2)) 1.05e+10))	247.6a
Q_10.5G	expr	value((- (imag(zpm('sp 1 1)) / real(zpm('sp 1 1)))) 1.05e+10)	4.386K

Figure 11: S-parameter calculation of the capacitor size and the Q using formulas (3), (8) respectively

The graph of the simulation can be found in Appendix C.

4.1.2.2 A single cell

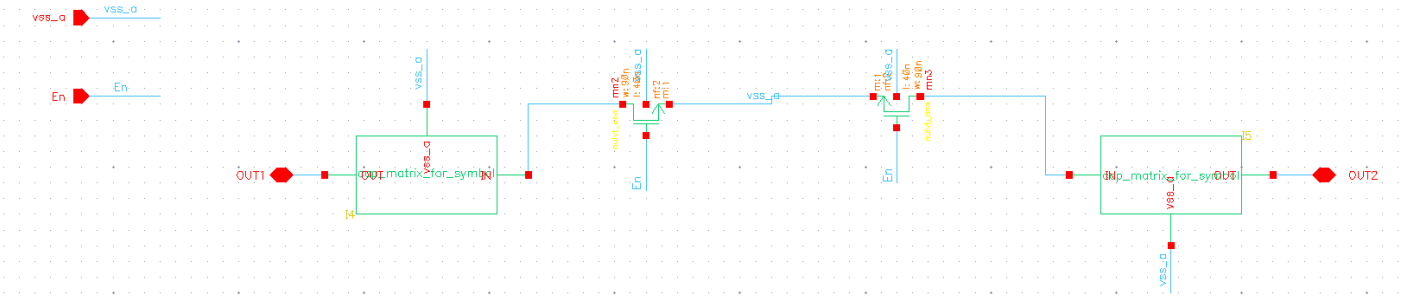

Figure 14: Schematic of A single cell

The schematic used for the simulation of the single cell and the corresponding results can be found in appendices Appendix A and Appendix B, respectively.

The simulation is performed to check the ΔC and the value of Q for both operation modes: Enable = 0 when the cell is OFF and Enable = 1 when the cell is ON.
From this simulation, ΔC of $47.4aF$ is obtained.

4.1.2.3 A single cell with logic

The relation between the inputs of the matrix and the enable signal of a cell is:

(10) $$En[i][j] = \sim col\_off[i] + col[i] \cdot row[j]$$

meaning that cell[i][j] is ON if both col[i] (row) and row[j] (column) are 1,
or if col_off[i] (row) is 0. It is implemented by connecting two NAND gates and the signals Row, Col, and Col_off. This logic block is connected to each cell separately.

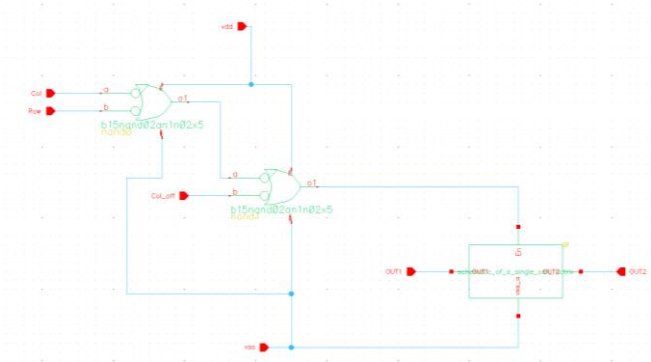

Figure 15: Schematic of A single cell with logic

4.1.2.4 4-cells Block

An in-between block of four cells is added to the hierarchy to ease the routing. This stage contains a schematic and layout, presented in appendices Appendix A and Appendix C, respectively.

4.1.2.5 The Matrix

The last stage of the capacitor matrix includes assembling the whole matrix, routing and simulating the block.

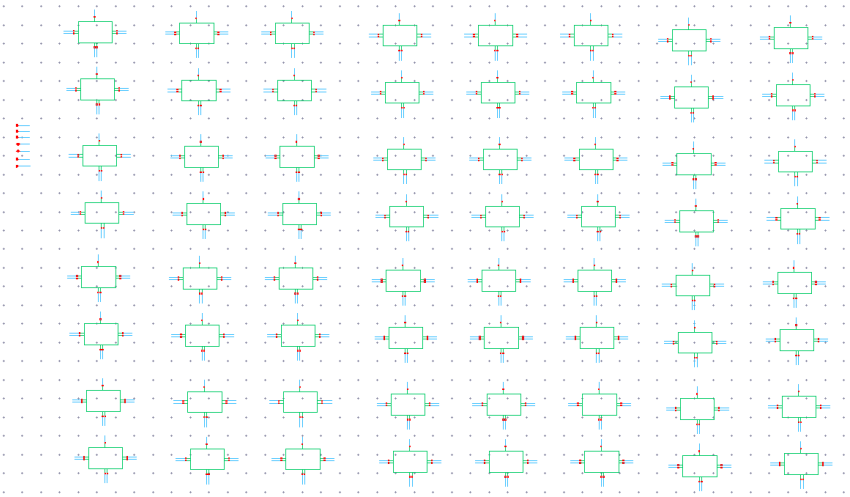

Figure 16: Schematic of the whole matrix, 64 blocks of 4-cells block, in total 256 cells

4.1.2.5.1 Matrix simulation

After DRC and LVS checks are clean, we perform extraction of the block and a simulation to check that the ΔC meets the requirements. The operation of the matrix is presented in figure 17.

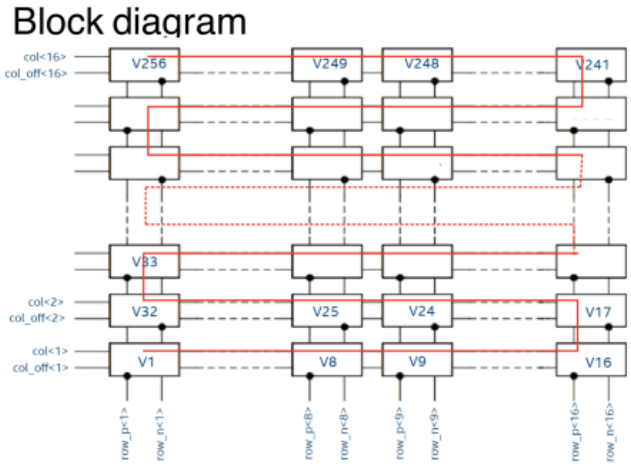

Figure 17: The logic and order of turning ON the cells in the matrix.

The cells are turned ON one by one, starting from cell V1 to V16. Once the first row (col<1>) is ON, V17 cell is the next cell to be turned ON, then V18 until V32 – then the second row (col<2>) is ON. This routine continues until the last cell is turned ON. In order to calculate the ΔC, two simulations are conducted. First, when the matrix is OFF – which is achieved by connecting col<0:15> and Row<0:15> to VSS, and Col_off<0:15> to VDD. Then, when the matrix is ON – which is achieved by connecting col<0:15> and Row<0:15> are to VDD, and Col_off<0:15> to VSS. The schematic used for these simulations is presented in Appendix A.

Each of the simulations should provide the capacitance value and a Q value:

C_10.5G	expr	abs(value((1 / (xval(zpm('sp 1 1)) * imag(zpm('sp 1 1)) * 3.14 * 2)) 1.05e+10))
Q_10.5G	expr	value((- (imag(zpm('sp 1 1)) / real(zpm('sp 1 1)))) 1.05e+10)

Figure 18: S-parameter calculation of the capacitor size and the Q using formulas (3), (8) respectively

dco_project_may...	C_10.5G	51.71f
dco_project_may...	Q_10.5G	42.51

dco_project_may...	C_10.5G	41.29f
dco_project_may...	Q_10.5G	69.89

Figure 19: Results of ON and OFF modes of the matrix

Subtracting the capacitance of the OFF matrix from the capacitance of the ON matrix and dividing it by the number of cells gives us the estimated ΔC of a single cell:

$$\Delta C_{\,One\ Cell} = \frac{C_{\,ON} - C_{\,OFF}}{256} \tag{11}$$

$$\Delta C_{\,One\ Cell} = \frac{51.71 \times 10^{-15} - 41.29 \times 10^{-15}}{256} = 40.07 \times 10^{-18} = 40.07aF$$

4.1.3 Block C – The Capacitor Bank

From formula (4), the number of required sub-bands is determined to be 27. In order to reduce parasitics, further division of the bank into two coarse cells of 36 fF each, and eight fine cells of 4 fF each is implemented. Hence, the capacitor bank consists of two larger cells for coarse tuning, and eight smaller cells for fine tuning.

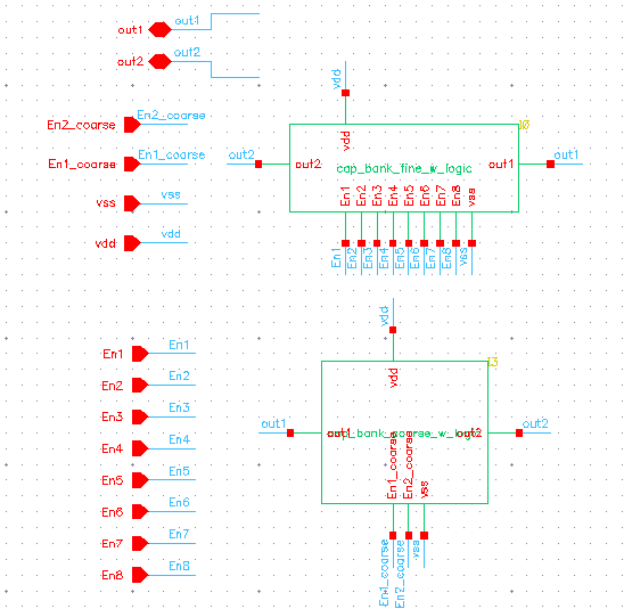

Figure 20: Capacitor bank

The layout of the block and its sub-blocks can be found in Appendix C.

4.1.3.1 Fine-Tuning Sub-block

The cells use differential switches which, in comparison to single-ended switches used in the matrix, improve Q at the expense of the area required for the biasing resistors.

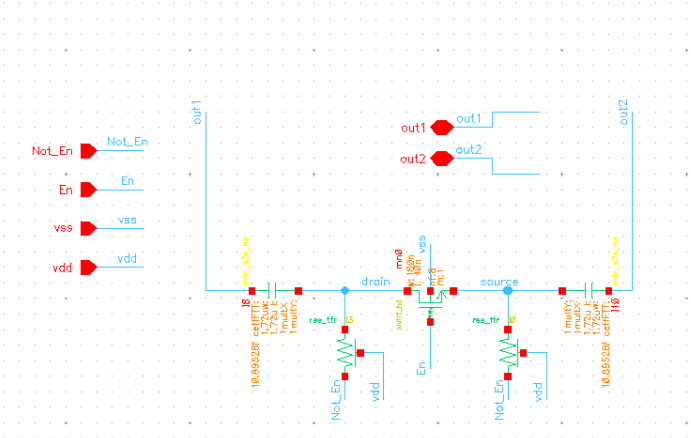

Figure 21: Differentially switched cell for fine tuning

The results of the simulation of a single cell both before and after its extraction can be found in Appendix B. ΔC of 5.03fF and 4.77fF is obtained before and after the extraction, respectively. This corresponds to the goal of 4fF, taken with some spare. It is noted that the Q obtained for the OFF state is too low to correspond to realistic

behavior. This issue was investigated together with the instructor and it was determined that there is likely an issue with the library model of the used transistor. Eight of such cells are connected in parallel in order to create the fine-tuning part of the bank. The cells were also connected to inverters which are needed for the biasing.

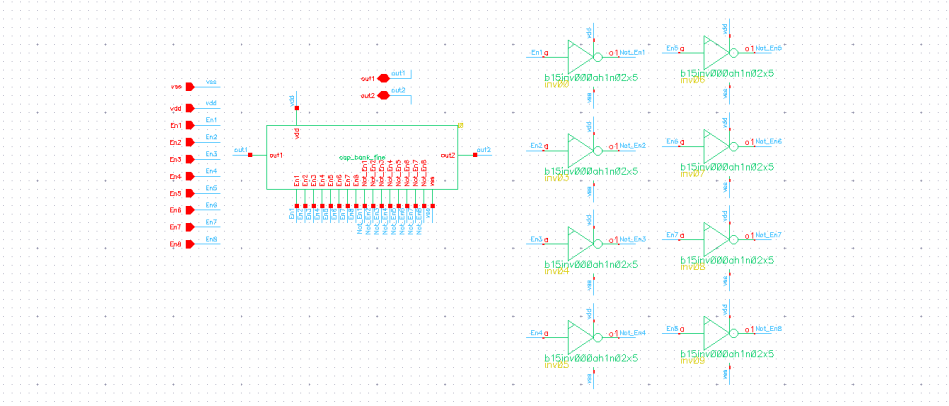

Figure 22: Fine-tuning sub-block of the capacitor bank

4.1.3.2 Coarse-Tuning Sub-block

The cells for coarse tuning are identical to those for fine tuning, except for the sizes of the capacitors and the transistors used. The simulation results and the layout can be found in appendices Appendix B and Appendix C, respectively.

4.1.4 Integrating the LC tank

The final step of the LC tank is to integrate all its sub blocks together – the inductor, the capacitor bank and the capacitor matrix.

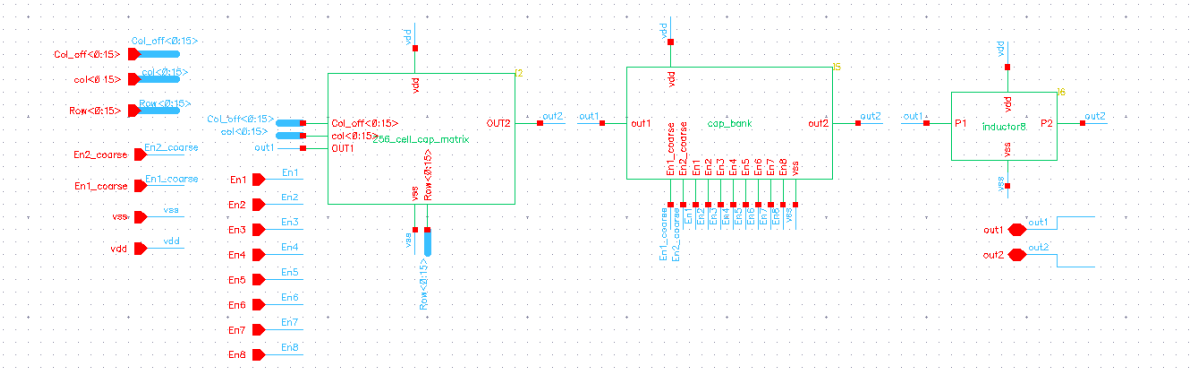

Figure 23: LC tank

4.2 Amplifier

The amplifier's purpose is to boost the output signal of the DCO to a level suitable for driving other circuits or components. This ensures that the signal can be effectively transmitted over longer distances or to load components without significant loss.
The amplifier is composed of four transistors: two PMOS transistors and two NMOS transistors. Its layout is shown in Appendix C.

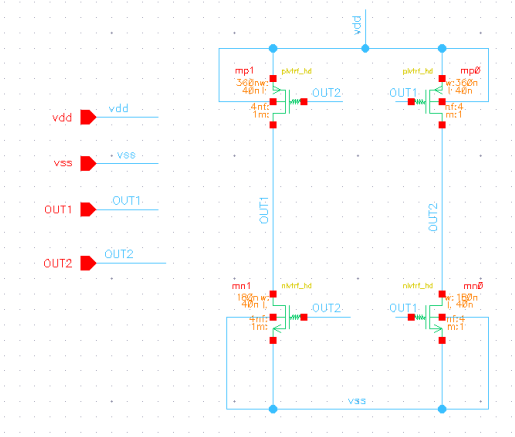

Figure 24: Amplifier

4.3 DCO

The final step of the implementation is the integration of the LC tank with the amplifier, which creates a cross-coupled DCO. The full layout can be found in Appendix B.

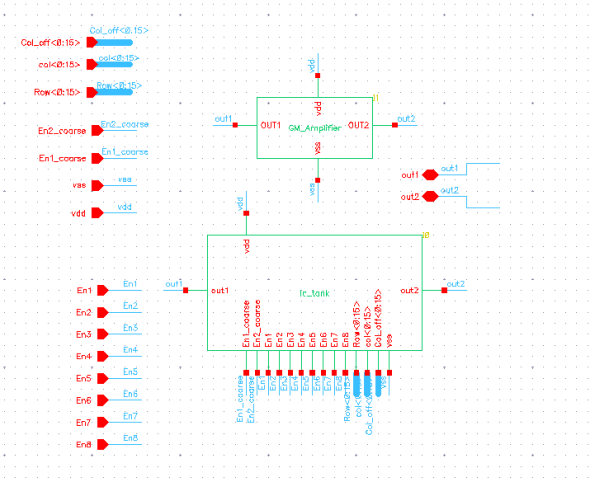

Figure 25: Final schematic of the DCO

4.4 DCO - Final simulations

The simulations were performed both in ON and OFF state (Cap Bank and Cap Matrix inputs are all connected to VDD/VSS respectively), to achieve full frequency cover and examine the results in comparison to the spec requirements.
The following simulations were conducted:
Transient simulation, Stability simulation, HB simulation, HB noise simulation.

All simulations results appear in Appendix B.
As seen in section 5 and in Appendix B, the results are a bit off spec but still in the vicinity of the required results.

The initial simulations' results showed that the gain of the amplifier was too low (i.e the amplifiers are too small comparing to the LC Tank) thus, more amplifiers blocks were connected in parallel to get better results.
An optimal solution would be the increase the size of the amplifiers.

5 Analysis of results

In this section a comparison between spec requirements and simulation results is presented.

The results are a bit off spec but still in the vicinity of the required results.

As expected, the simulation do not perfectly match the targets which will require iterative process of adjustments and simulations which were not conducted due to the challenges described in section 6.

Table 1: Results

	Parameter	Target - spec	Simulation results
1.	Is - Operational current	< 3mA	ON – 2.367 mA OFF – 2.194 mA
2.	f_bot - Bottom oscillation frequency	9.5 GHz (with spare 8.55GHz)	8.98 GHz
3.	f_top - Upper oscillation frequency	10.5 GHz (with spare 11.235 GHz)	12.34 GHz
4.	mtrx_n - Digital varactor capacitor states	256	256
5.	df_mtrx – Minimal jump in tuning range	< 1.2 MHz	1.1 MHz
.6	Pn_100K – Phase noise at 100kHz offset	-77 dBc/Hz	ON – -72.547 dBc/Hz OFF – -64.955 dBc/Hz
.7	Pn_1M – Phase noise at 1 MHz offset	-100 dBc/Hz	ON – -100.130 dBc/Hz OFF – -93.412 dBc/Hz
.8	Pn_10M – Phase noise at 10 MHz offset	-120 dBc/Hz	ON – -122.913 dBc/Hz OFF – -117.403 dBc/Hz

In order to reach the spec above, calculations based on the formulas in section 2.2 were made to extract the basic components' parameters:

	Parameter	Target - spec	Simulation results
9.	Inductor Size	$1.2nH$	$1.238nH$
10.	Capacitor Bank – course capacitors size	$36\ fF$	$38.27fF$
11.	Capacitor Bank – fine capacitors size	$4\ fF$	$4.77\ fF$
12.	Capacitor Matrix – very fine capacitors size	$250aF$	$247.6aF$
13.	Capacitor Matrix – single cell size including parasitic (standalone)	$50aF$	$47.4aF$
14.	Capacitor Matrix – single cell size in the Matrix	$32.7aF$	$40.07aF$

6 Conclusions and further work

In this project, we successfully designed and built all the key components of the Digitally Controlled Oscillator (DCO) and conducted simulations to validate the design. However, during the final stages for a long period of time we were unable to perform the complete set of final simulations, including layout extraction, due to external changes in the code used in the extraction process in the university environment. This issue prevented us from completing the extraction and full simulation process until a day before presentation day. These steps are essential to verify that the DCO meets all required specifications.
As a result, we had only one day left to perform final simulations with no time left to perform any changes in the design to get the exact required specifications.

Throughout the project, we accomplished several key milestones in the development of the DCO. First, we successfully built an inductor with the required inductance for the LC tank, ensuring proper resonance for the oscillator. In addition, we designed small capacitors that enable fine frequency tuning and integrated them with transistors and logic cells to create a tunable capacitor matrix. This matrix allows for precise control over the oscillation frequency. We also developed a two-level capacitor bank, which includes both fine and coarse tuning mechanisms, providing flexibility in frequency adjustments. Furthermore, we integrated all components with an amplifier, resulting in complete DCO. All of our layouts underwent and passed the Design Rule Check (DRC) and Layout Versus Schematic (LVS) verification processes, ensuring that the designs are both physically and electrically correct according to the design specifications. These achievements demonstrate that the foundational elements of the DCO are fully functional and prepared for further testing and optimization.

The final steps performed involved completing the extraction of the final layout and running comprehensive simulations to ensure the DCO operates as intended.
Future work would focus on improving the DCO's performance by increasing frequency accuracy, reducing phase noise, and minimizing the area of the design to make it more efficient for integration into larger systems.

7 Project Documentation

Description of the project files

All project deliverables have been documented in a GitHub repository as required.

This Booklet provides an overview of the deliverables of the project.

The repository is divided into sections according to the sub-blocks in the project:

- **LC TANK –** This section includes schematic files for each one of the sub-components below and the relevant layout as well as the simulations for calculating the components' values
    - **Inductor**
    - **Capacitor Bank**
    - **Capacitor Matrix**
- **Amplifier -** This section includes the schematic and the layout of the amplifier.
- **DCO** – This section includes the schematic and the layout of all the components integrated together

8 References

Books:

[1] Niknejad, A. M. (2007b). *Electromagnetics for High-Speed analog and digital communication circuits*. Cambridge University Press.

[2] Razavi, B. (2011). RF Microelectronics. Prentice Hall.

Papers:

[3] Levinger, R., Levi Roi, Shumaker, E., Levin, S., & Horovitz, G. (n.d.). A 3.9-4.7 GHz 0.35 mW DCO with-187.4 dBc FoM in 28nm CMOS. ResearchGate. https://www.researchgate.net/publication/329175398_A_39-47_GHz_035_mW_DCO_with-1874_dBc_FoM_in_28nm_CMOS

Links:

[4] Wikipedia contributors. (2024, September 10). *Leeson's equation*. Wikipedia. https://en.wikipedia.org/wiki/Leeson%27s_equation

Appendix A. Subject 1 – Intermediate Schematics

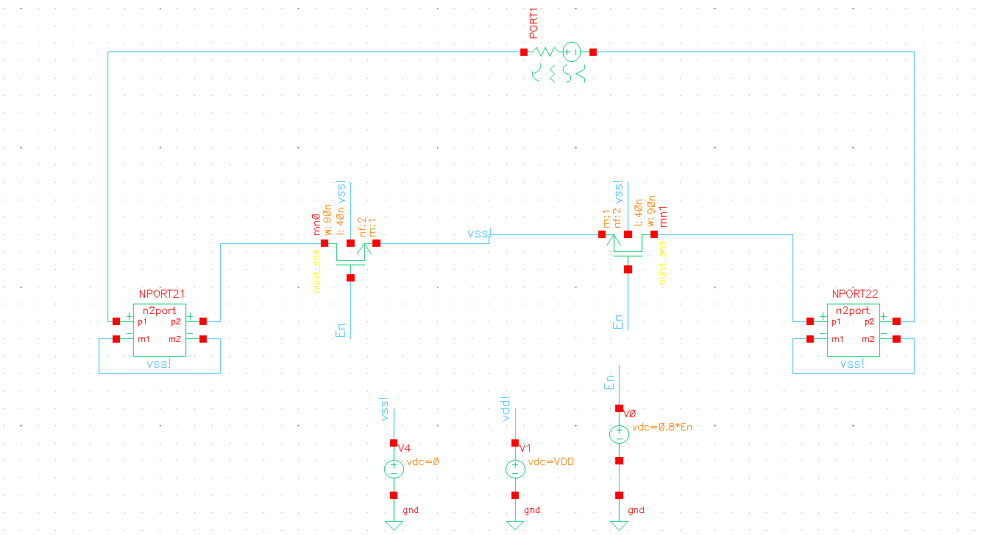

Figure 26: Schematic of A single cell for the simulation of ΔC

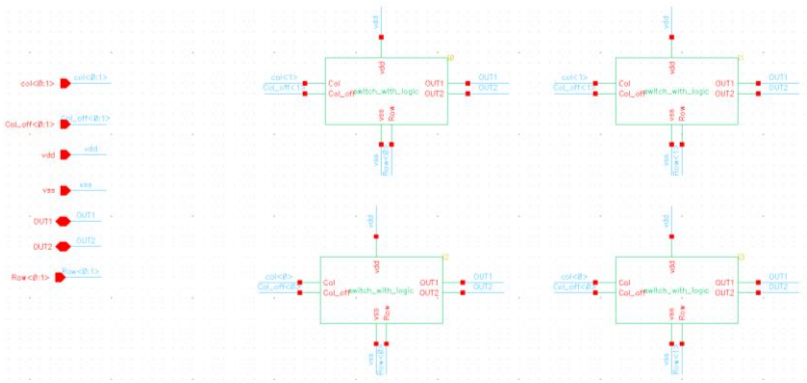

Figure 27: Schematic of A 4-cells block

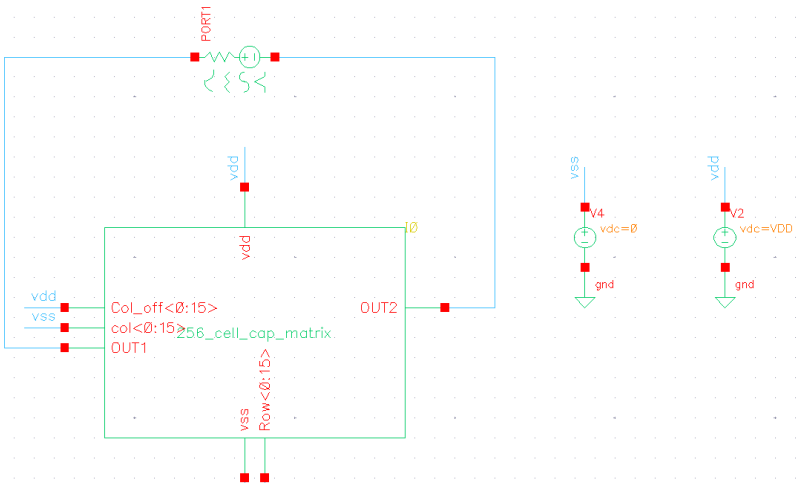

Figure 28: Schematic of simulation for OFF / ON matrix

Appendix B. Subject 2 – Simulation Results

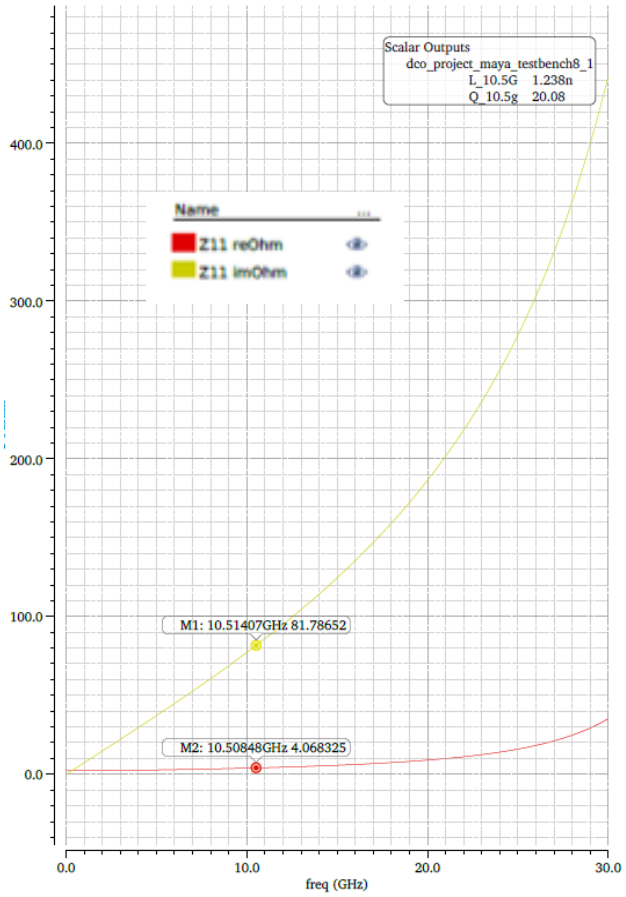

Figure 30: Graphic simulation results of 1.2 nH inductor

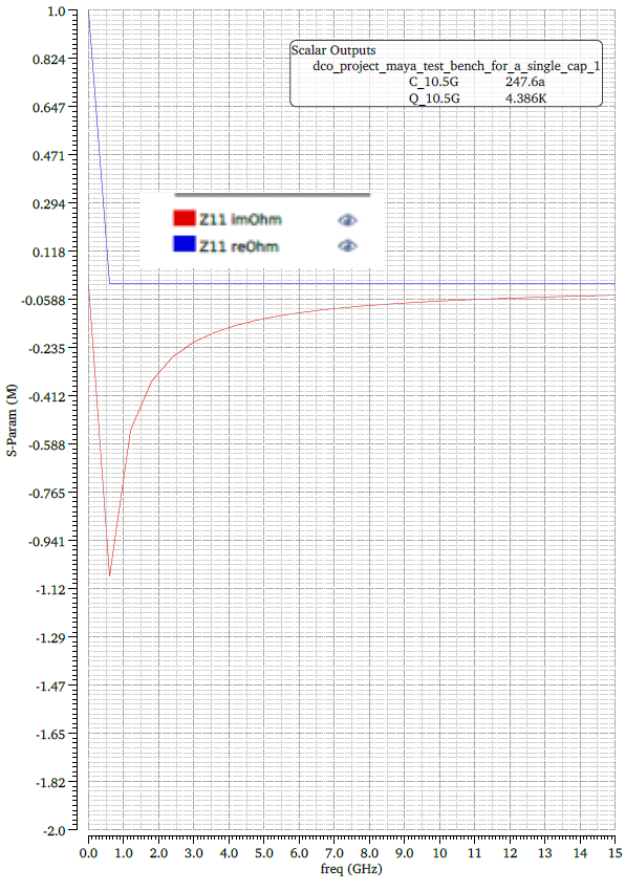

Figure 29: Graphic simulation results of a single capacitor in the matrix ~250aF

Point	Test	Output	Nominal
Filter	Filter	Filter	Filter
Parameters: Er=0			
1	dco_project_maya_se_switch_cap10_1	S11 re	
1	dco_project_maya_se_switch_cap10_1	S11 im	
1	dco_project_maya_se_switch_cap10_1	Z11 reOhm	
1	dco_project_maya_se_switch_cap10_1	Z11 imOhm	
1	dco_project_maya_se_switch_cap10_1	C_10.5G	247.7a
1	dco_project_maya_se_switch_cap10_1	Q_10.5G	7.072K
1	dco_project_maya_se_switch_cap10_2	S11 mag	
1	dco_project_maya_se_switch_cap10_2	S11 re	
1	dco_project_maya_se_switch_cap10_2	S11 im	
1	dco_project_maya_se_switch_cap10_2	Z11 reOhm	
Parameters: Er=1			
2	dco_project_maya_se_switch_cap10_1	S11 re	
2	dco_project_maya_se_switch_cap10_1	S11 im	
2	dco_project_maya_se_switch_cap10_1	Z11 reOhm	
2	dco_project_maya_se_switch_cap10_1	Z11 imOhm	
2	dco_project_maya_se_switch_cap10_1	C_10.5G	247.7a
2	dco_project_maya_se_switch_cap10_1	Q_10.5G	7.072K
2	dco_project_maya_se_switch_cap10_2	S11 mag	
2	dco_project_maya_se_switch_cap10_2	S11 re	
2	dco_project_maya_se_switch_cap10_2	S11 im	
2	dco_project_maya_se_switch_cap10_2	Z11 reOhm	
2	dco_project_maya_se_switch_cap10_2	Z11 imOhm	
2	dco_project_maya_se_switch_cap10_2	C_10.5G	146.1a

Figure 31: Simulation results of a single cell in the matrix

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter	Filter
Parameters: Er=0						
1	dco_project_diff...	C_10G	977.8a			
1	dco_project_diff...	Q_10G	861.4m			
Parameters: Er=1						
2	dco_project_diff...	C_10G	6.004f			
2	dco_project_diff...	Q_10G	24.65			

Figure 32: Simulation results for a single fine cell in the bank - before extraction

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter	Filter
Parameters: Er=0						
1	dco_project_diff...	C_10G	1.397f			
1	dco_project_diff...	Q_10G	1.462			
Parameters: Er=1						
2	dco_project_diff...	C_10G	6.167f			
2	dco_project_diff...	Q_10G	23.6			

Figure 34: Simulation results for a single fine cell in the bank - after extraction

Point	Test	Output	Nominal
Filter	Filter	Filter	Filter
Parameters: En=0			
1	dco_project_diff...	C_10_5G	7.517f
Parameters: En=1			
2	dco_project_diff...	C_10_5G	47.88f

Figure 33: Simulation results for a single coarse cell in the bank - before extraction

Point	Test	Output	Nominal
Filter	Filter	Filter	Filter
Parameters: Er=0			
1	dco_project_diff_...	C_10_5G	10.37f
Parameters: Er=1			
2	dco_project_diff_...	C_10_5G	48.64f

Figure 35: Simulation results for a single coarse cell in the bank - after extraction

Final Simulation Results

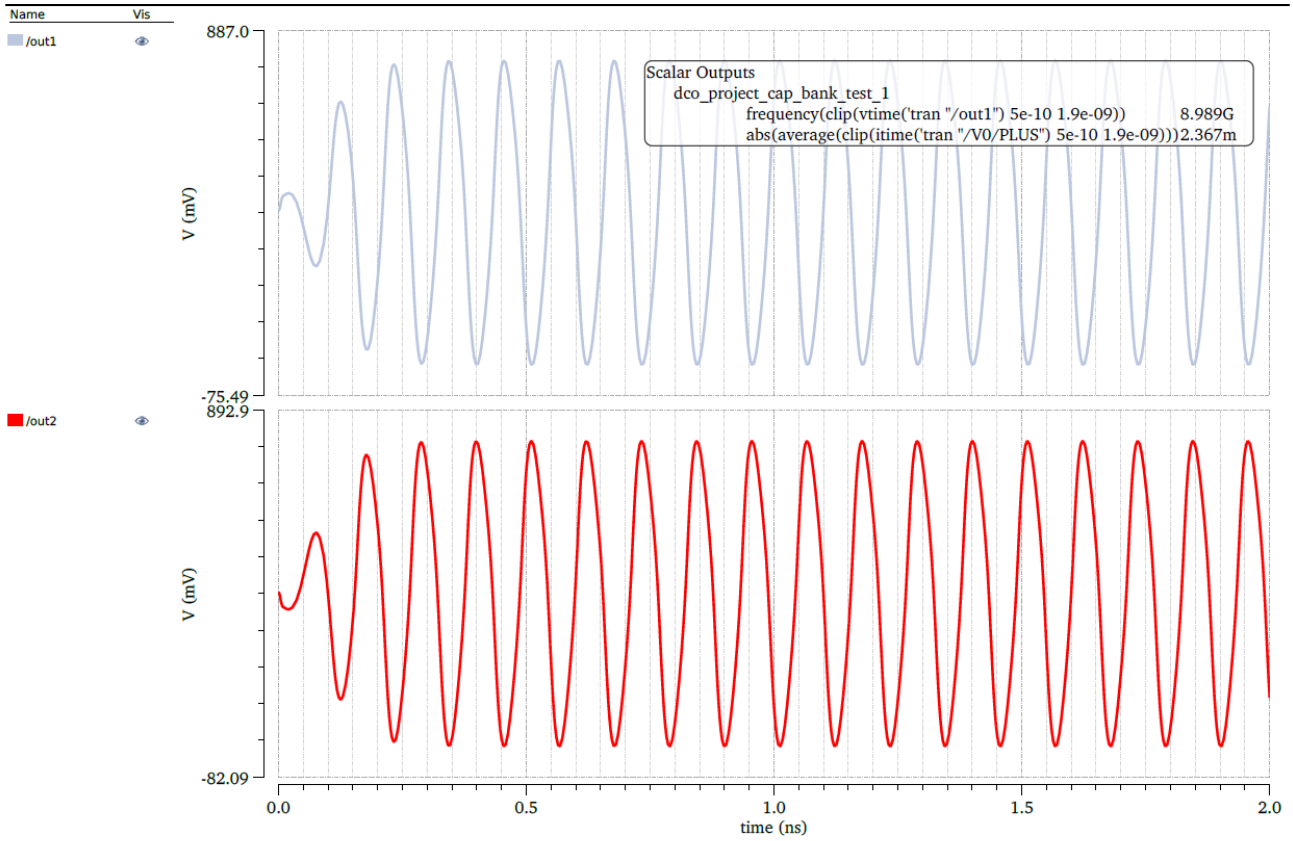

Figure 36: Transient response of the ON-mode including oscillation, Bottom frequency and current consumption

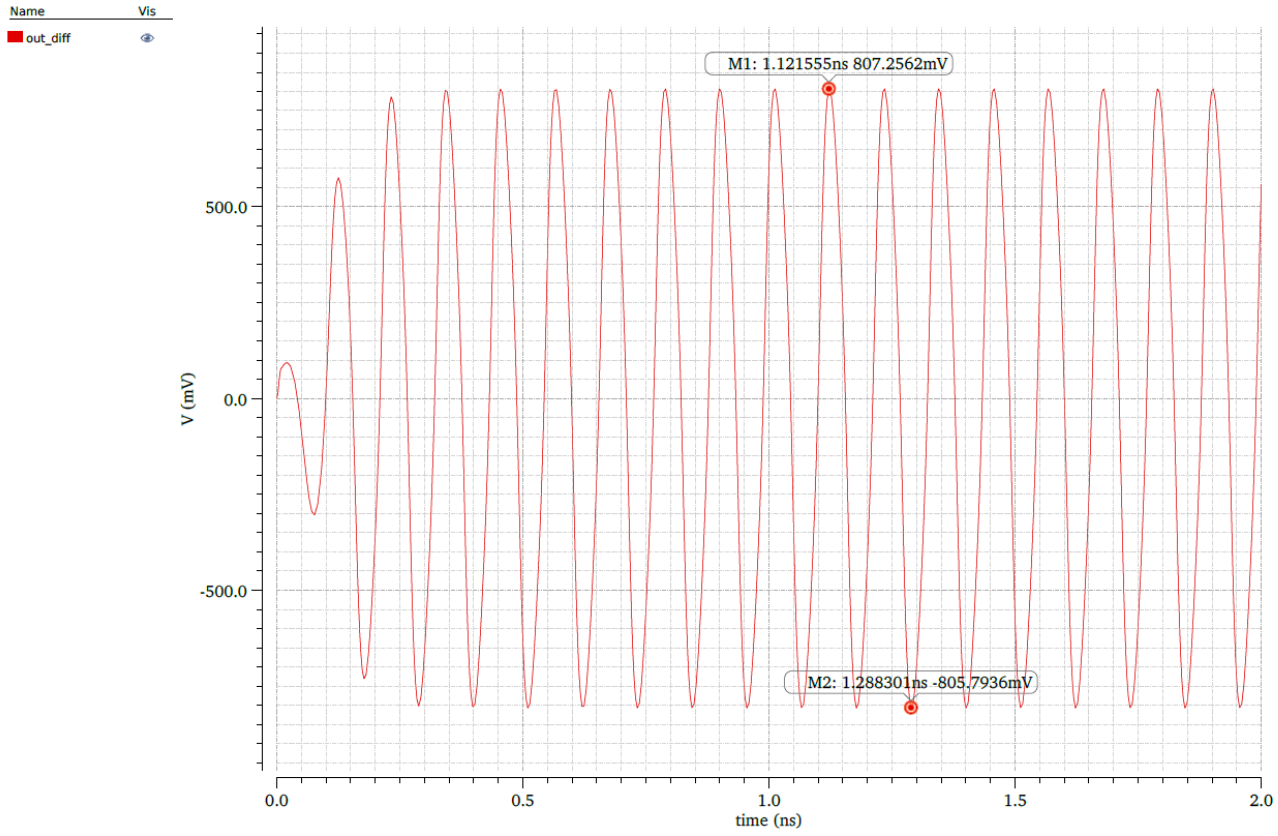

Figure 37: Transient response of the ON-mode Amplitude differential oscillations

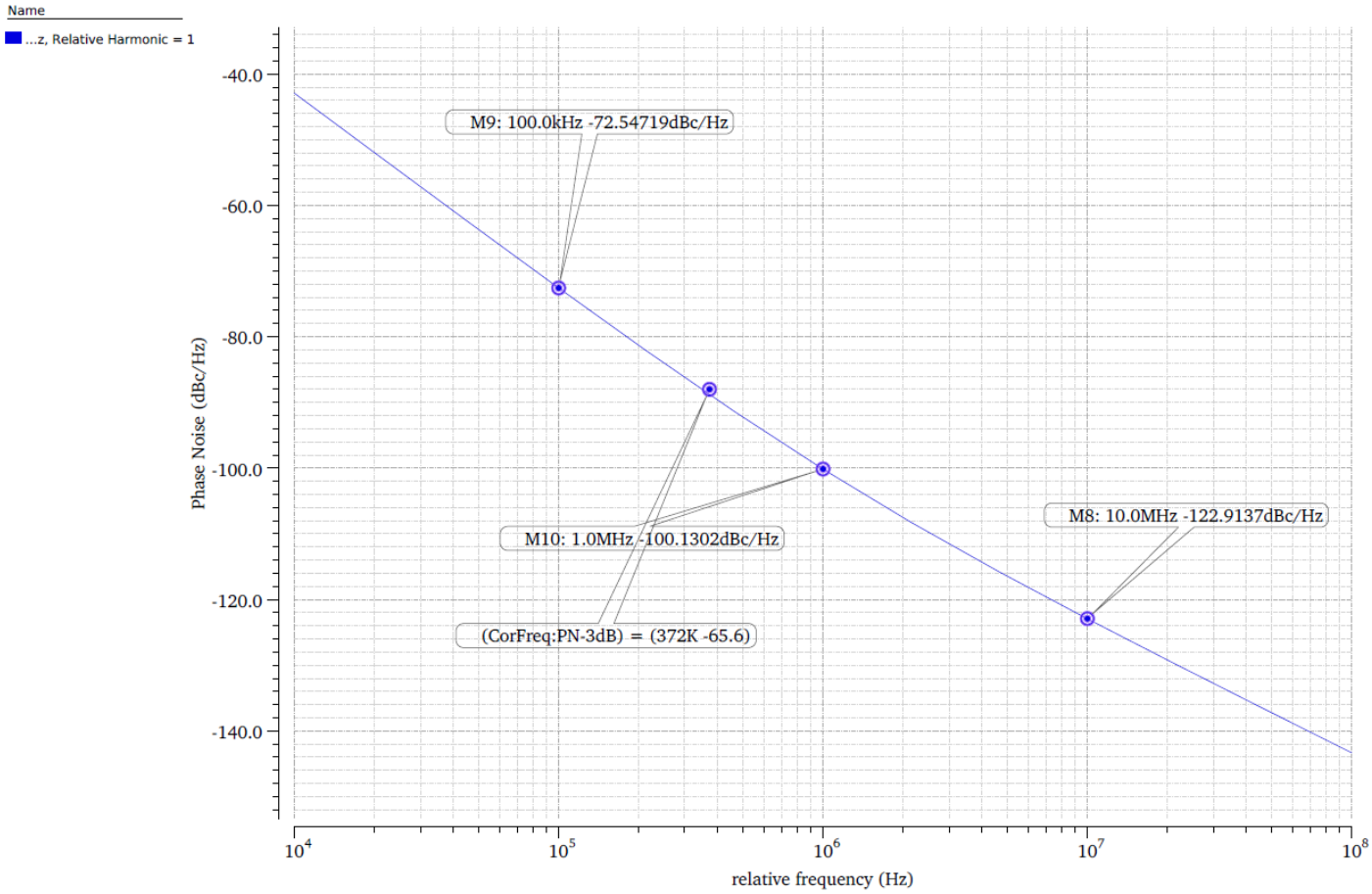

Figure 39: Harmonic Balance noise Analysis for phase noise in ON-mode

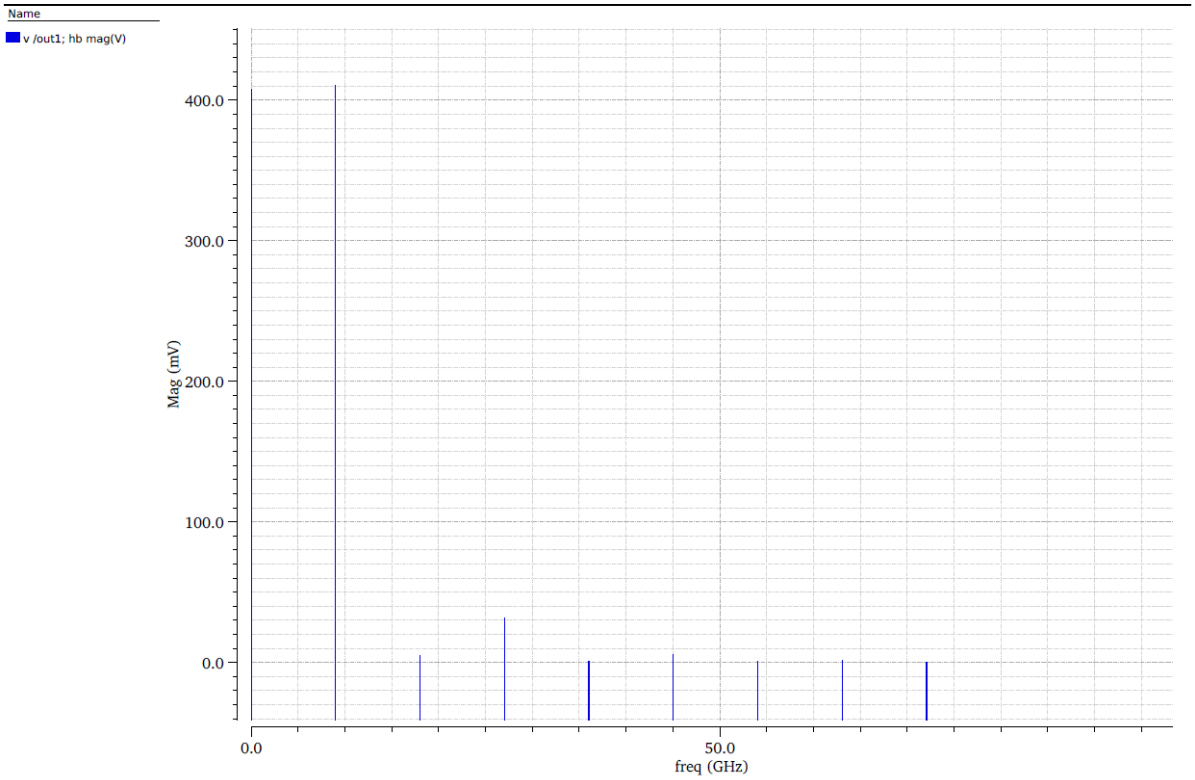

Figure 38: Harmonic Balance for phase noise in ON-mode

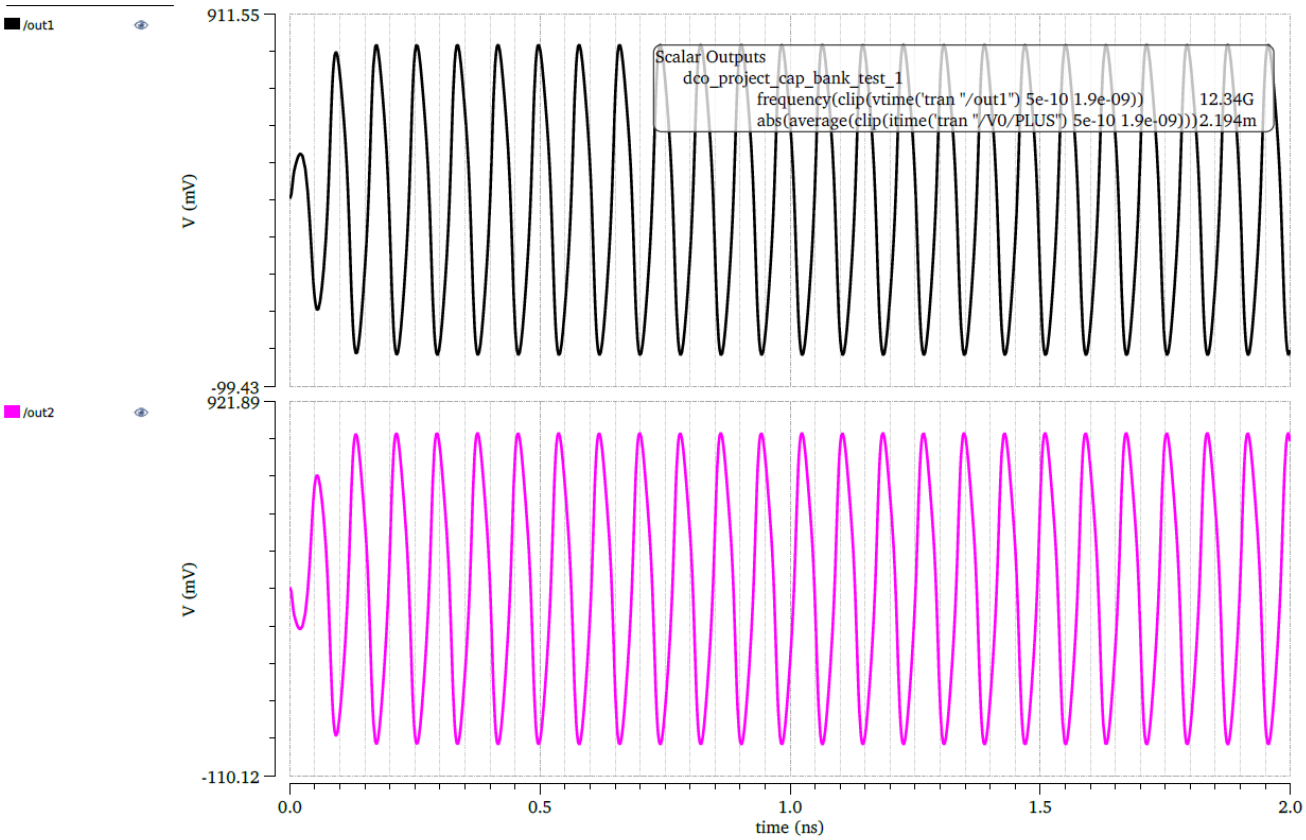

Figure 40: Transient response of the OFF-mode including oscillation, Bottom frequency and current consumption

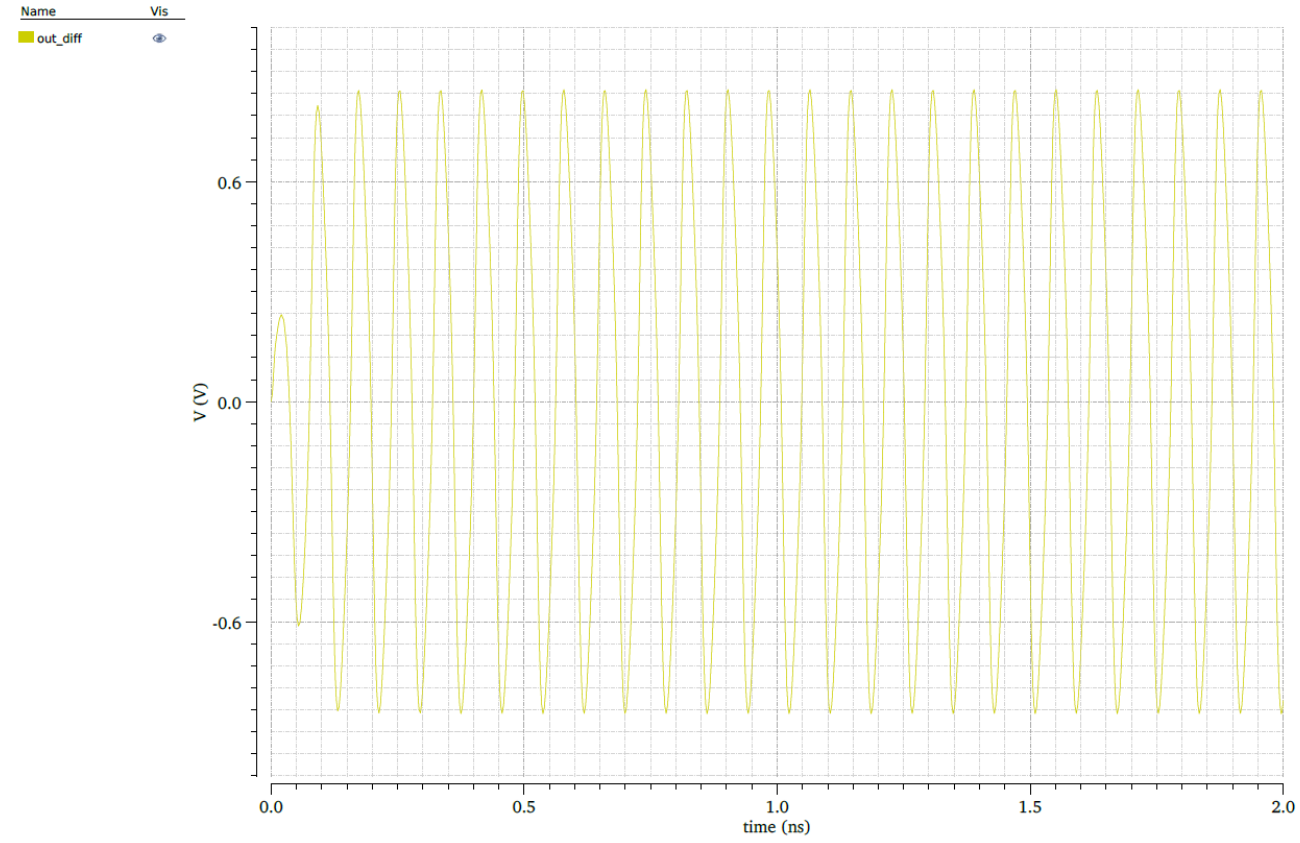

Figure 41: Transient response of the OFF-mode Amplitude differential oscillations

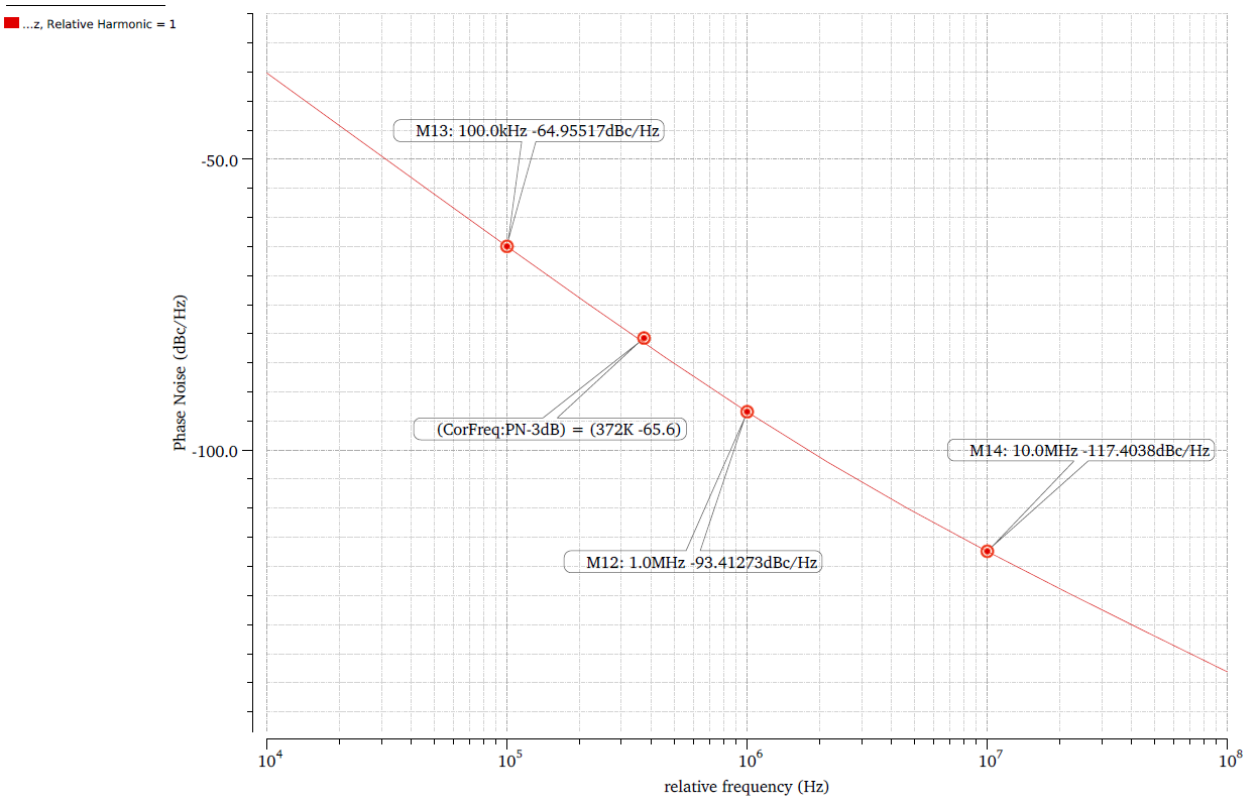

Figure 42: Harmonic Balance noise Analysis for phase noise in OFF-mode

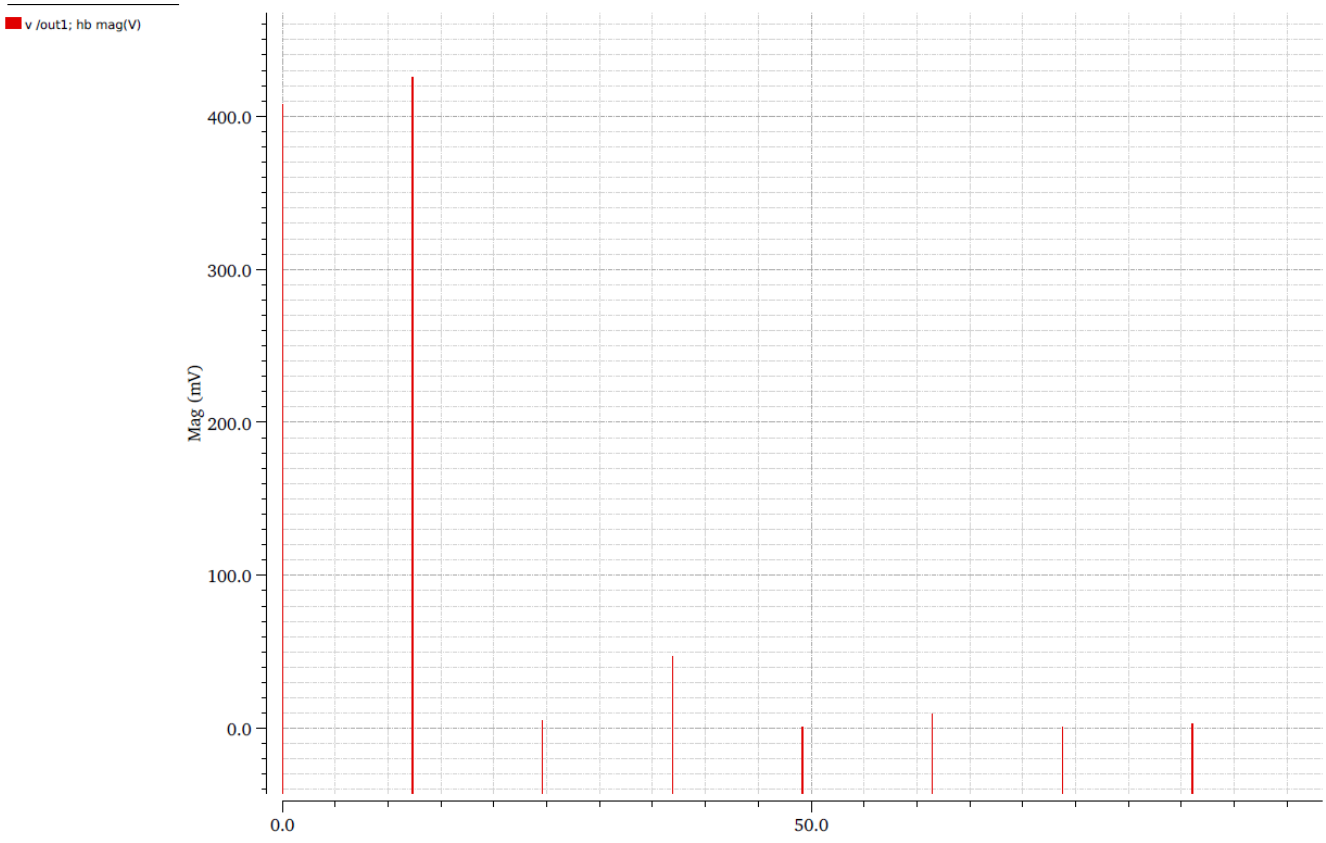

Figure 43: Harmonic Balance for phase noise in OFF-mode

Appendix C. Subject 3 – Layout

The layout of the capacitor matrix is assembled in a hierarchical manner

Single capacitor ⟶ Single cell ⟶ Single cell with logic ⟶ 4-cells with logic⟶ The matrix (256 cells).

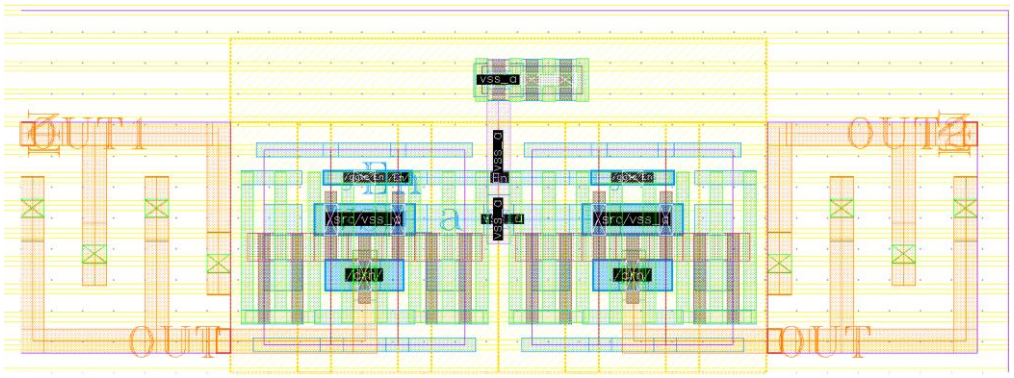

Figure 44: The Layout of a single cell

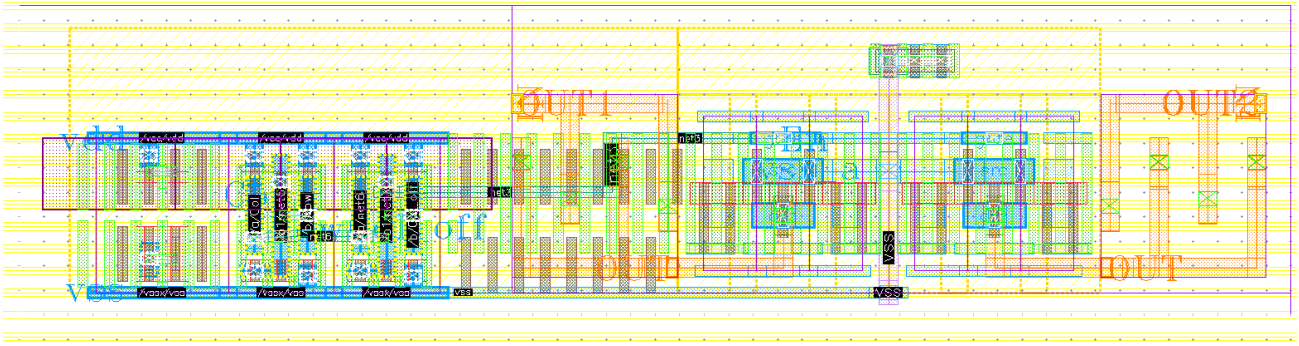

Figure 45: The Layout of a single cell with logic

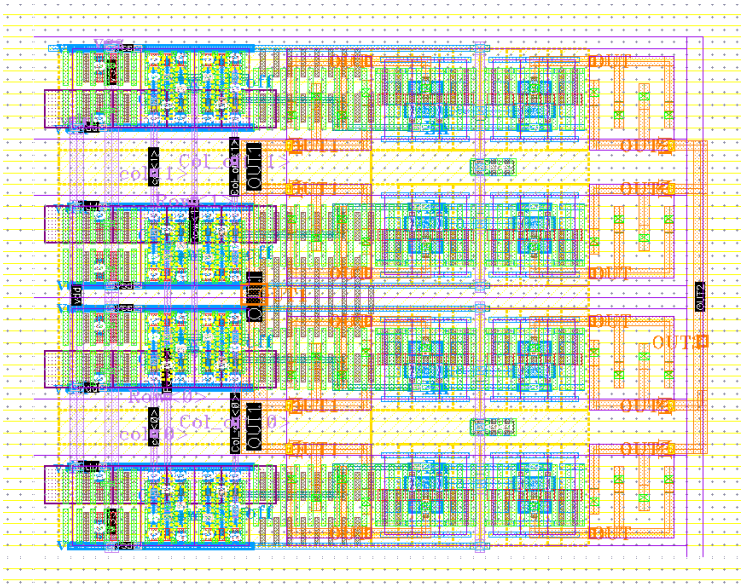

Figure 46: Layout of A 4-cells block

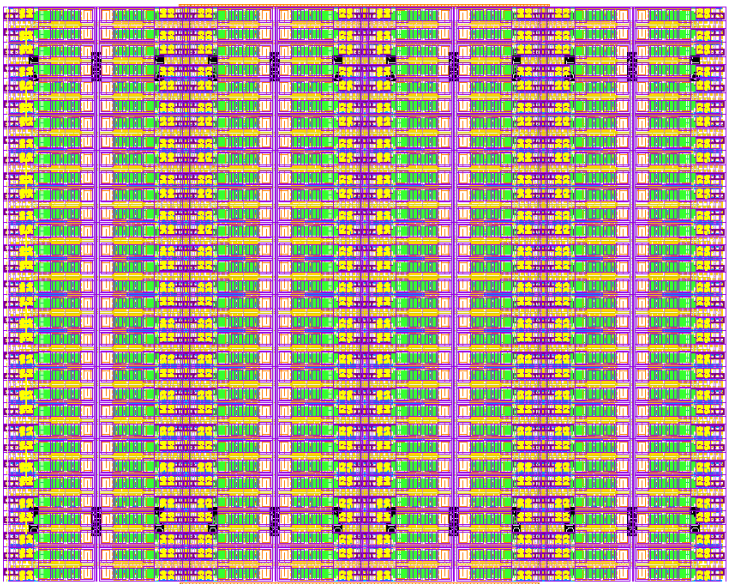

Figure 47: Layout of the whole matrix

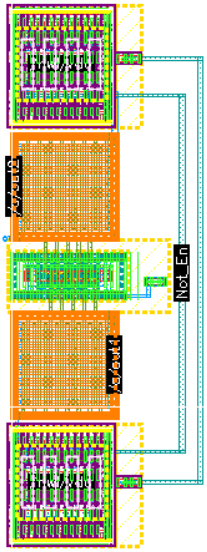

Figure 48: Layout of a differentially switched cell for fine tuning

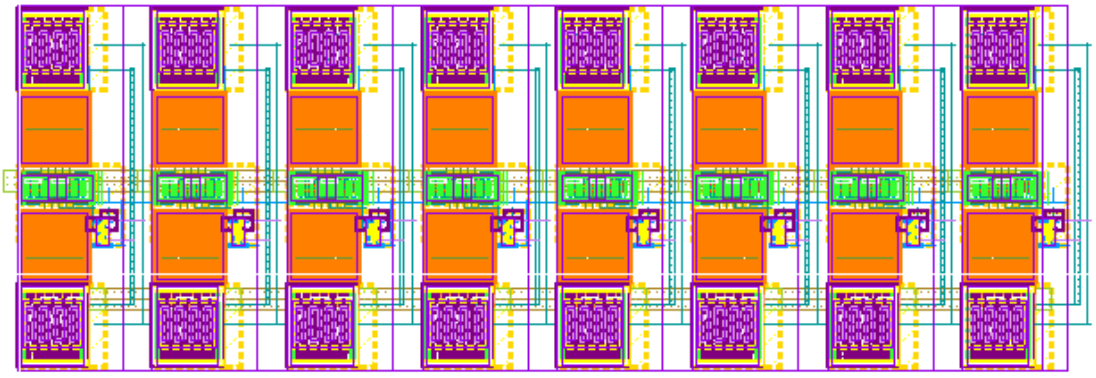

Figure 49: Layout of the fine-tuning sub-block of the bank

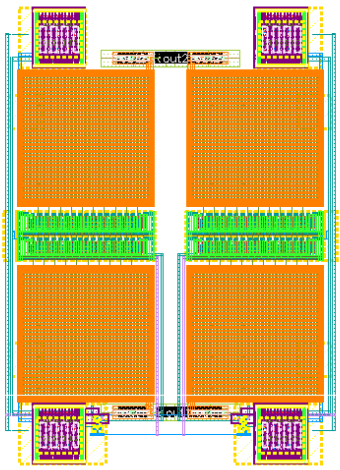

Figure 50: Layout of the coarse-tuning sub-block of the bank

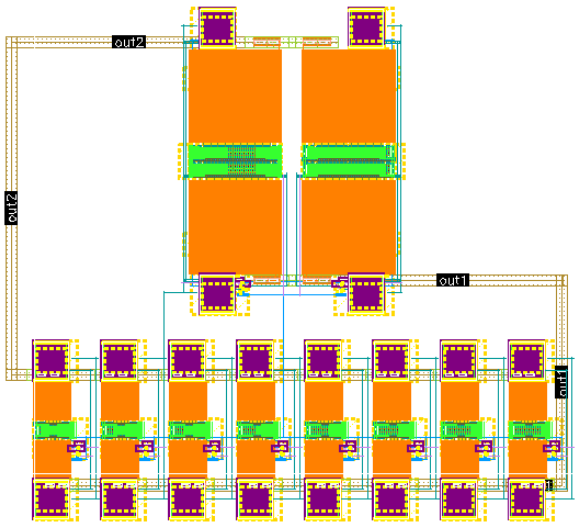

Figure 51: Layout of the capacitor bank

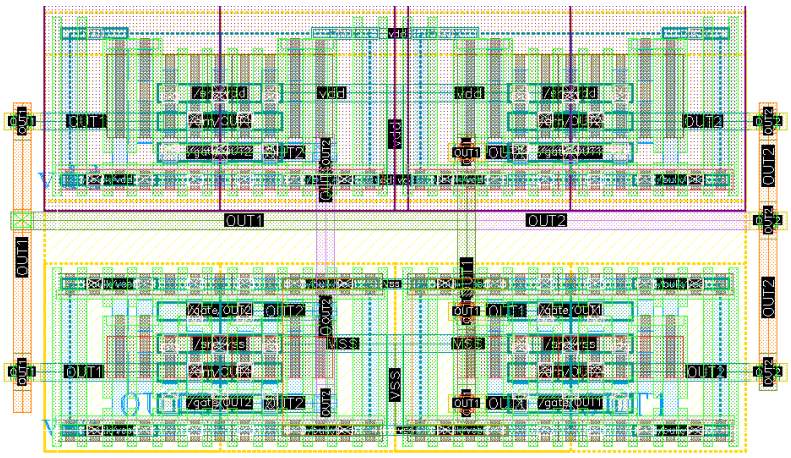

Figure 52: Layout of the amplifier

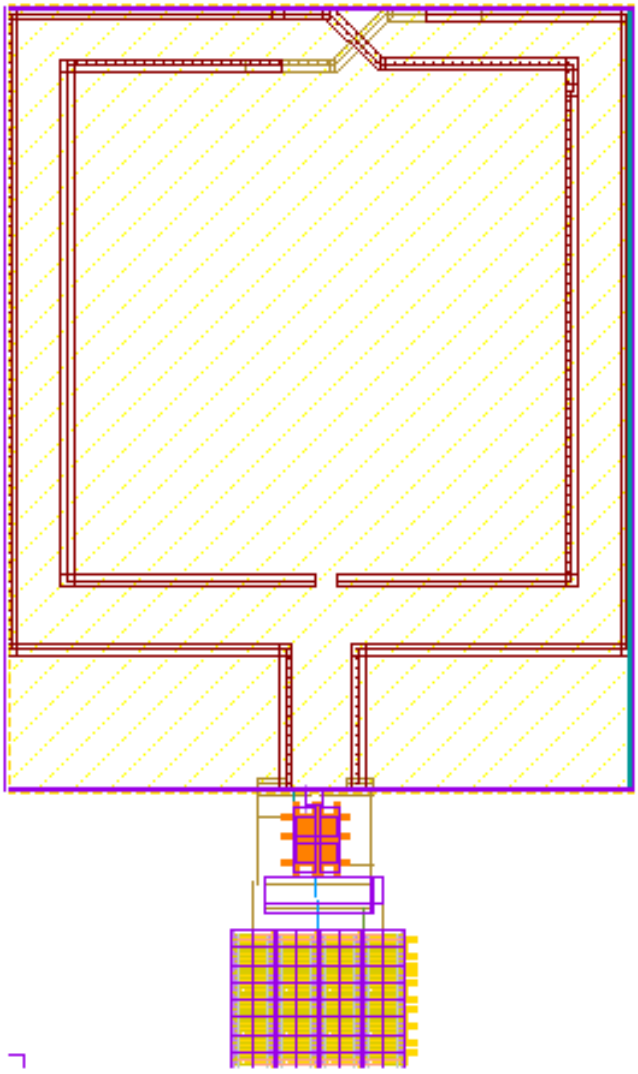

Figure 53: Final layout of the DCO