**Report Computer Architecture 2022**

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| *Implementation* | *Area*  *(with SRAM / without SRAM)* | *Critical Path (ns)* | *Maximum Operating Frequency* | *Number of Cycles for program MULT\** | *Minimal time to execute the program MULT* |
| *Single Cycle* | *408393.738746* | *69.03* | *14.43 MHz* | *2300* | *158 769 ns* |
| *Single Cycle with Multiplication Support* | *419684.594178* | *63.92* | *15.64MHz* | *40* | *2556.8 ns* |
| *Pipelined* |  |  |  |  |  |
| *Pipelined with hazard and stall logic* |  |  |  |  |  |
| *Advanced acceleration* |  |  |  |  |  |

*\* The program MULT1 is used for “Single cycle”, MULT2 for “Single Cycle with Multiplication Support” and “Pipelined”, MULT3 is used for “Pipelined with hazard and stall logic”, MULT4, or your modified version of it, is used for “Advanced acceleration”.*

*Questions:*

* *For the single cycle processor, which kind of instruction would stimulate the critical path found? How would you improve it without adding any pipe stage?*

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* *For the single cycle processor, which resources constitute most part of the gates? What is your explanation for this distribution? Is it possible to reduce the number of gate cells?*

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* *What are the advantages of using a single cycle processor compared with more advanced implementations? Can you imagine/propose an application scenario of such cores?*

*One of the benefits is that it is a really simple implementation and, as a result of this, generally very cheap. The implementation is also relatively fast if the instruction set is small.*

* *Is the critical path affected when hardware support for multiplication is added to the single cycle processor? What is your explanation for this? Do you know any multiplier implementation that can improve timing?*

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* *Is adding hardware support for multiplication a good choice for every microprocessor? Motivate your answer.*

*No, because it increases the critical path. If multiplication is not required, or rarely used, it is better to not implement it to benefit more from the reduced critical path and thus a higher possible clock frequency.*

* *How much larger is the pipelined implementation compared to the single cycle processor? What is the main cause for its increase? How is the critical path affected when we pass from a single cycle processor to a pipelined implementation?*

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* *Considering the critical path found for the pipelined processor, how would it be possible to increase the performance of the system? Would your solution significantly speed up the core? Also, what will be the new critical path?*

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* *What microarchitecture techniques did you apply to accelerate MULT4? Explain under what conditions/type of workload you will have the maximum/minimum performance.*

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* *Is the addition of hardware improvements, like pipelining, correlated with higher power consumption? How can we assess if a specific modification to our processor improves or diminishes the energy efficiency of the system?*

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