

Question #1

Design Superscalar architecture with given instruction set

Instructions

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Load	LDRH	<Rd>	<Rn>	#<5_bit_offset>					Rd = zeroExtend(Mem[Rn + Offset * 2])							
	0	1	1	1	1	Offset					Rn			Rd		

Store STRH <Rd> <Rn> #<5_bit_offset> Mem[Rn+ Offset *2] = Rd[15:0]

0	1	1	1	0	Offset	Rn	Rd
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Add	ADD	<Rd>	<Rn>	#<8 bit imm>	Add Imm value to Rd and store the value in Rd	N, Z, C, V
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0	0	1	0	0	Rd	Imm
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Sub	SBC	<Rm>	<Rn>	Rd = Rd – Rm – C	N, Z, C, V
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0	1	0	0	0	0	0	1	0	1	Rm	Rd
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Jump B <target address> PC = PC + (signExt(offset)<<1)

1	1	1	0	0	Offset
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Shift	ASR	<Rm>	<Rn>	Rd = Rd (Arithmetic)>> Rm	N, Z, C
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0	1	0	0	0	0	1	0	1	0	Rm	Rd
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BIC	BIC	<Rm>	<Rn>	Rd = Rd AND NOT Rm	N, Z
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0	1	0	0	0	0	1	1	1	1	Rm	Rd
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B	B	LE	#<8 bit_offset>	if cond then PC = PC + (signExt(offset)<<1)	Cond. Is N flag
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1	1	0	1	0	0	1	0	Offset
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Exceptions(Arithmetic Overflow and Undefined Instruction)