

OPTIMIZING APPLICATION PERFORMANCE WITH CUDA® PROFILING TOOLS

Swapna Matwankar, April 7, 2016



CUDA PROFILING TOOLS

- **NVIDIA® Visual Profiler**
 - Standalone (nvvp)



Integrated into NVIDIA® Nsight™ Eclipse Edition (nsight)





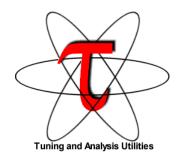
NVIDIA® Nsight™ Visual Studio Edition



Old environment variable based command-line profiler is discontinued from 8.0.

* Android CUDA APK profiling not supported (yet)

3RD PARTY PROFILING TOOLS



TAU Performance System ®



VampirTrace



PAPI CUDA Component



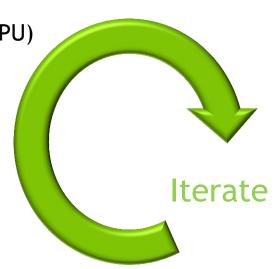
PERFORMANCE OPPORTUNITIES

Application level opportunities

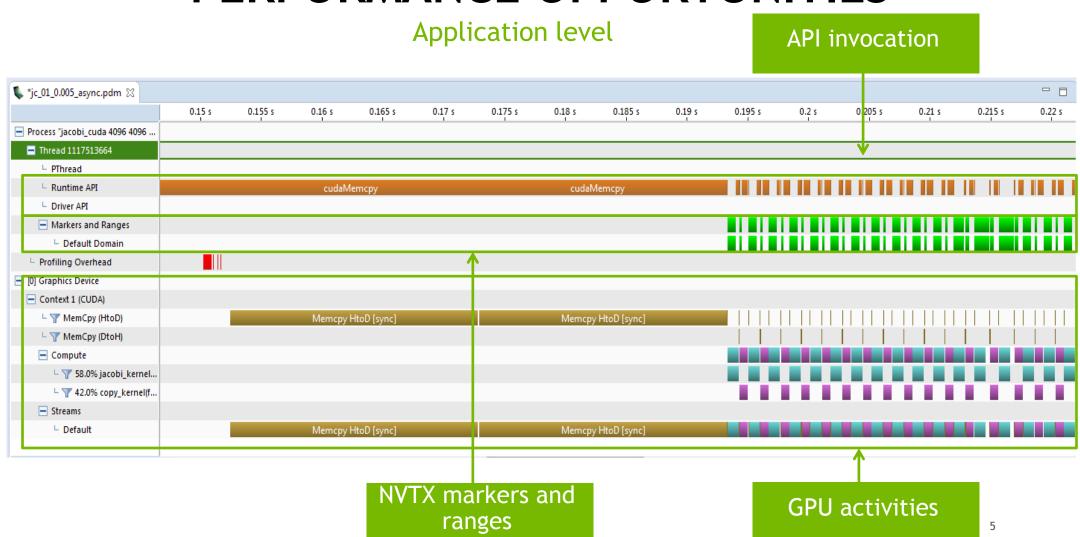
- Overall application performance
 - Overlap CPU and GPU work, identify the bottlenecks (CPU or GPU)
- Overall GPU utilization and efficiency
 - Overlap compute and memory copies
 - Utilize compute and copy engines effectively

Kernel level opportunities

- Use memory bandwidth efficiently
- Use compute resources efficiently
- Hide instruction and memory latency



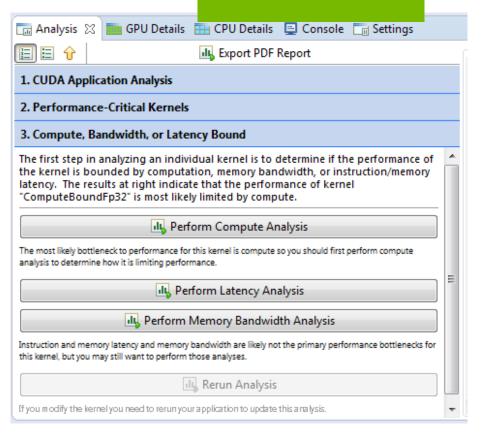
PERFORMANCE OPPORTUNITIES

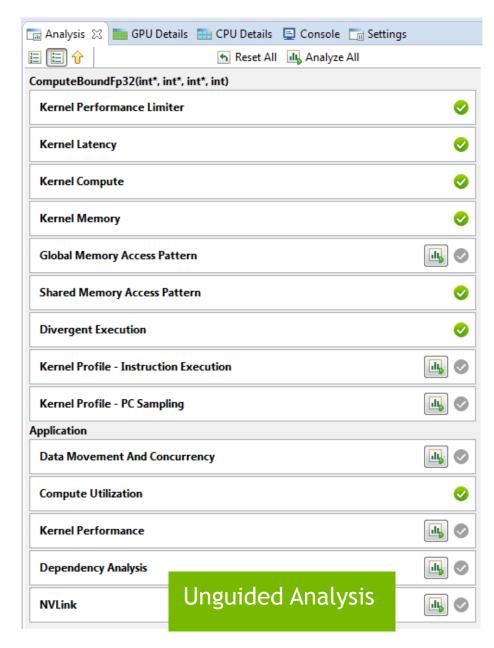


PERFORMANCE OPPORTUNITIES

Kernel level

Guided Analysis





What's new in 8.0?

- Dependency Analysis
- NVLink Analysis
- Unified memory profiling
- Instruction Level Profiling (PC sampling)
- Combined source-assembly view
- FP16 Analysis
- OpenAcc on Timeline
- CPU profiling
- Nvidia Tools Extension V2

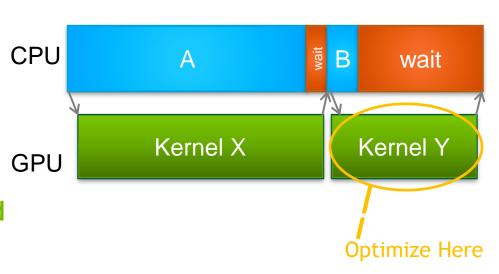
Features listed in green are Pascal specific features

Motivation

Not always

- GPU kernels are bottleneck in application
- Optimizing kernel taking highest time will give more performance benefits

It is important to identify right bottlenecks in the application to get good ROI



How is it done?

In 8.0, profiling tools supports identifying critical path in the application

- Analyzes CPU threads (POSIX) and GPU activities
- Graph is generated by post-processing execution traces of application (negligible execution overhead)
- Dependencies are defined by CUDA API contract

Results

- Critical path that includes CUDA APIs, GPU activities, thread activities
- For all CUDA APIs, GPU activities and thread activities
 - Time on Critical Path Optimizing this will improve overall execution time
 - Waiting time Reducing waiting time will improve load imbalance
 - Inbound/outbound dependencies To traverse the issues in both directions

nvprof

Command: ./nvprof --dependency-analysis --cpu-thread-tracing on ./jacobi_cuda 4096 4096 0.005

Output:

```
==13269== Dependency Analysis:
==13269== Analysis progress: 100%
Critical path(%) Critical path Waiting time
         70.99%
                  994.926674ms
                                         Ons <Other>
         13.95%
                  195.570089ms
                                         Ons cudaMalloc
          5.69%
                 79.785085ms
                                         Ons jacobi kernel(float const *, float*, int, int, float*)
                 66.064614ms
                                              copy kernel(float*, float const *, int, int)
          4.71%
                                              cudaMemcpv
          2.87%
                   40.197672ms
                                 19.969822ms
           1.42%
                   19.969822ms
                                              [CUDA memcpy DtoH]
```

Note: --cpu-thread-tracing on option is required only for multithreaded applications

nvprof

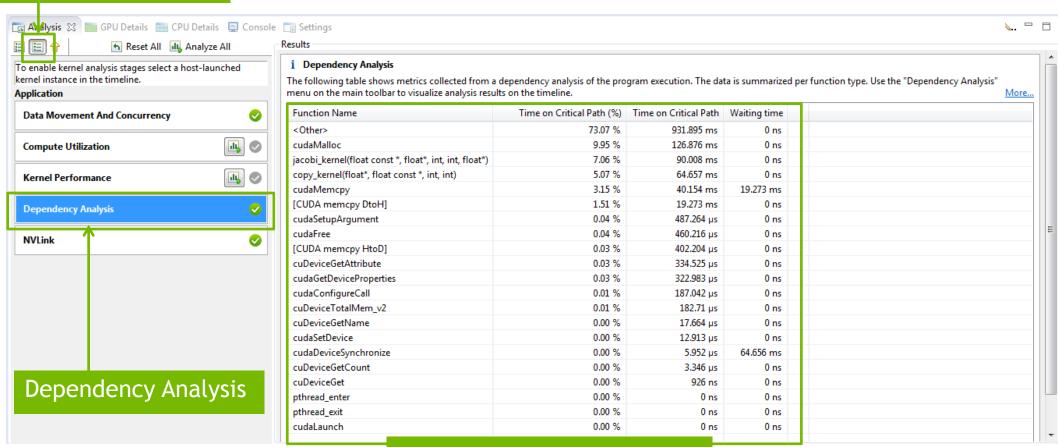
Use --print-dependency-analysis-trace argument along with --dependency-analysis to get the time on critical path and waiting time of each instance of a function

Command: ./nvprof --print-dependency-analysis-trace --dependency-analysis --cpu-thread-tracing on ./jacobi cuda 4096 4096 0.005

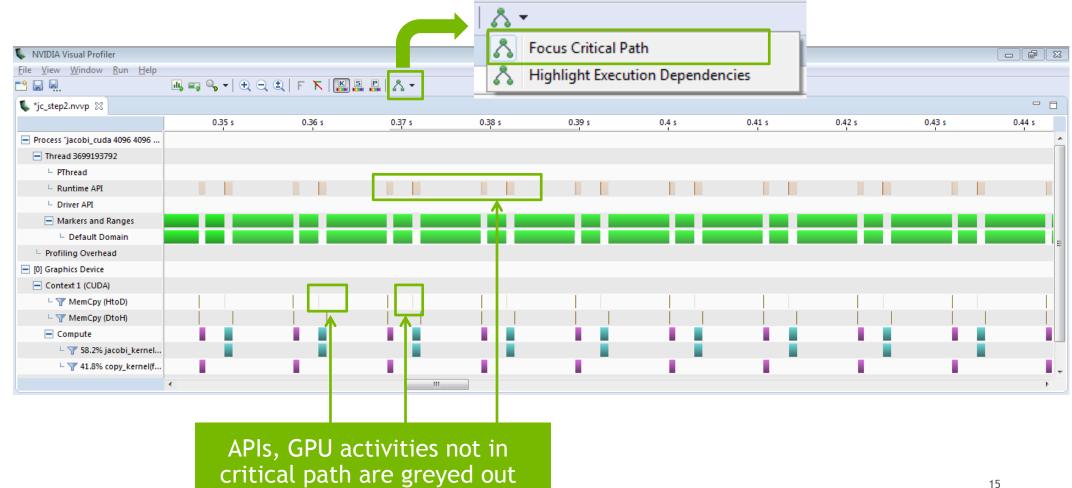
```
==6012== Dependency Analysis:
==6012== Analysis progress: 100%
   Start Duration Critical path Waiting time
118.84ms 1.6540us
                       1.654000us
                                                 cuDeviceGetCount
118.85ms
             350ns
                            350ns
                                                 cuDeviceGetCount
             265ns
118.85ms
                            265ns
                                                 cuDeviceGet
118.85ms
             506ns
                            506ns
                                                 cuDeviceGetAttribute
118.86ms
             487ns
                            487ns
                                                 cuDeviceGet
                                            0ns
118.87ms
             383ns
                            383ns
                                                 cuDeviceGetAttribute
430.86ms 9.2270us
                                                 cudaLaunch
                              0ns
                                            0ns
430.86ms 2.3360us
                       2.336000us
                                                 [CUDA memcpy HtoD]
                                            0ns
430.87ms 819.60us
                                     1.696000us
                                                 cudaMemcpv
                              0ns
                                                 jacobi kernel(float const *, float*, int, int, float*)
430.88ms 796.50us
                     796.500000us
                                                 [CUDA memcpy DtoH]
431.68ms 1.6960us
                       1.696000us
                                            0ns
438.51ms 10.439us
                              0ns
                                            0ns
                                                 cudaMemcpy
438.52ms 43.980us
                              0ns
                                     1.696000us
                                                 cudaMemcpv
438.53ms 11.775us
                      11.775000us
                                            0ns
                                                 [CUDA memcpv HtoD]
```

Unguided Analysis

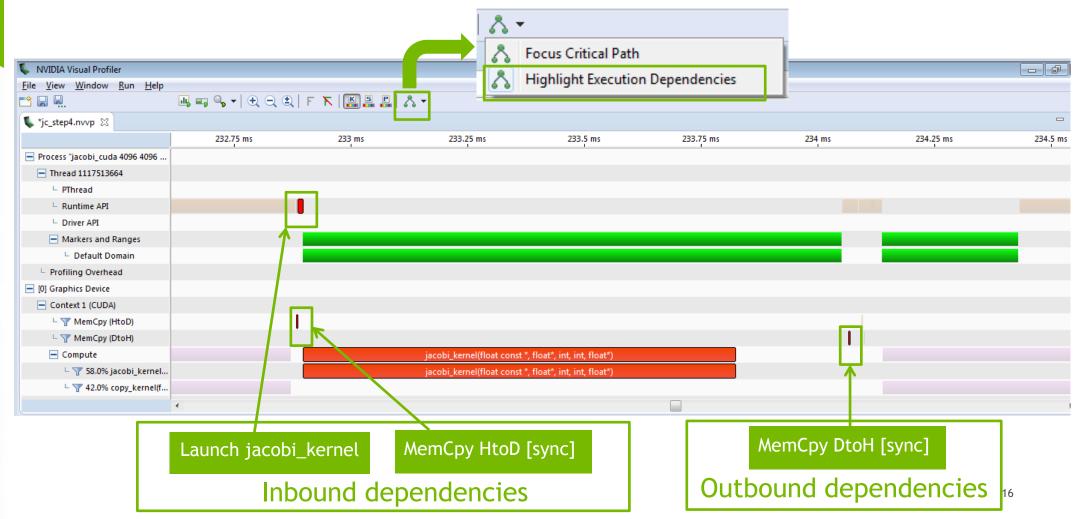
Visual Profiler: Critical path



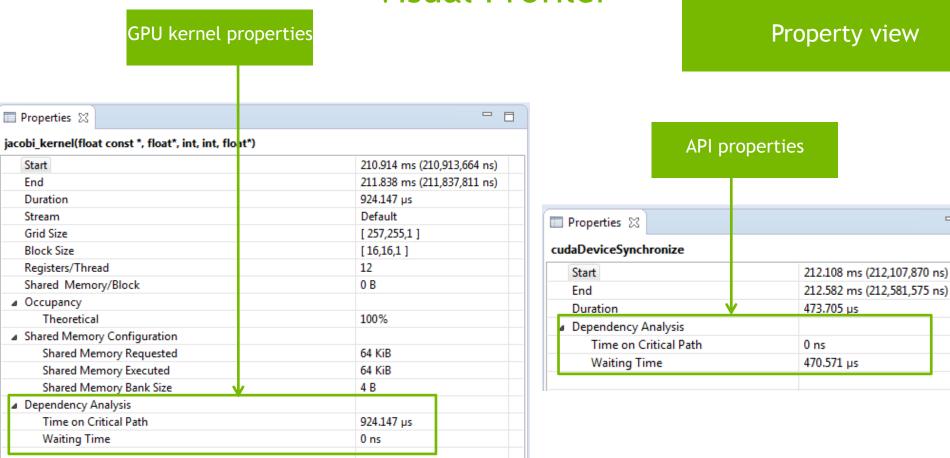
Visual Profiler



Visual Profiler



Visual Profiler



- -

Example: Step 1

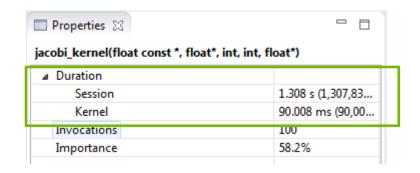


Iterative execution pattern: 1. compute GPU+CPU 2. copy GPU+CPU

Example: Step 1

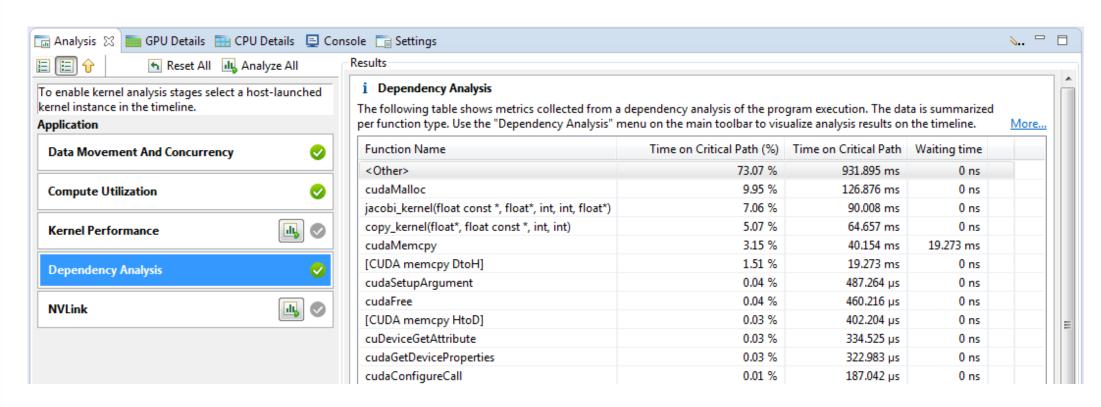
R	Results							
i Kernel Optimization Priorities								
		owing kernels are ordered by optimization importance based on execution time and achieved occupancy. Optimization of higher kernels (those that appear first in the list) is more likely to improve performance compared to lower ranked kernels.						
	Rank	Description						
	100	[100 kernel instances] jacobi_kernel(float const *, float*, int, int, float*)						
П	71	[100 kernel instances] copy_kernel(float*, float const *, int, int)						

Guided analysis: Optimize jacobi_kernel



Kernel duration 6% of total session duration, kernel optimization may not impact application performance

Example: Step 1



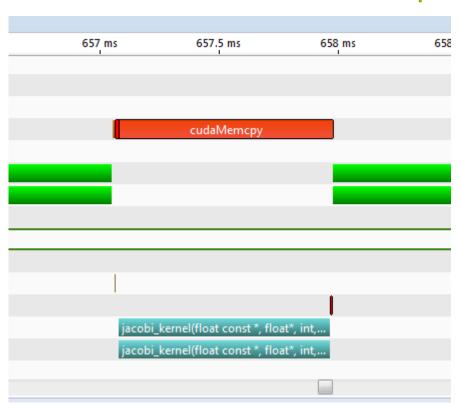
Dependency analysis feature points that 'Other' CPU accounts for 73% of critical path

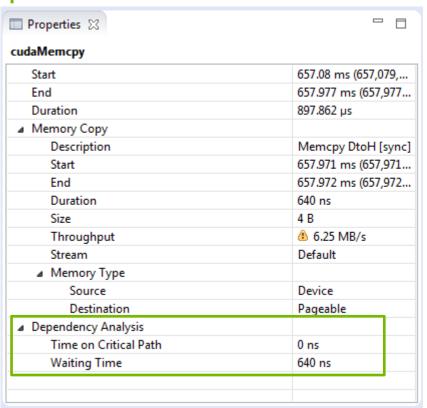
Example: Step 1

Dependency Analysis The following table shows metrics collected from a dependency analysis of the program execution. The data is summarized per function type. Use the "Dependency Analysis" menu on the main toolbar to visualize analysis results on the timeline.					
cudaDeviceSynchronize	0.00 %	5.952 µs	64.656 ms		
cudaMemcpy	3.15 %	40.154 ms	19.273 ms		
pthread_enter	0.00 %	0 ns	0 ns		
pthread_exit	0.00 %	0 ns	0 ns		
cuDeviceGetCount	0.00 %	3.346 µs	0 ns		
cuDeviceGet	0.00 %	926 ns	0 ns		
cuDeviceGetAttribute	0.03 %	334.525 μs	0 ns		
cuDeviceGetName	0.00 %	17.664 µs	0 ns		
cuDeviceTotalMem_v2	0.01 %	182.71 µs	0 ns		
cudaGotDovicoDroportios	0.02 %	222.002	0 nc		

Critical path sorted by waiting time

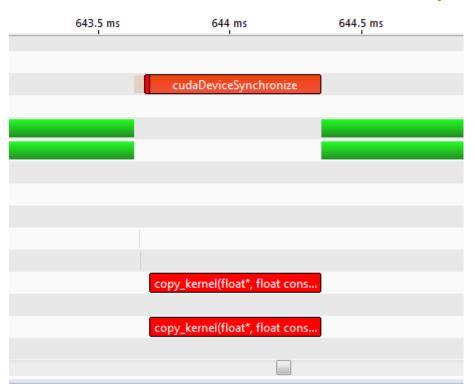
Example: Step 1

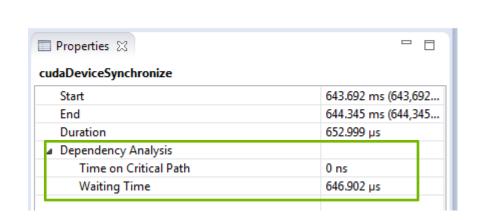




cudaMemcpy waiting for jacobi_kernel to finish

Example: Step 1





cudaDeviceSynchronize waiting for copy_kernel to finish

Sample code

Step 1 code

```
jacobi_kernel<<< ... >>> (...);
cudaMemcpy(...);

compute_cpu

copy_kernel<<< ... >>> (...);
cudaDeviceSynchronize(...);

copy_cpu
```

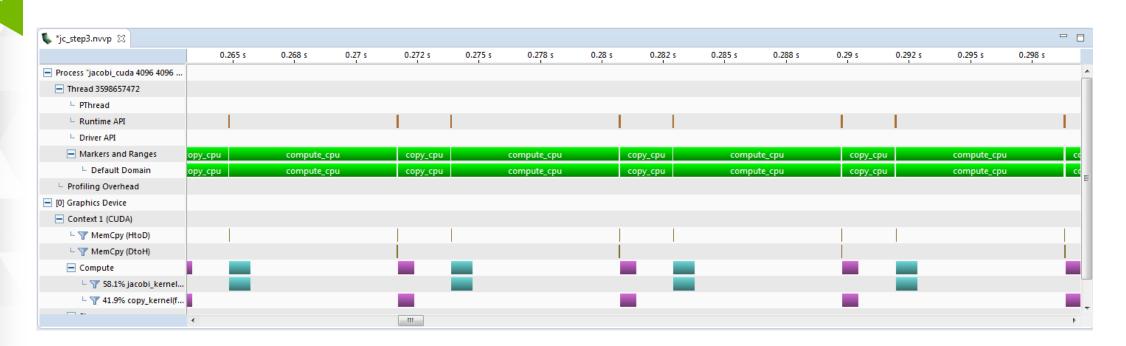
Step 2 code

```
jacobi_kernel<<< ... >>> (...);
compute_cpu

cudaMemcpy(...);
copy_kernel<<< ... >>> (...);

copy_cpu
cudaDeviceSynchronize(...);
```

Example: Step 2

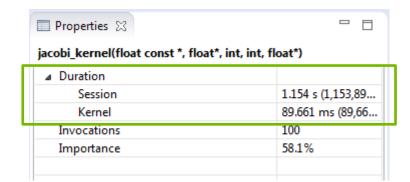


CPU and GPU activities are overlapped

Results i Dependency Analysis The following table shows metrics collected from a dependency analysis of the program execution. The data is summarized per function type. Use the "Dependency Analysis" menu on the main toolbar to visualize analysis results on the timeline. More... Function Name Time on Critical Path (%) Time on Critical Path Waiting time <Other> 82.89 % 930.587 ms 0 ns cudaMalloc 11.39 % 127.891 ms 0 ns cudaMemcpy 3.56 % 39,997 ms 18.94 ms 1.69 % [CUDA memcpy DtoH] 18.94 ms 0 ns cudaLaunch 0.20 % 2.196 ms 0 ns cudaDeviceSynchronize 0.05 % 599.217 us 0 ns cudaFree 0.04 % 503.849 us 0 ns cudaSetupArgument 0.04 % 498.877 µs 0 ns [CUDA memcpy HtoD] 0.04 % 402.07 us 0 ns cuDeviceGetAttribute 0.03 % 333.537 us 0 ns cudaGetDeviceProperties 0.03 % 323.848 us 0 ns cudaConfigureCall 0.02 % 195.514 us 0 ns

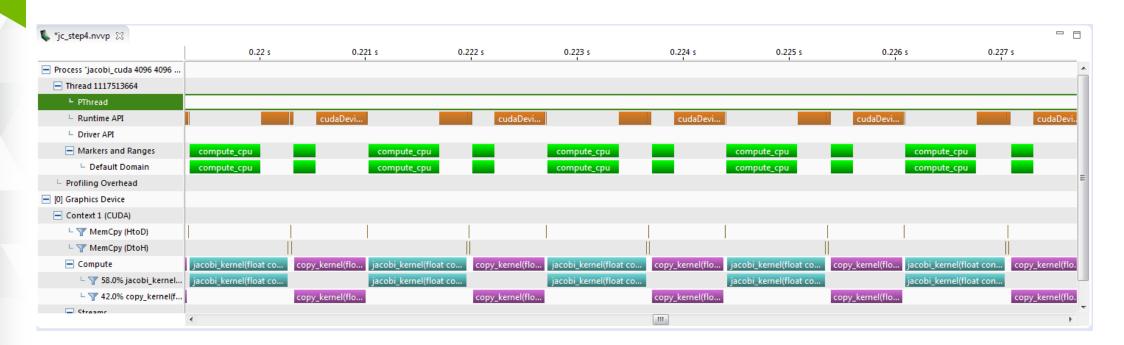
Example: Step 2

GPU kernels are no more in critical path

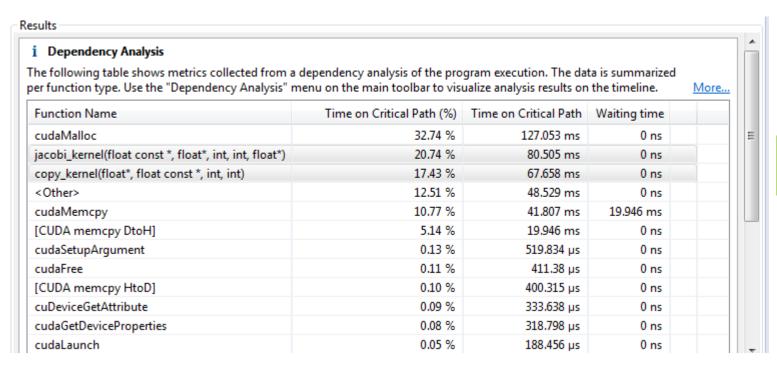


Session time is reduced from 1.3s to 1.15s due to overlap but kernel time is still very less compared to session time

Example: Step 3

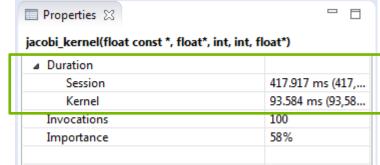


Offload more work on GPU activity by changing CPU compute ratio from 5% to 0.5%



Example: Step 3

GPU kernels are on critical path. Time to optimize GPU kernels!



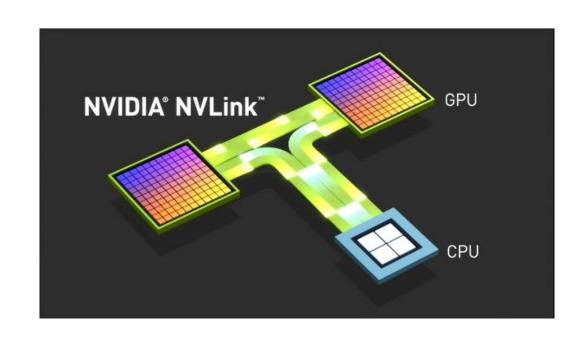
Session time is reduced significantly. 2.7X performance improvement without changing kernel

Limitations

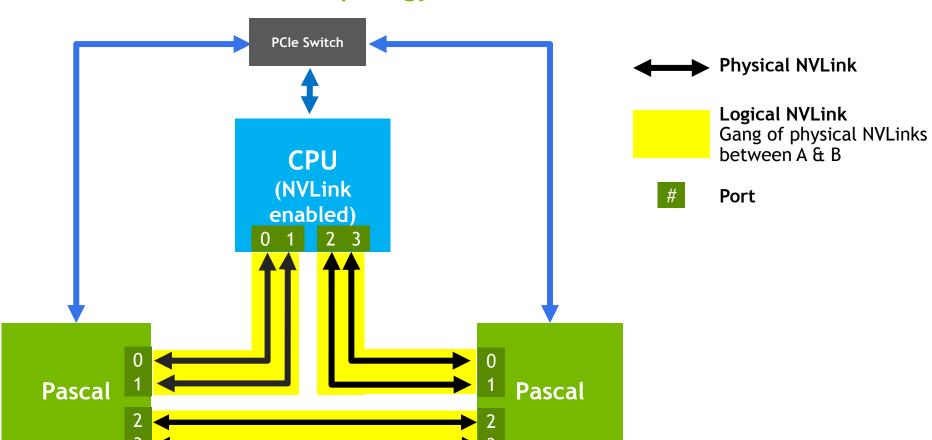
- Doesn't take into account wait states caused by CPU synchronization methods
- Doesn't account for synchronization done by polling memory location that will be updated by GPU activity
- Doesn't include synchronization caused by resource contention
- Limited support for dynamic parallelism No dependency tracking for device launched kernels

NVIDIA NVLINK HIGH-SPEED INTERCONNECT

- High-bandwidth, energy-efficient interconnect
- Enables ultra-fast communication between the CPU and GPU, and between GPUs
- Allows data sharing at rates 5 to 12 times faster than the traditional PCIe Gen3 interconnect



Topology



nvprof

- nvprof supports a new event collection mode "continuous"
- Supported only on Tesla GPUs
- Collects event samples every 2ms (fixed period for now)
- Metrics are collected at device level

nvprof new argument for sampling events

- Example: ./nvprof --aggregate-mode off --event-collection-mode continuous -metrics nvlink_total_data_transmitted,nvlink_total_data_received,nvlink_transmit_throughp ut,nvlink_receive_throughput -f -o memcpy.out ./memcpy
- To get detailed output i.e metric value along with timestamp for each sample use -- print-gpu-trace

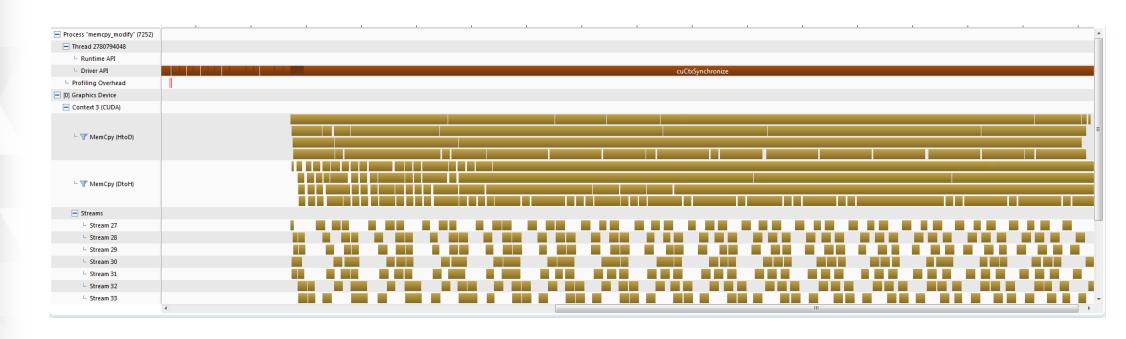
nvprof

- Nvprof also gives topology information
- Example: nvprof --print-nvlink-topology ./app_name
- Output:

Graphics Device 1 port 0, 1, CPU, Nvlink Bandwidth 40.00GB/s, Physical Links 2, Sysmem Access True, Sysmem Atomic Access False, Peer Access False, Peer Atomic Access False Graphics Device 0 port 2, 3, CPU, Nvlink Bandwidth 40.00GB/s, Physical Links 2, Sysmem Access True, Sysmem Atomic Access False, Peer Access False, Peer Atomic Access False Graphics Device 0 port 0, 1, Graphics Device 1 port 3, 2, Nvlink Bandwidth 40.00GB/s, Physical Links 2, Sysmem Access False, Sysmem Atomic Access False, Peer Access True, Peer Atomic Access True

 NVLink metrics have to be correlated by matching port number in topology record with instance number of metric

Visual Profiler

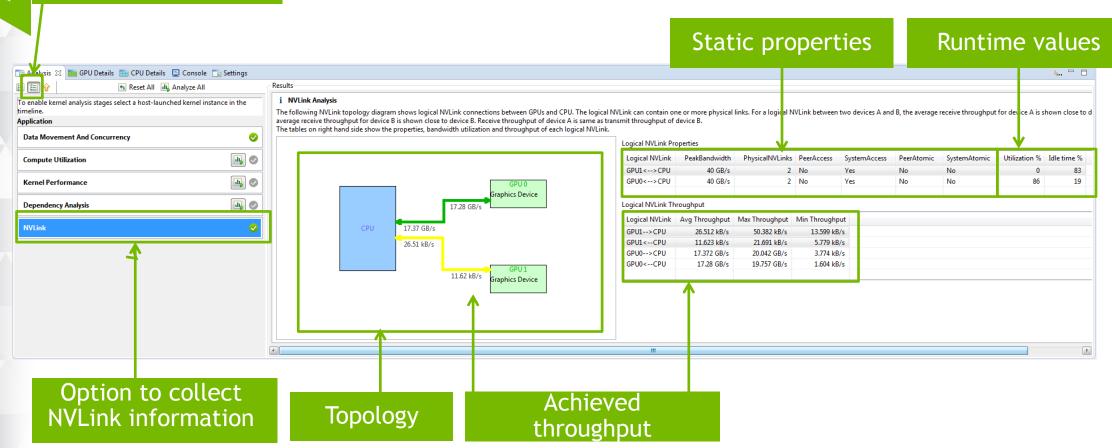


Bidirectional memory transfers between CPU and GPU0

Unguided Analysis

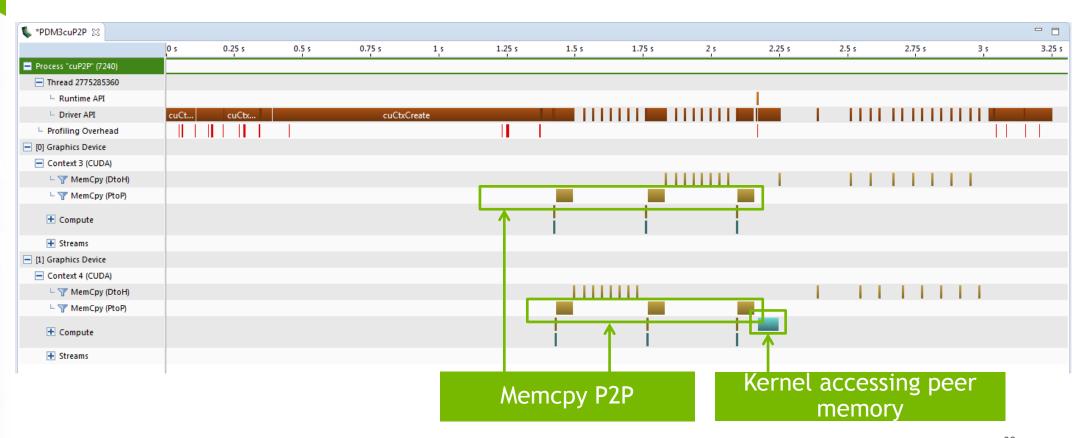
NVLINK ANALYSIS

Visual Profiler



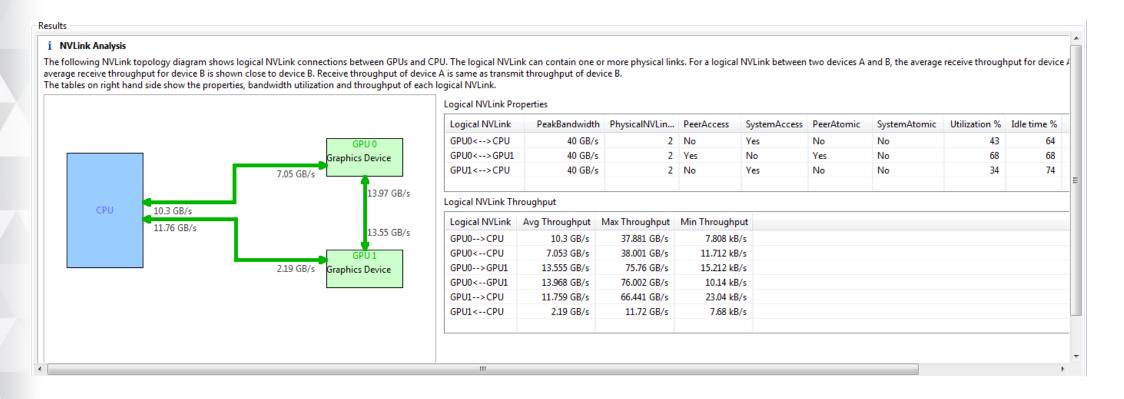
NVLINK ANALYSIS

Visual Profiler



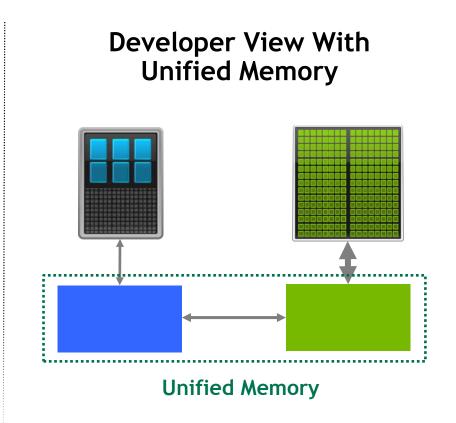
NVLINK ANALYSIS

Visual Profiler



Starting with Kepler and CUDA 6

Custom Data Management System GPU Memory Memory



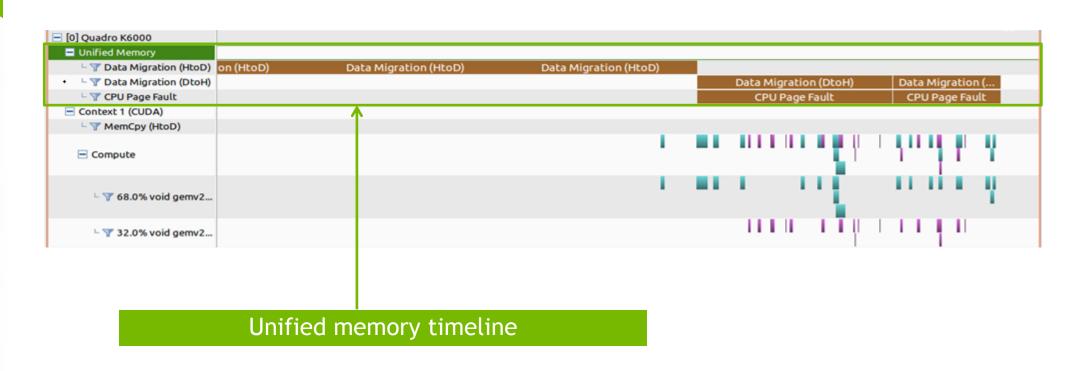
- Single allocation, single pointer accessible everywhere
- Pascal GPUs support demand paging
 - Pages populated and data migrated on first touch, overhead of transferring entire allocation is eliminated
 - Concurrent access to memory from CPU and GPU
 - Enables applications with large data models by allowing to oversubscribe
 GPU memory by spilling over to CPU memory
 - Can access OS controlled memory on supporting system

CUDA 6.0+ code

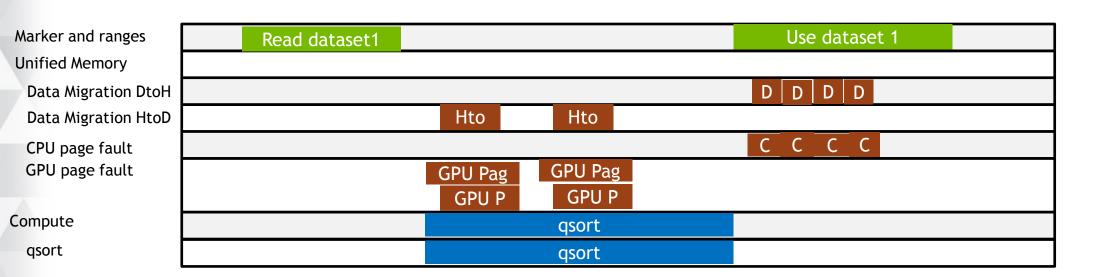
CUDA 8.0 Code *

```
void sortfile(FILE *fp, int N) {
void sortfile(FILE *fp, int N) {
                                                             char *data;
char *data;
                                        Pages allocated in
                                                                                                        Empty, no pages
                                                             cudaMallocManaged(&data, N);
cudaMallocManaged(&data, N);
                                        GPU memory
                                                                                                          anywhere
                                                                                                       CPU page fault, data
                                                             fread(data, 1, N, fp);
fread(data, 1, N, fp);
                                        CPU page fault, data
                                                                                                      allocates on CPU
                                        migrates to CPU
                                                                                                      GPU page fault, data
                                        Kernel launch, data
                                                             qsort<<<...>>>(data,N,1,compare);
qsort<<<...>>>(data,N,1,compare);
                                                                                                       migrates to GPU
                                       migrates to GPU
                                                             cudaDeviceSynchronize();
cudaDeviceSynchronize();
                                                             use data(data);
use data(data);
                                                             cudaFree(data);
cudaFree(data);
```

Visual profiler - 6.0+ unified memory



Visual profiler - 8.0 unified memory timeline



Visual profiler - Properties of faults and migrations

CPU Fault	
Fault generated	19.250ms
Fault resolved	19.251ms
Page address	0x23456000
Page size	4KB
Access type	Read

GPU Fault	
Fault generated	19.236ms
Fault resolved	19.240ms
Page address	0x23456000
Page size	4KB
Access type	RW

Data Migration (Dtol	H)				
Start 19.250 ms					
End	19.251ms				
Duration	1us				
Start address	0x23456000				
Size	4KB				
Process	16763				

Data Migration (Htol	D)
Start	19.237 ms
End	19.239ms
Duration	2us
Start address	0x23456000
Size	8KB
Process	16763

Visual profiler - Fault-migration correlation

Marker and ranges
Unified Memory
Data Migration DtoH
Data Migration HtoD
CPU page fault
GPU page fault
GPU Pag

Visual profiler - Fault-migration correlation

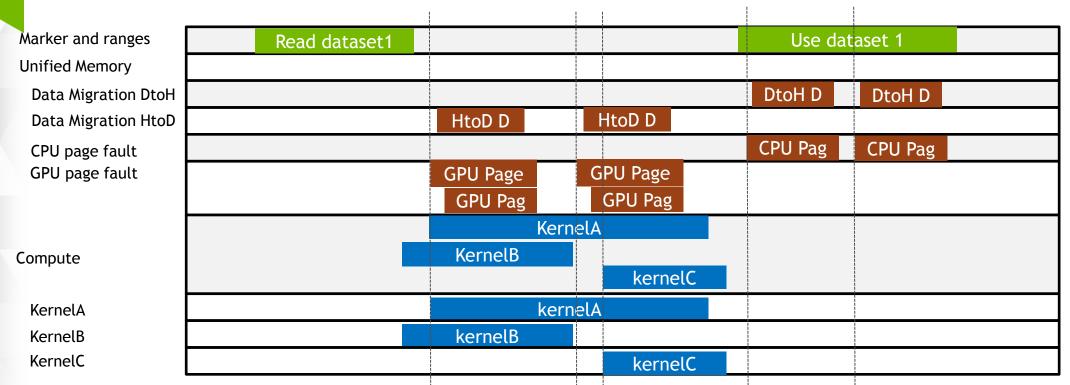
Marker and ranges Use dataset 1 Read dataset1 **Unified Memory** Data Migration DtoH Hto Data Migration HtoD Hto CPU page fault GPU page fault **GPU Pag GPU Pag GPU P** GPU P Compute gsort qsort gsort

Visual profiler - Correlating fault to source

Use dataset 1 Marker and ranges Read dataset1 **Unified Memory** Data Migration DtoH Hto **Data Migration HtoD** Hto CPU page fault GPU page fault **GPU Pag GPU Pag GPU P** GPU P Compute gsort qsort gsort

Manually map the GPU page faults to kernels and CPU page faults to NVTX annotated regions on timeline

Visual profiler - Correlating fault to source



Use VA range of allocations used in kernels to correlate with page address from corresponding page fault

INSTRUCTION LEVEL PROFILING (PC SAMPLING)

PC SAMPLING

- PC sampling feature is introduced in 7.5, available for CC >= 5.2
- Provides CPU PC sampling parity + additional information for warp states/stalls reasons for GPU kernels
- Effective in optimizing large kernels, pinpoints performance bottlenecks at specific lines in source code or assembly instructions
- Maxwell architecture gives overall view of scheduling in GPU
 - Samples warp states periodically in round robin order over all active warps
 - Sampling rate is fixed in visual profiler for a GPU
 - No overheads in kernel runtime, CPU overheads to parse the records

PC SAMPLING ALGORITHM

Warp scheduler 0

Warp scheduler 1 Warp scheduler 2

16

Warp scheduler 3

Max warps
Active warps

16 8 (w0, w4, w8, ..., w28) 16 8 (w1, w5, w9, ..., w29)

8 (w2, w6, w10, ..., w30)

8 (w3, w7, w11, ..., w31)

16

Time in cycles	Warp scheduler 0	Warp scheduler 1	Warp scheduler 2	Warp scheduler 3
0	w0			
256		w1		
512			w2	
768				w3
1024	w4			
1280		w5		
1536			w6	
1792				w7

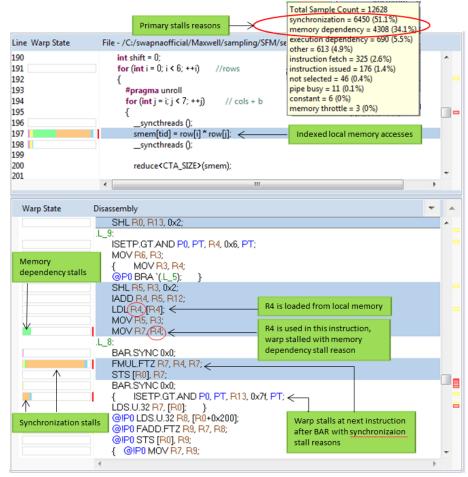
PC SAMPLING

Example

Iterative Closest Point algorithm

Primary stall reasons:

- Memory dependency:
 - LDL ("load local") instructions.
 - Not because of register spilling
 - Local memory is used for local variables with indexed access
- Synchronization stalls
 - BAR.SYNC barrier instruction i.e. __syncthreads()



PC SAMPLING EXAMPLE

Original Code

```
float row[7]
//Initialize array row
int shift = 0:
shared float smem[CTA SIZE];
for (int i = 0; i < 6; ++i)
                            // rows
  #pragma unroll
  for (int j = i; j < 7; ++j) // cols + b
     __syncthreads ();
                                  // sync
     smem[tid] = row[i] * row[j];
                                   // local load
     __syncthreads ();
     reduce(smem);
     if (tid == 0)
       gbuf.ptr (shift++)[blockldx.x + gridDim.x * blockldx.y]
          = smem[0];
```

New Code (LDL removed)

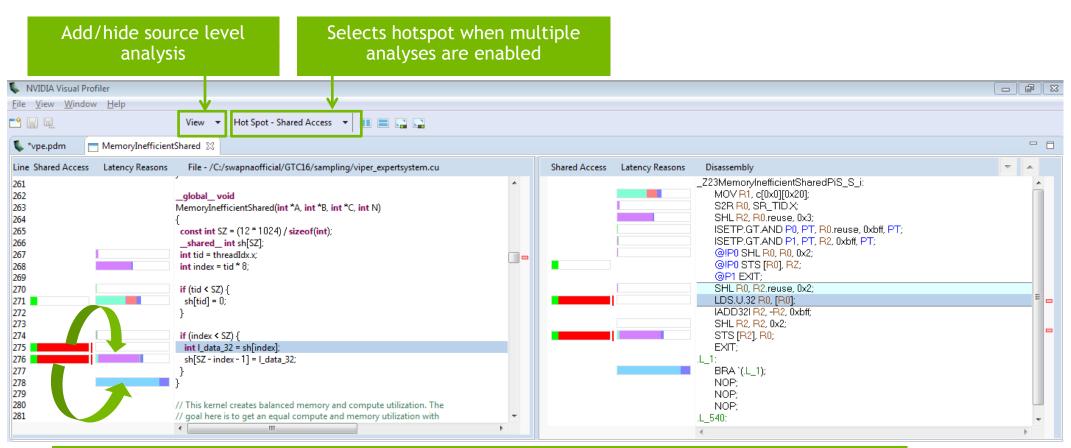
```
float row0, row1, row2, row3, row4, row5, row6;
//Initialize all elements
#define UNROLL REDUCE(val, buf)
  do {
    smem[tid] = val;
       __syncthreads();
       reduce(smem);
       if (tid == 0)
         buf.ptr (shift++)[blockldx.x + gridDim.x * blockldx.y]
           = smem[0];
  } while(0)
UNROLL REDUCE(row0*row0, gbuf);
UNROLL REDUCE(row0*row1, gbuf);
UNROLL_REDUCE(row0*row2, gbuf);
UNROLL_REDUCE(row0*row3, gbuf);
UNROLL_REDUCE(row0*row4, gbuf);
```

Visual profiler

All the source level analysis are combined in the same view

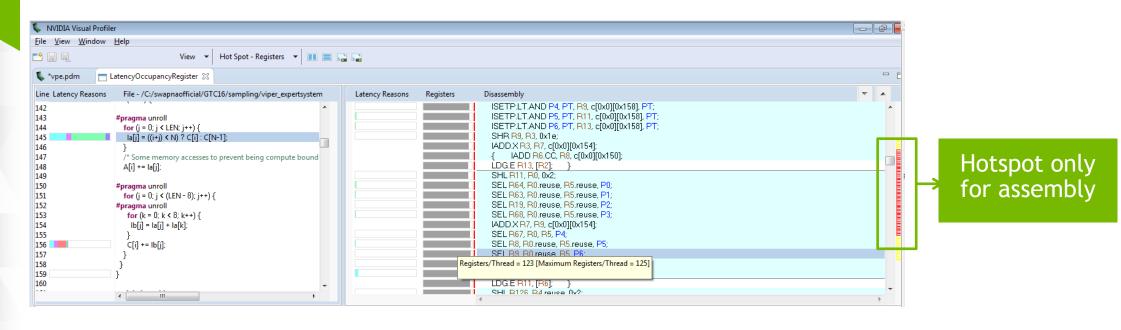
- Global access
- Shared access
- Divergent branch
- Instruction level execution
- PC sampling
- Register pressure

Easy analysis, can pinpoint issues for stalls in some cases



Shared memory load/store bank conflicts cause execution dependency and memory throttle stalls

Register pressure



Registers

Registers/Thread	128	65536	0		8192	1	16384	1 2	24576)	32768	3 4	40960) (49152)	57344	ļ (55536
Registers/Block	28672	65536	0				16k				32k				48k				64k
Block Limit	2	32	0	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32

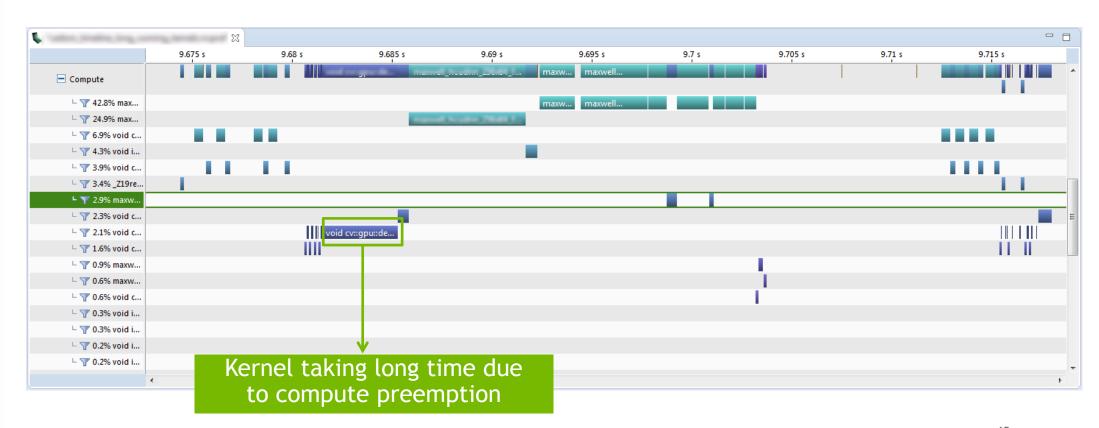
Register is the limiting factor for occupancy

Pascal architecture introduces a new feature compute to give fair chance for all compute contexts while running long tasks.

How it affects profiling results?

- If multiple contexts are running in parallel it is possible that long kernels will get preempted.
- Some kernels may get preempted occasionally due to timeslice expiry for the context
- In CUDA 8.0, if kernel has been preempted mid execution, the time the kernel spends preempted is still counted towards kernel duration
- This can affect the kernel optimization priorities given by visual profiler as there is randomness introduced due to preemption

Visual profiler



How to get accurate results?

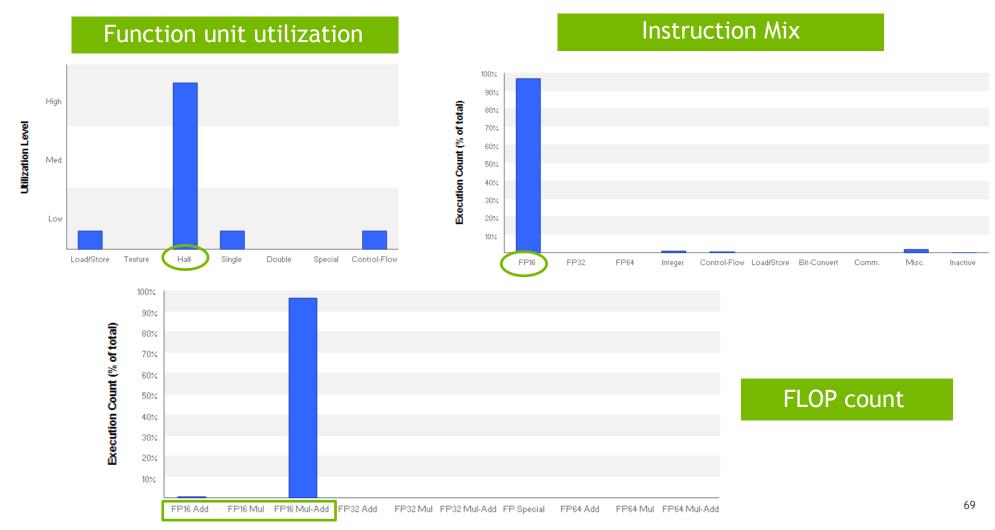
- Run only one context at a time
 - use as secondary GPU
 - unload display driver in linux
 - run only one process (that uses GPU) at one time

FP16 ANALYSIS

FP16 ANALYSIS

- FP16 (half precision) support added in CC 5.3 and 6.0 (Pascal architecture)
- Stores up to 2x larger models in GPU memory.
- Reduce memory bandwidth requirements by up to 2x.
- Profiler gives the instruction counts, half precision function unit utilization and floating point operations count to analyze performance of fp16

FP16 ANALYSIS



NVIDIA TOOLS EXTENSION (NVTX) V2

- NVTX is used for annotating events, code ranges, resources
- Multiple middleware annotating using same strings cause collision
- NVTX V2 introduces domain concept, each middleware can use its own domain
 - Now middleware and your application don't need to collide
 - Visual profiler shows markers/ranges of each domain on separate timeline
- Synchronization primitives can also be named
 - Tools can track and present why you are blocked with a custom message

Sample code

Module A

```
eventAttrib.message.ascii = "Range1";
nvtxRangeId_t idex0 =
nvtxRangeStartEx(&eventAttrib);
//CPU code
nvtxRangeEnd(idex0);
```

Module B

```
eventAttrib.message.ascii = "Range1";
nvtxRangeId_t idex1 =
nvtxRangeStartEx(&eventAttrib);
//CPU code
nvtxRangeEnd(idex1);
```

```
Module A
nvtxDomainHandle_t domain_a =
nvtxDomainCreateA("ModuleA");
eventAttrib.message.ascii = "Range1";
nvtxRangeId_t idex0 =
nvtxDomainRangeStartEx(domain_a, &eventAttrib);
//CPU code
nvtxDomainRangeEnd(domain_a, idex0);
Module B
nvtxDomainHandle t domain b =
nvtxDomainCreateA("ModuleB");
eventAttrib.message.ascii = "Range1";
nvtxRangeId_t idex1 =
nvtxDomainRangeStartEx(domain_b, &eventAttrib);
//CPU code
nvtxDomainRangeEnd(domain_b, idex1);
```

Domain A

Domain B

nvprof

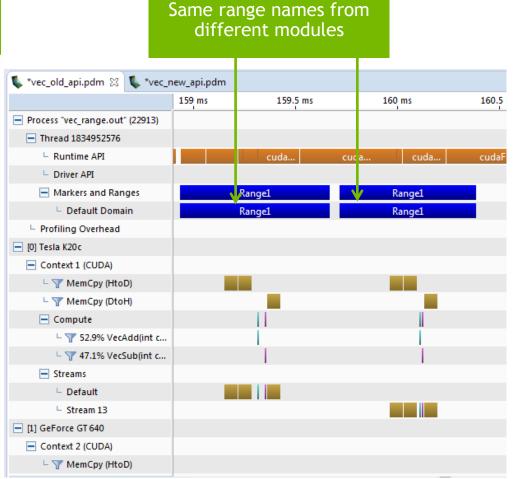
```
=23855== NVTX result:
           Thread <unnamed> (id = 3129952128)
==2385 ===
              Domain "<unnamed>"
                Range "Range1" (4 times, total time: 1.7567ms
             Time
                      Calls
                                            Min
Time(%)
                                  Avg
                                                      Max
                                                           Name
 60.12%
        392.61us
                            49.076us 32.799us 64.833us
                                                           [CUDA memcpy HtoD]
        188.32us
                             47.080us 32.159us 62.113us
                                                           [CUDA memcpy DtoH]
 28.84%
  5.64% 36.863us
                            9.2150us 4.3200us 14.143us VecAdd(int const *, int const *, int*, int)
  5.40% 35.295us
                          4 8.8230us 3.7440us 13.792us VecSub(int const *, int const *, int*, int)
 =23855==
              API calls:
Time (%)
             Time
                      Calls
                                  Avq
                                            Min
                                                      Max
                                                          Name
 89.32% 830.67us
                        12 69.222us 9.9990us
                                                207.59us
                                                          cudaMemcpyAsync
10.68% 99.355us
                          8 12.419us 6.6150us 26.464us cudaLaunch
```

Range information is grouped based on range name

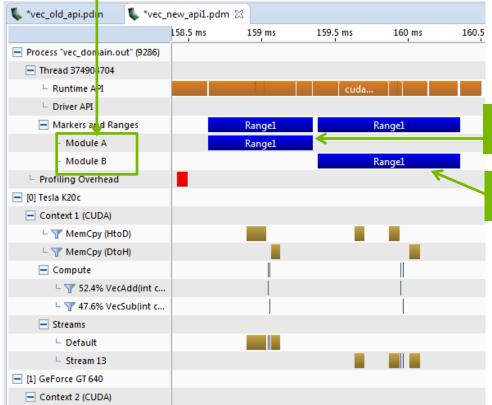
Range information is grouped based on domain first and then range name

```
==23845== NVTX result:
==23845== Thread <unnamed> (id = 3199170432)
==23845==
             Domain "Module A"
==23845==
                Range "Range1" (2 times, total time: 962.08us)
 59.04% 195.78us
                         4 48.944us 33.279us 64.065us
                                                         [CUDA memcpy HtoD]
        98.752us
 29.78%
                                     36.895us 61.857us
                                                         [CUDA memcpy DtoH]
 5.67% 18.815us
                         2 9.4070us 4.7680us 14.047us VecAdd(int const *, int const *, int*, int)
  5.50% 18.240us
                         2 9.1200us 4.0960us 14.144us VecSub(int const *, int const *, int*, int)
 =23845==
             API calls:
            Time
                     Calls
                                 Avg
Time (%)
                                           Min
                                                     Max Name
 87.91% 441.43us
                         6 73.572us 21.199us 168.55us cudaMemcpyAsync
 12.09%
       60.69603
                         4 15.174us 7.1780us 25.665us cudaLaunch
==23845==
             Domain "Module B"
==23845==
               Range "Range1" (2 times, total time: 890.51us)
Time (%)
        201.73us
                         4 50.432us 33.183us 70.274us
                                                         [CUDA memcpy HtoD]
 59.80%
 29.35%
        99.008us
                         2 49.504us
                                     36.895us 62.113us
                                                         [CUDA memcpy DtoH]
 5.55% 18.720us
                         2 9.3600us 4.2560us
                                               14.464us VecAdd(int const *, int const *, int*, int)
  5.29% 17.855us
                         2 8.9270us 3.6800us 14.175us VecSub(int const *, int const *, int*, int)
             API calls:
=23845==
Time (%)
            Time
                     Calls
                                 Avq
                                           Min
                                                     Max
                                                         Name
 91.21%
        436.15us
                         6 72.691us
                                     19.169us 204.58us
                                                         cudaMemcpyAsync
  8.79% 42.031us
                         4 10.507us 7.0370us 14.902us
                                                         cudaLaunch
```

Visual Profiler



Domain names



From

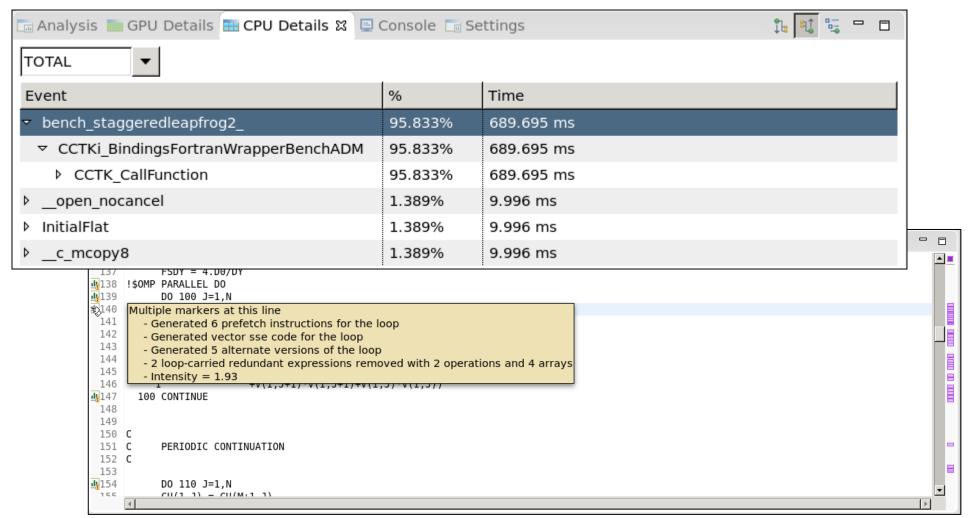
domain 1

From

domain 2

CPU PROFILING

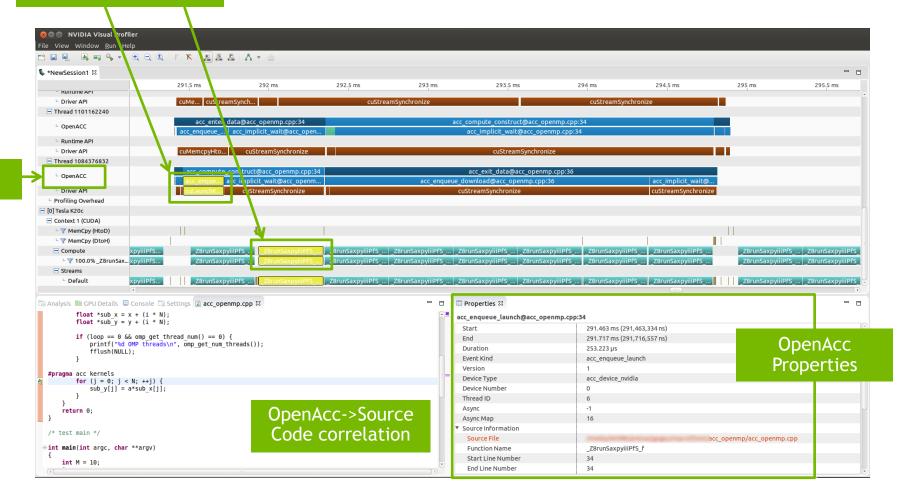
CPU PROFILING



OPENACC PROFILING

OpenAcc->Driver API->Compute correlation

OPENACC PROFILING



OpenAcc timeline

OTHER PRESENTATIONS

CUDA 8.0 features:

S6224 - Featured Presentation: CUDA 8 and Beyond

Unified memory:

- S6216 The Future of Unified Memory
- S6134 High Performance and Productivity with Unified Memory and OpenACC: A LBM Case Study

Tools presentations:

- S6615 Developer Tools Arsenal for Tegra Platforms
- S6784 Maximize OpenACC Performance with the PGPROF Profiler
- S6531 CUDA® Debugging Tools in CUDA 8
- S6111 NVIDIA CUDA® Optimization with NVIDIA Nsight™ Eclipse Edition: A Case Study
- S6112 NVIDIA CUDA® Optimization with NVIDIA Nsight™ Visual Studio Edition: A Case Study

REFERENCES

NVIDIA toolkit documentation:

http://docs.nvidia.com/

Pascal architecture:

https://devblogs.nvidia.com/parallelforall/inside-pascal/

PC sampling blog:

• https://devblogs.nvidia.com/parallelforall/cuda-7-5-pinpoint-performance-problems-instruction-level-profiling/



THANK YOU

JOIN THE CONVERSATION

#GTC16 **У** f **□**





JOIN THE NVIDIA DEVELOPER PROGRAM AT developer.nvidia.com/join

