Mayank Parasar

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CARRIER OBJECTIVE

I work in the field of **Computer Architecture** and my research focus is to come-up with breakthrough solutions in the field of **Interconnection Networks**, **Memory System** and system software/application layer co-design. I am looking for full time opportunities starting in summer.

EDUCATION

Georgia Institute of Technology, Atlanta, Georgia, USA

- Ph.D. in Electrical and Computer Engineering — Aug 2015 – *Present*
  - Thesis: Novel and Efficient Techniques for Guaranteeing Routing and Protocol Level Deadlock Freedom in Interconnection Networks
  - Adviser: Prof. Tushar Krishna
  - Focus: Interconnection Networks, On-Chip Network, Performance, Deadlock, Cache Coherence, Memory System.
  - Cumulative GPA: 4.0/4.0
- Minor in Computer Science — Aug 2016 – May 2017
  - Cumulative GPA: 4.0/4.0
- M.S. in Electrical and Computer Engineering — May 2015 – Aug 2017
  - Cumulative GPA: 4.0/ 4.0

Indian Institute of Technology, Kharagpur (IIT Kharagpur), Kharagpur, West Bengal, India

- B.Tech(Hons.) in Electrical Engineering Department — Aug 2009 – May 2013
  - Cumulative GPA: 8.41 / 10

PUBLICATIONS

CONFERENCES

[1] M. Parasar, N. Enright Jerger, P. Gratz, J. San Miguel, and T. Krishna, "SWAP: Synchronized Weaving of Adjacent Packets for Network Deadlock Prevention," in *Proceedings of International Symposium on Microarchitecture (MICRO)*, Columbus, Ohio, USA, Oct 2019.

[2] M. Parasar and T. Krishna, "BINDU: Deadlock-freedom with one bubble in the network," in *Proceedings of International Symposium on Networks-on-Chip (NOCS)*, New York, USA, Oct 2019.

[3] M. Parasar, A. Sinha, and T. Krishna, "Brownian Bubble Router: Enabling deadlock freedom via guaranteed forward progress," in *Proceedings of International Symposium on Networks-on-Chip (NOCS)*, Torino, Italy, Oct 2018.

[4] M. Parasar, A. Bhattacharjee, and T. Krishna, "SEESAW: Using superpages to improve VIPT caches," in *Proceedings of International Symposium on Computer Architecture (ISCA)*, Torino, Italy, Jun 2018.

[5] M. Parasar, and T. Krishna, "Lightweight emulation of virtual channels using swaps," in *Proceedings of the 10th International Workshop on Network on Chip Architectures (NoCArc)*, Boston, USA, Oct 2017.

AWARDS & SCHOLARSHIPS

- AMD Student Ambassador at Georgia Tech — 2018 – 2019
- Otto & Jenny Krauss Fellow — 2015 – 2016

PROJECTS

Convolutional neural network for number recognition (CUDA C),
Georgia Institute of Technology — Feb 2018 – Apr 2018

- Implemented the computation graph of a convolutional neural network to perform image recognition on a gray-scale image.
- Optimized kernel execution times using shared memory, constant memory and memory coalescing for NVIDIA GPUs.

Implemented distributed server [Client:Store:Vendor] using gRPC framework,
Advanced Operating System, Georgia Institute of Technology Oct 2016 – Nov 2016

- Implemented Client:Store:Vendor communication, with specifications provided in proto file using gRPC.
- Implemented Master for managing mapper and reducer threads. Implemented 'Mapper' and 'Reducer'

Devised C++ kernel to analyze underlying memory system,
High performance cache replacement policies: RRIP, DRRIP, SHiP and EAF
DRAM Page closure policies and Memory Scheduling policies
Advanced Memory System, Georgia Institute of Technology Jan 2016 – Mar 2016

- Used infrastructure from Cache Replacement championship-ISCA2010.
- USIMM is used for implementing DRAM Page Closure: Open-Page, Close-Page, Open-Page-for-Read-Close-Page-for-Write; Memory Scheduling Polices(MCP): FCFS, FR-FCFS-CapN, Fair Scheduling Policy

The Distributed Two-Dimensional Discrete Fourier Transform,
The Multi-Threaded Two-Dimensional Discrete Fourier Transform,
Advanced Programming Techniques, Georgia Institute of Technology Aug 2015 – Oct 2015

- Used MPI (Message Passing Interface) to implement 2-D DFT in C++.
- Used pthreads to implemented Danielson-Lanczos Algorithm (aka Cooley-Tukey FFT Algorithm) to compute 2-D DFT

Dependency Tracking and Forwarding for 5-stage Superscalar Pipeline with Branch Prediction,
Out of Order Pipeline with In-Order Commit,
Chip Multiprocessor (CMP) Memory System Design,
Advanced Computer Architecture, Georgia Institute of Technology Aug 2015 – Nov 2015

- Implemented G-Share Branch predictor
- Implemented Tomasulo's algorithm to implement Out of Order Execution, using Reorder Buffer (ROB) and Register Alias Table (RAT) in Super Scalar machine
- Implemented Static Way Partitioning and Utility based Cache Partitioning for shared L2 Cache

WORK EXPERIENCE

Graduate Research Assistant, Synergy Lab, Georgia Institute of Technology, Atlanta, GA, USA.
May 2016 – *Present*

- Formulating meaningful research optimizations both at micro-architectural level as well as at system software level.

Co-Op Engineer at AMD Research, Advanced Micro Devices, Inc. ("AMD"), Austin, TX, USA.
Aug 2017 – Dec 2017

- Worked on optimizing micro-architectural support for virtual address translation in heterogeneous system architecture involving accelerators. Work involved adding support in gem5 simulator.

Graduate Teaching Assistant, Georgia Institute of Technology, Atlanta, GA, USA.
Aug 2015 – May 2016

- Teaching assistant in course ECE-3056: Architecture, Concurrency, and Energy in Computation under late professor Sudhakar Yalamanchili.
- Designed and implementing programming assignment for the students
- Provided student assistance during office hours

CPU Validation Engineer, NVIDIA Corporation, Bangalore, India.
Jul 2013 – Jun 2015

- Involved in Implementing big.LITTLE architecture functionality in simulator for ARM Cortex-A53 and ARM Cortex-A57 processors
- Implemented ARMv8.1 extensions, including 16 bit ASID and VMID size along with new instructions for atomically accessing memory, in architectural simulator

SKILLS

Computer Architecture Simulators

- gem5, Garnet2.0, USIMM, Cacti

Programming Languages

- C, C++, R, Python, Bash, tcsh, Matlab/Octave, Verilog, HTML

LANGUAGES

- Hindi: Native language.
- English: Proficient (speaking, reading, writing).