

# Mayank Parasar

## Curriculum Vitae

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## Career Objective

I am fourth year PhD student in the School of Electrical and Computer Engineering at Georgia Institute of Technology. My advisor is Dr. Tushar Krishna. I am the recipient of “Otto & Jenny Krauss Fellow” award and also hold the position of Student Ambassador of AMD at Georgia Tech.

I work in the field of **Computer Architecture** and **my research focus** is to come-up with breakthrough solutions in the field of **NoC** (Network on Chip)/ICN (Interconnection Networks), **memory system** and system software/application layer co-design.

## Education

- Aug 2015–Present **Georgia Institute of Technology**, *Doctorate of Philosophy (Ph.D.), Computer Engineering*.  
GPA: 4.0/4.0
- Aug 2016–May 2017 **Georgia Institute of Technology**, *Minor, Computer Science*.  
GPA: 4.0/4.0
- Aug 2015–May 2017 **Georgia Institute of Technology**, *Masters of Science (M.S.), Computer Engineering*.  
GPA: 4.0/4.0
- Aug 2009–May 2013 **Indian Institute of Technology Kharagpur (IIT Kharagpur)**, *Bachelor of Technology (B.Tech(Hons.)), Electrical Engineering Dept.*  
CGPA: 8.41/10.0

## Publications

**Mayank Parasar** and T. Krishna, “Guaranteeing deadlock freedom in arbitrary network topologies using packet swaps,” in *MICRO 51 ACM Student Research Competition (SRC)*, ser. **MICRO SRC**, 2018. [Online]. Available: [https://mayank-parasar.github.io/Mayank-Parasar/papers/micro\\_src.pdf](https://mayank-parasar.github.io/Mayank-Parasar/papers/micro_src.pdf)

**Mayank Parasar**, A. Sinha, and T. Krishna, “Brownian bubble router: Enabling deadlock freedom via guaranteed forward progress,” in *Proceedings of the Twelfth IEEE/ACM International Symposium on Networks-on-Chip*, ser. **NOCS**, 2018. [Online]. Available: [https://mayank-parasar.github.io/Mayank-Parasar/papers/brownianbubble\\_nocs2018.pdf](https://mayank-parasar.github.io/Mayank-Parasar/papers/brownianbubble_nocs2018.pdf)

**Mayank Parasar**, A. Bhattacharjee, and T. Krishna, “Seesaw: Using superpages to improve vpt caches,” in *2018 ACM/IEEE 45th Annual International Symposium on Computer Architecture (ISCA)*, June 2018, pp. 193–206. [Online]. Available: <https://ieeexplore.ieee.org/document/8416828>

**Mayank Parasar** and T. Krishna, “Lightweight emulation of virtual channels using swaps,” in *Proceedings of the 10th International Workshop on Network on Chip Architectures*, ser. **NoCArc’17**. New York, NY, USA: ACM, 2017, pp. 1:1–1:6. [Online]. Available: <http://doi.acm.org/10.1145/3139540.3139541>

**Mayank Parasar**, A. Bhattacharjee, and T. Krishna, "VESPA: VIPT enhancements for superpage accesses," *CoRR*, vol. abs/1701.03499, 2017. [Online]. Available: <http://arxiv.org/abs/1701.03499>

## Skills & Abilities

Computer Architecture Simulators	GEM5, GARNET2.0, USIMM, CACTI
Software-libraries	GRPC, LIBVIRT (VIRTUALIZATION APIs), MPI, PTHREADS, GMP (GNU MULTIPLE PRECISION ARITHMETIC LIBRARY), OpenGL AND GLUT, CUDA C, OPENCV
Programming Languages	C, C++, PYTHON, BASH, TCSH, MATLAB/OCTAVE, VERILOG, R, HTML
Software	LATEX, MS WORD, MS EXCEL, MS POWERPOINT, XILINX, CADENCE VIRTUOSO, INTEL QUARTUS PRIME

## Projects

- Feb 2018 – **Convolutional neural network for number recognition (CUDA C)**, GPU ARCHITECTURE, Georgia Institute of Technology.
  - Implemented the computation graph of a convolutional neural network to perform image recognition on a gray-scale image.
  - Optimized kernel execution times using shared memory, constant memory and memory coalescing for NVIDIA GPUs.
- Oct 2016 – **Implemented distributed server [Client:Store:Vendor] using gRPC framework**
- Nov 2016 – **Implemented MapReduce algorithm using gRPC framework**, ADVANCED OPERATING SYSTEM, Georgia Institute of Technology.
  - Implemented Client:Store:Vendor communication, with specifications provided in proto file using gRPC
  - Implemented Master for managing mapper and reducer threads. Implemented 'Mapper' and 'Reducer'
- Sept 2016 – **Implemented Circuit-Logic Simulator**
- Nov 2016 – **Design and Implement circuit fault simulator**
  - **Test generator for VLSI circuits using PODEM algorithm**, DESIGN AND TESTING OF DIGITAL CIRCUITS, Georgia Institute of Technology.
  - Implemented Circuit simulator and deductive fault detection algorithms for Stuck-at-0/1 faults in circuit.
  - Test generator was implemented using PODEM: Path Oriented Decision Making algorithm.
- Jan 2016 – **Devising C++ kernel to analyze underlying memory system**
- Mar 2016 – **High performance cache replacement policies: RRIP, DRRIP, SHiP and EAF**
  - **DRAM Page closure policies and Memory Scheduling policies**, ADVANCED MEMORY SYSTEM, Georgia Institute of Technology.
  - Infrastructure of Cache Replacement championship-ISCA2010 is used.
  - USIMM is used for implementing DRAM Page Closure: Open-Page, Close-Page, Open-Page-for-Read-Close-Page-for-Write; Memory Scheduling Policies(MCP): FCFS, FR-FCFS-CapN, Fair Scheduling Policy
- Aug 2015 – **The Distributed Two-Dimensional Discrete Fourier Transform**
- Sept 2015 – **The Multi-Threaded Two-Dimensional Discrete Fourier Transform**, ADVANCED PROGRAMMING TECHNIQUES, Georgia Institute of Technology.
  - Used MPI (Message Passing Interface) to implement 2-D DFT in C++
  - Used pthreads to implement Danielson-Lanczos Algorithm (aka Cooley-Tukey FFT Algorithm) to compute 2-D DFT

- Aug 2015 – **Dependency Tracking and Forwarding for 5-stage Superscalar Pipeline with Branch Prediction**  
 Nov 2015
- **Out of Order Pipeline with In-Order Commit**
  - **Chip Multiprocessor (CMP) Memory System Design**, ADVANCED COMPUTER ARCHITECTURE, Georgia Institute of Technology.
  - Implemented Data Forwarding, in a cycle accurate 5-staged Superscalar pipeline simulator with pipe-width 2
  - Implemented G-Share Branch predictor
  - Implemented Tomasulo's algorithm to implement Out of Order Execution, using Reorder Buffer (ROB) and Register Alias Table (RAT) in Super Scalar machine
  - Build a multi-level cache simulator with DRAM based main memory
  - The system is extended to incorporate multiple cores, where each core has a private L1 and a shared L2.
  - Implemented Static Way Partitioning and Utility based Cache Partitioning for shared L2
- Aug 2013 – **Design and Implementation of 5 staged Integer MIPS64 processor pipeline in Verilog**,  
 Dec 2013 UNDERGRADUATE COMPUTER ARCHITECTURE, Indian Institute of Technology Kharagpur (IIT Kharagpur).
- Implemented 5-stage pipelined version of MIPS64 processor for 64-bit integer operations with data forwarding and delayed branch for control hazard handling
  - Separate instruction and data memory, no cache
  - All type of instructions (I-type, J-type, R-type) were implemented with TRAP instruction to terminate program

## Work Experience

- Jun 2016 – **Graduate Research Assistant**, SYNERGY LAB, GEORGIA INSTITUTE OF TECHNOLOGY, Atlanta, GA, USA.  
 Present
- Formulating meaningful research optimizations both at micro-architectural level as well as at system software level.
- Aug 2017 – **Co-Op Engineer at AMD Research**, ADVANCED MICRO DEVICES, INC. ("AMD"), Austin, TX, USA.  
 Dec 2017
- Worked on optimizing micro-architectural support for virtual address translation in heterogeneous system architecture involving accelerators. Work involved adding support in gem5 simulator.
- Aug 2015 – **Graduate Teaching Assistant**, GEORGIA INSTITUTE OF TECHNOLOGY, Atlanta, GA, USA.  
 May 2016
- Teaching assistant in course *ECE-3056: Architecture, Concurrency, and Energy in Computation* under professor Sudhakar Yalamanchili. Work included:
- Designing and implementing programming assignment for the students
  - Creating solutions for the homework assignment
  - Taking doubt clearing sessions as per requirement of the course.
- Oct 2013 – **CPU Validation Engineer II**, NVIDIA CORPORATION, Bangalore, India.  
 Jun 2015
- As a part of CPU Simulator team, endowed with development of critical functionality of ARMv8 64-bit architecture in simulator. Also, involved in coordinating and customizing simulator as per need of different teams within organization. Involved in post-silicon validation of processor, where I did invasive debugging with the help of ARM's external debugger, DStream, paired with DS-5 Development Studio.
- July 2013 – **CPU Validation Engineer I**, NVIDIA CORPORATION, Bangalore, India.  
 Oct 2014
- Involved in Implementing big.LITTLE architecture functionality in simulator for ARM Cortex-A53 and ARM Cortex-A57 processors
  - Implemented ARMv8.1 extensions, including 16 bit ASID and VMID size along with new instructions for atomically accessing memory, in architectural simulator
  - Bug fixing for corner cases of ARMv8-A RISC architecture in simulator
- May 2012 – **Undergraduate Intern**, DEFENSE RESEARCH AND DEVELOPMENT ORGANIZATION (DRDO), Bangalore, India.  
 Jun 2012
- Analog Signal Processing for Sensors developed for Light Combat Aircraft.
  - Designed the filters and signal conditioning circuit for Humidity Polymeric Capacitive Sensor and Zirconia based Oxygen sensor.

## Relevant Coursework

- Advance Computer Architecture
- Advanced Programming Technique
- GPU Architecture
- Advanced Operating System
- Random Processes
- Internet Architecture and Protocols
- Machine learning by Andrew Ng(online)
- Advance Memory Systems
- Interconnection Network
- Advance Digital Design Using Verilog
- Digital System Test
- Compilers and Interpreters
- Introduction to interactive programming in python(online)
- CAD for VLSI

## Languages

English Proficient  
Hindi Native Speaker

## Extracurricular

Running (2018-present)	Georgia Institute of Technology	<i>Runner in 'Team Asha – Georgia Tech' an organization to support education of underprivileged children and women in India</i>
NSO Swimming (2009-11)	Indian Institute of Technology (IIT Kharagpur)	<i>Selected for Swimming by National Sports Organization (NSO), during first and second year of undergraduate studies respectively</i>