GEORGIA INSTITUTE OF TECHNOLOGY
SCHOOL of ELECTRICAL and COMPUTER ENGINEERING

ECE 8813A Spring 2017
Problem Set #1

Assigned: 17-Jan-17
Due Date: 26-Jan-17

Your homework will be due at the *start* of class on **Thursday, January 26.**. This is a review homework so we did not cover this material in class. Please read the text book to find the answer for the first two problems.

PROBLEM 1.1:

Write the truth table for the following gates:

(a) AND

(b) OR

(c) NOR

(d) NAND

(e) XOR

(f) XNOR

PROBLEM 1.2:

Define De Morgan's law and show how it would be used to simplify the following Boolean equation.

$$Y = \overline{A + \overline{A}B + \overline{AB}} + \overline{A + \overline{B}} \tag{1}$$

PROBLEM 1.3:

Given the following Truth Table that represents a 16QAM signal.

I	Q	Symbol	I	Q	Symbol
-3	-3	0000	1	-3	1100
-3	-1	0001	1	-1	1101
-3	1	0011	1	1	1111
-3	3	0010	1	3	1110
-1	-3	0100	3	-3	1000
-1	-1	0101	3	-1	1001
-1	1	0111	3	1	1011
-1	3	0110	3	3	1010

Find:

(a) The Boolean Equation for each bit of the Symbol using a Karnaugh Map.

(b) Create a schematic of digital gates to represent the Boolean Equation. Label each gate and each wire.

(c) Implement the schematic in Verilog using Altera's Schematic Entry tool

(d) Program the schematic in Verilog using a text based tool.