MAYANK PARASAR

Senior Engineer

8+ years of experience in the field of computer Architecture| Research focus on breakthrough Solutions in the field of Interconnection Networks, Memory System, and system software/application layer co-design| Enjoy Coding| Self-starter with excellent management & communications skills | Worked on open-source simulators like gem5| Passionate about designing cycle-accurate system simulators

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AREAS OF EXPERTISE

Computer Architecture Simulators and Tools

Verilator
gem5
Verdi- Synopsys
Garnet2.0
USIMM
Cacti

Programming/Scripting Languages

C
C++
R
Python
Bash
Tcsh
Matlab/Octave
Verilog
System Verilog
UVM

Soft Skills

Communication Excellence
Detail Orientation
Innovation Mindset
Entrepreneurial Spirit
Presentation Excellence

PROFESSIONAL EXPERIENCE

8 yrs. 11 mos.

Samsung Austin R&D Centre (SARC)

1 yr. 7 mos.

Senior Engineer

Aug 2020 – Present. (1 yr. 7 mos.) — Austin, TX, USA

- Performance engineer for Memory Controller for LPDDR4, and LPDDR5
- Features included AES encryption, In-band ECC, Arm Memory Tagging Extension (MTE)
- Verilator modelling of Memory Controller
- Performance engineer for Coherent Interconnect

Advanced Micro Devices, Inc. (“AMD”)

5 mos.

Co-Op Engineer at AMD Research (Internship)

Aug 2017 – Dec 2017 (5 mos.) — Austin, TX, USA

- Worked on optimizing micro-architectural support for virtual address translation in Heterogeneous System Architecture (HSA)
- Added support in gem5 simulator.

Synergy Lab, Georgia Institute of Technology

4 yrs. 2 mos.

Graduate Research Assistant

May 2016 – July 2020 (4 yrs. 2 mos.) — Atlanta, GA, USA

- Formulating meaningful research optimizations both at micro-architectural level as well as at system software level.
- Optimizing processor cache based on OS memory management
- Network-on-Chip micro-architecture performance optimization and deadlock freedom

Georgia Institute of Technology

11 mos.

Graduate Teaching Assistant

Aug 2015 – May 2016 (11 mos.) — Atlanta, GA, USA

- Teaching assistant in course ECE-3056: Architecture, Concurrency, and Energy in Computation under late professor Sudhakar Yalamanchili.
- Designed and implementing programming assignment for the students
- Provided student assistance during office hours

NVIDIA Corporation

1 yr. 11 mos.

CPU Validation Engineer

Jul 2013 – Jun 2015 (1 yr. 11 mos.) — Bangalore, India

- Involved in Implementing big.LITTLE architecture functionality in simulator for ARM Cortex-A53 and ARM Cortex-A57 processors
- Implemented ARMv8.1 extensions, including 16 bit ASID and VMID size along with new instructions for atomically accessing memory, in architectural simulator

PROJECTS

Convolutional neural network for number recognition (CUDA C)
Georgia Institute of Technology
Feb 2018 – Apr 2018

Implemented distributed server [Client:Store:Vendor] using gRPC framework,
Georgia Institute of Technology
Oct 2016 – Nov 2016

DETAILS

- Implemented the computation graph of a convolutional neural network to perform image recognition on a gray-scale image.
- Optimized kernel execution times using shared memory, constant memory and memory coalescing for NVIDIA GPUs.

- Implemented Client:Store:Vendor communication, with specifications provided in proto file using gRPC.
- Implemented Master for managing mapper and reducer threads. Implemented ‘Mapper’ and ‘Reducer’

Devised C++ kernel to analyze underlying memory system,
High performance cache replacement policies: RRIP, DRRIP, SHiP and EAF DRAM Page closure policies and Memory Scheduling policies
Georgia Institute of Technology
Jan 2016 – Mar 2016

- Used infrastructure from Cache Replacement championship-ISCA2010.
- USIMM is used for implementing DRAM Page Closure: Open-Page, Close-Page, Open-Page-for-Read-Close-Page-for-Write; Memory Scheduling Polices (MCP): FCFS, FR-FCFS-CapN, Fair Scheduling Policy

Dependency Tracking and Forwarding for 5-stage Superscalar Pipeline with Branch Prediction, Out of Order Pipeline with In-Order Commit, Chip Multiprocessor (CMP) Memory System Design
Georgia Institute of Technology
Aug 2015 – Nov 2015

- Implemented G-Share Branch predictor
- Implemented Tomasulo's algorithm to implement Out of Order Execution, using Reorder Buffer (ROB) and Register Alias Table (RAT) in Super Scalar machine
- Implemented Static Way Partitioning and Utility based Cache Partitioning for shared L2 Cache

EDUCATION

Ph.D. in Electrical and Computer Engineering
Georgia Institute of Technology
Aug 2015 – July 2020 — Atlanta, GA, USA

Thesis	Subactive Techniques for Guaranteeing Routing and Protocol Deadlock Freedom in Interconnection Networks
Adviser	Prof. Tushar Krishna
Focus	Interconnection Networks, On-Chip Network, Performance, Deadlock, Cache Coherence, Memory System.
Cumulative GPA	4.0/4.0

Minor in Computer Science
Georgia Institute of Technology
Aug 2015 – July 2020 — Atlanta, GA, USA

Cumulative GPA 4.0/4.0

M.S. in Electrical and Computer Engineering
Georgia Institute of Technology
Aug 2015 – July 2020 — Atlanta, GA, USA

Cumulative GPA 4.0/4.0

Bachelor of Technology – Instrumentation Engineering from Electrical Eng. Department
Indian Institute of Technology, Kharagpur (IIT Kharagpur)
Aug 2009 – May 2013 — Kharagpur, West Bengal, India

DETAILS

PUBLICATIONS

CONFERENCES ***(First Author Publications)***

1. "SEEC: Stochastic Escape Express Channel", in The International Conference for High Performance Computing, Networking, Storage and Analysis (SC21), Nov. 2021 (**Best Paper Finalist**), M. Parasar, N. Enright Jerger, P. Gratz, J. San Miguel, and T. Krishna

2. "DRAIN: Deadlock Removal for Arbitrary Irregular Networks," in the 26th IEEE International Symposium on High-Performance Computer Architecture (HPCA), San Diego, California, USA, Feb 2020, M. Parasar, H. Farrokhbakht, N. Enright Jerger, P. Gratz, T. Krishna, and J. San Miguel

3. "SWAP: Synchronized Weaving of Adjacent Packets for Network Deadlock Prevention," in Proceedings of International Symposium on Microarchitecture (MICRO), Columbus, Ohio, USA, Oct 2019. M. Parasar, N. Enright Jerger, P. Gratz, J. San Miguel, and T. Krishna

4. "BINDU: Deadlock-freedom with one bubble in the network," in Proceedings of International Symposium on Networks-on-Chip (NOCS), New York, USA, Oct 2019. M. Parasar and T. Krishna

5. "Brownian Bubble Router: Enabling deadlock freedom via guaranteed forward progress," in Proceedings of International Symposium on Networks-on-Chip (NOCS), Torino, Italy, Oct 2018. M. Parasar, A. Sinha, and T. Krishna

6. "SEESAW: Using superpages to improve VIPT caches," in Proceedings of International Symposium on Computer Architecture (ISCA), Los Angeles, California, USA, Jun 2018. M. Parasar, A. Bhattacharjee, and T. Krishna

7. "Lightweight emulation of virtual channels using swaps," in Proceedings of the 10th International Workshop on Network on Chip Architectures (NoCArc), Boston, USA, Oct 2017. M. Parasar, and T. Krishna

AWARDS AND SCHOLORSHIPS

AMD Student Ambassador at Georgia Tech 2018 – 2019
Otto & Jenny Krauss Fellow 2015 – 2016