Traffic Light Controller

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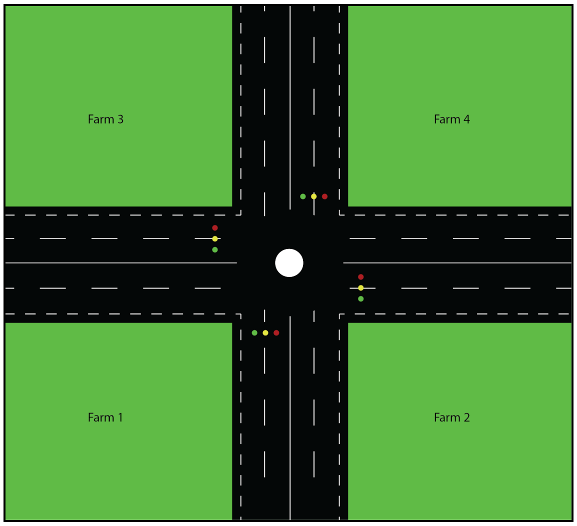
Introduction

Traffic lights are an integral part of modern life. Their proper operation can spell the difference between smooth flowing traffic and four-lane gridlock. Proper operation entails precise timing, cycling through the states correctly, and responding to outside inputs.

The heart of the system is a Finite State Machine (FSM) that directs the unit to light the main and side street lights at appropriate times for the specified time intervals. This unit depends on several inputs which are generated outside the system. To make the system more efficient, we implemented sensors on each traffic light which will tell us whether there is traffic at the light or not.The precedence of the traffic flow is based on which traffic light has higher priority than the other.

System Overview

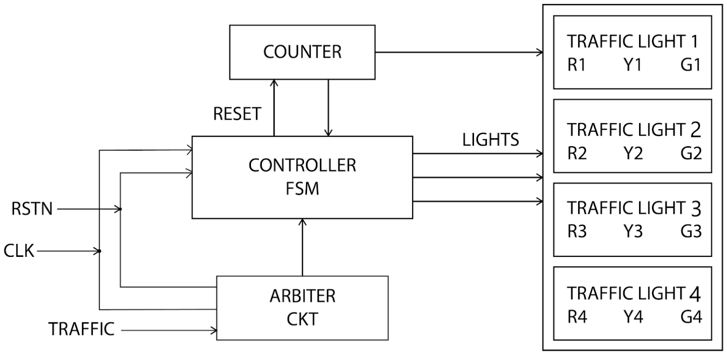
A set of 4 traffic lights have been designed for a 4-way junction as shown in the figure. Only one green signal will be activated at a time. We give a continuous clock input. This design uses a standard two process finite state machine where one process is used to change states on every clock cycle while the other process is used to combinatorially calculate what the next state should be based on the current inputs and the current state.



We have also designed an Arbiter circuit component to accept request signals from each of the traffic lights depending on whether there is any traffic on any of them. The priority of the traffic lights are : **TL4 > TL3 > TL2 > TL1.**

The Arbiter component will return the grant signals to the FSM Controller based on the priority defined above and it will determine which state needs to be activated.

Block Diagram



Implementation Overview

A simple traffic light controller can be implemented by a state machine. Its state progresses according to the value of the timer used . When the value of timer reaches a specific value, the state of the system changes . The states are defined in terms of the output . Timer goes from 0 to 120 and then it is reset to 0.

Each traffic light is programmed to run as follows:

1. It is GREEN for 20 s.
2. Then it remains YELLOW for 10s.

During this time all other lights remain RED.

This process is continued for all the lights successively so that each traffic light is activated (GREEN bit is set) at least once.

There is a sensor too on each road where the traffic lights are placed to indicate if there is any traffic there. For each traffic light, it's TRAFFIC bit is 1 if there is traffic there and the bit is 0 otherwise.

The Arbiter circuit processes the requests from the sensors and depending on the priorities of the traffic lights, it produces the desired outputs.

Implementation Details

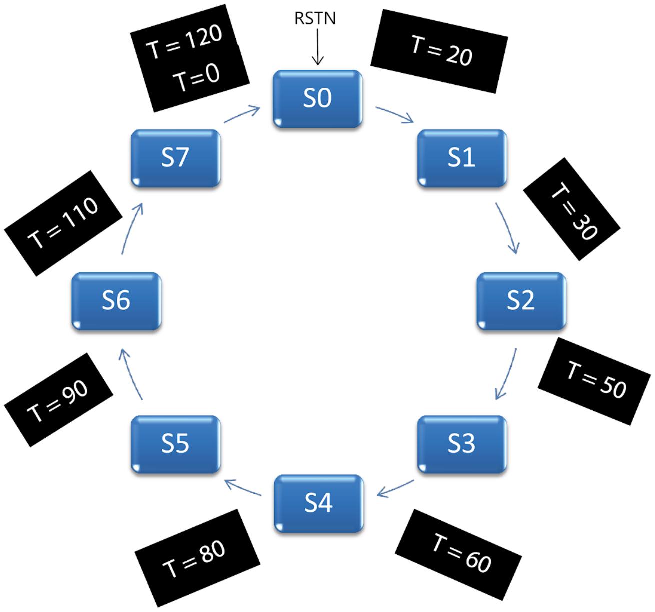
1. Finite State Machine

A synchronous sequential circuit is also known as a Finite State Machine/FSM, if it has a finite number of states. There are two types of FSMs.

- Moore State Machine : Output depends only on the present states.
- Mealy State Machine : Output depends on both the present inputs and the present states.

We have implemented a **Moore type FSM** in our project.

There are a total of 8 states in our project and the state diagram is below



The initial state at time T=0 is S0 and the next state transition takes place at time T=20 and the state then becomes S1. This cycle continues until all the traffic lights are green at least once, ie, at time T=120. At this point, the counter is reset to 0 and the state is reset to S0 and the cycle continues.

The state table for the FSM is as follows

Time	Current State	Next State	Output
0	S0	S0	1234
20	S0	S1	1234
30	S1	S2	1234
50	S2	S3	1234
60	S3	S4	1234
80	S4	S5	1234
90	S5	S6	1234
110	S6	S7	1234
120	S7	S0	1234

2. Arbiter Circuit

Arbiters are electronic devices that allocate access to shared resources. Typical shared resources are busses, memories and multipliers Arbiter circuits may be synchronous or asynchronous.
There are two main arbitration disciplines:

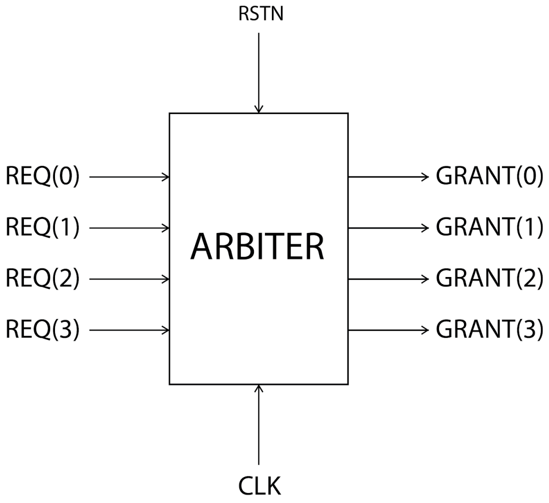
- Static Priority which is based on input port number.
- Round Robin which is based on the previous user.

We have implemented a **Static Priority Arbiter Circuit** in our project.

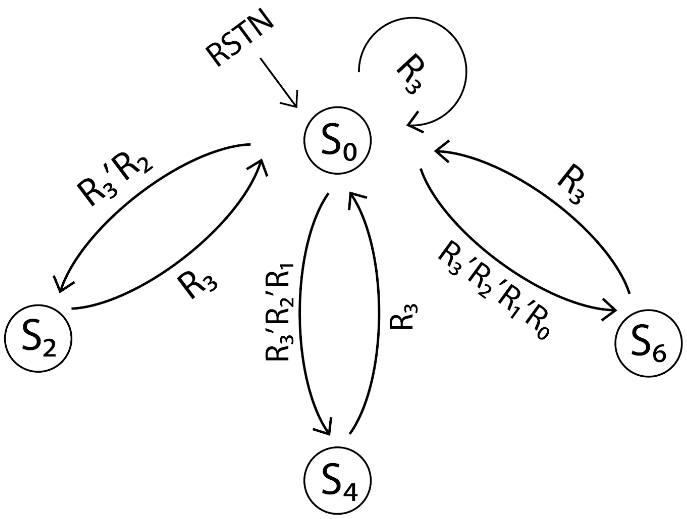
The general working of the Arbiter circuit we have implemented is as follows

- Let's suppose there are only two inputs R1 and R and the circuit gives results in the form of G1 and G2.
- Priority of R1 > R2.
- For the condition of R1=0 and R2=1 it gives G2 =1 it means when request R2 is high and R1 is low, then grant (G2=1) will be high and for condition of R1=1, it gives output as G1=1 irrespective of the value of R2.

The block diagram of the Arbiter Circuit implemented in our project is



The state diagram used to design the Arbiter circuit is as follows



The priorities of the request signals are **R3 > R2> R1> R0.** TL4 (Traffic light 4) sends a request signal R3 and its priority is highest as we have predefined the priorities of the traffic lights, which is : TL4> TL3> TL1> TL1.

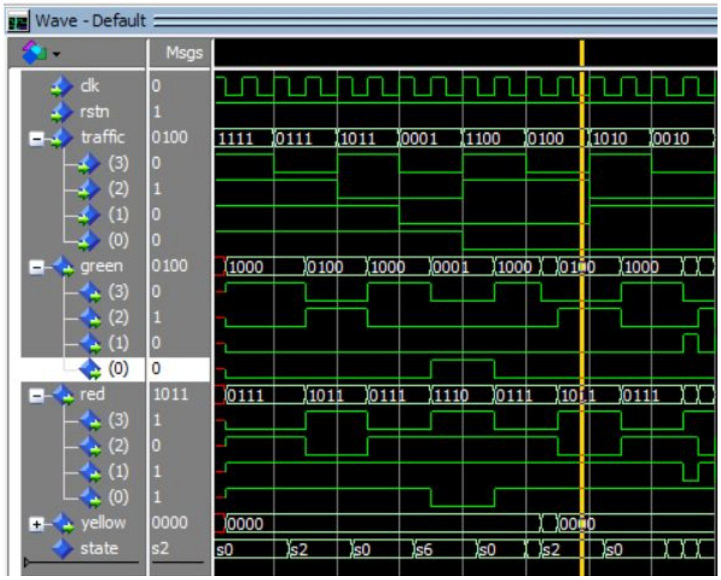
The states considered for the Arbiter Circuit are the following

States	Value (T4 T3 T2 T1)	Signal required to activate
S0	G R R R	R3 or RSTN
S1	R G R R	R3'R2
S2	R R G R	R3'R2'R1
S3	R R R G	R3'R2'R1'R0

State S0 is the default state which will be activated when either the RSTN signal is activated (RSTN=0) or the R3 bit is set (R3=1). Depending on the values of R3, R2, R1 and R0, the Arbiter circuit will allow the desired traffic light to be green and to allow the traffic at that road to pass through first.

Simulation

Note: The simulation below is not exhaustive.



Conclusion

A Traffic Light Controller is quite essential for smooth and efficient functioning of roads. We have simulated and designed a Traffic Light Controller system consisting of a Moore Type FSM and a Static Priority Arbiter Circuit. The designed circuit is quite robust and can prioritise which traffic light needs to be activated (GREEN =1) depending on whether there is any traffic on the roads or not.

References

- Moodle Lectures
- Fundamentals of Digital Logic with VHDL Design by Stephen Brown and Zvonko Vranesic
- Digital Design with an Introduction to Verilog HDL by M.Morris Mano
- Understanding Arbiter Circuit Part 1
- Understanding Arbiter Circuit Part 2
- Introduction to Finite State Machines
- FSM Properties and Types

Links

- Google Drive Folder
- Presentation Video