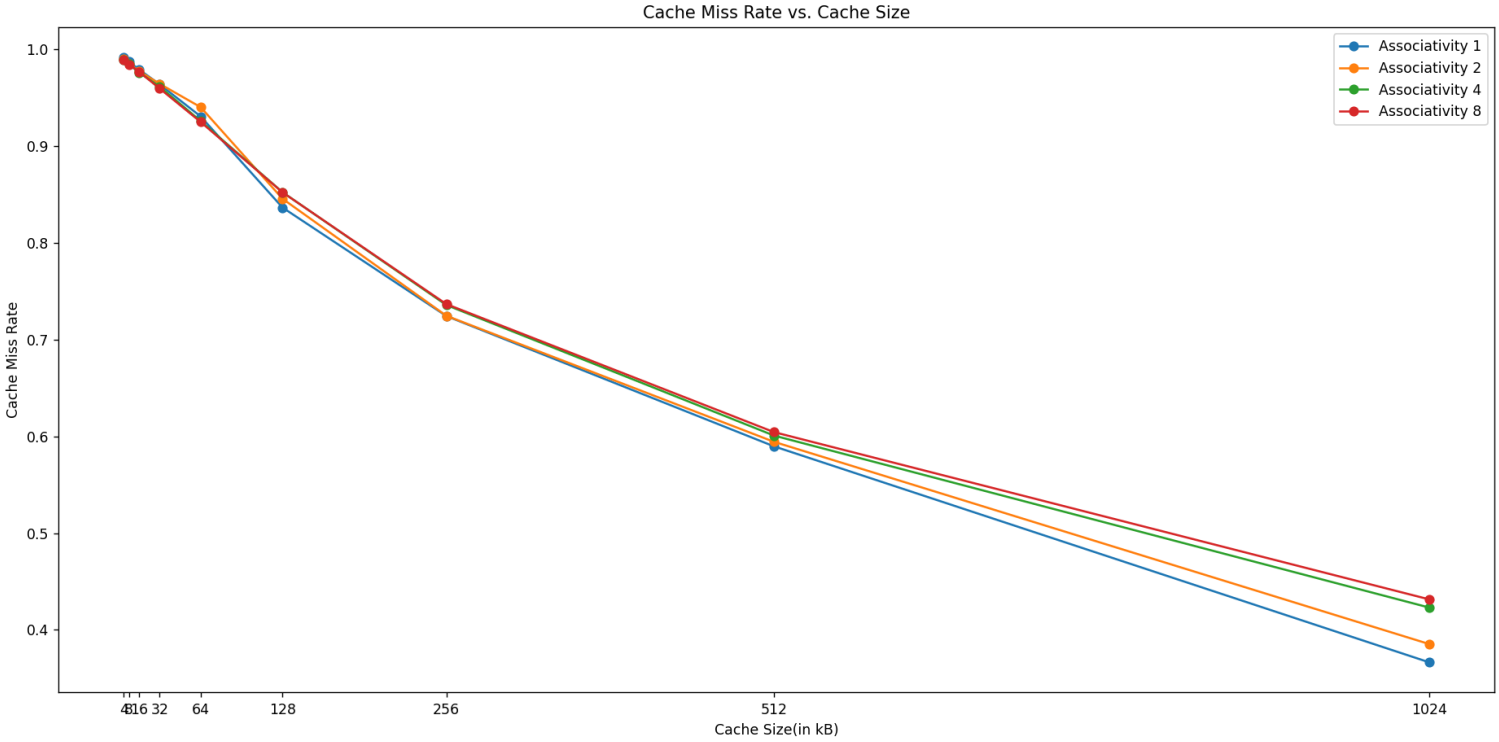
1)Observation Table

Miss cache rate	L2_Size(in kB)	L2_associativity
0.992201	4	1
0.990223	4	2
0.989613	4	4
0.989427	4	8
0.987463	8	1
0.985470	8	2
0.984840	8	4
0.984746	8	8
0.979320	16	1
0.977586	16	2
0.976224	16	4
0.976940	16	8
0.963995	32	1
0.964583	32	2
0.961608	32	4
0.959723	32	8
0.930879	64	1
0.940462	64	2
0.926140	64	4
0.925180	64	8
0.836640	128	1
0.845729	128	2
0.852489	128	4
0.852353	128	8

0.724489	256	1
0.724747	256	2
0.735865	256	4
0.736818	256	8
0.589730	512	1
0.594389	512	2
0.600862	512	4
0.604438	512	8
0.366380	1024	1
0.385275	1024	2
0.423008	1024	4
0.431481	1024	8



Observations

In this architecture we have two cache levels i.e L1 cache and L2 cache.The first-level (L1) cache is small enough to provide a one- or two-cycle access time. The second-level (L2) cache is larger, and therefore slower, than the L1 cache. The processor first looks for the data in the L1 cache. If the L1 cache misses, the processor looks in the L2 cache. If the L2 cache misses, the processor fetches the data from main memory.

In a cache, memory addresses are divided into sets, and each set contains a certain number of cache lines or slots. Associativity refers to the number of cache lines in each set. In a direct-mapped cache (associativity of 1), each set contains only one cache line, while in a fully associative cache, there's only one set with all cache lines.

- It can be seen from the graph as we increase the size of L2 cache , the cache miss rate decreases. It can be said that the cache miss rate is inversely proportional to the L2 cache size. Increasing the L2 size means the more data can be stored in cache and when the processor needs the data and it looks in the L2 cache , there is a better chance of finding it. Thus the miss rate reduces as Increasing cache capacity can reduce conflict and capacity misses.
- For small cache sizes and low associativity (1 or 2), conflict misses are a significant source of cache misses. Since there are only a few cache sets, the chances of different memory blocks mapping to the same set are high.Increasing associativity to 4 or 8 helps mitigate conflict misses. More cache lines per set mean that a cache can accommodate more memory blocks without evictions, reducing the likelihood of cache conflicts and associated misses. This leads to a reduction in miss rates which is seen in the graph and in the observation table.
- With each increase in associativity, the improvement in conflict miss reduction becomes smaller. This is because the cache is already quite capable of accommodating a diverse set of memory blocks with the existing associativity levels.