# UNIT 2

# Chapter 1

# INTERFACING OF I/O DEVICES

## 1.1 INTRODUCTION

The I/O devices, such as keyboards and displays are like communication channels between MPU and the outside world. Data can enter or exit in group of eight bits using entire data bus; this is called parallel I/O mode. The other method is serial I/O in which one bit is transferred at a time using one data line.

The 8085 microprocessor uses a 16-bit address bus for identifying and accessing memory locations. This results in a memory space of $2^{16}$ = 64 KB, which ranges from 0000H to FFFFH.

## 1.2 BASIC INTERFACING CONCEPTS

In 8085 based systems, I/O devices can be interfaced using two techniques:
1) Memory Mapped I/O 2) Peripheral Mapped I/O (I/O Mapped I/O)

Memory Mapped I/O means interfacing I/O devices using addresses from memory space (0000H to FFFFH). While Peripheral Mapped I/O or I/O Mapped I/O means interfacing I/O devices using separate numbering scheme reserved for I/O ports addresses from I/O space (00H to FFH). In Memory Mapped I/O, a device is identified with 16-bit address and enabled by memory control signals. While in I/O Mapped I/O, a device is identified with 8-bit address and enabled by I/O control signals. In Memory Mapped I/O, data bytes are transferred using memory related data transfer instructions (LDA, STA, LHLD, SHLD, LDAX, STAX etc). While in I/O Mapped I/O, data bytes are transferred using I/O related data transfer instructions (IN, OUT).

### 1.2.1 Peripheral I/O instructions

The 8085 has two instructions for data transfer between the processor and I/O device that are IN and OUT. The instruction IN inputs data from an input device such as switch into the accumulator and the instruction OUT sends content of accumulator to an output device such as LED.

| Instruction | Operand | Description |
|---|---|---|
| IN | 8-bit Port address | 2-byte instruction, where second byte is port address of input device. This instruction transfers data from input device to accumulator |
| OUT | 8-bit Port address | 2-byte instruction, where second byte is port address of output device. This instruction transfers data from accumulator to output device |

### 1.2.2 I/O Execution

The execution of I/O instructions can be illustrated using the examples of IN and OUT instructions.

**Execution of IN instruction:** If IN 01H instruction is written on address 7005H

- In 1st machine cycle, μp places higher order address 70H on $A_{15} – A_8$ and the low order address 05H on $AD_7 – AD_0$.
- At the same time ALE goes high indicating presence of address bits on $AD_7 – AD_0$ and $IO/\overline{M}$ goes low indicating memory operation.
- Then μp sends $\overline{RD}$ control signal, which is combined with $IO/\overline{M}$ to generate $\overline{MEMR}$ signal and processor fetches opcode (byte 1) of instruction IN using data bus. Then μp is ready for reading port address (byte 2) of the instruction.
- In 2nd machine cycle μp places the next address, 7006H on address bus and gets the device address 01H (byte 2) via data bus.
- In 3rd machine cycle $IO/\overline{M}$ goes high indicating I/O operation and μp places the device address 01H on $AD_7 – AD_0$ as well as $A_{15} – A_8$.
- The contents of I/O device are placed on data bus, followed by control signal $\overline{RD}$ . Hence generating $\overline{IOR}$ to read data of from I/O device which appears in accumulator.

**Execution of OUT instruction:** If IN 01H instruction is written on address 7008H

- In 1st machine cycle, μp places higher order address 70H on $A_{15} – A_8$ and the low order address 08H on $AD_7 – AD_0$.
- At the same time ALE goes high indicating presence of address bits on $AD_7 – AD_0$ and $IO/\overline{M}$ goes low indicating memory operation.
- Then μp sends $\overline{RD}$ control signal, which is combined with $IO/\overline{M}$ to generate $\overline{MEMR}$ signal and processor fetches opcode (byte 1) of instruction OUT using data bus. Then μp is ready for reading port address (byte 2) of the instruction.
- In 2nd machine cycle μp places the next address, 7009H on address bus and gets the device address example - 01H via data bus.
- In 3rd machine cycle $IO/\overline{M}$ goes high indicating I/O operation and μp places the device address 01H on $AD_7 – AD_0$ as well as $A_{15} – A_8$.
- The Accumulator contents are placed on data bus, followed by control signal $\overline{WR}$ . Hence generating $\overline{IOW}$ to write data of accumulator in I/O device.

## 1.3 INTERFACING USING LOGIC GATES

Note: This topic diagrams were drawn in class with examples of interfacing 2KB RAM whose address starts from 8000H. Also for 4KB RAM whose address starts from 7000H.

## 1.4 MEMORY-MAPPED I/O

In memory-mapped I/O, the input and output devices are assigned and identified by 16-bit address. To transfer data between MPU and I/O devices, memory-related instructions (such as LDA, STA etc) and memory control signals ($\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$) are used.

### 1.4.1 Memory-Related Data Transfer Instructions

Note: Refer ppt / excel sheet of data transfer instructions mailed to your class.

### 1.4.2 Execution of Memory-Related Data Transfer Instruction

The execution of memory-related data transfer instructions is similar to the execution of IN and OUT instructions, except that the memory-related instructions have 16-bit addresses.

For example: To execute the instruction STA 8000H written on RAM location 7003H.

- In 1st machine cycle higher order address 70H is placed on $A_{15} – A_8$ and lower order address 03H is placed on $A_{D7} – A_{D0}$.
- At the same time ALE goes high indicating presence of address bits on multiplexed bus and $IO/\overline{M}$ goes low indicating memory operation.
- Then μp sends $\overline{\text{RD}}$ control signal, which is combined with $IO/\overline{M}$ to generate $\overline{\text{MEMR}}$ signal and processor fetches opcode (byte 1) of instruction STA using data bus. Then μp is ready for reading port address (byte 2 and byte 3) of the instruction.
- In 2nd machine cycle μp places the next address, 7004H on address bus and gets the lower byte of 16-bit address i.e., 00H.
- In 3rd machine cycle μp places the next address, 7005H on address bus and gets the higher byte of 16-bit address i.e., 80H. This is how 16-bit address 8000H is read.
- In 4th machine cycle also $IO/\overline{M}$ remains low indicating memory operation. This time μp sends $\overline{\text{WR}}$ control signal, which is combined with $IO/\overline{M}$ to generate $\overline{\text{MEMW}}$ signal and μp writes accumulator content on selected memory address 8000H.

## 1.5 TESTING AND TROUBLESHOOTING I/O INTERFACING CIRCUITS

- To troubleshoot the circuit the first step is to check the wiring and pin connections.
- After preliminary check, we need to generate a constant and identifiable signal by executing a continuous loop called diagnostic routine.
- In this diagnostic routine we send some known data from input to accumulator using IN instruction in a continuous loop and check if input data is matching with data of accumulator. If the data match then input interfacing circuit is working properly if there is a mismatch then the mismatched bit is needed to be recognized.
- Similarly to check output interfacing circuit, we send some known data from accumulator to output using OUT instruction in a continuous loop and check if output data is matching with data of accumulator. If the data match then output interfacing

circuit is working properly if there is a mismatch then the mismatched bit is needed to be recognized.