UNIT 5

Chapter 1

THE PENTIUM AND PENTIUM PRO MICROPROCESSORS

1.1 INTRODUCTION

The Pentium is a fifth-generation (80586) microprocessor developed and manufactured by Intel.

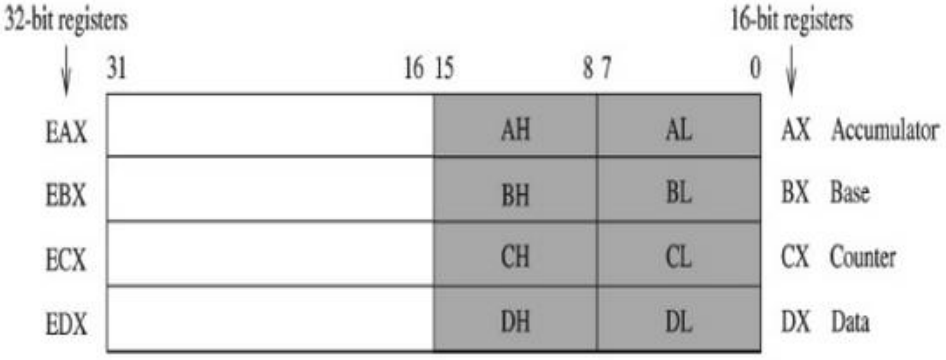
- 237 pin PGA (Pin Grid array)
- 32-bit Address Bus hence 4 GB addressable memory.
- 64-bit data bus
- Wider internal data paths
- Added second execution pipeline for
    - Superscalar performance
    - Two instructions/clock
- Doubled on-chip cache
    - 8 KB for data
    - 8 KB for instruction
- Branch prediction logic allows programs that branch to execute more efficiently

The Pentium Pro is a sixth-generation (80586) microprocessor developed and manufactured by Intel.

- 387 pin PGA (Pin Grid array)
- Three-way superscalar
    - 3 instructions/clock
- 36-bit address bus, 64 GB address space
- Introduced dynamic execution
    - Out-of-order execution
    - Speculative execution
- In addition to the L1 cache has 256 KB L2 cache

1.2 Special Pentium registers

a) General Purpose Registers



- Four 32-bit registers that can be used as
  - Four 32-bit registers (EAX, EBX, ECX, EDX)
  - Four 16-bit registers (AX, BX, CX, DX)
  - Eight 8-bit registers (AH, AL, BH, BL, CH, CL, DH, DL)

- EAX: Accumulator for holding operands and result.
- EBX: Base Index. Holds address to access a memory location.
- ECX: Counter for string and loop operations.
- EDX: Data register for holding operands. Holds I/O addresses.

b) Pointer / Index Registers

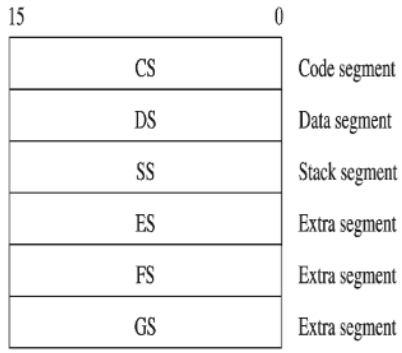
- SP (16-bit Stack Pointer) / ESP (Extended 32-bit Stack Pointer) – Used to address the memory location in the stack segment with stack segment register.
- BP (16-bit Base Pointer) / EBP (Extended 32-bit Base Pointer) – Random Pointer for Stack Segment (SS)
- SI (16-bit Source Index) / ESI (Extended 32-bit Source Index) – Holds the source data for string instructions. For other instructions it is used to select location in data segment.
- DI (16-bit Destination Index) / EDI (Extended 32-bit Destination Index) - Holds the destination data for string instructions. For other instructions it is used to select location in data segment.

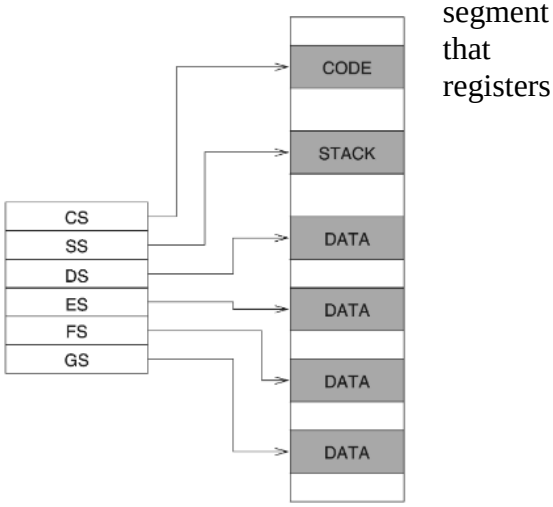
c) Instruction Pointer

- EIP (32-bit Extended Instruction Pointer)
- Holds the offset address within a segment of the next instruction to be executed.
- The offset is always relative to the base pointed by code segment register.
- Lower 16-bit of EIP contain 16-bit Instruction Pointer (IP) used for 16-bit offset addressing.

d) Segment Registers

There are six segment registers that hold 16-bit segment selectors. A segment selector is a special pointer that identifies a segment in memory. The six segment registers are:





- CS: code segment register
- SS: stack segment register
- DS: data segment registers
- ES, FS, GS: Extra segment Registers for Data

Four data segment registers provide programs with flexible and efficient ways to access data.

- When writing application code, you generally create segment selectors with assembler directives and symbols.
- The assembler and/or linker then create the actual segment selectors associated with these directives and symbols. If you are writing system code, you may need to create segment selectors directly.

e) Flag Register

The following diagram shows the structure of 32-bit Extended Flag (EFLAG) Register

31			22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
..	..	..	..	ID	VIP	VIF	AC	VM	R	-	NT	I/O PL	I/O PL	O	D	I	T	S	Z	-	A	-	P	1	C

Status Flag
C = Carry Flag
P = Parity Flag
A = Auxiliary Carry Flag
Z = Zero Flag
S = Sign Flag
O = Overflow Flag

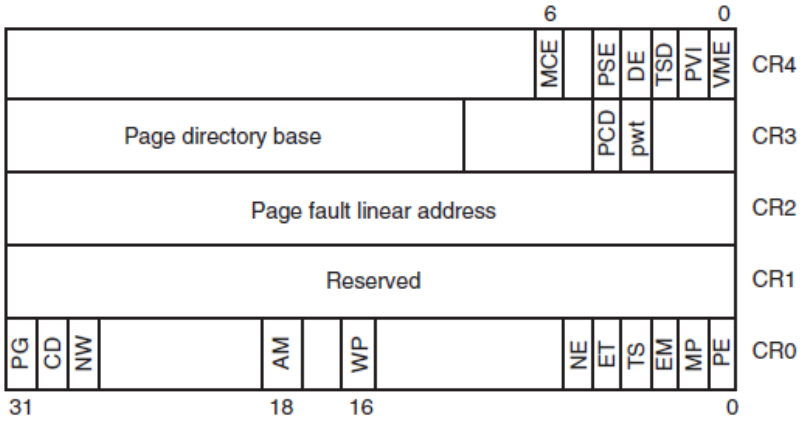
Control Flag
D = Direction Flag

System Flag
T = Trap Flag
I = Interrupt Flag
I/OPL = I/O Privilege Flag
NT = Nested Task
RF = Resume Flag
VM = Virtual Mode
AC = Alignment Check
VIF = Virtual Interrupt Flag
VIP = Virtual Interrupt Pending
ID = Identification Flag

- C (Carry): Holds Carry after addition or Borrow after subtraction.
- P (Parity): Logic 0 for odd parity, logic 1 for even parity.
- A (Auxiliary Carry): Holds Carry after addition or borrow after subtraction between lower and upper nibble.
- Z (Zero): Logic 1 if result of arithmetic logic operation is zero.
- S (Sign): Holds the sign (MSB) of the result after arithmetic logic operation.
- T (Trap flag): Enables trapping through on-chip debugging feature. Used in single step mode.
- I (Interrupt Flag): Controls operation of INTR (interrupt request) pin
- D (Direction Flag):
- O (Overflow): Occurs when Signed numbers are added or subtracted. Overflow indicates that the result has exceeded the machine capacity.
- I/OPL (Input / Output Privilege): Used in Protected Mode operation to select the privilege level for I/O devices.
- NT (Nested Task): Indicates, the current task is nested with another task in protected mode.
- R (resume): Used with debugging to control resumption of execution of the next instruction.
- VM (Virtual Mode): Selects virtual Mode operation.
- AC (Alignment Check): Indicates the state of AM bit in control register 0 (CR0)
- VIF (Virtual Interrupt Flag): Virtual image of Interrupt Flag. Used to enable or disable interrupt when processor is operating in virtual mode.

- VIM (Virtual Interrupt Pending): Indicates virtual interrupt is pending.
- ID (Identification): Its identification for CPUID instruction. If program can set and clear ID flag the processor supports CPUID instruction.

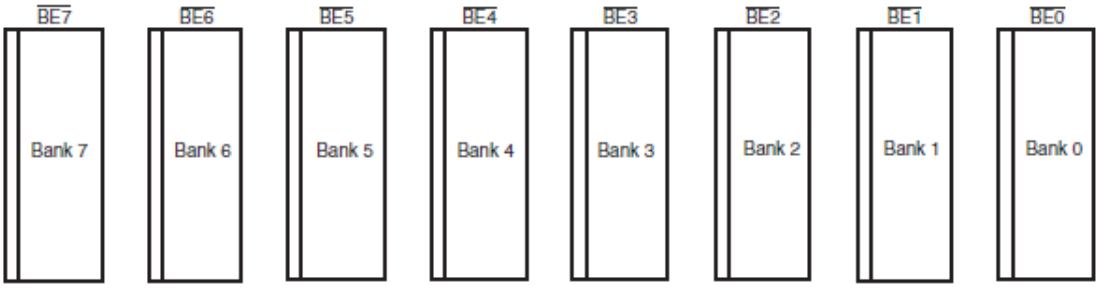
f) Control Register



- Control registers (CR0, CR1, CR2, CR3, and CR4) determine operating mode of the processor and the characteristics of the currently executing task.
- These registers are 32 bits.
- **CR0** — Contains system control flags that control operating mode and states of the processor.
    - **CD (Cache Disable):** controls the internal cache.
    - **NW (Not Write-through):** selects the mode of operation for the data cache.
    - **AM (Alignment Mask):** enables alignment checking when set.
    - **WP (Write Protect):** protects user-level pages against supervisor-level write operations.
    - **NE (Numeric Error):** enables standard numeric coprocessor error detection.
- CR1 — Reserved.
- CR2 — Contains the page-fault linear address (the linear address that caused a page fault)
- CR3 — Contains the physical address of the base of the page directory and two flags (PCD and PWT). This register is also known as the page-directory base register. The PCD and PWT flags control caching of the page directory in the processor's internal data caches.
- CR4 — Contains a group of flags that enable several architectural extensions, and indicate operating system or executive support for specific processor capabilities. The control registers can be read and loaded (or modified) using the MOV instruction.

1.3 MEMORY MANAGEMENT

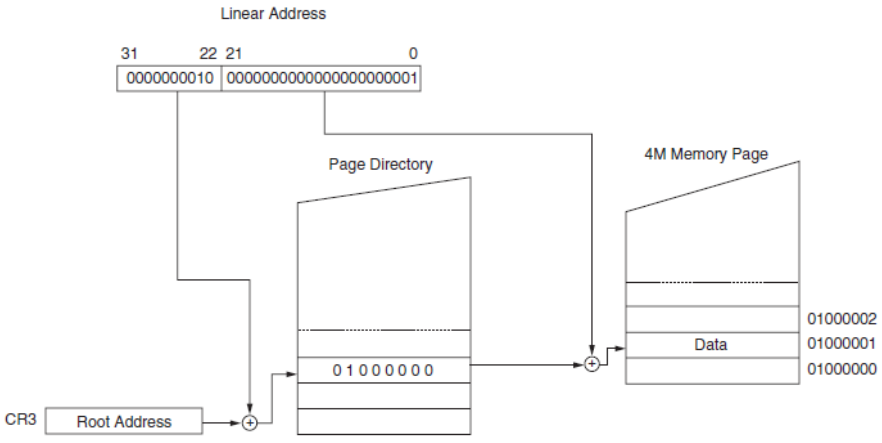
1.3.1 The Memory System



- Eight banks where each bank stores byte-wide (8-bit) data with a parity bit.
- The 64-bit-wide memory for double-precision floating-point data.
- Memory selection is accomplished with the Bank Enable signals (Pins $\overline{BE7}$ *to* $\overline{BE0}$).
- These separate memory banks allow the Pentium to access any single byte (8-bit), word (16-bit), double-word (32-bit) or quad-word (64-bit) with one memory transfer cycle.

1.3.2 Paging Unit

- The paging mechanism functions with 4K-byte memory pages or with 4M-byte memory pages.
- The new 4M-byte page sizes are selected by the PSE bit in control register 0.
- In 4K byte paging scheme there is page table entry in linear address.
- In 4M byte paging scheme there are no page tables; instead, the page directory addresses a 4M-byte memory page.



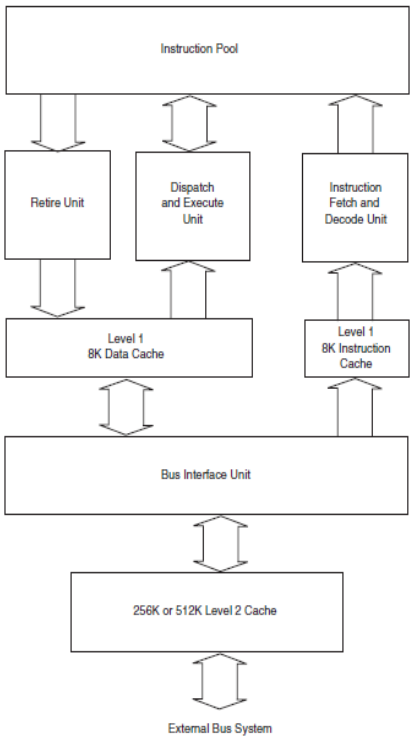
1.3.3 Memory Management Mode

- The SMM (System Memory management Mode) is not used as an application or a system-level feature.
- It is intended for high-level system functions such as power management and security, which are controlled by the operating system.
- Access to the SMM is accomplished via external hardware interrupt applied to the pin $\overline{SMI}$.
- When this interrupt is activated, the processor begins executing system-level software in the SMMRAM (System Management RAM) called the SMM state dump record.
- The $\overline{SMI}$ interrupt disables all other interrupts that are normally handled by user applications and the operating system.
- A return from the SMM interrupt is accomplished with a new instruction called RSM.

1.4 PENTIUM INSTRUCTIONS

Instruction	**Function**	
CMPXCHG8B	Compare and exchange eight bytes	• CMPXCHG8B instruction compares the 64-bit number stored in EDX : EAX pair with the contents of a 64-bit data of destination operand (memory location or register pair). • If the values are equal, the 64-bit value in ECX:EBX is stored in the destination operand. • If the values are not equal then value in the destination operand is loaded into EDX:EAX
CPUID	Return CPU identification code	• CPUID instruction reads the CPU identification code and other information from the Pentium. • To use the CPUID instruction, first load EAX with the input value and then execute CPUID. • If a 0 is placed in EAX before executing the CPUID instruction, the microprocessor returns the vendor identification in EBX, EDX, and EBX. • For example, the Intel Pentium returns "GenuineIntel" in ASCII code with the "Genu" in the EBX, "ineI' in EDX, and "ntel" in ECX.
RDTSC	Read time-stamp counter	• RDTSC instruction reads the time-stamp counter into EDX:EAX. • The time-stamp counter counts CPU clocks from the time the microprocessor is reset
RDMSR	Read model-specific register	• RDMSR instructions allow the model-specific registers to be read • Use ECX to convey the register number to the microprocessor and use EDX:EAX for the 64-bit-wide read
WRMSR	Write model-specific register	• WRMSR instructions allow the model-specific registers to be written • Use ECX to convey the register number to the microprocessor and use EDX:EAX for the 64-bit-wide write
RSM	Return from system management interrupt	

1.5 INTERNAL STRUCTURE OF PENTIUM PRO

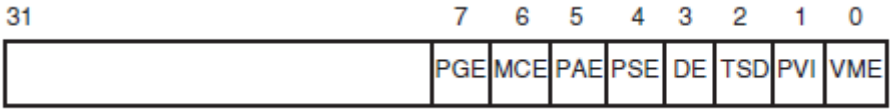


- The system buses, which communicate to the memory and I/O, connect to an internal level 2 cache
- The level 2 cache in the Pentium Pro is either 256K bytes or 512K bytes. It speeds the processing.
- The bus interface unit (BIU) controls the access to the system buses through the level 2 cache.
- The BIU generates the memory address and control signals, and passes and fetches data or instructions to either a level 1 data cache or a level 1 instruction cache.
- The implementation of separate caches improves performance.
- The instruction cache is connected to the instruction fetch and decode unit (IFDU).
- IFDU contains three separate instruction decoders that decode three instructions simultaneously.
- IFDU includes a branch prediction logic section that looks ahead in code sequences that contain conditional jump instructions. If a conditional jump is located, the branch prediction logic tries to determine the next instruction in the flow of a program.
- Once decoded the instructions are passed to the instruction pool, where they remain until the dispatch and execution unit or retire unit obtains them.
- The Dispatch and Execute Unit (DEU) retrieves decoded instructions from the instruction pool when they are complete, and then executes them.
- The Retire Unit (RU) checks the instruction pool and removes decoded instructions that have been executed. The RU can remove three decoded instructions per clock pulse.

1.6 SPECIAL PENTIUM PRO FEATURES.

Control Register 4

- CR4 has two new control bits that are added to the control register array.



  - **VME (Virtual Mode Extension): E**nables support for the virtual interrupt flag in protected mode. If VME = 0, virtual interrupt support is disabled.
  - **PVI (Protected mode Virtual Interrupt): E**nables support for the virtual interrupt flag in protected mode.
  - **TSD (Time Stamp Disable):** Controls the RDTSC instruction.
  - **DE (Debugging Extension):** Enables I/O breakpoint debugging extensions when set.
  - **PSE (Page Size Extension):** Enables 4M-byte memory pages when set in the Pentium, or 2M-byte pages when set in the Pentium Pro whenever PSE is also set.
  - **PAE (Page Address Extension):** Enables address lines A35–A32 whenever a special new addressing mode, controlled by PGE, is enabled for the Pentium Pro.
  - **PGE (Page Extension):** This bit along with PSE enables decides the page size.
  - **MCE (Machine Check Enable):** Enables the machine checking interrupt.