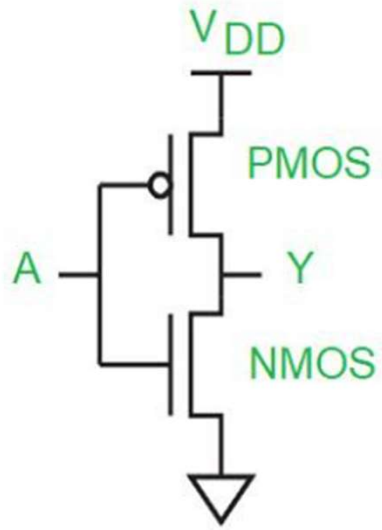
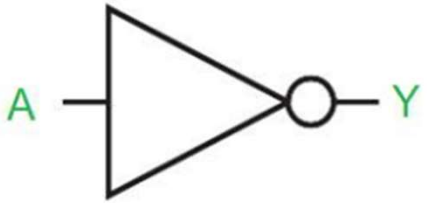
# CMOS logic gates

- The logic gates are the basic building blocks of all digital circuits and computers. These logic gates are implemented using transistors called MOSFETs.
- A MOSFET transistor is a voltage-controlled switch. The MOSFET acts as a switch and turns on or off depending on whether the voltage on it is either high or low.
- There are two types of MOSFETs: NMOS and PMOS.

- The NMOS turns on when the voltage is high and off when the voltage is low.
- The PMOS, on the other hand, turns on whenever the voltage is low and goes off as the voltage goes high.
- When the two are used together to realize the logic gates, they are called CMOS (Complementary MOS).
- The reason they are called complementary is that NMOS and PMOS work in a complementary fashion. When the NMOS switch turns on, the PMOS gets off, and vice-versa.

# CMOS Inverter:

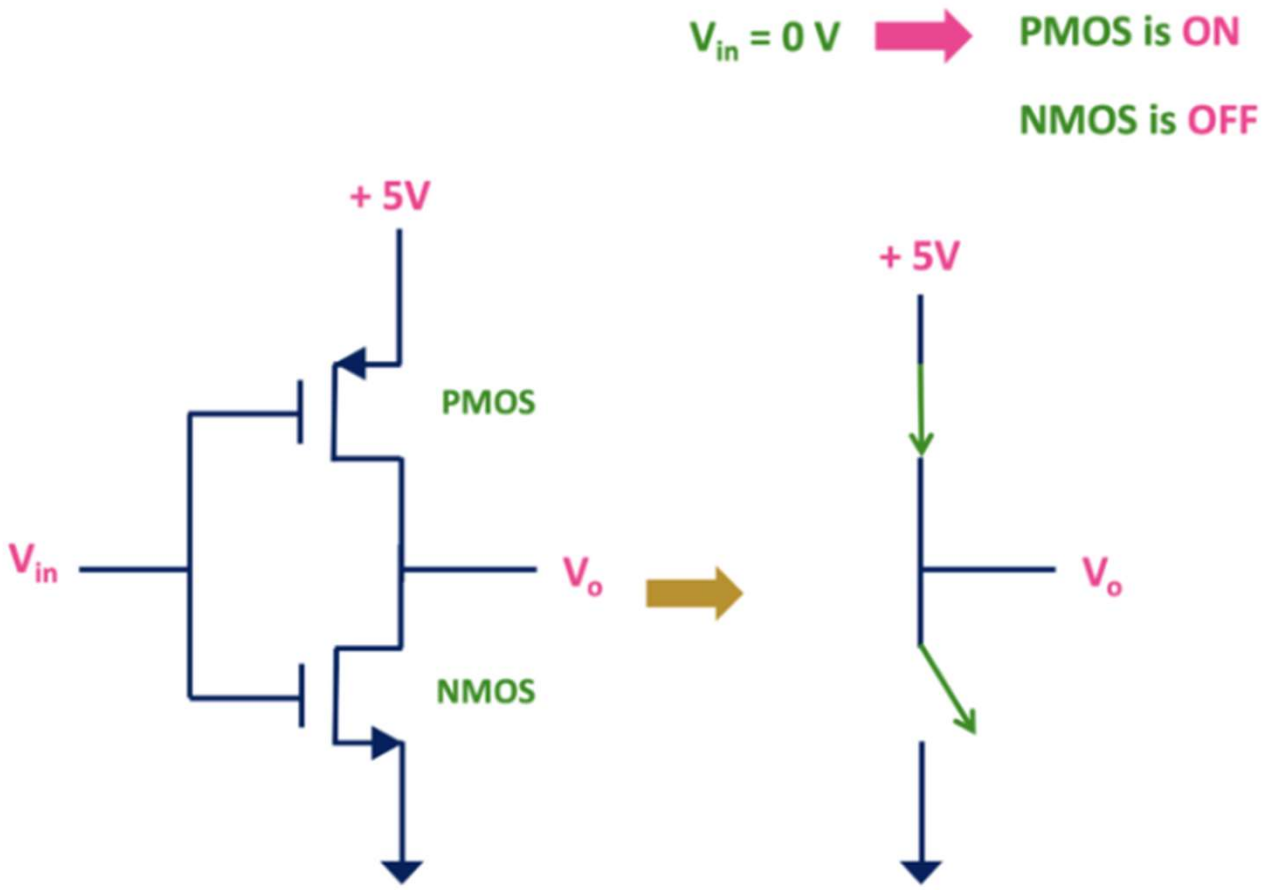


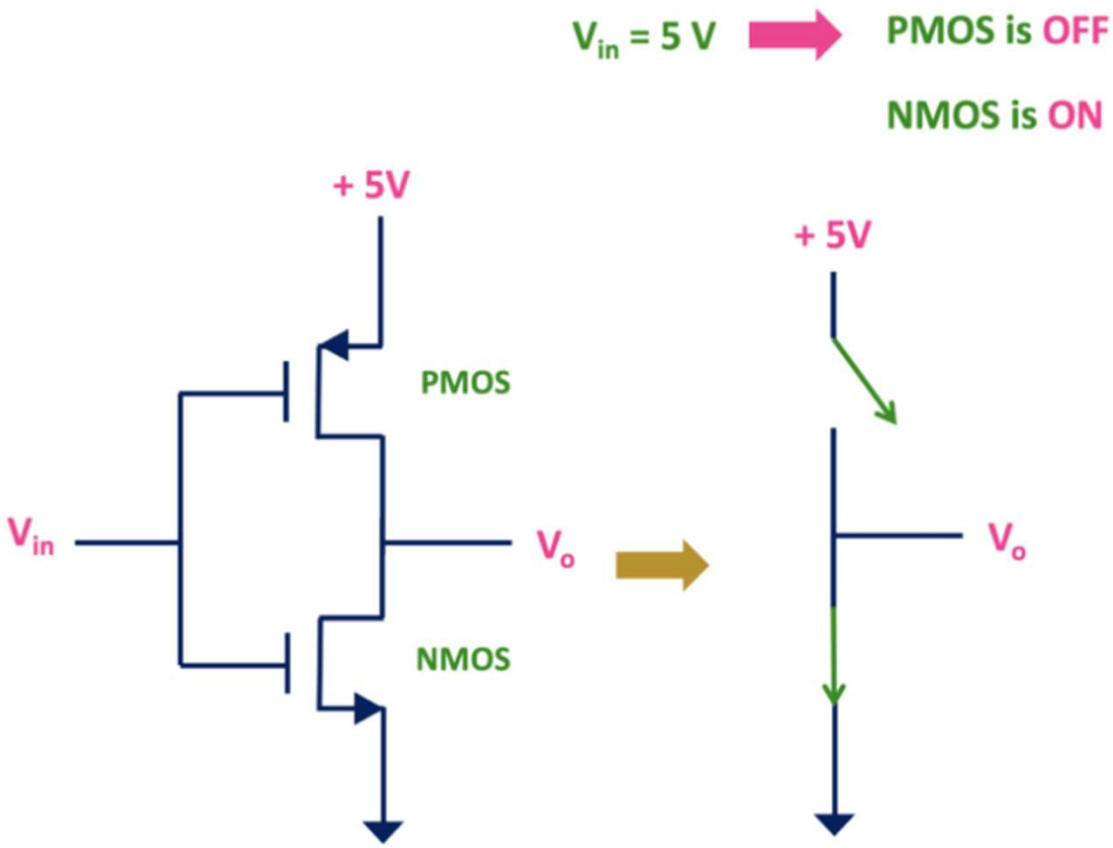




| A | Y |
|---|---|
| 0 | 1 |
| 1 | 0 |

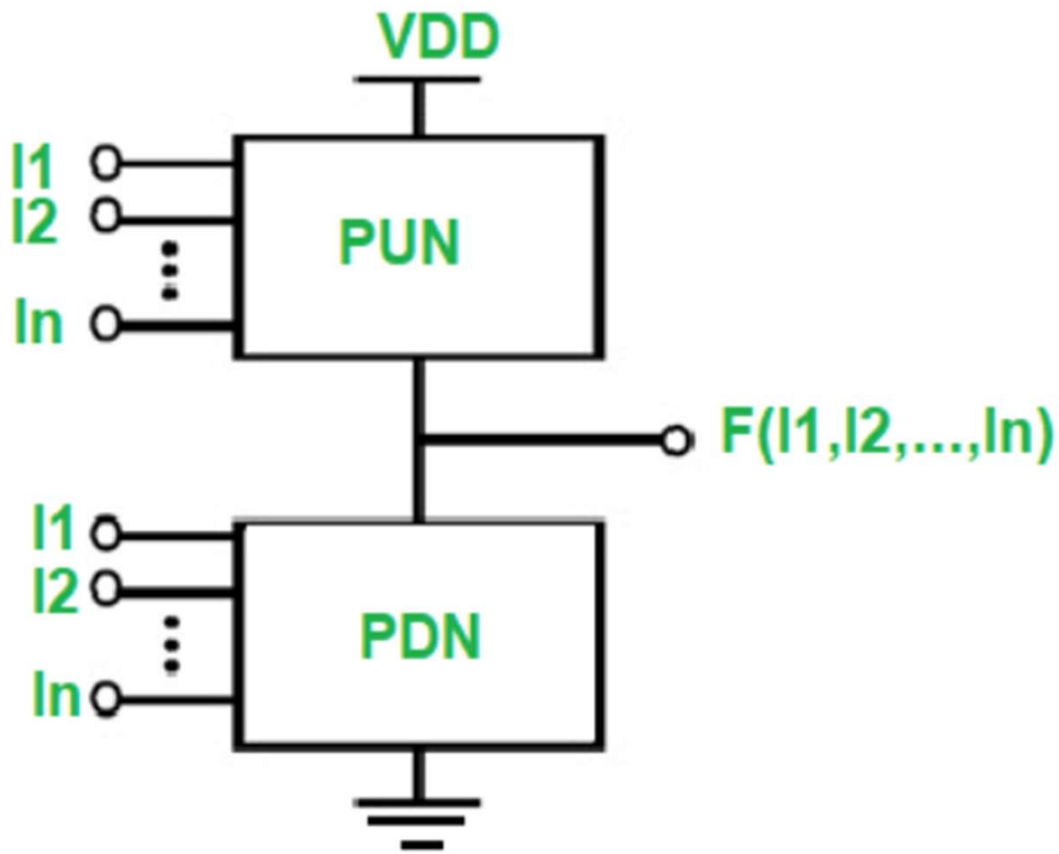
*CMOS Inverter*

- The CMOS inverter is shown below. It consists of a series connection of a PMOS and an NMOS.
- VDD represents the voltage of logic 1, while the ground represents logic 0.
- Whenever the input is high or 1, the NMOS is switched on while the PMOS is turned off. Thus output Y is directly connected to the ground and thus comes to be logic 0.
- When the input is logic 0, the reverse happens – NMOS goes off and PMOS goes on. This provides a direct path between VDD and output Y. Hence Y becomes high.
- This is the basic principle of operation of a CMOS inverter.

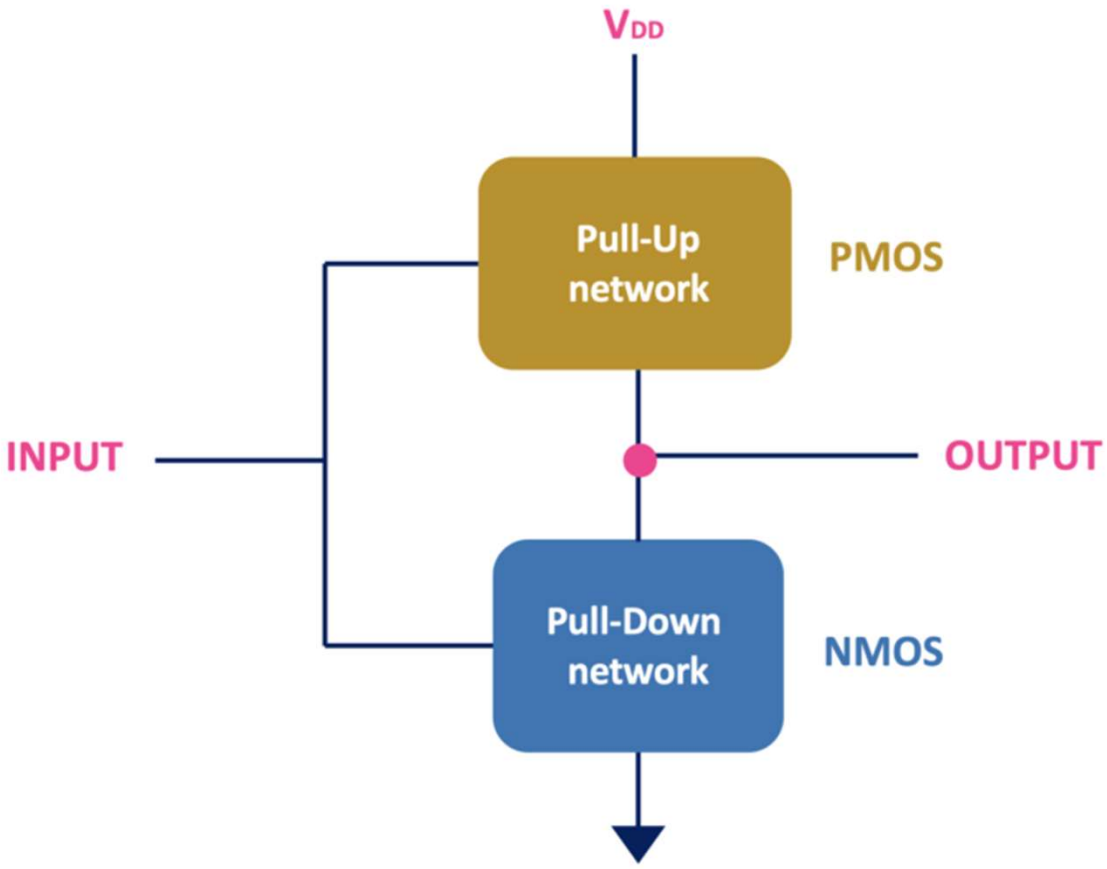

$V_{in}$ = 0 V
PMOS is ON
NMOS is OFF
+ 5V
PMOS
$V_{in}$
$V_o$
NMOS
+ 5V
$V_o$


$V_{in}$ = 5 V
PMOS is OFF
NMOS is ON
+ 5V
PMOS
$V_{in}$
$V_o$
NMOS
+ 5V
$V_o$

- *From the above analysis, we can infer that for implementing any Boolean function using CMOS technology, we need to make a switching circuit with PMOS switches in the upper block that turns on when its inputs are low, and NMOS switches in the lower block that turns on when its inputs are high.*
- *The two blocks must operate in a complementary sense.*
- *The upper block consisting of only PMOS is called a **pull-up network (PUN)** because it pulls up the output to VDD or logic high.*
- *The lower block consisting of NMOS is called a **pull-down network (PDN)** because it pulls down the output to ground or logic low.*
- *Any Boolean function can be realized using PUN and PDN.*

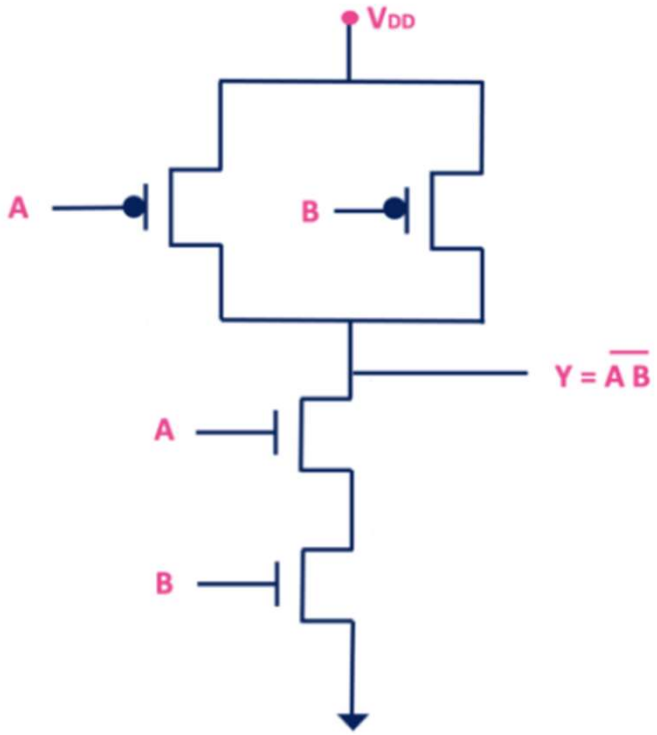



*PUN and PDN*


VDD
Pull-Up network
PMOS
INPUT
OUTPUT
Pull-Down network
NMOS

- Suppose we have Y = F(A, B, C, D). We have to obtain the PDN and PUN blocks from this given Boolean expression.
- For getting the PDN block, we need to obtain Y’ in terms of non-complementary variables A, B, C, and D. If we have AND in the expression of Y’, then it means two NMOS in series to ground. If there is an OR, it means two NMOS in parallel.
- For the PUN, we need Y in terms of complemented variables A’, B’, C’, and D’. Again here if we have AND in the expression of Y, we need two PMOS in series, and an OR means two PMOS in parallel.

# Implementation of NAND and NOR gate using CMOS Logic:



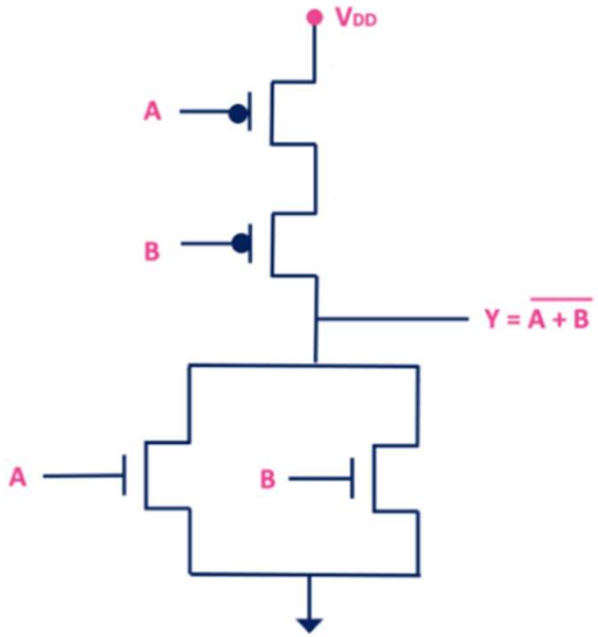

Truth Table

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

- For two input NAND gate, if A and B are the inputs then its output Y = (A.B)'.
- In NMOS network when we have AND operation between the two variables, then two NMOS transistors will get connected in series. And the output will be complement of it.
- The PMOS network is dual of the NMOS network. In the NMOS network, if two transistors are connected in series then in the PMOS network, the two PMOS transistors will get connected in parallel.

**NOR Gate:**

## NOR Gate



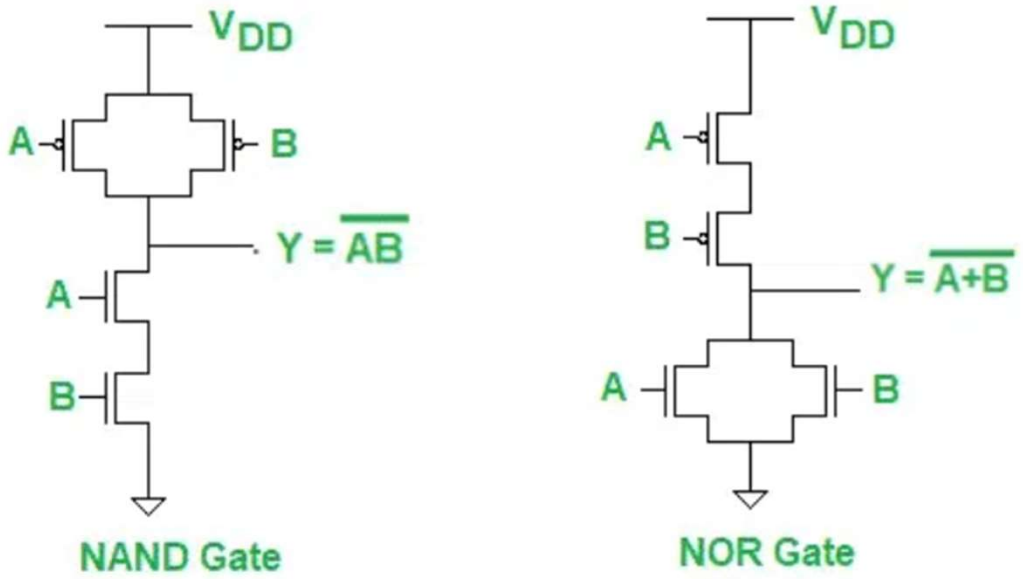

### Truth Table

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

- For two input NOR gate, if A and B are the inputs then its output Y = (A+B)'.
- In the NMOS network, whenever there is an OR operation between the two variables then two NMOS transistors will get connected in parallel. And the output will be complement of it.
- The PMOS network will be the dual of the NMOS network. Therefore, in the PMOS network, the two PMOS transistors will get connected in series.

## NAND Gate and NOR Gate:

NAND and NOR gates can be easily realized using CMOS logic as shown below.



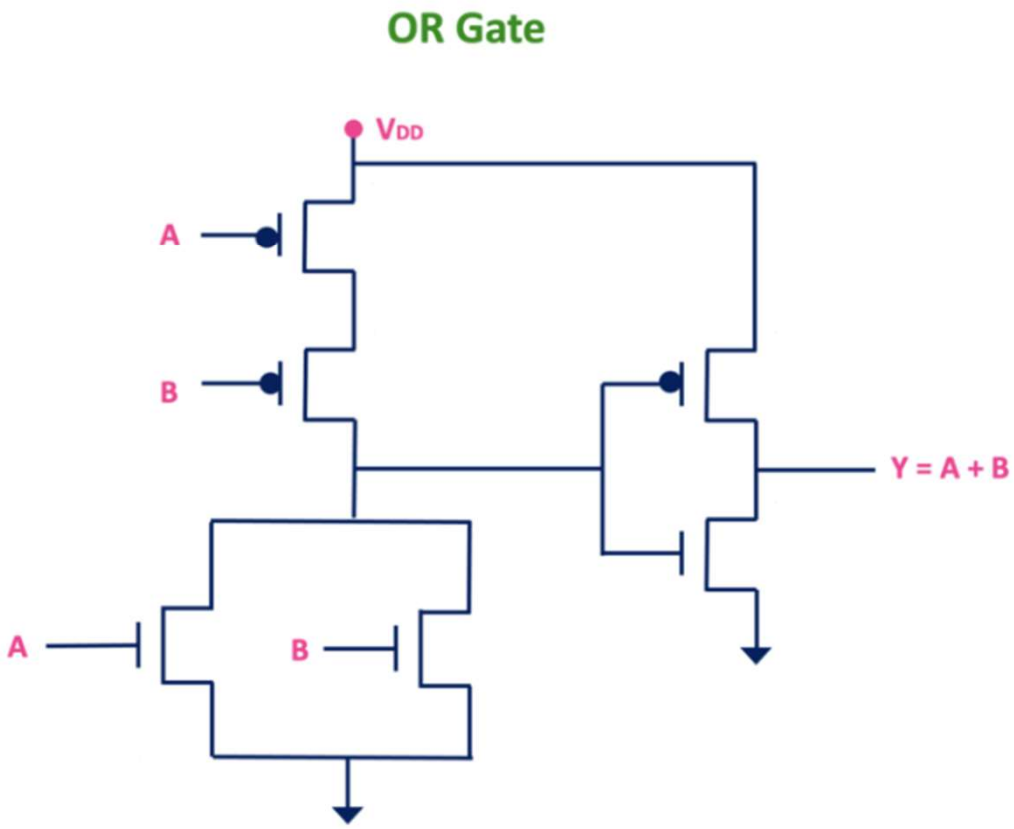

*NAND Gate and NOR Gate*

AND and OR gates are usually realized by using a NAND gate in series with a NOT gate, or a NOR gate in series with a NOT gate.

## Implementation of AND and OR gate using CMOS Logic:

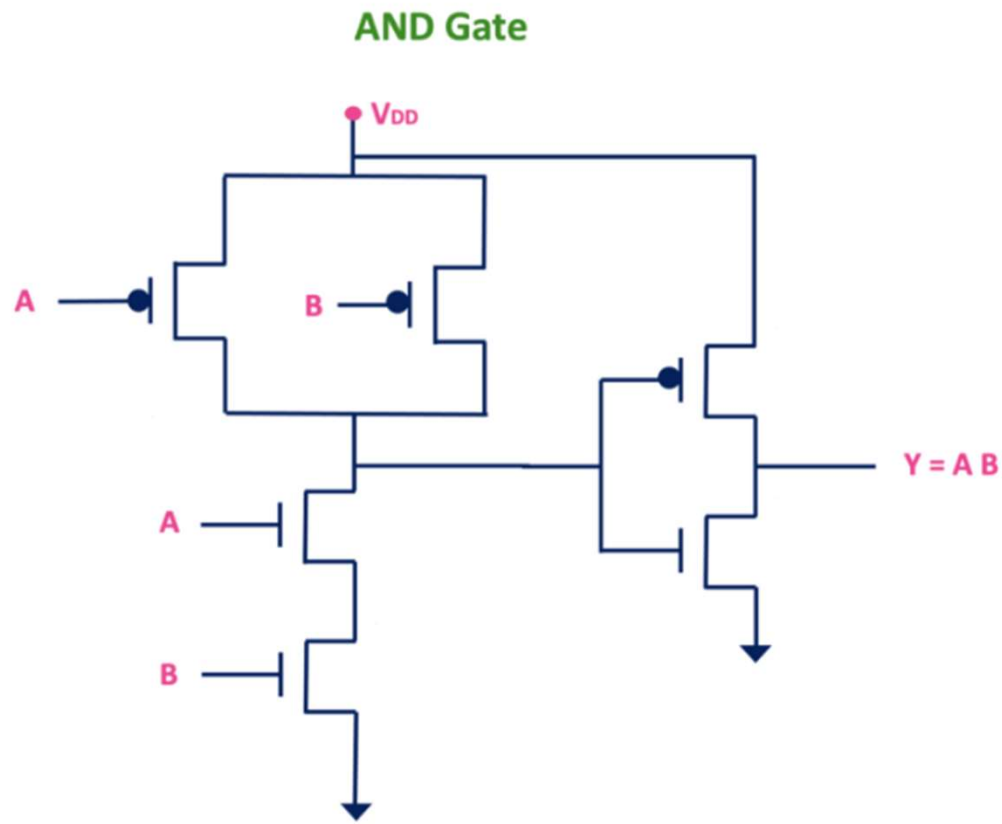
**OR Gate:**

To implement the OR gate, just add the inverter at the output of the NOR gate. The CMOS OR gate is shown below.

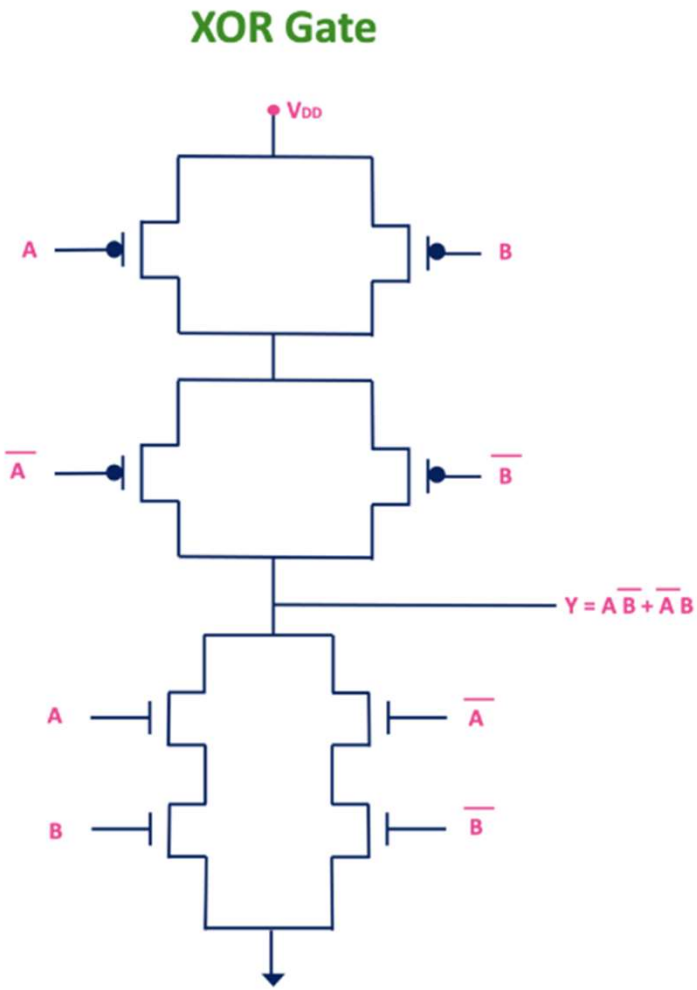


**AND Gate :**

Similarly, by connecting the inverter at the output of the NAND gate, we can implement AND gate. The CMOS AND gate is shown below.



**XOR Gate:**


XOR Gate
VDD
A
B
$\overline{A}$
$\overline{B}$
Y = A $\overline{B}$ + $\overline{A}$ B
A
$\overline{A}$
B
$\overline{B}$

**XNOR Gate :**